ETH zürich IBM Research | Zurich

Bachelor Thesis Presentation

Low Jitter Phase-Locked Loop
Integrated Circuit

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Presentation Overview

-Project Goal

-Phase-Locked Loops: Background

-Sub-Sampling PLL

-Double-Sampling PLL

-Double-Sampling PLL: Implementation

-Results

Project Goal

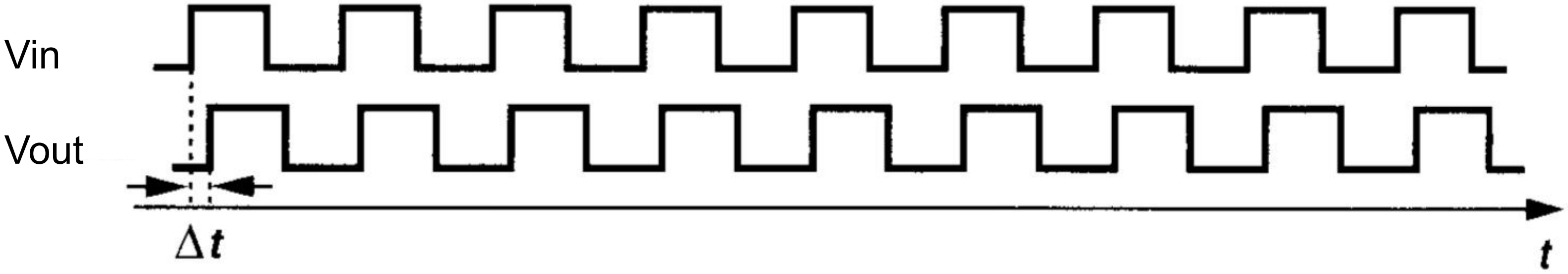
-Reduce the jitter of a PLL

-Keep in mind power and area constraints

-Investigate the literature to find feasible solutions

Phase-Locked Loops: Background

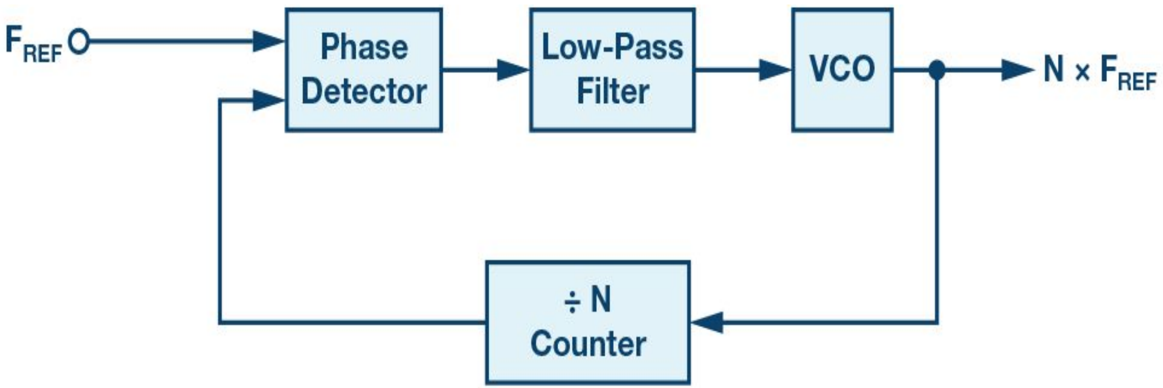
A Phase-Locked Loop is a control system that generates an output signal whose phase is fixed relative to the phase of an input signal



Phase-Locked Loops: Background

Circuit whose output is proportional to its inputs' phase difference

Voltage controlled oscillator: circuit whose output frequency is proportional to its input voltage



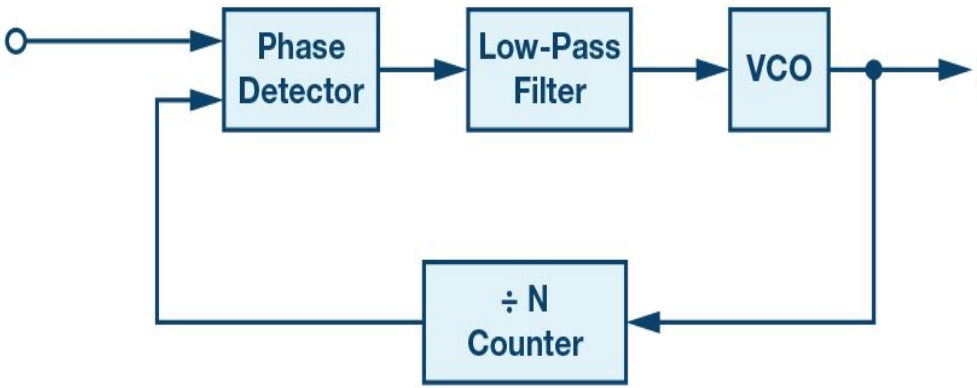
Possibly, a feedback factor of N

Phase-Locked Loops: Background

Our specific PLL requirements:

Limited chip area -> ring oscillator instead of an LC tank oscillator

FREF = 100 MHz



FOUT = 16 GHz

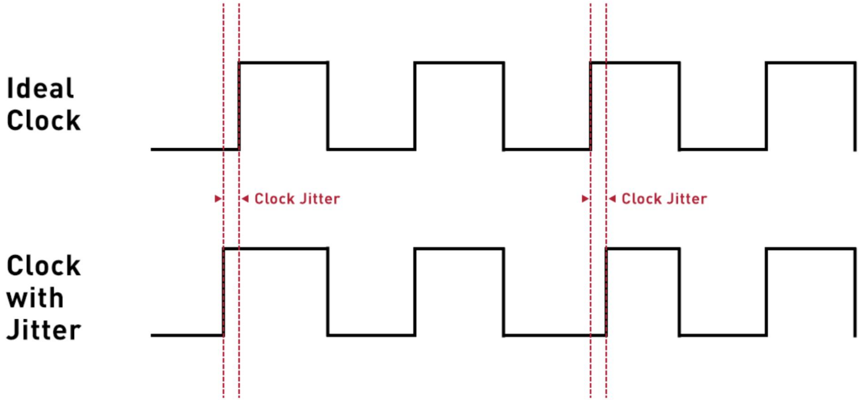
Feedback factor of 160

Phase-Locked Loops: Background

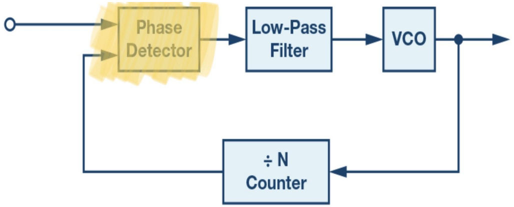
PLL’s problem: Jitter

The jitter is the difference between the ideal zero-crossings and the actual zero-crossings

$$\Delta T_{abs,rms} = \lim_{N\to\infty} \frac{1}{N}\sqrt{\Delta T_1^2 + \Delta T_2^2 + ... + \Delta T_N^2}$$



Goal of the project: design a PLL with low jitter

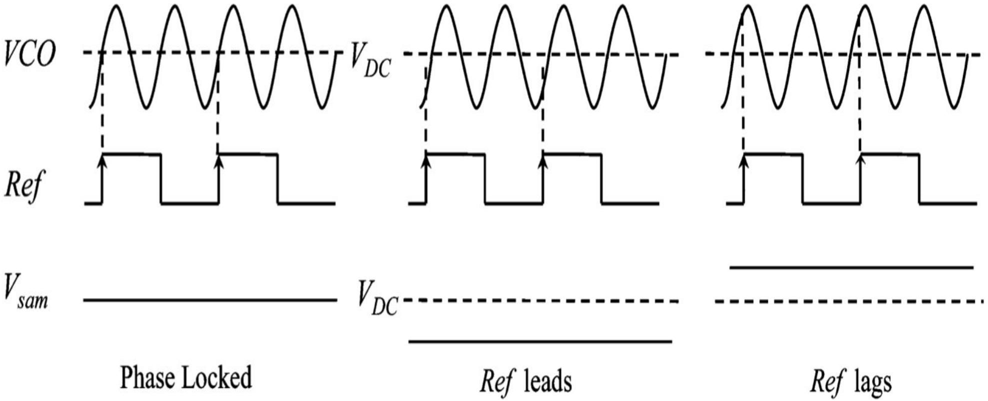


Sub-Sampling PLL

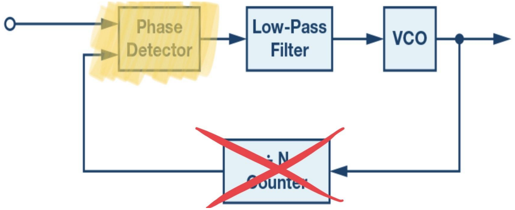
-Bring the VCO to the desired frequency

-From this point, sample the output with the input and compare it to the DC common level

-There is no divider in the feedback path



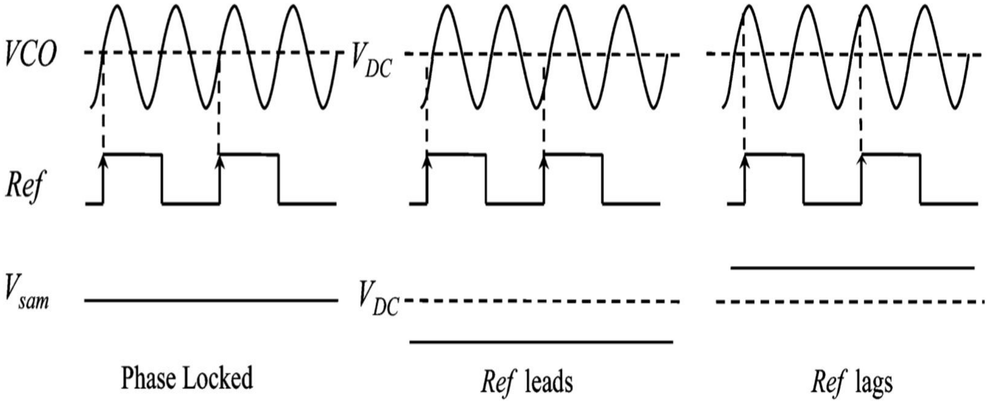
Xiang Gao. “Low Jitter Low Power Phase Locked Loops Using Sub-Sampling Phase Detection”. PhD thesis. University of Twente, 2010



Sub-Sampling PLL

Advantage: very good jitter performance, because there is no divider in the feedback path

Disadvantage: every time the PLL is not locked, the VCO must be brought back to the locked state



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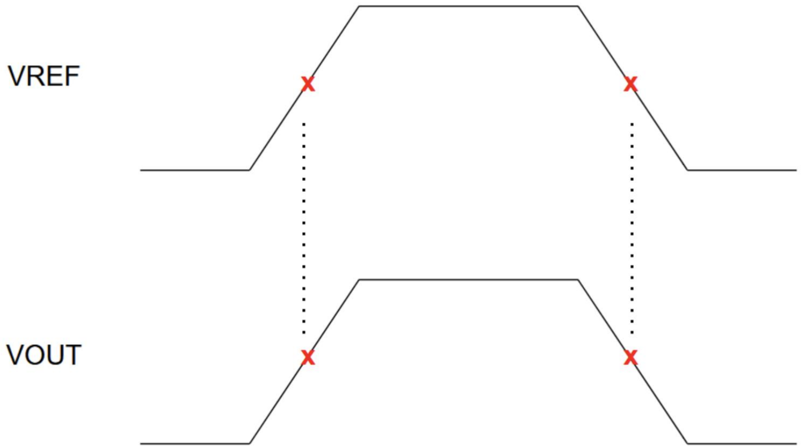
Double-Sampling PLL

-In this topology, there is a divider in the feedback path

-Sample the input phase with the output phase

-Take the difference between the rising edge's sampled value and the falling edge's sampled value



Yu Zhao. "Low Jitter Techniques for High-Speed Phase-Locked Loops". PhD thesis. University of California, 2022

Double-Sampling PLL

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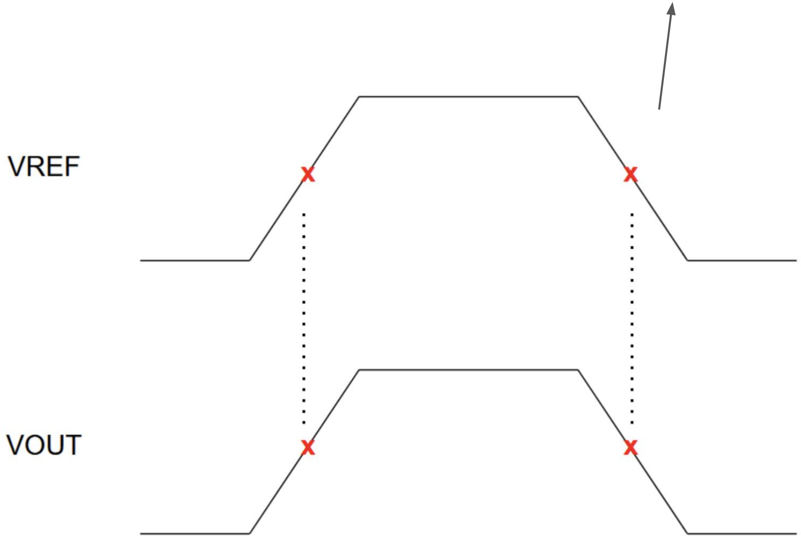


Input and output are aligned: the sampled values are the same

Yu Zhao. "Low Jitter Techniques for High-Speed Phase-Locked Loops". PhD thesis. University of California, 2022

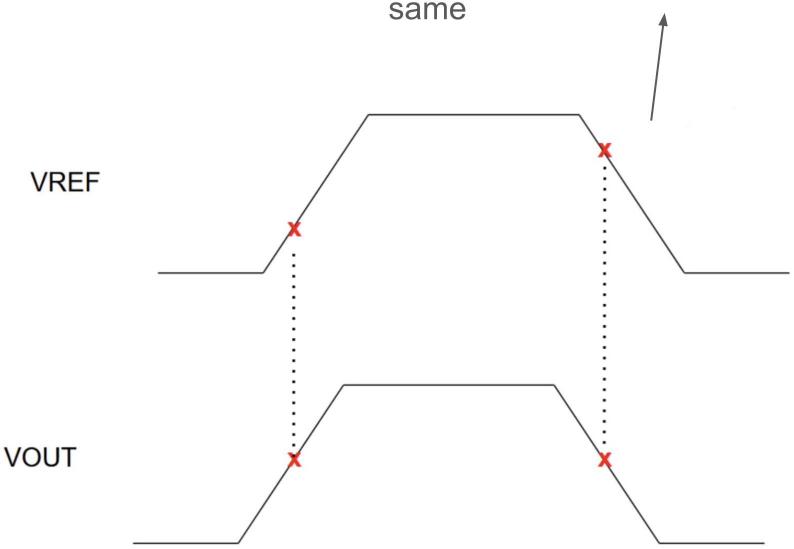
Double-Sampling PLL

-In this topology, there is a divider in the feedback path

-Sample the input phase with the output phase

-Take the difference between the rising edge's sampled value and the falling edge's sampled value

Input and output are not aligned: the sampled values are not the same



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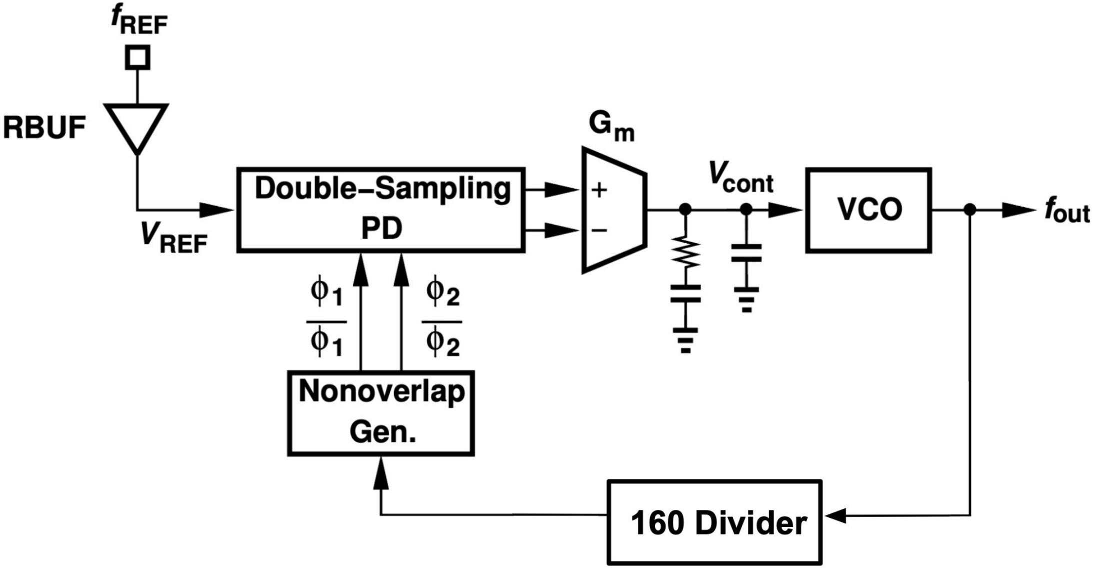
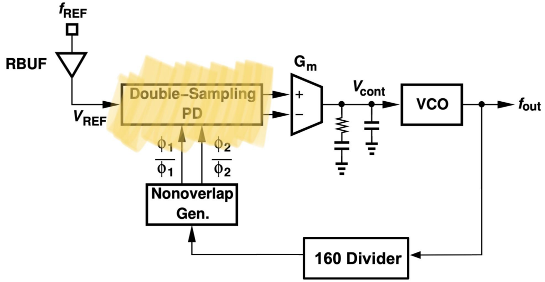
Double-Sampling PLL: Implementation

General Schematic



Double-Sampling PLL: Implementation



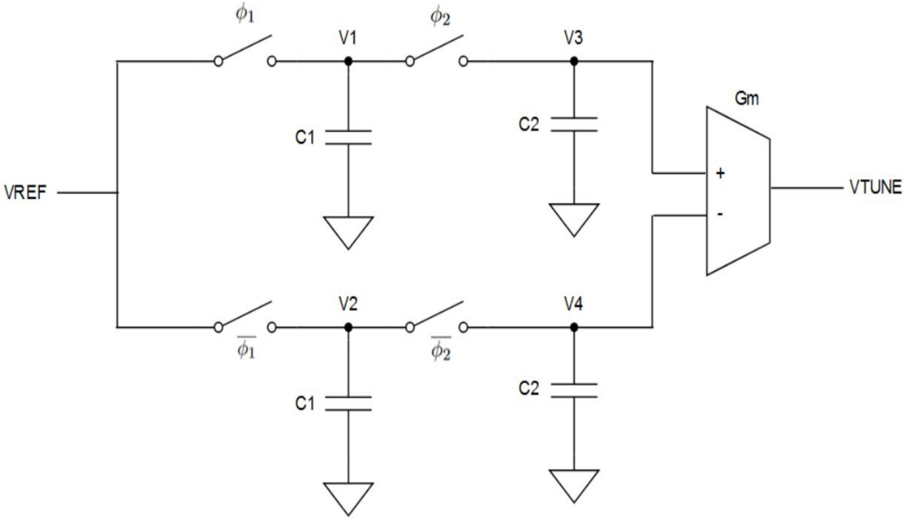
Double-Sampling unit

ϕ_1 and ϕ_2 follow the output and sample the rising edges of the input

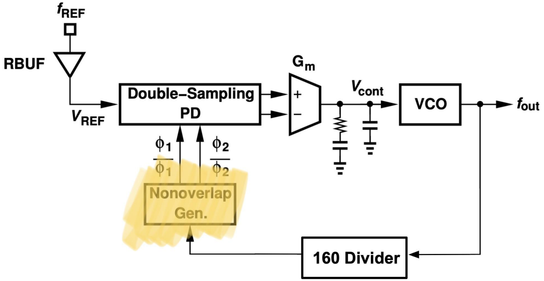
$\overline{\phi_1}$ and $\overline{\phi_2}$ follow the inverse of the output and sample the falling edges of the input

Phase Detector gain:

$K_{PD} = SR_{REF}A_{v,inv} \,/\, \pi f_{REF}$ = 11.25



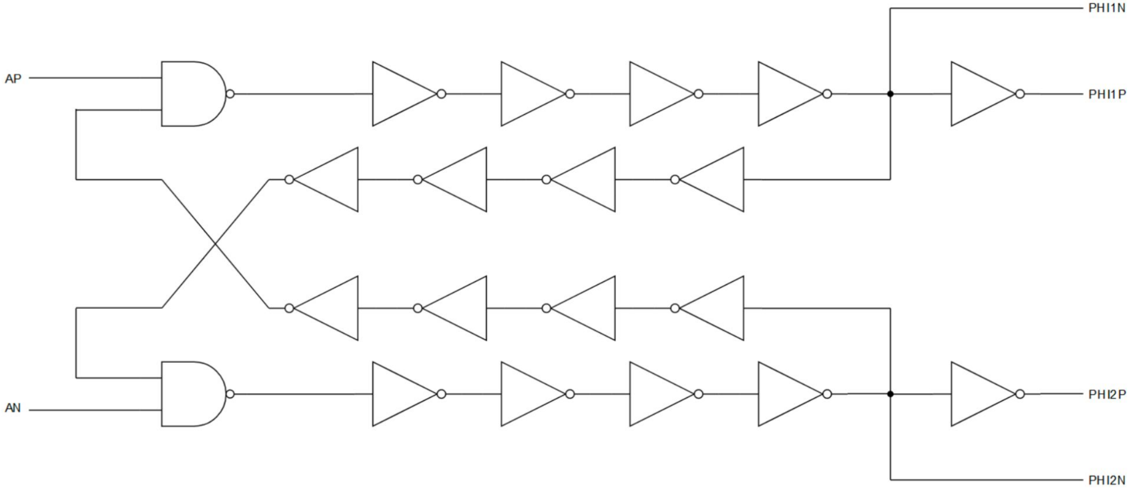
Double-Sampling PLL: Implementation



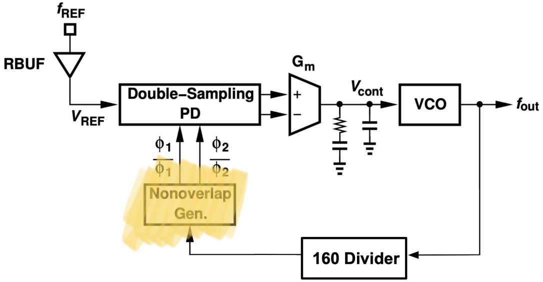
Non Overlap Generator

$$\overline{\phi_1} = \overline{V_{out} \wedge \overline{\phi_2}}$$

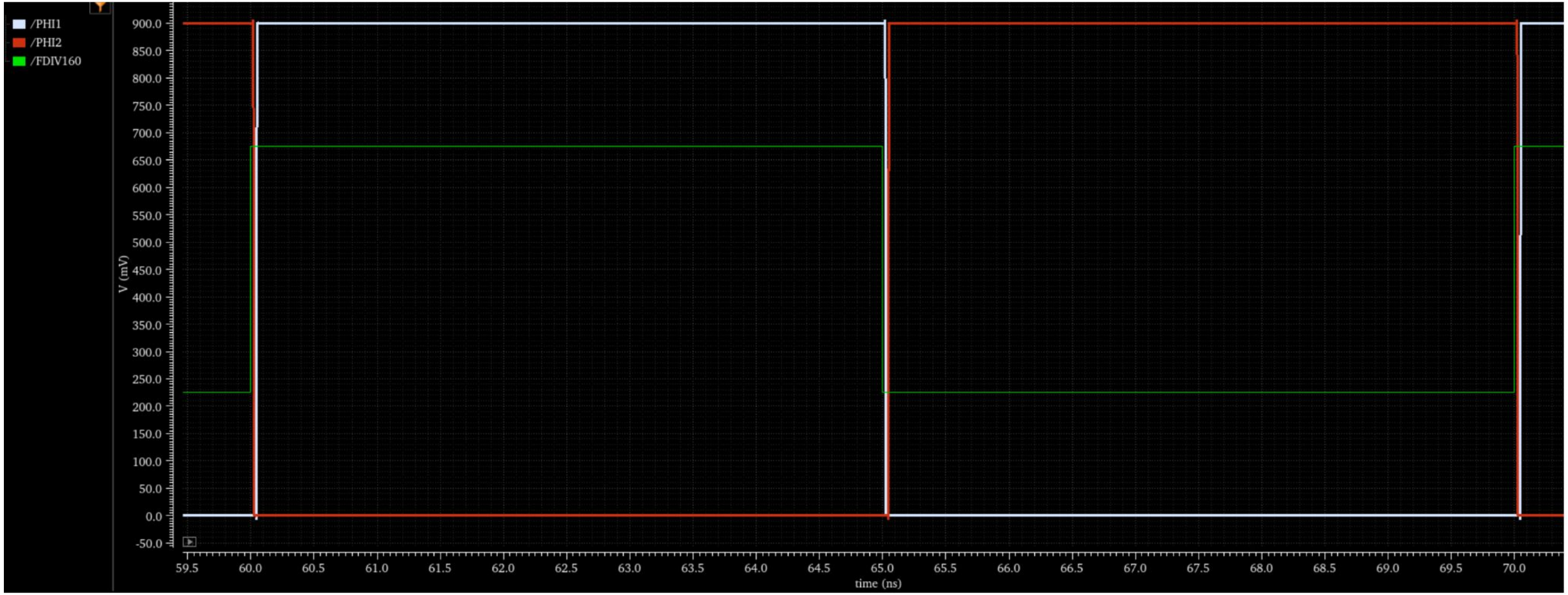
$$\overline{\phi_2} = \overline{\overline{V_{out}} \wedge \overline{\phi_1}}$$



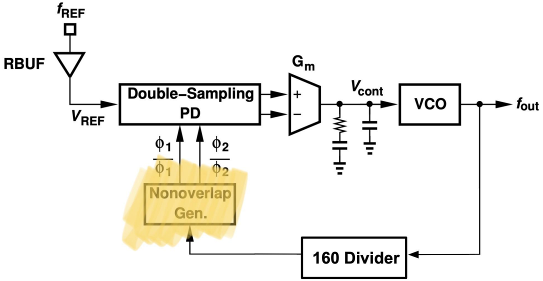
Double-Sampling PLL: Implementation



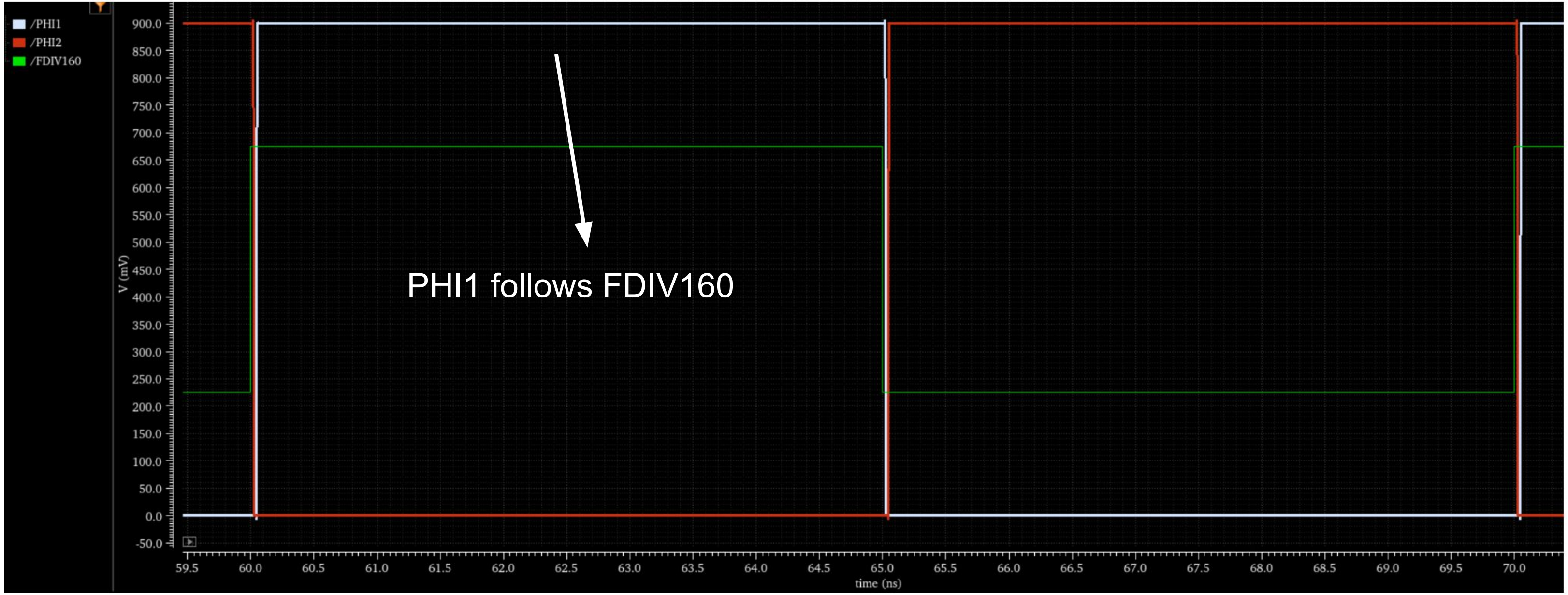
Non Overlap Generator



Double-Sampling PLL: Implementation

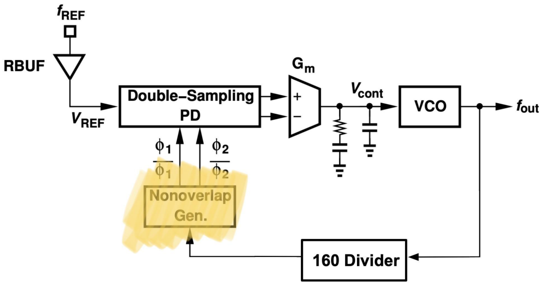


Non Overlap Generator

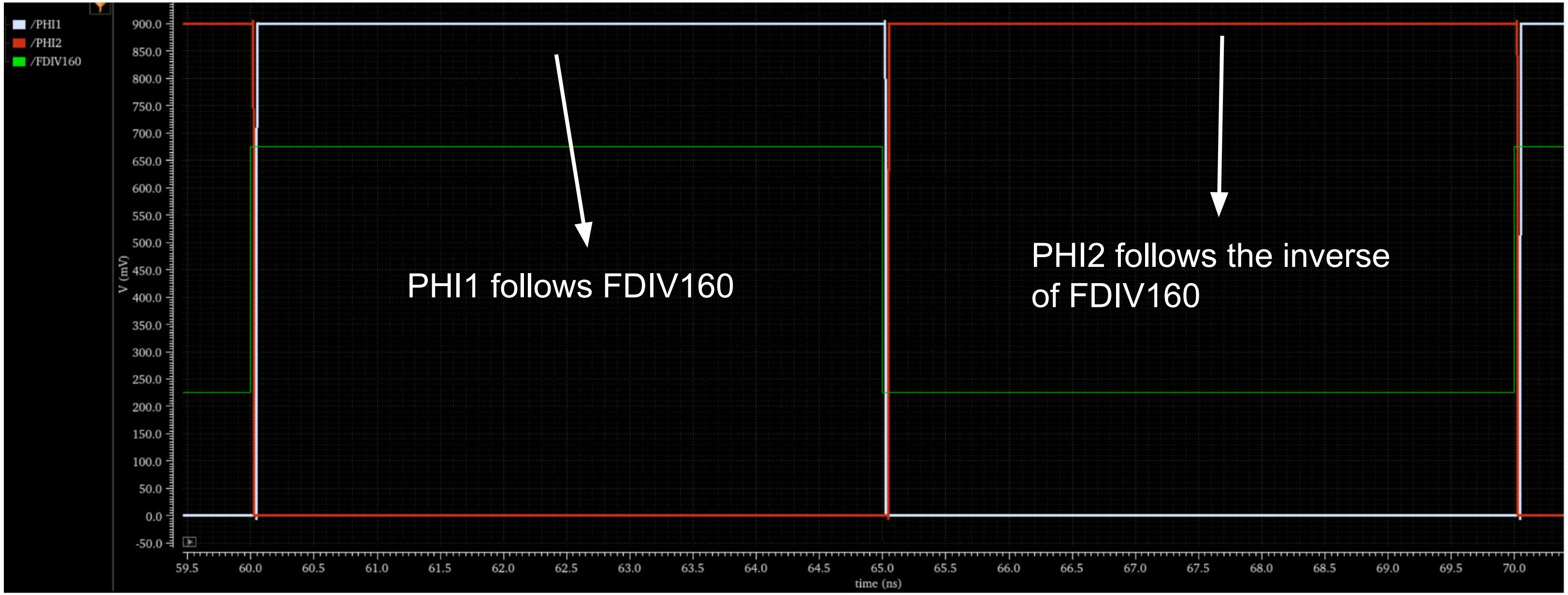


PHI1 follows FDIV160

Double-Sampling PLL: Implementation



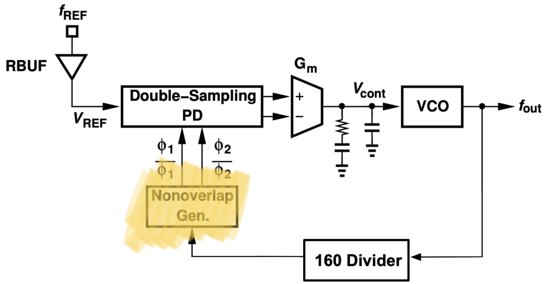
Non Overlap Generator



PHI1 follows FDIV160

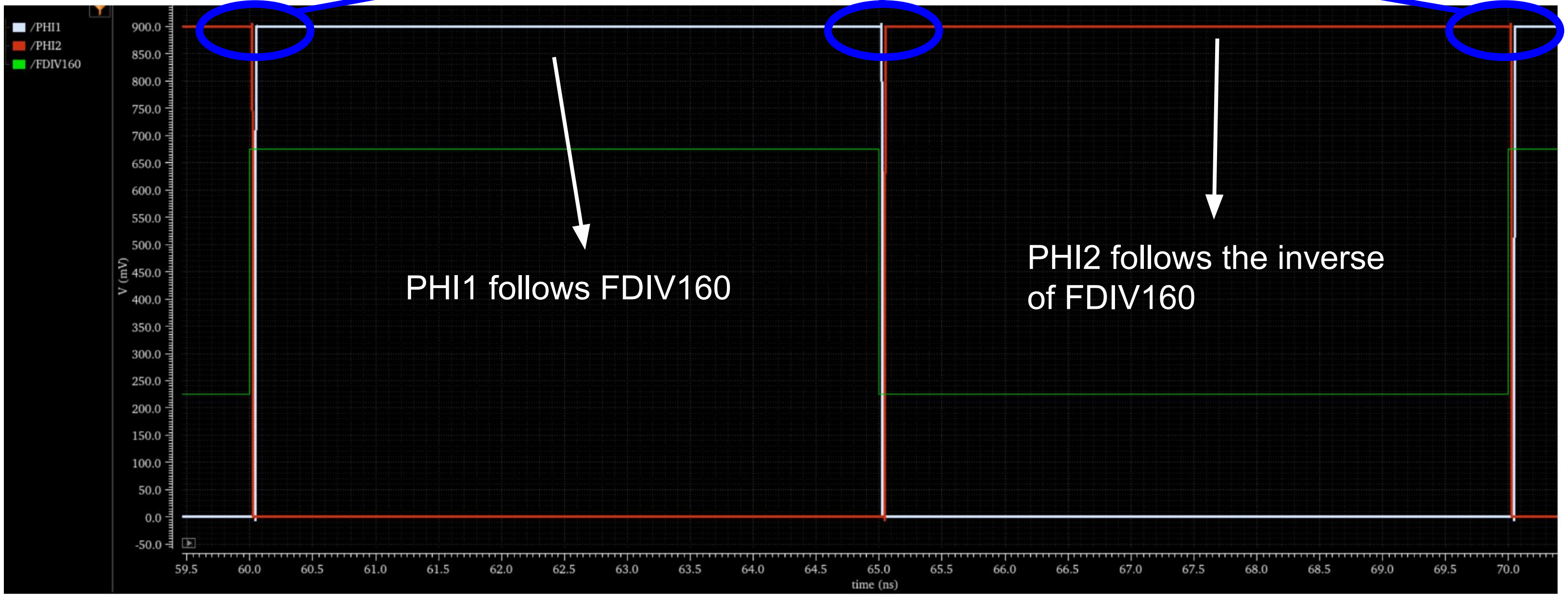
PHI2 follows the inverse of FDIV160

Double-Sampling PLL: Implementation



Non Overlap Generator

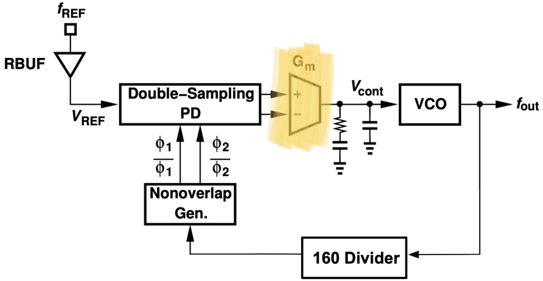
They never overlap!



PHI1 follows FDIV160

PHI2 follows the inverse of FDIV160

Double-Sampling PLL: Implementation



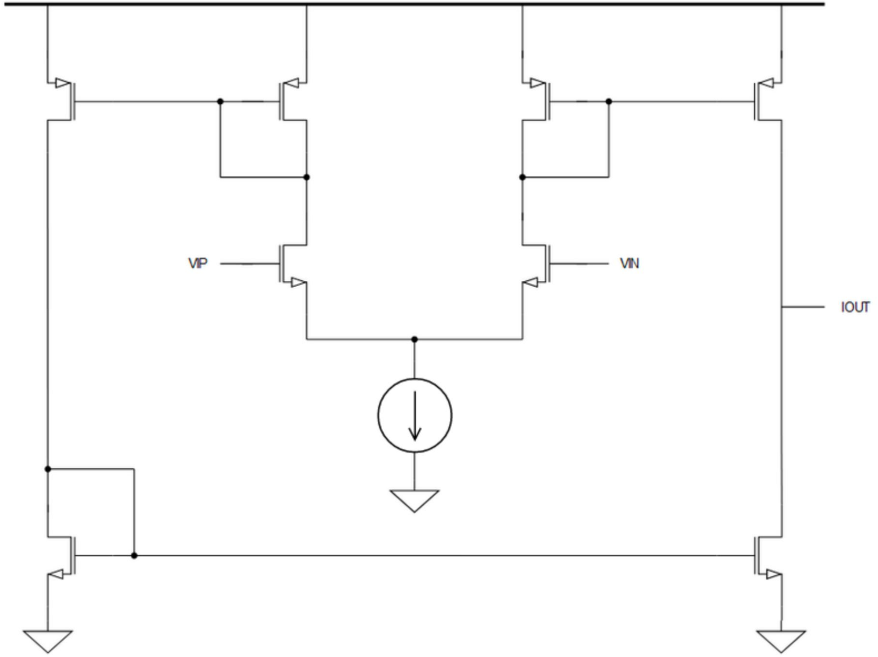
Gm Amplifier

-It takes the difference between the sampled values, transforms it into a current and injects it into the loop filter

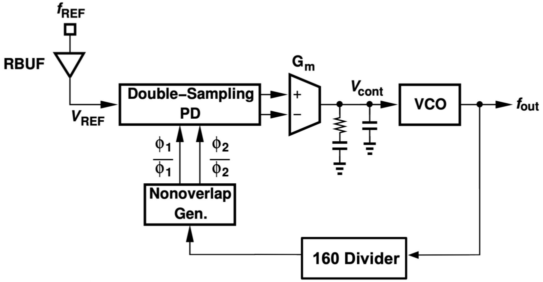
-The gain is regulated by the ratio of the widths in the current mirror stage

Gm gain:

0.228 µA/V



Double-Sampling PLL: Implementation

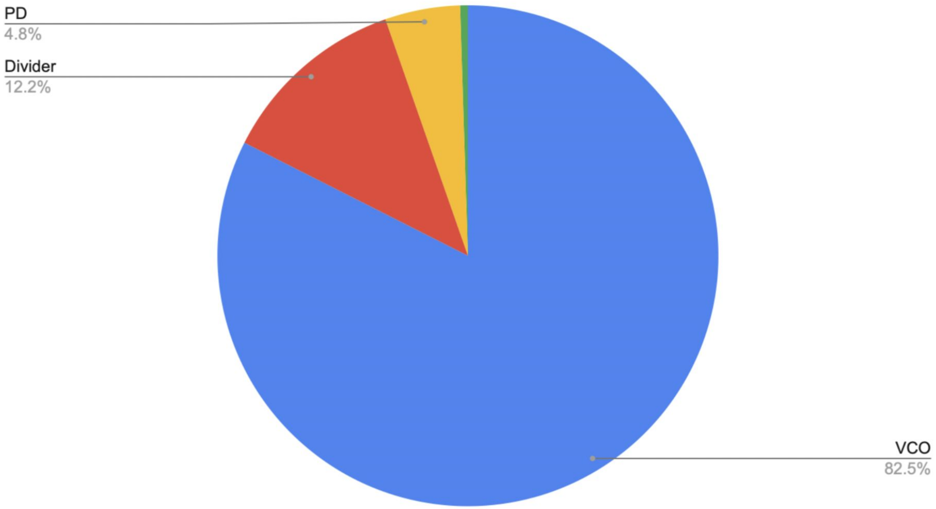


Overview of the circuit

Phase detector gain: 11.25
Gm gain: 0.228 μA/V
Loop filter parameters: Rp = 30 kΩ, Cp1 = 5 pF, Cp2 = 500 fF
VCO gain: 13.9 MHz/mV
Reference buffer gain: 12.5

Power consumption: 1.88 mW
VCO: 1.48 mW
Divider: 0.219 mW
PD: 0.087 mW
Buffer: 0.009 mW

Power Consumption Contributions



Double-Sampling PLL: Implementation

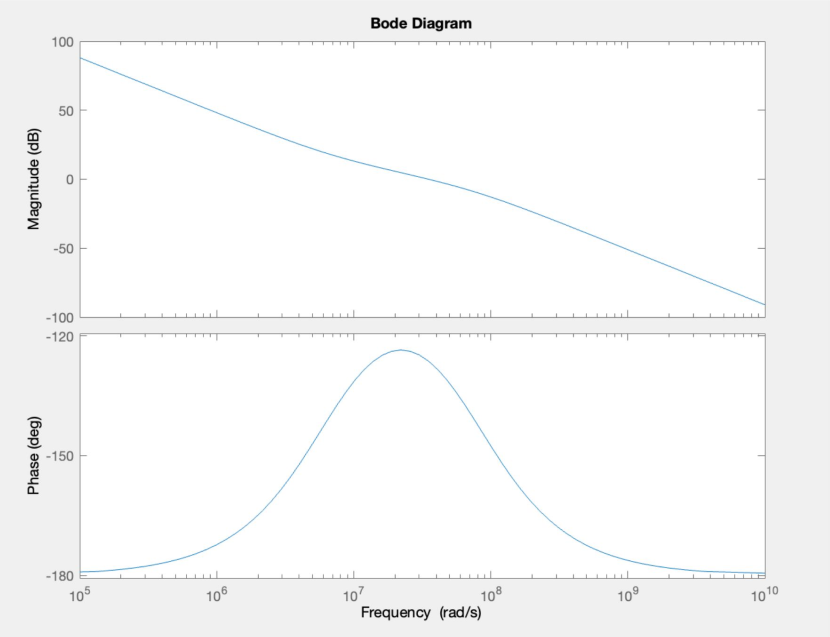
Overview of the circuit: Stability

Phase margin: 54°

Open loop transfer function:

$$\frac{K_{PD}K_{VCO}g_m}{s^2}\frac{sR_PC_{P1}+1}{sC_{P1}C_{P2}R_P+C_{P1}}$$

Open loop transfer function bode plot

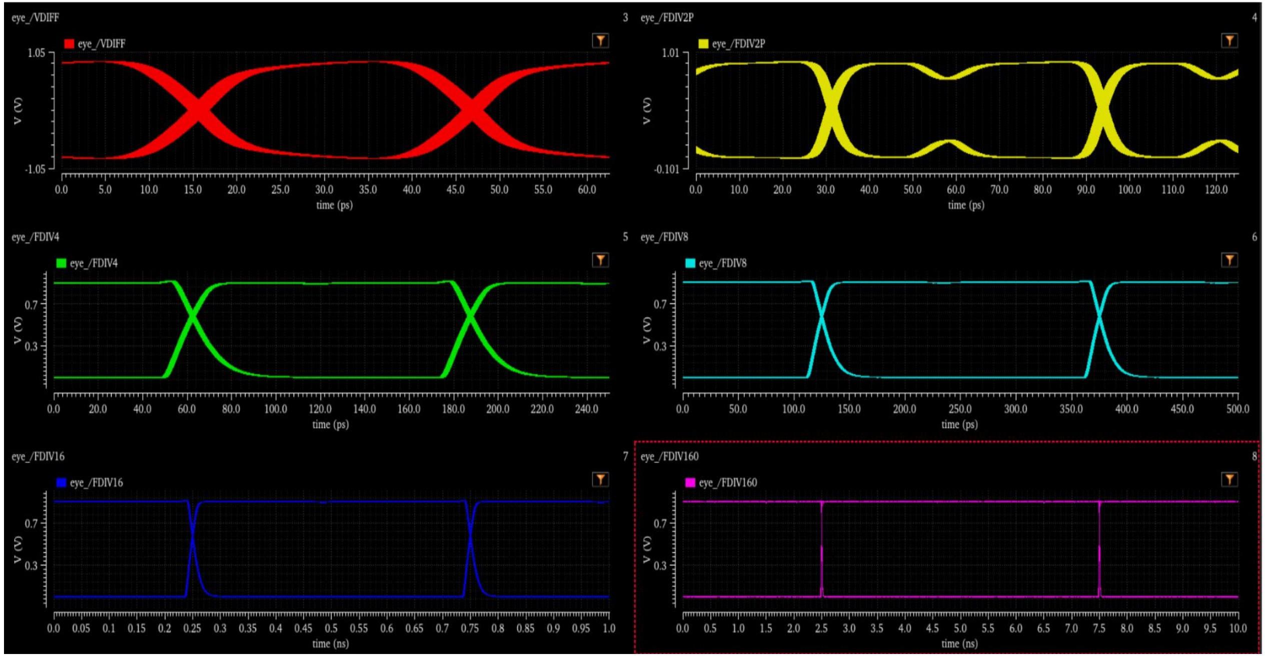


Results

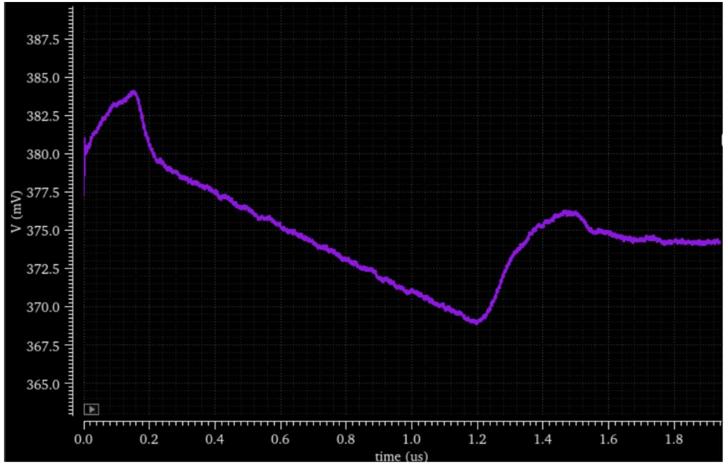
Jitter at the output: 1 ps

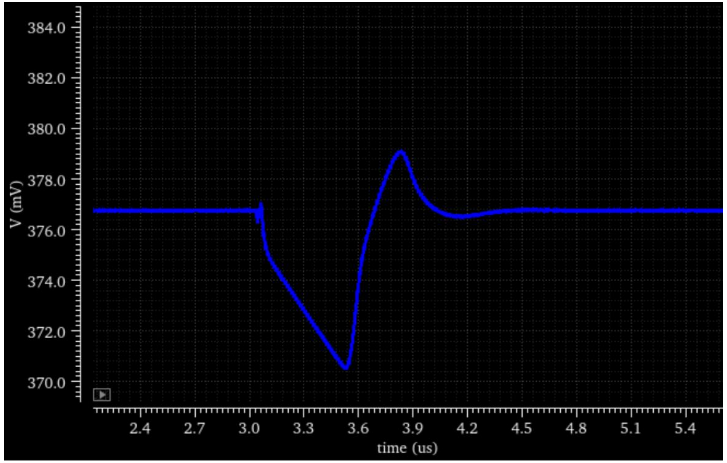
Power consumption: 1.88 mW

Eye Diagrams of all the generated frequencies



Results

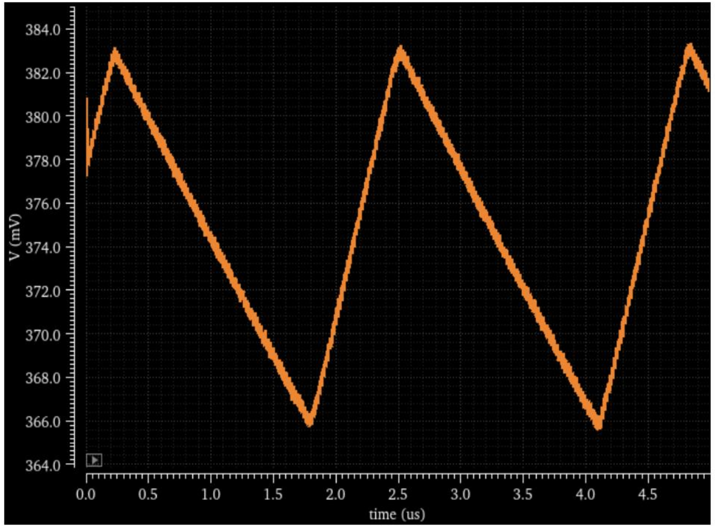


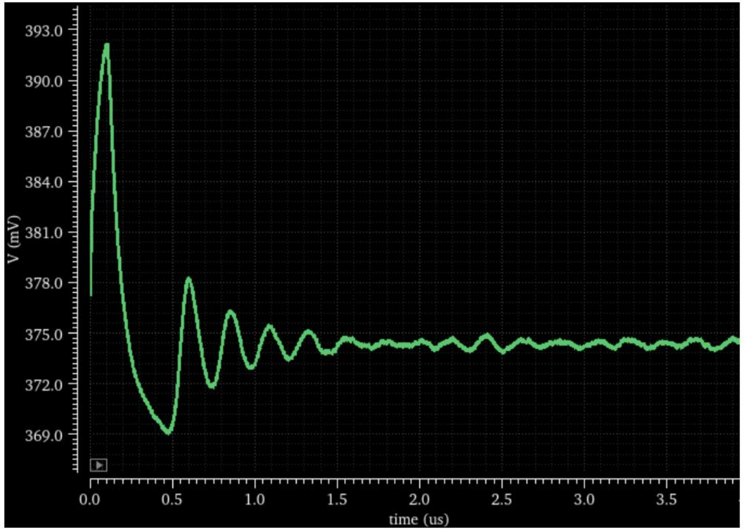


Settling of the PLL at the beginning of the simulation (1.8 µs settling time)

90 deg phase step response

Results





Behavior of unstable PLLs (wrong Loop Filter parameters)

Questions

Thank you for listening