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Low Jitter Phase-Locked Loop Integrated Circuit

Bachelor's Thesis

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Abstract

Phase-Locked Loop (PLL) are fundamental components in a wide range of electronic systems, playing a crucial role in clock generation, synchronization, and signal processing. The performance of a PLL is often constrained by its jitter characteristics, particularly in high-frequency applications.

Current state-of-the-art PLL designs include a variety of oscillator types, with ring oscillators and LC tank oscillators being the most prominent. While LC tank oscillators are known for their superior phase noise performance, their larger silicon area makes them less suitable for applications with stringent area constraints. Conversely, ring oscillators are more suitable for such applications despite their traditionally higher phase noise.

This thesis addresses the need for a low-jitter PLL suitable for integration in a UCIe transceiver. The proposed solution involves a double-sampling PLL topology featuring a double sampling phase detector, designed to optimize phase noise and minimize jitter. Implemented in 5 nm FinFET CMOS technology, the PLL operates at a frequency of 16 GHz with a reference frequency of 100 MHz.

The simulated achieved jitter is 1-2 ps, with a power consumption of 1.88 mW, demonstrating the effectiveness of the design.

Contents

Chapter 1

Introduction

1.1 Project Overview

This Bachelor Thesis focuses on the design of a ring-oscillator based PLL in 5nm FinFET CMOS technology, optimized for phase noise performance and operated at 16 GHz . The project was undertaken at the IBM Research Center in Rüschlikon; a working Charge-Pump PLL had already been implemented. The goal of the project was to develop a design that minimizes jitter, possibly reusing existing PLL components, while adhering to constraints related to area and power consumption, which are critical for the intended application of UCIe transceiver.

The project comprised the following work items:

1. Literature study;
2. Circuit implementation on a schematic level, including PSS and PNOISE analysis of the control loop using Cadence;
3. Parameter tuning by modeling the transfer function with MATLAB;
4. Documentation of the work in the Bachelor Thesis report.

After evaluating different options for a low-jitter PLL, we decided to implement the so-called double-sampling PLL, shown in [1]. The other main option that was taken into consideration was the so-called sub-sampling PLL, presented in [2] and [3]; however, we opted for a double-sampling PLL, because of the problems linked to the lock acquisition phase and phase step response of the sub-sampling PLL (where the sub-sampling unit works only as a phase detector, but not as a phase-frequency detector).

1.2 Thesis Organization

This thesis is organized into 7 chapters. Chapter 2 reviews the fundamentals of PLLs, focusing on the simple PLL and the Charge-Pump PLL. Chapter 3 discusses the jitter and the phase noise in PLLs. Chapter 4 proposes a 16-GHz double-sampling PLL, that samples both the rising and falling edges of the reference clock. Chapter 5 explores the implementation of the circuit at a schematic level and shows the partial simulation results obtained for the various components. Chapter 6 shows the results obtained throughout the project. Chapter 7 provides an overview of the thesis and the work conducted. Finally, chapter 8 explores potential improvements for the circuit.

Chapter 2

Phase-Locked Loops

2.1 Simple PLL

A PLL is a feedback system that compares the output phase with the input phase, with the goal of making the output phase equal to the input phase. The components of a simple PLL include the Phase Detector (PD), a Low-Pass Filter (LPF) and finally a Voltage-Controlled Oscillator (VCO).

2.1.1 Simple PLL Architecture

The first component of a simple PLL is the PD. It is a circuit whose average output $\overline{V_{out}}$ is linearly proportional to the phase difference $\Delta\phi$ between its two inputs. Typically, it is an exclusive OR (XOR) gate, which produces pulses with widths proportional to the phase difference. As the phase difference increases, the width of the pulses, and thus $\overline{V_{out}}$, increases. The slope of the characteristic curve between $\overline{V_{out}}$ and $\Delta\phi$ is denoted as K_{PD}.

An LPF is necessary after the PD to eliminate the high-frequency components of the PD output due to the pulses, retaining only the average value. The gain of the LPF is assumed to be unity at low frequencies.

The output of the LPF, V_{cont}, controls the frequency of the VCO with the following relationship:

$$\omega_{out} = \omega_0 + K_{VCO}V_{cont} \tag{2.1}$$

where K_{VCO} is the gain of the VCO. The PD, LPF and VCO are placed in series so that any phase difference between input and output can be corrected by adjusting ω_{out}.This adjustment allows the output phase to increase faster or slower, aligning it with the input phase.

Figure 2.1 shows the high-level schematic of the simple PLL.

The topology of the Simple PLL is composed of the three aforementioned components arranged in a unity-gain feedback system. Let us assume that there is a significant phase difference between the input and output; $\overline{V_{PD}}$ will gradually increase, while the high-frequency components are filtered out by the LPF. Consequently, V_{cont} increases, leading to a higher output frequency. The output will accumulate phase faster, and eventually, the phase will align with the input phase with a small steady state phase error ϕ_0. At this point, the whole circuit stabilizes around that phase difference. Note that ω_{out} is exactly equal to ω_{in}.

The relationship between the phase difference and the parameters of the circuit given by:

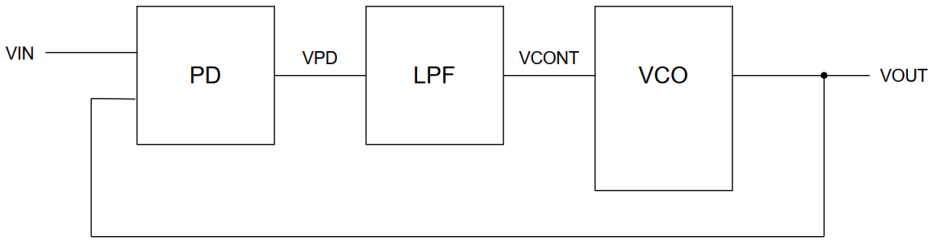

Figure 2.1: Simple PLL

$$\phi_0 = \frac{\omega_{in} - \omega_0}{K_{PD} K_{VCO}} \tag{2.2}$$

Equation 2.2 shows that to minimize the phase error, the gains of the PD and of the VCO must be maximized.

2.1.2 Dynamics of a Simple PLL

Since we are interested in the phases of the input and output, we derive a transfer function for the excess phases of input and output. The excess phase is denoted by Φ; this transfer function illustrates how effectively Φ_{out} can track variations in Φ_{in}. The transfer function of the LPF (from voltage to voltage) is $1/(1+s/\omega_{LPF})$, the PD (from phase to voltage) is $K_{PD}(\phi_{out} - \phi_{in})$, and the VCO (from voltage to phase) is K_{VCO}/s (derived from $\omega_{out} = \omega_0 + K_{VCO} V_{cont}$ and $d\phi_{out}/dt = \omega_{out}$). The open-loop transfer function is thus:

$$H(s)|_{open} = \frac{\Phi_{out}}{\Phi_{in}}(s)|_{open} = K_{PD} \cdot \frac{1}{1 + \frac{s}{\omega_{LPF}}} \cdot \frac{K_{VCO}}{s} \tag{2.3}$$

Analysing the open-loop transfer function, there is a pole at $s = \omega_{LPF}$ and a pole at the origin. This means that the gain of the loop approaches infinity as s approaches zero, implying that ϕ_{out} exactly tracks changes in ϕ_{in}. However, we also observe an important trade-off: higher values of K_{VCO} and K_{PD} reduce the phase error but affect the stability of the closed-loop system.

From 2.3, we can write the closed-loop transfer function as:

$$H(s)|_{closed} = H(s) = \frac{K_{PD} K_{VCO}}{\frac{s^2}{\omega_{LPF}} + s + K_{PD} K_{VCO}} \tag{2.4}$$

We note that the transfer function is the same for input and output frequency, since frequency and phase are related by a linear operator.

Since we have a second-order transfer function, we can write it as:

$$H(s) = \frac{\omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \tag{2.5}$$

where

$$\omega_n = \sqrt{\omega_{LPF} K_{PD} K_{VCO}} \tag{2.6}$$

$$\zeta = \frac{1}{2}\sqrt{\frac{\omega_{LPF}}{K_{PD}K_{VCO}}} \tag{2.7}$$

The two poles of the systems are given by

$$s_1 = (-\zeta + \sqrt{\zeta^2 - 1})\omega_n \tag{2.8}$$

$$s_2 = (-\zeta - \sqrt{\zeta^2 - 1})\omega_n \tag{2.9}$$

Here, we observe several trade-offs. The first concerns ω_{LPF}. The settling speed, a critical parameter in a PLL, is given by $(\zeta\omega_n)^{-1} = (\frac{1}{2}\omega_{LPF})^{-1}$. Thus, while a lower ω_{LPF} improves the suppression of high-frequency components from the PD, it also increases the settling time constant.

Another significant trade-off involves the value of ζ. Both the phase error and ζ are inversely proportional to $K_{PD}K_{VCO}$, but at the same time ζ must be greater than $\sqrt{2}/2$ to avoid ringing. This means that reducing the phase error inevitably reduces system stability.

This theoretical framework (2.1) is based on the concepts presented in [4].

2.2 Charge-Pump PLLs

The main problem with simple PLLs is their limited acquisition range. In fact, if there is a large difference between ω_{out} and ω_{in} at the beginning of the operation, the PLL will not settle, and the transition between unlocked and locked state will not occur. Typically, the so-called acquisition range is of the order of ω_{PLF}, which is not enough for some applications. This is the main reason why a second type of PLL, the Charge-Pump PLL (CPPLL), has been studied.

2.2.1 Phase-Frequency Detector

To overcome the problem of the limited acquisition range, the PD can be substituted by a Phase-Frequency Detector (PFD). This component is usually built as two D-Flip Flops, where the input is given by V_{DD}, and the input clock signal is given by the input and output phases. The AND combination of the outputs of the D-Flip Flops, Q_A and Q_B, serves as the reset signal of the D-Flip Flops. In this topology, if ω_{out} and ω_{in} are different, the circuit functions as a frequency detector; if ω_{out} and ω_{in} are equal, it functions as a normal PD. Figure 2.2 shows a typical PFD schematic.

The output of the PFD could be low-pas filtered, similar to the Simple PLL topology, but a common strategy is to insert a CP between the PFD and the VCO. In this new topology, Q_A and Q_B serve as controllers for switches S_1 and S_2. Switch S_1 allows a positive current to flow into the output capacitor C_P, while switch S_2 allows a negative current to flow into C_P. C_P drives the output voltage; this switching mechanism charges and discharges the output capacitor, thereby adjusting the output voltage. The output voltage is in turn connected to the tune voltage of the VCO.

In a basic CPPLL, one of the D-Flip Flops is clocked by the input signal, while the other one is clocked by the output signal. The PFD senses the phase/frequency difference between input and output and produces an output current into C_P, therefore increasing or decreasing the output frequency to align both the frequency and the phase of the input and output.

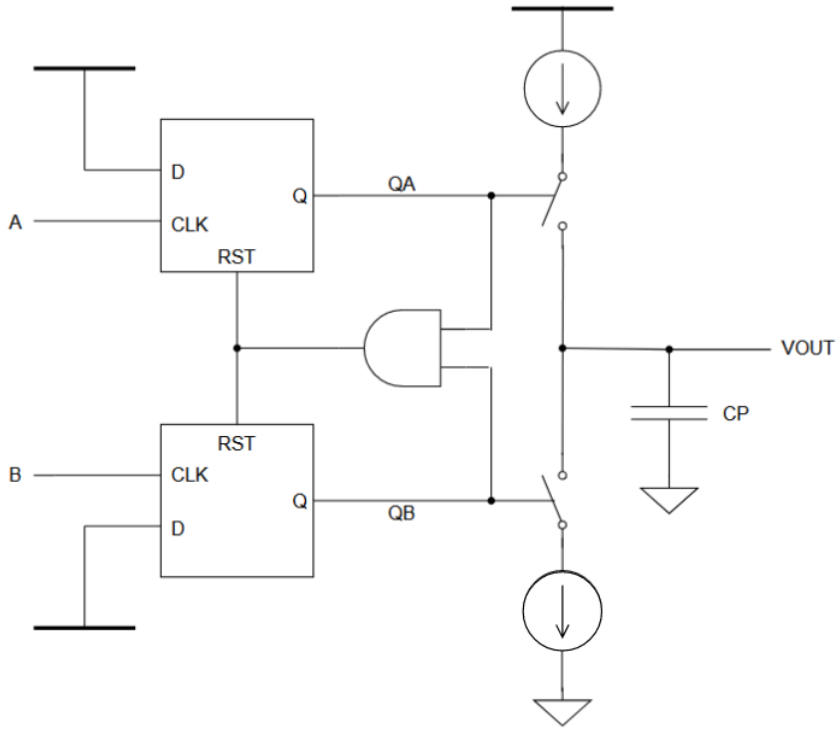

Figure 2.2: PFD/Charge-Pump (CP) schematic

2.2.2 Dynamics of a Charge-Pump PLL

The output characteristics of the PFD/CP are not strictly linear. However, by making an approximation and considering only the increase in the output voltage over an entire period of the frequency, the PFD/CP can be considered as a linear component. Its transfer function, employing this approximation, is:

$$\frac{V_{out}}{\Delta\phi}(s) = \frac{I_P}{2\pi C_P} \cdot \frac{1}{s} \tag{2.10}$$

This leads to an open-loop transfer function of:

$$\frac{\Phi_{out}}{\Phi}(s)|_{open} = \frac{I_P}{2\pi C_P} \cdot \frac{K_{VCO}}{s^2} \tag{2.11}$$

This equation presents a problem, as it results in two imaginary poles when calculating the closed-loop transfer function, making the system unstable. To address this issue, a small correction is applied by inserting a resistor R_P in series with the capacitor. The new transfer function of the PFD/CP becomes:

$$\frac{V_{out}}{\Delta\phi}(s) = \frac{I_P}{2\pi}(R_P + \frac{1}{C_P s}) \tag{2.12}$$

This results in an open-loop transfer function of:

$$\frac{\Phi_{out}}{\Phi}(s)|_{open} = \frac{I_P}{2\pi}(R_P + \frac{1}{C_P s})\frac{K_{VCO}}{s} \tag{2.13}$$

and a closed-loop transfer function of:

$$H(s) = \frac{\frac{I_P K_{VCO}}{2\pi C_P}(R_P C_P s + 1)}{s^2 + \frac{I_P}{2\pi} K_{VCO} R_P s + \frac{I_P}{2\pi C_P} K_{VCO}} \tag{2.14}$$

which can be represented as in 2.5. With this representation we derive the following equations:

$$\omega_n = \sqrt{\frac{I_P K_{VCO}}{2\pi C_P}} \tag{2.15}$$

$$\zeta = \frac{R_P}{2}\sqrt{\frac{I_P C_P K_{VCO}}{2\pi}} \tag{2.16}$$

With complex poles, the decaying time constant is given as $1/\zeta\omega_n = 4\pi/R_P I_P K_{VCO}$.

An important drawback of a CPPLL is that each time a current is injected into the loop filter, the control voltage experiences a significant jump. To mitigate this behavior, a parallel capacitor, smaller than C_P, is inserted inside of the loop filter. This elevates the PLL to third order, but selecting a smaller size of the capacitor (usually around one fifth to one tenth of C_P) pushes the third pole away.

2.2.3 Stability Issues of a CPPLL

The stability analysis of a CPPLL differs from that of a simple PLL. The open-loop transfer function exhibits two poles at the origin and a zero at $1/C_P R_P$. Consequently, the phase is -180° at small frequencies and increases to -90° around the zero. For an improved stability, the gain crossover should occur at higher frequencies, where the phase is far from -180°. This suggests, in contrast to a simple PLL, that increasing the loop gain ($I_P K_{VCO}$) leads to better stability. Equation 2.13 suggests that increasing R_P would increase the system's stability; however, in reality, an excessively high resistance degrades the stability.

2.2.4 Frequency Multiplication

A PLL can be modified to multiply its input frequency by an integer factor M. This modification involves placing a frequency divider in the feedback path. Since the transfer function between input and output is the same in the frequency domain, dividing the output frequency by the factor M and applying it to the phase detector results in $f_{out} = M f_{in}$. This alters the transfer system's transfer function:

$$H(s) = \frac{\frac{I_P K_{VCO}}{2\pi C_P}(R_P C_P s + 1)}{s^2 + \frac{I_P}{2\pi}\frac{K_{VCO}}{M} R_P s + \frac{I_P}{2\pi C_P}\frac{K_{VCO}}{M}} \tag{2.17}$$

Note that $H(s) \to M$ as $s \to 0$. We derive that 2.15 and 2.16 can be rewritten as:

$$\omega_n = \sqrt{\frac{I_P}{2\pi C_P}\frac{K_{VCO}}{M}} \tag{2.18}$$

$$\zeta = \frac{R_P}{2}\sqrt{\frac{I_P C_P}{2\pi}\frac{K_{VCO}}{M}} \tag{2.19}$$

Additionally, the decay time constant is modified to $(\zeta\omega_n)^{-1} = 4\pi M/(R_P I_P K_{VCO})$. Therefore, inserting a divider degrades both stability and settling speed, necessitating a proportional increase in the charge-pump current.

Figure 2.3 shows the graph of a PLL with frequency division.

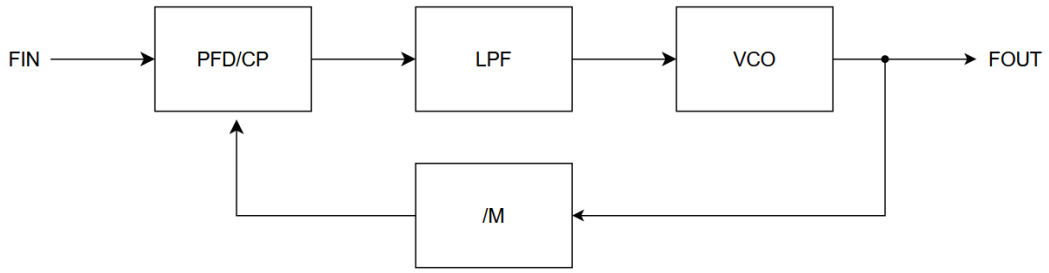

Figure 2.3: PLL with frequency division

This theoretical framework (2.2) is again based on the concepts presented in [4].

Chapter 3

Jitter in Phase-Locked Loops

3.1 Phase Noise and Jitter

3.1.1 Phase Noise

Considering an ideal oscillator, its output could be expressed as a perfect sinusoid, $V_{out} = V_0 \cos \omega_0 t$ and its spectrum consists of two pulses located at $\pm\omega_0$, meaning that the signal carries energies only at ω_0. However, in actual oscillators, circuit and system noise vary the period of oscillation randomly, meaning that the oscillator occasionally operates at frequencies other than ω_0. The zero crossings do not occur only at integer multiples of T_0, and the output spectrum presents some "skirts" around the two pulses of the original sinusoid. This type of noise can be represented as phase noise:

$$V_{out} = V_0 \cos \left[\omega_0 t + \phi_n(t)\right] \tag{3.1}$$

where $\phi_n(t)$ is a small random phase component with zero average. It (more specifically, its spectrum S_{ϕ_n}) is called phase noise. We derive that:

$$\begin{aligned} V_{out} &= V_0 \cos \omega_0 t \cos \left[\phi_n(t)\right] - V_0 \sin \omega_0 t \sin \left[\phi_n(t)\right] \\ &\approx V_0 \cos \omega_0 t - V_0 \phi_n(t) \sin \omega_0 t \end{aligned} \tag{3.2}$$

It follows that the spectrum of V_{out} consists of the sum of two pulses at $\pm\omega_0$ and the spectrum of $\phi_n(t)$, shifted by $\pm\omega_0$ due to the multiplication by $\sin \omega_0 t$, i.e., $S_{\phi_n}(\omega \pm \omega_0)$.

To quantify S_{ϕ_n}, we measure the average power carried in 1 (ore more) Hz at a specified "offset" frequency, $\Delta\omega$ from ω_0. Usually, the power measured in 1 Hz at $\omega_0 + \Delta\omega$ is normalized to the "carrier" power P_C, i.e. the power carried by the pulse at ω_0. The result is expressed as:

$$\text{Relative Phase Noise } |_{\Delta\omega} = 10 \log \frac{P_{1Hz}|_{\Delta\omega}}{P_C} \text{ dBc/Hz} \tag{3.3}$$

Another often used quantity is the so called single-side-band noise power to carrier power ratio $\mathscr{L}$, which is approximately half of the phase noise power spectral density [2].

3.1.2 Jitter

The jitter is a quantity closely related to the phase noise. If we have a signal whose zero crossings are not integer multiples of T_0, we can measure the deviation of each positive transition from its ideal point as ΔT_1, ΔT_2, etc. Since the deviations are random, we measure a very large number of deviations and determine the root mean square value of absolute jitters as:

$$\Delta T_{abs,rms} = \lim_{N\to\infty} \frac{1}{N}\sqrt{\Delta T_1^2 + \Delta T_2^2 + ... + \Delta T_N^2} \tag{3.4}$$

Since the jitter is very difficult to measure, it is beneficial to derive a relationship between jitter and phase noise. We derive that:

$$\begin{aligned}
\Delta T_{abs,rms}^2 &= \lim_{N\to\infty} \frac{1}{N}\sum_{j=1}^{\infty} \Delta T_j^2 \\
&= \left(\frac{2\pi}{T_0}\right)^2 \lim_{N\to\infty} \frac{1}{N}\sum_{j=1}^{\infty} \phi_{n,j}^2 \\
&\approx \left(\frac{2\pi}{T_0}\right)^2 \lim_{T\to\infty} \frac{1}{T}\int_{-T/2}^{+T/2} \phi_n^2(t)dt \\
&= \left(\frac{2\pi}{T_0}\right)^2 \int_{-\infty}^{+\infty} S_{\phi_n}(f)\, df
\end{aligned} \tag{3.5}$$

Noting that the deviation from the ideal zero crossings is $\Delta T_j = (2\pi/T_0)\phi_{n,j}$, where $\phi_{n,j}$ indicates the phase noise value in the vicinity of the ideal zero crossing j.

The variance of the long term absolute jitter is, using the single-side-band noise power to carrier ratio [2]:

$$\sigma^2 = \frac{2\int_0^{\infty} \mathscr{L}(f)\, df}{(2\pi f_{out})^2} \tag{3.6}$$

This theoretical framework (3.1) is based on the concepts presented in [5].

3.2 Jitter in a Charge-Pump PLL

To find the jitter in a CPPLL we first need to determine the phase noise of each component, which will be added to the signal, and the transfer function from that component to the output, which will determine how the phase noise produced by that component will propagate to the output. The main sources of noise are the input (phase noise coming from the reference), the VCO, and the loop (the PFD, the LPF and the divider).

3.2.1 VCO Noise

The transfer function from the VCO to the output is:

$$H_{VCO}(s) = \frac{1}{1 + G(s)} \tag{3.7}$$

Where G(s) denotes the open-loop transfer function. This transfer function presents high-pass filter characteristics, meaning that the VCO will dominate out-of-band. Usually the VCO has a phase noise of the form [2]:

$$\mathscr{L}_{VCO}(f) \propto \frac{1}{f^2} \tag{3.8}$$

3.2.2 CP Noise

In the PD/CP noise, the CP noise usually dominates. This noise appears as a noisy CP current, so we need to derive a transfer function from the CP output current to the PLL output. This transfer function has the form:

$$H_{CP}(s) = \frac{1}{\beta_{CP}} \cdot \frac{G(s)}{1 + G(s)} \tag{3.9}$$

where β_{CP} is the feedback gain from the PLL output to the CP output current. It can be derived that the feedback gain factor is:

$$\beta_{CP} = \frac{I_P}{2\pi} \cdot \frac{1}{M} \tag{3.10}$$

where I_P is the bias current of the CP. This means that the noise from the CP will dominate in-band. The power spectral density of the noise coming from the CP can be estimated to be [2]:

$$S_{iCP,n,PFD} = 8kT\gamma g_m \frac{\tau_{PFD}}{T_{REF}} \tag{3.11}$$

where γ is a noise model parameter of the MOS transistor, g_m is the transconductance of a single MOS transistor, τ_{PFD} is the fraction of time for which the CP is switched in the steady state and T_{REF} is the period of the reference. Thus, the in-band phase noise seen at the output of the PLL due to the CP will be [2]:

$$\mathscr{L}_{in-band,CP} \approx \frac{1}{2} S_{iCP,n} |H_{CP}(s)|^2 \approx \frac{S_{iCP,n}}{2\beta_{CP}^2} \tag{3.12}$$

meaning that the noise from the CP will be significant due to the multiplication with the square of the division factor M.

3.2.3 Reference Noise

Finally, we concentrate on the noise coming from the reference. This phase noise comes from both the crystal oscillator and the buffer, usually an inverter used to sharpen the waveform produced by the crystal. We have already seen that a CPPLL presents low-pass filter characteristics, suggesting that slow jitter at the input propagates to the output unattenuated, while fast jitter does not.

The transfer function from the reference is:

$$H_{loop}(s) = M \frac{G(s)}{1 + G(s)} \tag{3.13}$$

The phase noise of an inverter due to the transistors' white noise is expressed as [1]:

$$S_{REF}(f) = \frac{\pi^2}{SR_{out}^2 C_L^2} \frac{\Delta T}{T_{REF}} [S_{I,N}(f) + S_{I,P}(f)] \tag{3.14}$$

where SR_{out} denotes the slew rate at the output of the inverter, C_L the load capacitance, ΔT the time window (approximately half the rise time) in which the transistors produce a thermal noise envelope, and $S_{I,N}$ and $S_{I,P}$ are respectively the noise current spectra of the NMOS and PMOS devices.

As a result, the reference noise, as the CP noise, will dominate in-band. This phase noise, seen at the output of the PLL, will be:

$$\mathscr{L}_{in-band,REF} \approx \frac{1}{2} S_{REF} |H(s)|^2 \approx \frac{1}{2} S_{REF} M^2 \tag{3.15}$$

We note that, similarly to the case of the CP noise, this phase noise will be significant due to the multiplication with the square of the division factor M.

Chapter 4

16-GHz Double-Sampling PLL Analysis

The PLL explored and analyzed in this Bachelor Project is the so-called Double-Sampling PLL. Instead of using D-Flip-Flops for the phase detection, followed by a CP, this PLL employs a double-sampling PD, followed by a Operational Transconductance Amplifier (OTA), which injects current into the loop filter. The goal is to reduce the in-band noise, which is significant in a CPPLL, mainly because of the CP and the multiplication with the square of the division factor M. The rest of the PLL is similar to the Simple PLL.

The intended application of such PLL takes a crystal with frequency of 100 MHz, while the output frequency must reach 16 GHz. This implies a division factor of 160, making the multiplication by M^2 significant in the noise analysis of the PLL and its design challenging.

4.1 PLL Architecture

In this PD the output signal, after being divided by M, samples the reference signal. Let us first take into consideration only a single-sampling PD. The divided output signal is passed through a non-overlap clock generator, which produces two phases ϕ_1 and ϕ_2; ϕ_1 follows the divided phase, while ϕ_2 follows the inverted divided phase. They do not overlap, i.e. they are never both high at the same time. These two phases are used to sample the reference signal; when ϕ_1 is high, the voltage V_1, shown in Figure 4.1, tracks the reference, and when ϕ_2 is high, the voltage V_3 assumes the new value of V_1. The result is that the output voltage will be equal to the value of V_{REF} when ϕ_1 goes from high to low.

Let us assume that the PLL is in the locked state, ϕ_1 and ϕ_2 sample the rising edges of V_{REF}, and the phase of V_{REF} increases, meaning that the signal is shifted to the left. Therefore, the value that ϕ_1 and ϕ_2 sample will be greater, providing the circuit with the basic characteristic of a PD. The PD's gain is expressed as [1]:

$$K_{PD} = \frac{SR_{REF}}{2\pi f_{REF}} \tag{4.1}$$

Let us now take into consideration the double-sampling PD. From the divided frequency, we generate, in addition to ϕ_1 and ϕ_2, also $\overline{\phi_1}$ and $\overline{\phi_2}$. If, for example, ϕ_1 and ϕ_2 sample the rising edges of V_{REF}, $\overline{\phi_1}$ and $\overline{\phi_2}$ will sample the falling edges of V_{REF}. Now, let us assume that the phase of V_{REF} increases; V_3, shown in Figure 4.2, increases, while V_4 decreases. If we take the difference between V_3 and V_4, it will increase, providing the circuit with the basic characteristic of a PD, as for the single-sampling case. The PD's gain, since we are sampling both the rising and falling edges of V_{REF} and taking their difference, is going to be the double of the PD's gain in the single-sampling case:

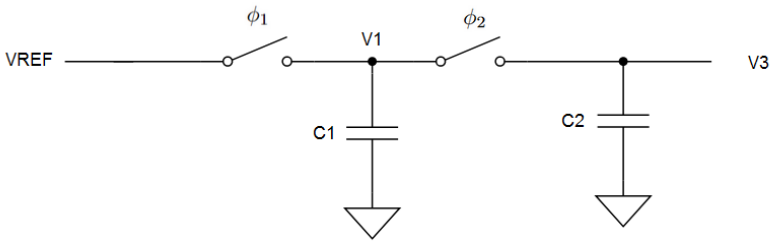

Figure 4.1: Single-Sampling PD

$$K_{PD} = \frac{SR_{REF}}{\pi f_{REF}} \tag{4.2}$$

The sampled values of V_{REF} provide the inputs for an OTA. Once the PLL is in the locked state, the OTA stops injecting current into the loop filter and the tuning voltage is supposed to stay constant.

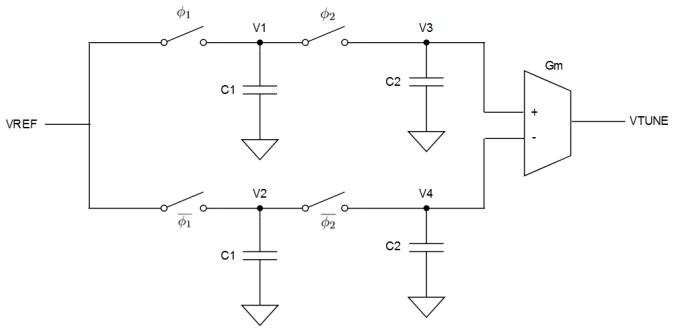

Figure 4.2: Double-Sampling PD

The loop filter is the same as the CPPLL's; the series combination of a capacitor and a resistor provides a zero and a pole to the open-loop transfer function, while the parallel capacitor is supposed diminish the skews of the tuning voltage. The value of this capacitor should be small, in comparison to the other capacitor, in order to add a second pole (which can be neglected) far from the origin to the open-loop transfer function.

4.2 Double-Sampling PLL Dynamics

4.2.1 PD Transfer Function

We have already derived the gain of the PD. It can be shown that the transfer function of the PD is the following [1]:

$$H_{PD}(s) = \frac{SR_{REF}}{\pi f_{REF}} \cdot \frac{1}{1 + \frac{C_2}{C_1 f_{REF}} s} \cdot \frac{1 - e^{-sT_{REF}}}{sT_{REF}} \tag{4.3}$$

Since the bode plot of this transfer function is quite flat in the bandwidth of the PLL, it can be ignored, while taking into consideration only the factor K_{PD}.

4.2.2 Open-Loop Transfer Function

The open-loop transfer function is given by:

$$\begin{aligned} H(s)|_{open} &= \frac{K_{PD}K_{VCO}}{s} g_m \left(R_P + \frac{1}{sC_{P1}}\right) || \left(\frac{1}{sC_{P2}}\right) \\ &= \frac{K_{PD}K_{VCO}g_m}{s^2} \frac{sR_PC_{P1}+1}{sC_{P1}C_{P2}R_P + C_{P1} + C_{P2}} \\ &\approx \frac{K_{PD}K_{VCO}g_m}{s^2} \frac{sR_PC_{P1}+1}{sC_{P1}C_{P2}R_P + C_{P1}} \end{aligned} \tag{4.4}$$

This transfer function has the same structure of a CPPLL's transfer function, but instead of the CP's bias current I_P, we find the terms K_{PD} and g_m. It reveals two poles at the origin, one zero at $1/R_PC_{P1}$ and a third pole at $1/R_PC_{P2}$. To analyze the stability of the closed-loop system we need to divide this transfer function by the division factor M = 160; this will lower the gain crossover. Given C_{P1}, to obtain the best phase margin, R_P must be chosen such that the peak of the phase is reached at the same frequency as the gain crossover. Finally, C_{P2} must be chosen in way that the phase can reach -120 degrees to guarantee a phase margin of around 60 degrees.

In the final design of the PLL, presented in chapter 5, the parameters of the circuit are the following: $K_{PD} = SR_{REF}A_{v,inv}$ / πf_{REF}, where $A_{v,inv}$ is the gain of the inverter, used as buffer of the reference, and is equal to 12.5 (5.4); K_{VCO} = 0.0139 GHz/mV (5.1); g_m = 0.228 μA/V (5.3.3); R_P = 30 kΩ, C_{P1} = 5 pF, C_{P2} = 500 fF (5.5). Figure 4.3 shows the open-loop transfer function bode plot obtained from these parameters; the calculated phase margin is 54 degrees.

4.2.3 Closed-Loop Transfer Function

To analyze the closed-loop transfer function and find out its step response characteristics, we omit the parallel capacitor C_{P2}. Therefore, we derive that the closed-loop transfer function is:

$$H(s) = \frac{\frac{K_{PD}K_{VCO}g_m}{C_{P1}}(R_PC_{P1}s+1)}{s^2 + \frac{K_{PD}K_{VCO}g_mR_P}{M}s + \frac{K_{PD}K_{VCO}g_m}{MC_{P1}}} \tag{4.5}$$

Yielding the characteristic frequency and the damping ratio of:

$$\omega_n = \sqrt{\frac{K_{PD}K_{VCO}g_m}{MC_{P1}}} \tag{4.6}$$

$$\zeta = \frac{R_P}{2}\sqrt{\frac{K_{PD}K_{VCO}g_mC_{P1}}{M}} \tag{4.7}$$

As for the case of the CPPLL, the division by M degrades the stability of the loop.

Figure 4.4 shows the closed-loop transfer function's bode plot with the parameters of 4.2.3, while Figure 4.5 shows the step response forecast by this transfer function.

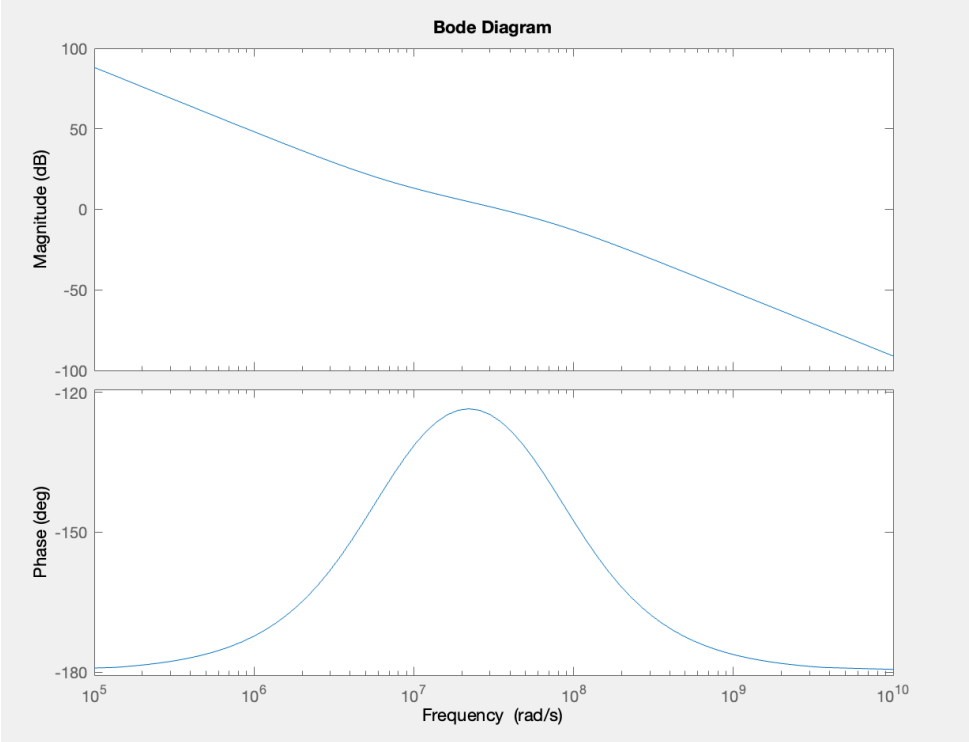

Figure 4.3: Bode Plot of the open-loop transfer function

4.3 Phase Noise and Jitter

The main advantage of this PLL is the reduction of the reference noise. Let us assume that the rising edge of V_{REF} is displaced by Δt_1 and the falling edge by Δt_2. This translates in a shift of V_3 and V_4 by, respectively:

$$\Delta V_3 = \Delta t_1 SR_{REF} \tag{4.8}$$

$$\Delta V_4 = \Delta t_2 SR_{REF} \tag{4.9}$$

And therefore the differential output noise of the PD is [1]:

$$\overline{V_{n,out}^2} = SR_{REF}^2(\sigma_{\Delta t_1}^2 + \sigma_{\Delta t_2}^2) \tag{4.10}$$

where $\sigma_{\Delta t_1}^2$ and $\sigma_{\Delta t_2}^2$ are respectively the jitter of the rising and falling transitions of V_{REF}. Hence, the phase noise referred to the PD input is:

$$\phi^2 = \frac{\pi^2}{T_{REF}^2}(\sigma_{\Delta t_1}^2 + \sigma_{\Delta t_2}^2) \tag{4.11}$$

which, converted to jitter, results in:

$$\overline{\sigma_j^2} = \frac{\sigma_{\Delta t_1}^2 + \sigma_{\Delta t_2}^2}{4} \tag{4.12}$$

proving a 3-dB reduction of the phase noise of both the crystal and the reference buffer, since the double-sampling PD averages the jitter of the falling and rising edges.

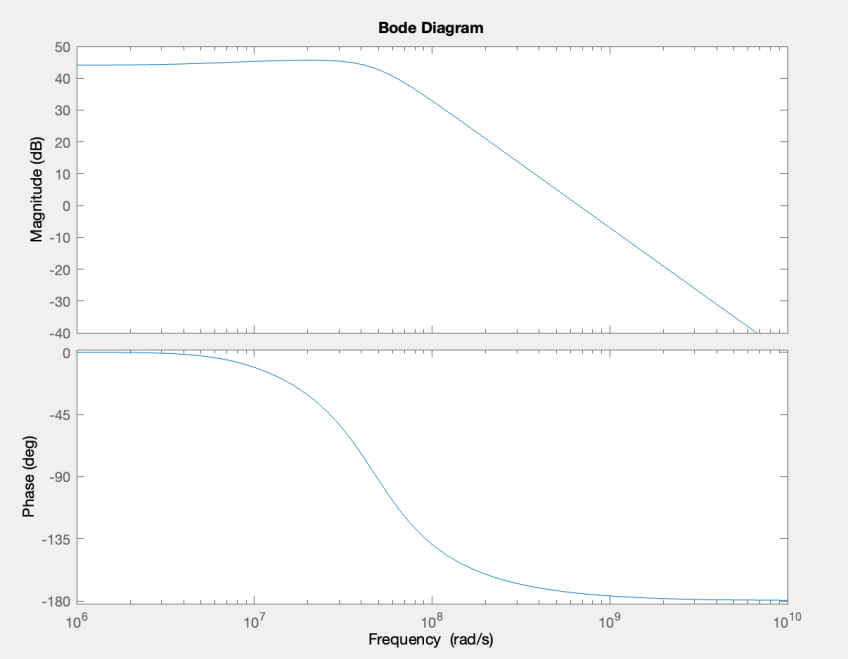

Figure 4.4: Bode Plot of the closed-loop transfer function

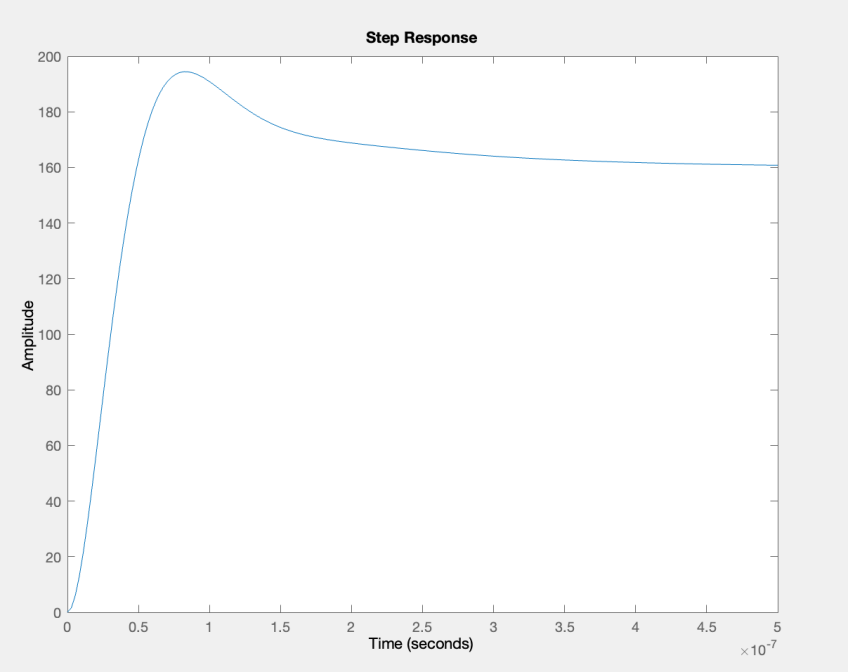

Figure 4.5: Step response of the closed-loop system predicted by MATLAB

Chapter 5

Double-Sampling PLL Implementation

Throughout the project, I focused on building the schematic of the PLL on Cadence, simulating it, and making improvements based on the simulation results. In this chapter, I will go through the implementation of the PLL at a schematic level and show the properties of the single components.

5.1 VCO

The first analyzed component is the VCO. It is a ring oscillator with a frequency controlled by varactors, with a range of around 1 GHz around the target frequency of 16 GHz.

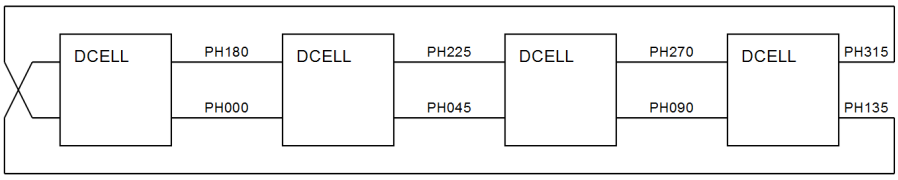

Figure 5.1: Ring oscillator's schematic

5.1.1 VCO Architecture

The VCO is differential; it contains 4 cells with an inverted feedback, thus providing 8 phases. This is shown in Figure 5.1. The oscillation frequency is controlled by a varactor (Figure 5.3): the load of each inverter is the source of a PMOS transistor, whose gate is controlled by the tuning voltage. The drain of the PMOS is connected to a capacitance made out of a couple of transistors with bulk, source and drain shorted. The effect of the varactor is thus providing a voltage-controlled capacitance as load of the inverter, changing the time needed for the inverter to invert its input.

5.1.2 VCO Simulation Results

For the analysis of PLL, we need to determine the gain of the VCO, K_{VCO}, which is 0.0139 GHz/mV around the settling point. The power consumed by the VCO is 1.49 mW, making it the main source of power consumption of the PLL.

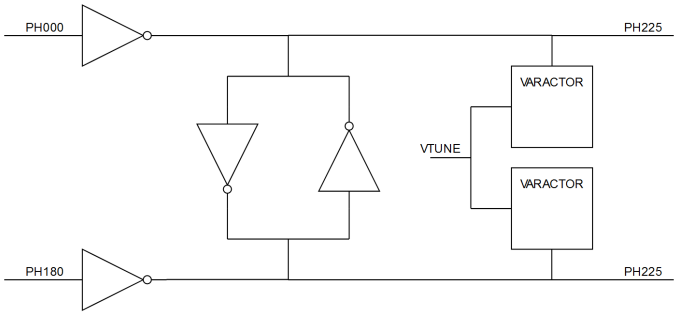

Figure 5.2: Single inverter cell

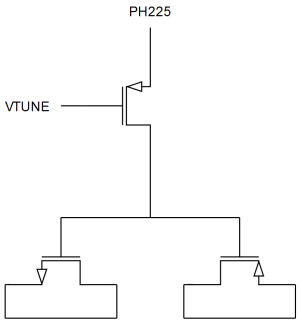

Figure 5.3: Varactor

Moving on to the PSS and PNOISE analysis, choosing 16 GHz as the beat frequency and 30 output harmonics, Figure 5.4 shows the power spectral density of the harmonics. The phase noise profile, plotted over a sweep range between 1 mHz and 2 GHz (Figure 5.5), is shown in Figure 5.5; the phase noise has a decay of 29 dBc/Hz per decade. Finally, the jitter obtained by integrating the phase noise is 43.8 fs.

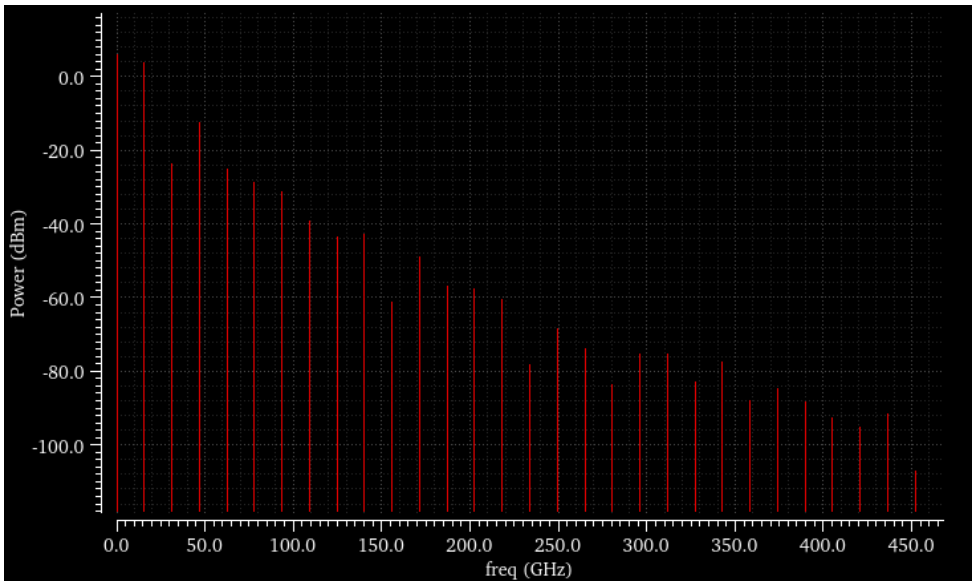

Figure 5.4: Power spectral density at the multiples of 16 GHz

5.2 Divider

The second component of the analysis is the divider. It divides the output frequency, 16 GHz, by 160, reaching the input frequency of 100 MHz.

5.2.1 Divider Architecture

The divider is composed of four 2-dividers and one 10-divider in series, reaching a division factor of 160. The 2-dividers are made out of a D-Flip Flop where the negative output, $\overline{Q}$, is fed

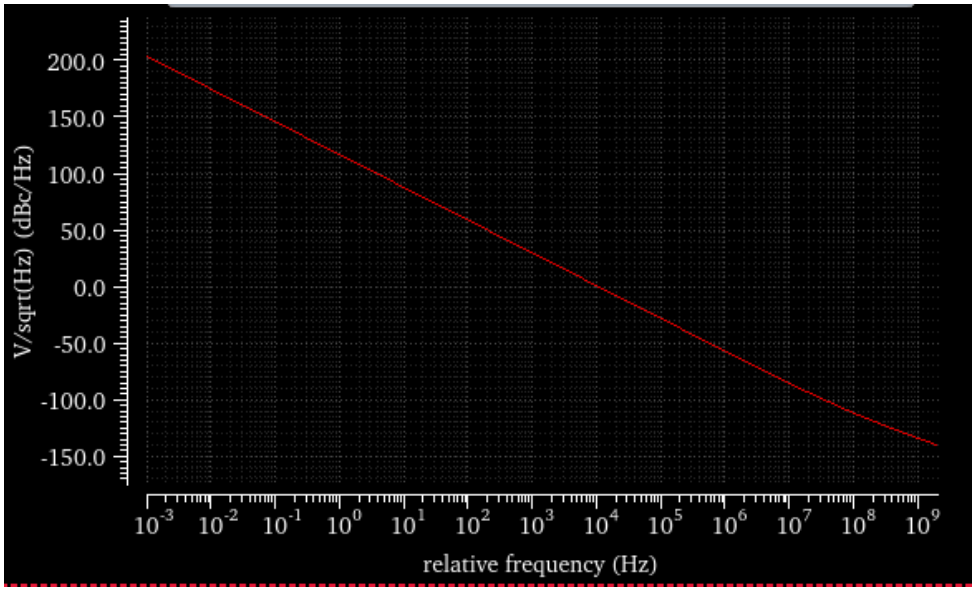

Figure 5.5: Phase noise profile

back to the input of the D-Flip Flop and the clock is given by the frequency to be divided; the D-Flip Flops are in turn made out of NAND gated SR-latches. Figure 5.7 shows the schematic of the 2-divider.

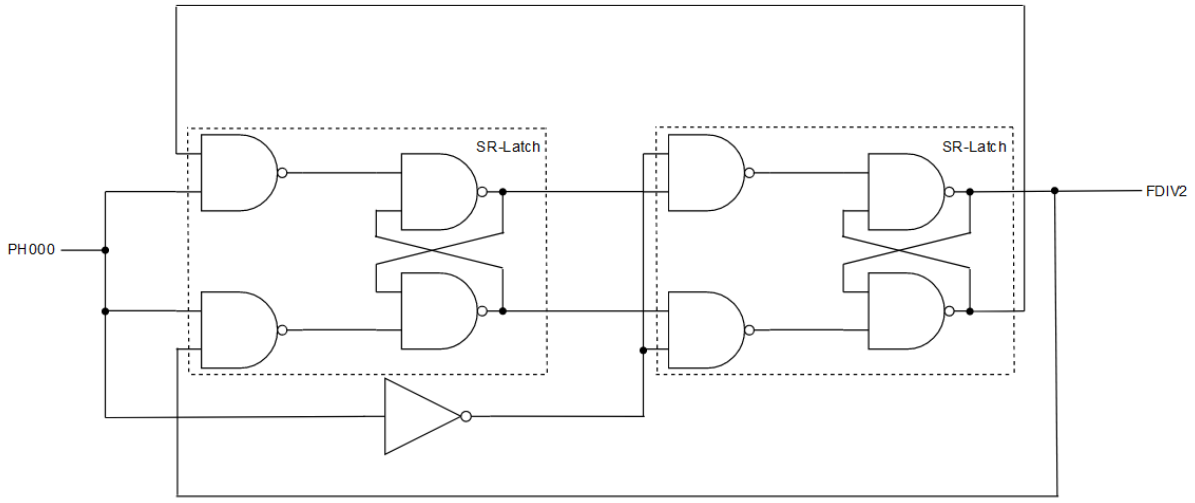

Figure 5.6: 2-Divider schematic

The 10-divider is made out of a 2-divider and a 5-divider. The 5-divider is implemented as a 3-bit counter, using three 2-dividers in series and resetting as soon as the counter has arrived at the 5th bit. The three 2-dividers now incorporate a negative reset, which is activated by the NAND combination of the output of the first and third 2-dividers. Note that the duty cycle of the 5-divider is not 50%, but this issue is solved by putting the 2-divider after the 5-divider, as the 2-divider is sensitive only to the transition from 0 to 1.

The negative reset is incorporated inside the 2-dividers by using 3-ports NAND gates, where

one of the ports is the negative reset.

The power consumption is 0.219 mW.

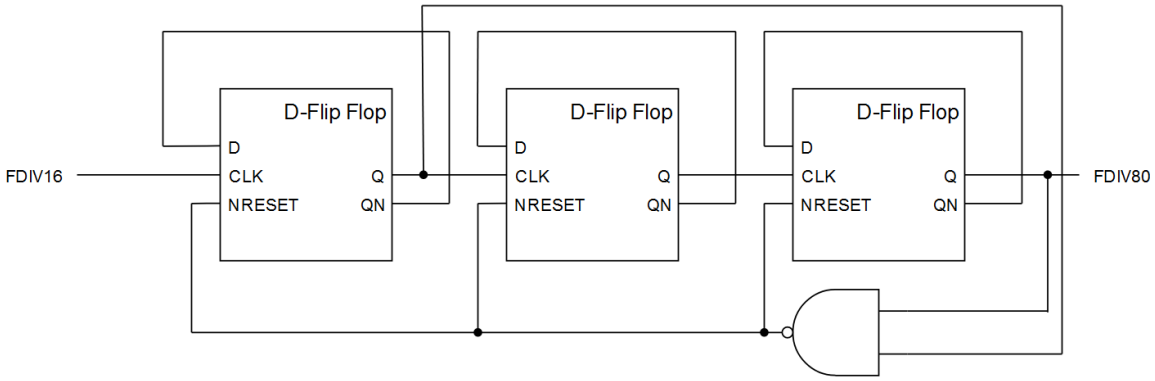

Figure 5.7: 10-Divider schematic

5.2.2 Divider Simulation Results

Moving on to the phase noise analysis, we have 5 nodes to analyze. Figure 5.8 shows the phase noise profile of the 160-divided frequency, 16-divided frequency, 8-divided frequency, 4-divided frequency, and 2-divided frequency, plotted over a sweep range between 1 kHz and half of the corresponding frequency.

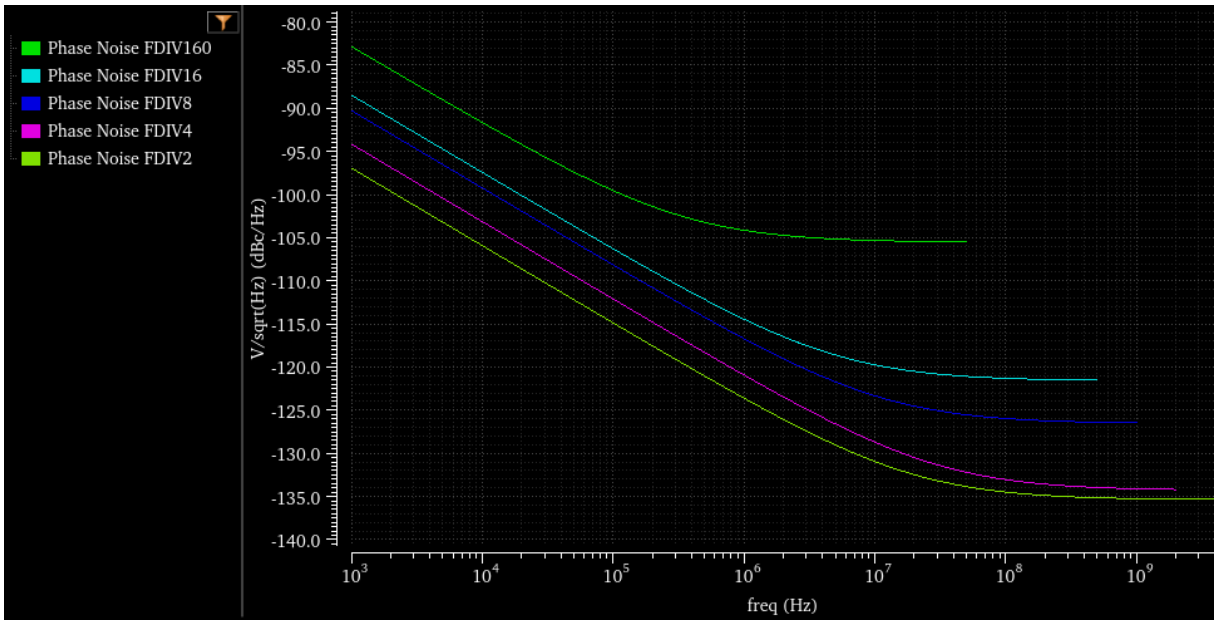

Figure 5.8: Phase Noise of the divider's nodes

Finally, the jitters of the 2-divided frequency, 4-divided frequency, 8-divided frequency, 16-divided frequency and 160-divided frequency are, respectively, 42 fs, 108 fs, 190 fs, 249 fs and

362 fs.

5.3 Phase Detector

Let us now move on to the phase detector, which is composed of the three components I am going to analyze next: the non-overlap generator, the double-sampling unit, and the Gm stage. The high-level schematic of the phase detector is shown in Figure 5.9; ϕ_1 and ϕ_2 are generated from the divided frequency, $\overline{\phi_1}$ and $\overline{\phi_2}$ are generated from the inverse of the divided frequency; they are used to sample the reference and the difference of the sampled voltages is amplified by the OTA.

The total power consumption of the PD is 0.087 mW.

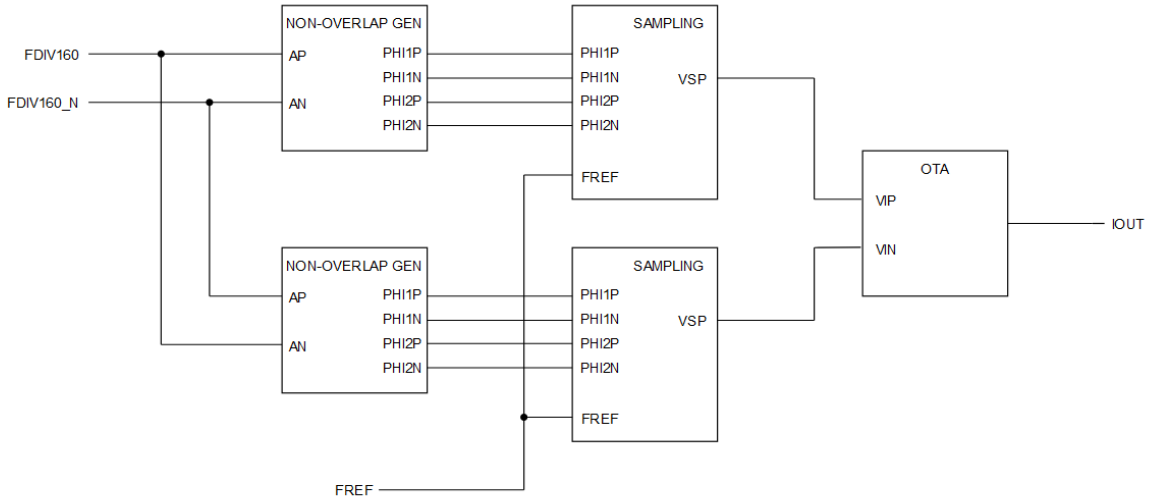

Figure 5.9: Phase Detector schematic

5.3.1 Non-Overlap Generator

The structure of the non-overlap generator is the traditional one; the goal is to create two phases from the input phase, which will be used to sample the reference. These two generated phases must not overlap, in order to avoid charge sharing. The schematic of the non-overlap generator is shown in Figure 5.10: the NAND combinations of CLK and delayed $\overline{\phi_2}$, $\overline{CLK}$ and delayed $\overline{\phi_1}$ produce, after being delayed in order enable the non-overlap generation, respectively, $\overline{\phi_1}$ and $\overline{\phi_2}$.

Figure 5.11 shows ϕ_1 and ϕ_2 generated by the divided frequency. As already said in 4.1, ϕ_1 follows the signal generated by the divider, while ϕ_2 follows the inverse of the signal generated by the divider.

5.3.2 Single-Sampling Unit

The double-sampling unit, made out of two single-sampling units, is again the traditional one. It uses both PMOS and NMOS transistors to sample the reference; the gates of the transistors

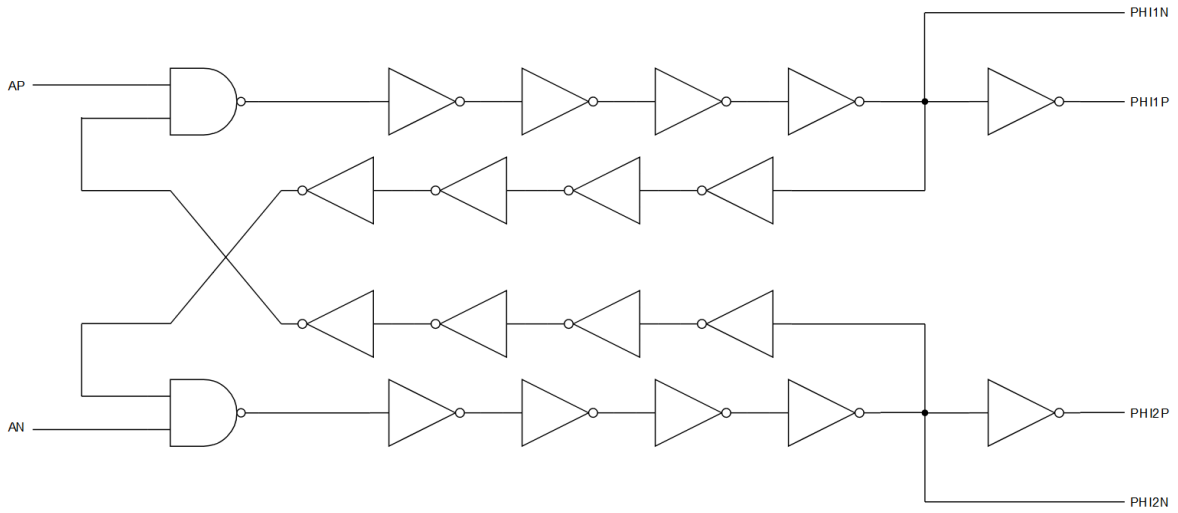

Figure 5.10: Non-Overlap Generator schematic

are activated by the phases generated by the non-overlap generator. The schematic of the single sampling unit is shown in Figure 5.12. The values chosen for the capacitors that will hold the charge are 100 fF and 44 fF for, respectively, C_1 and C_2.

5.3.3 Operational Transconductance Amplifier

The chosen design for the OTA is the following:

1. Input stage: a differential pair, consisting of NMOS transistors, takes the input;
2. Load stage: a couple of diode-connected PMOS transistors acts like active load of the NMOS differential pair;
3. Current mirror stage: the current flowing through the PMOS loads is mirrored into other transistors; the current of one of these current mirrors is mirrored again to allow a single-ended output.

The gain of the OTA can be chosen by varying the division ratio of the current mirrors. For the final design, the measured gain of the OTA is 0.228 μA/V.

Figure 5.13 shows the schematic of the OTA.

5.4 Reference Buffer

The sinusoidal input of the PLL comes from a crystal, which cannot be put directly in contact with the PLL. In the original PLL design the buffer at the input was a couple of inverters, with the result that the input was a square wave. However, the slew rate deriving from a couple of inverters increases excessively the gain, and the PD stops working. Therefore, the reference buffer consists of a single inverter (which will shift the phase by 180 degrees, but this does not represent a problem for the intended application of the PLL).

Figure 5.11: Signals generated by the non-overlap generator; the display range of the divided frequency, FDIV160, has been slightly changed for clarity, while the phase has not been modified

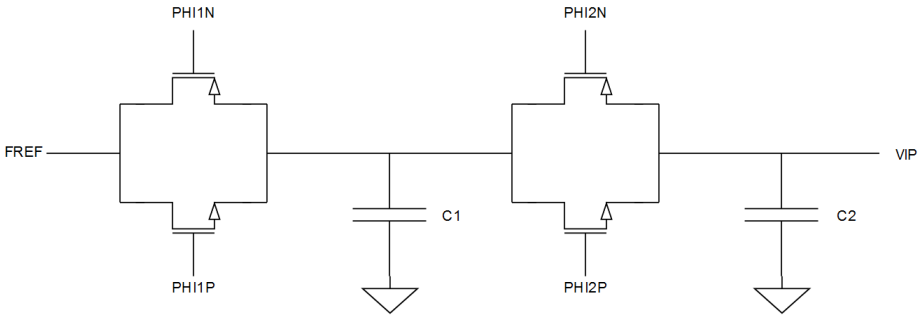

Figure 5.12: Single-Sampling schematic

The power consumption of the reference buffer is 0.009 mW, while the simulated jitter is 6 ps. The gain of the inverter is 12.5 around its operating point, i.e. where the divided phases sample the reference. This translates in a multiplication by 12.5 of the slew rate.

5.5 Loop Filter

The parameters of the components of the loop filter need to be chosen accordingly to the other parameters of the circuit, as the considerations in 4.2.2 show, to ensure a better stability. The chosen values for the final design are $R_P = 30$ kΩ, $C_{P1} = 5$ pF and $C_{P2} = 500$ fF.

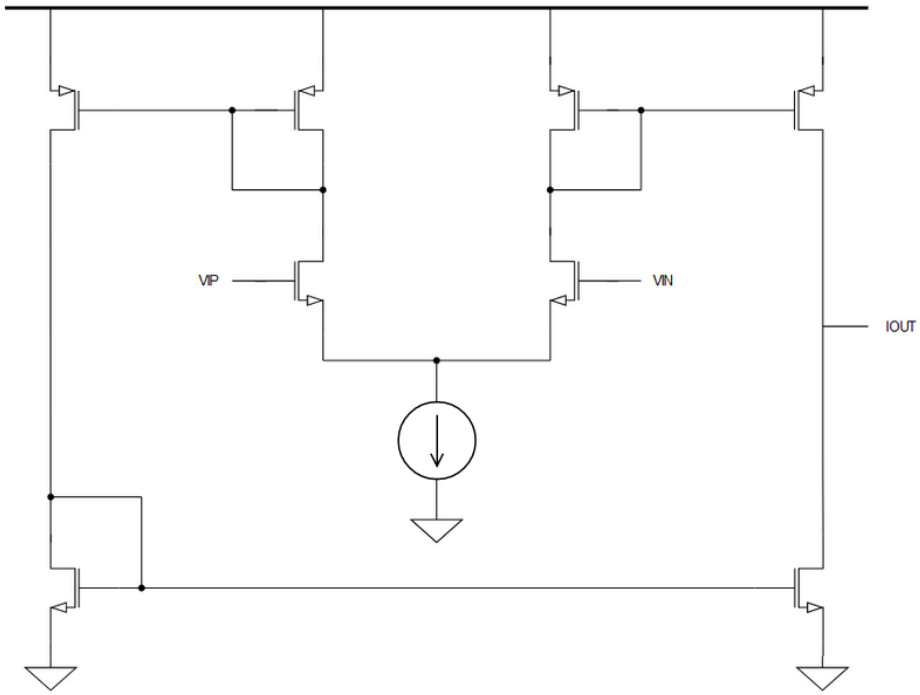

Figure 5.13: OTA schematic

Chapter 6

Results

The PLL with the parameters listed in chapter 5 achieves a jitter of around 1 ps, when plotting over a period of 200 ns. This value has been obtained with the eye tool provided by Cadence, since the PSS and PNOISE analysis were not feasible for this PLL. Figure 6.1 shows the plotted eye diagram resulting from the output frequency.

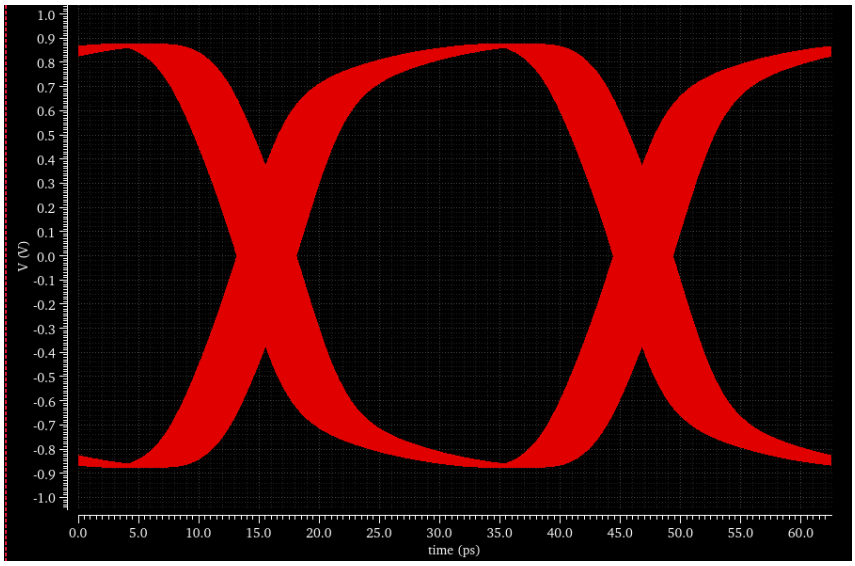

Figure 6.1: Eye Diagram of the output frequency

Figure 6.2 shows the eye diagrams of all the other frequencies produced by the divider.

Regarding the settling behavior, it takes 1.8 μs for the circuit to settle to the locked state; this value is higher than the settling time of the original PLL, which was 0.8 μs. However, when increasing the gain of the OTA or the slew rate of the reference, the value of the settling time decreases significantly; the trade-off in this case is a bigger value for the jitter. The value of VDD is 900 mV.

Figure 6.4 shows the behavior of V_{TUNE}, the voltage that controls the VCO (which is proportional to the output frequency), from the beginning of a simulation to the point where the PLL enters the locked state.

Figure 6.4 shows the step response of the PLL when applying a 90-degree phase step to the reference.

To demonstrate that the analysis of the transfer function obtained from MATLAB is correct (or at least indicative of the order of magnitude of the loop filter's parameters), Figures 6.5 and 6.6 show the behavior of the PLL when choosing the same value for the capacitors, but different

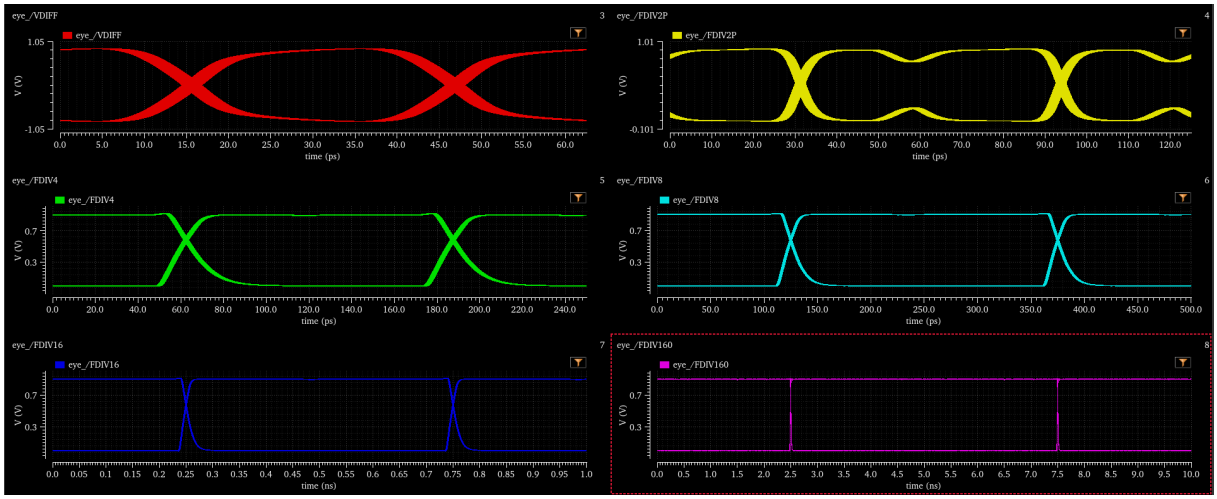

Figure 6.2: Eye Diagram of the frequencies generated by the divider

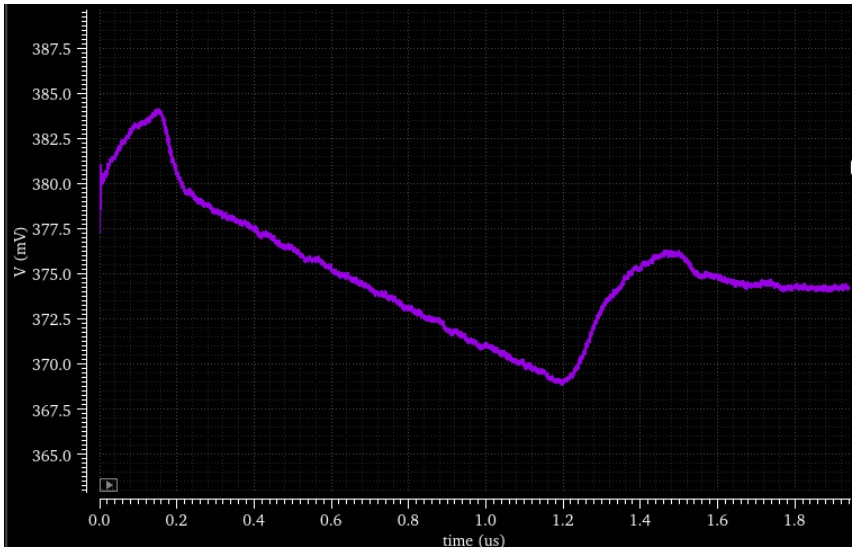

Figure 6.3: V_{TUNE} transient response

resistances (which corresponds to moving the zero away from the gain crossover). Specifically, Figure 6.5 shows the behavior of the circuit with $R_P = 1$ kΩ and Figure 6.6 with $R_P = 150$ kΩ.

With $R_P = 1$ kΩ, the pole and the zero move away from the gain crossover, resulting in a very small phase margin; in this case, the circuit does not even converge. With $R_P = 150$ kΩ, the zero and the pole due to the parallel capacitor are shifted too much towards the origin, therefore significantly degrading the phase margin; an excessively small phase margin translates in a high susceptibility to noise. Although the PLL reaches its settling point, it keeps oscillating around it, never fully reaching the locked state.

The power consumed by the PLL is 1.88 mW, which is slightly higher than the power consumed by the original PLL design, 1.80 mW. Most of it comes from the VCO and the divider.

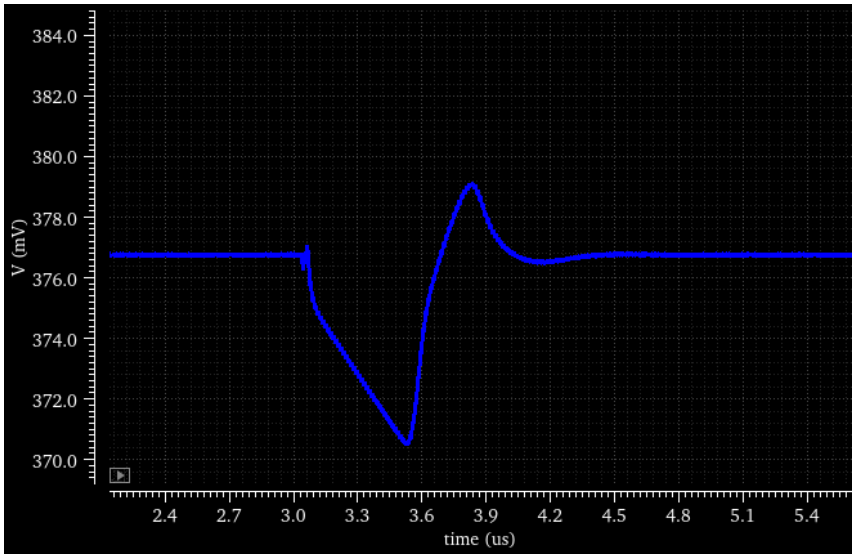

Figure 6.4: 90-degree step response of V_{TUNE}

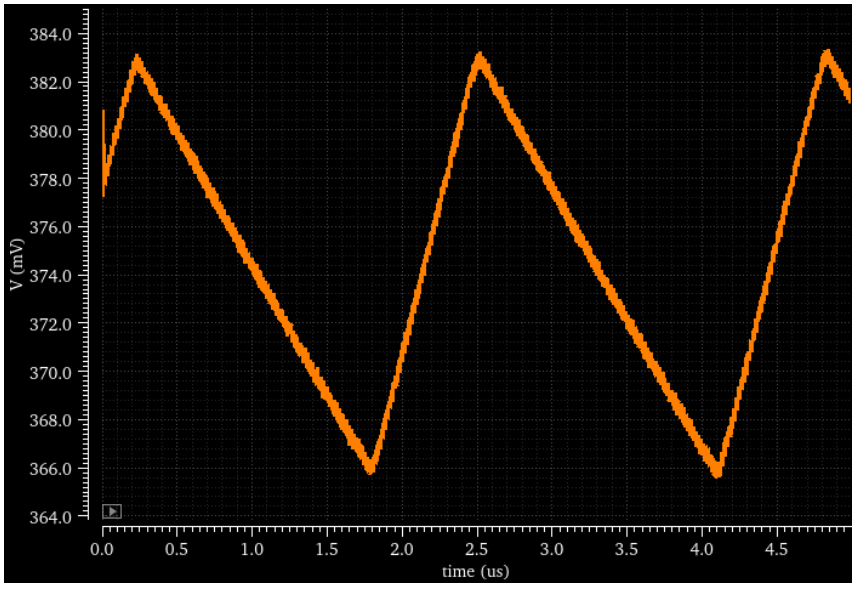

Figure 6.5: V_{TUNE} transient response with $R_P = 1$ kΩ

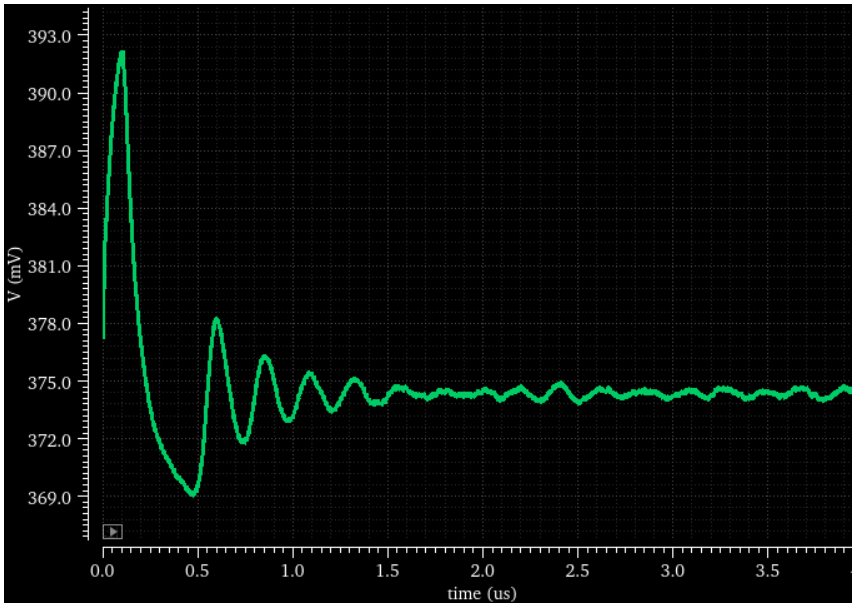

Figure 6.6: V_{TUNE} transient response with $R_P = 150$ kΩ

Chapter 7

Possible Improvements

The design of the PLL is not complete from some points of view and still needs some improvements.

From the jitter perspective, the obtained jitter is quite good; however, it happens that the PLL gets out of phase, and in this case, it takes some time for the PLL to return to the locked state. Therefore, when plotting the eye diagram over longer periods, there are groups of zero crossings at different positions from the ideal one, increasing the calculated jitter. This problem can potentially be addressed by means of duty cycle correction, as shown in [1]; in fact, due to the buffer, the generated phases do not sample the reference exactly at $V_{DD}/2$, and this originates the mentioned phenomenon. Additionally, controlling the slew rate of the reference could also reduce the jitter of the output.

Another issue with the design is that the VCO has a very low gain when the tuning voltage is low: since the capacitance seen by the inverters is controlled by a PMOS transistor, at low voltages the PMOS is completely open and is not sensitive to changes of V_{TUNE}. I have overcome this issue by putting NMOS transistors on top of the NMOS transistor mirroring the current from the left branch of the OTA, as shown in Figure 7.1. This transistor shifts up the common mode of V_{TUNE}, making it come to a point where the VCO is more sensitive to changes in the tuning voltage; I recognize that this solution is not optimal and could be improved.

Finally, an alternative topology could be considered for the OTA, possibly consuming less power and introducing less noise in V_{TUNE}.

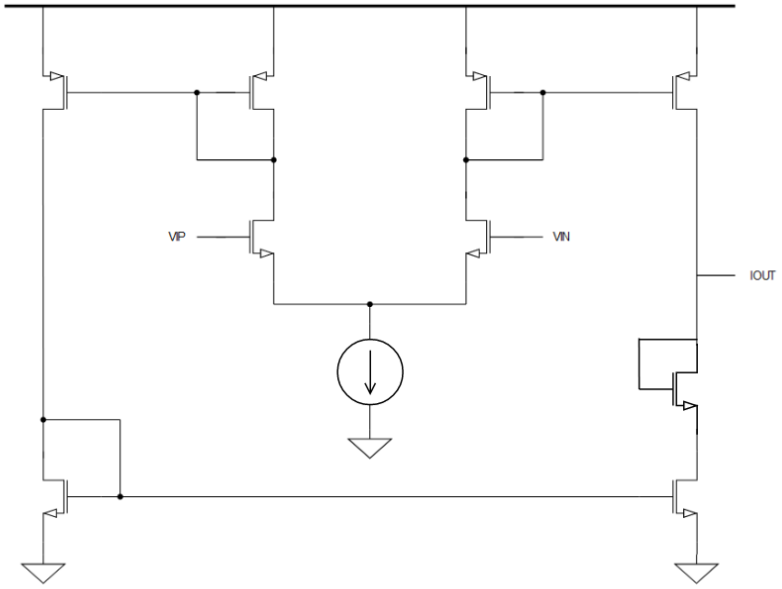

Figure 7.1: OTA increasing the common mode of V_{TUNE}

Chapter 8

Conclusion

This report addresses the problem of minimizing the jitter in PLLs. Initially, it gives a general overview of the existing types of PLLs, followed by an analysis of the various sources of phase noise in a PLL. Subsequently, it presents the work I have conducted throughout the project: starting from an already implemented CPPLL, I have experimented with various types of new PLLs, and focused on the one that yielded best results while considering area and power constraints dictated by the intended application.

Therefore, the thesis analyzes specifically the double-sampling PLL. First, I focused on optimizing the stability of the system and identifying the most effective combination of parameters; next, the thesis presents the schematics and the parameters of the design implemented in Cadence. Finally, it showcases the results obtained at the project's conclusion and outlines the possible improvements that could be undertaken to finalize the project.

I believe that I learned a lot throughout the project; I acquired familiarity with PLLs and the problem of jitter optimization; I explored the various techniques that have been implemented to address this problem; finally, I gained a lot of experience with Cadence, which is the main software I have been working on, and the way of analyzing and solving a problem in analog circuit design.

Acronyms

CP Charge-Pump. 4, 5, 10–12, 14

CPPLL Charge-Pump PLL. 4, 6, 9, 10, 12–14, 31

LPF Low-Pass Filter. 2, 3, 9

OTA Operational Transconductance Amplifier. 12, 13, 21, 22, 24, 25, 29, 30

PD Phase Detector. 2–4, 10, 12, 13, 15, 21, 22

PFD Phase-Frequency Detector. 4, 5, 9

PLL Phase-Locked Loop. ii, 1–4, 6, 7, 10–15, 17, 22, 25, 26, 29, 31

VCO Voltage-Controlled Oscillator. 2–4, 9, 10, 17, 25, 26, 29

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