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MSM8974 PMIC Software Driver Overview

80-NA157-49 A



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Revision History

Version	Date	Description
A	Aug 2012	Initial release

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Introduction

Objectives

- At the end of this presentation, you will understand PMIC software architecture for MSM8974.

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Feature Comparison



Feature Comparison

Block	Feature	PM8921	PM8941	PM8841
Input power management	Regulation type	Switch mode	Switch mode with Boost mode	N/A
	Charger pass device	Integrated	Integrated	N/A
	# of charger paths	2	2	N/A
	Path 1 OVP	28 V	28 V	N/A
	Path 2 OVP	External	15V	N/A
	Max charger current	2 A	3 A	N/A
	Autonomous charger	Yes	Yes	N/A
	Trickle charger	Yes	Yes	N/A
	Trickle charger indicator	Yes	Yes	N/A
	CC/CV charging	Yes	Yes	N/A
	Pulse charger	No	No	N/A
	USB Charger	Yes	Yes	N/A
	USB FLCB	Yes	Yes	N/A
	BATFET	External	Integrated	N/A
	BATFET optional	Yes	N/A	N/A
	BMS (fuel gauge)	Yes	Yes	N/A
Output power regulation	Buck regulator	2 FT, 6 HF	3 HF	6 FT, 2 HF
	LDO	29	24	0

Feature Comparison (cont.)

Block	Feature	PM8921	PM8941	PM8841
Output power regulation	Power switches	7	5	0
	5V boost > 500 mA	No	Yes, charger Boost mode	N/A
	Boost	No	Yes	No
	External buck\boost support	Yes	Yes	N/A
	NCP	Yes	No	No
Housekeeping	System clock generation	19.2 XO	19.2 XO	
	System clock buffers	5	6	0
	Sleep clock generation	XO/586	XO/586	
	32 kHz buffer	1 + 2 GPIO	1 + 2GPIO	0
	RTC (# of alarms)	Yes (1)	Yes (1)	0
	MP3 CLK buffer	Yes	Yes	No
	HKADC (XOADC)	Yes	Yes	No
	RF PA controller	No	No	No
	RUIM/SIM level translator	Dual	No, MSM does level translation	No
	USB OTG	Switch only	Switch only	No
	USB transceiver	No	No	No
	Automatic fault protection	No	Yes	No

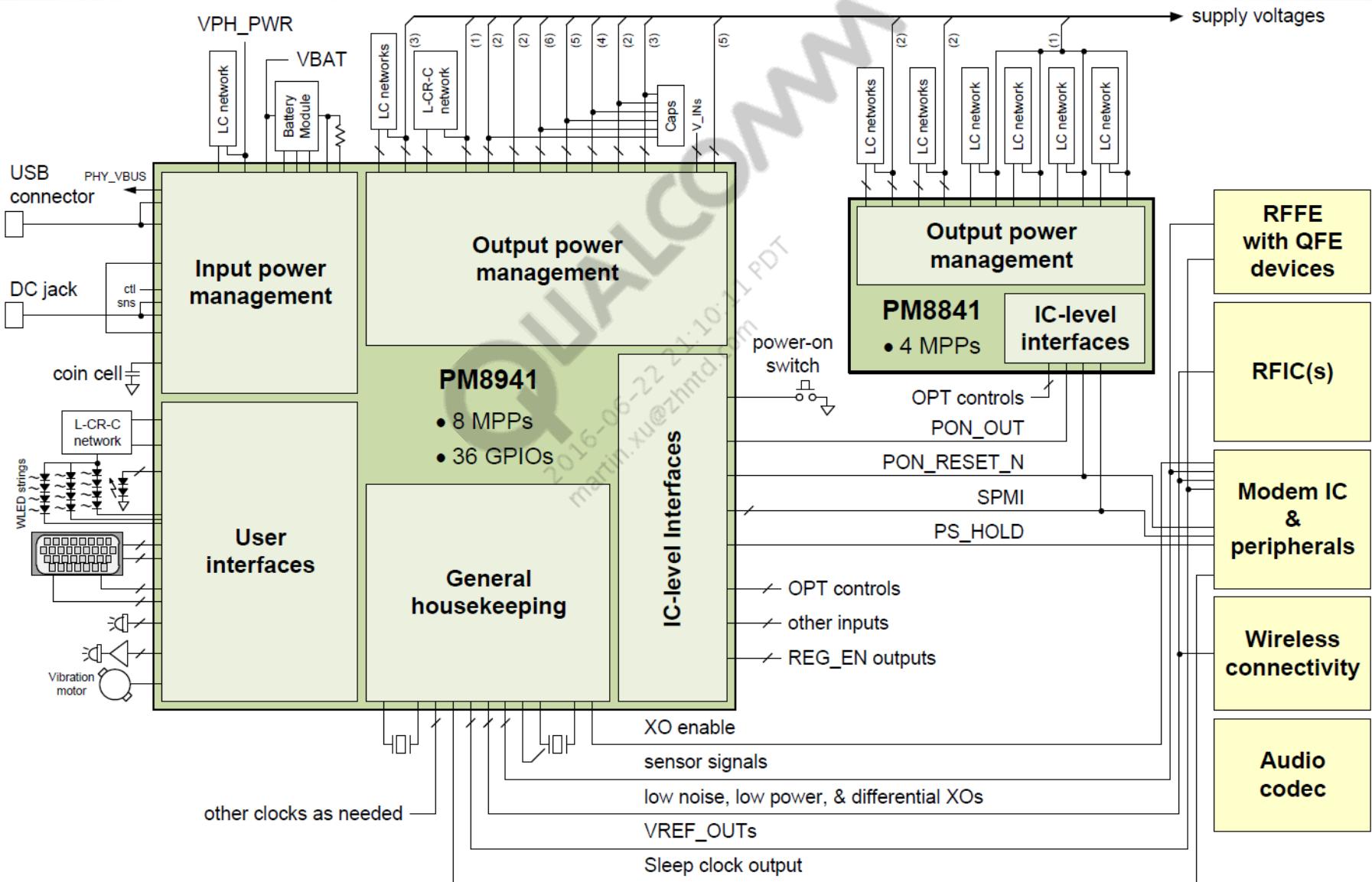
Feature Comparison (cont.)

Block	Feature	PM8921	PM8941	PM8841
User interface	Keypad scanner	8x18	8x10	No
	MPP	12	8	4
	GPIO	40	36	0
	LED driver (300 mA)	1	0	0
	Series WLED BL driver	No	Yes (3 strings of 8)	0
	LED driver (150 mA)	0	0	0
	LED driver (40 mA)	3	3 (RGB-capable)	0
	LPG (Light Pattern Gen)	8 channel	8 channel	No
	Vibrator driver	Yes	Yes	No
	Camera Flash driver	No	Yes	No
	Video amplifier	No	No	No
	Speaker driver	No	No	No
IC interface	OTHC (MIC BIAS)	3	0	0
	Control interface	SSBI	SPMI	SPMI
	IRQ manager	Secure (3)	Yes, message	Yes, message
	Cable detector	No	No	No
	SD\MMC card detector	Yes (GPIO)	Yes (GPIO)	No
	SMPL	Yes	Yes	N/A

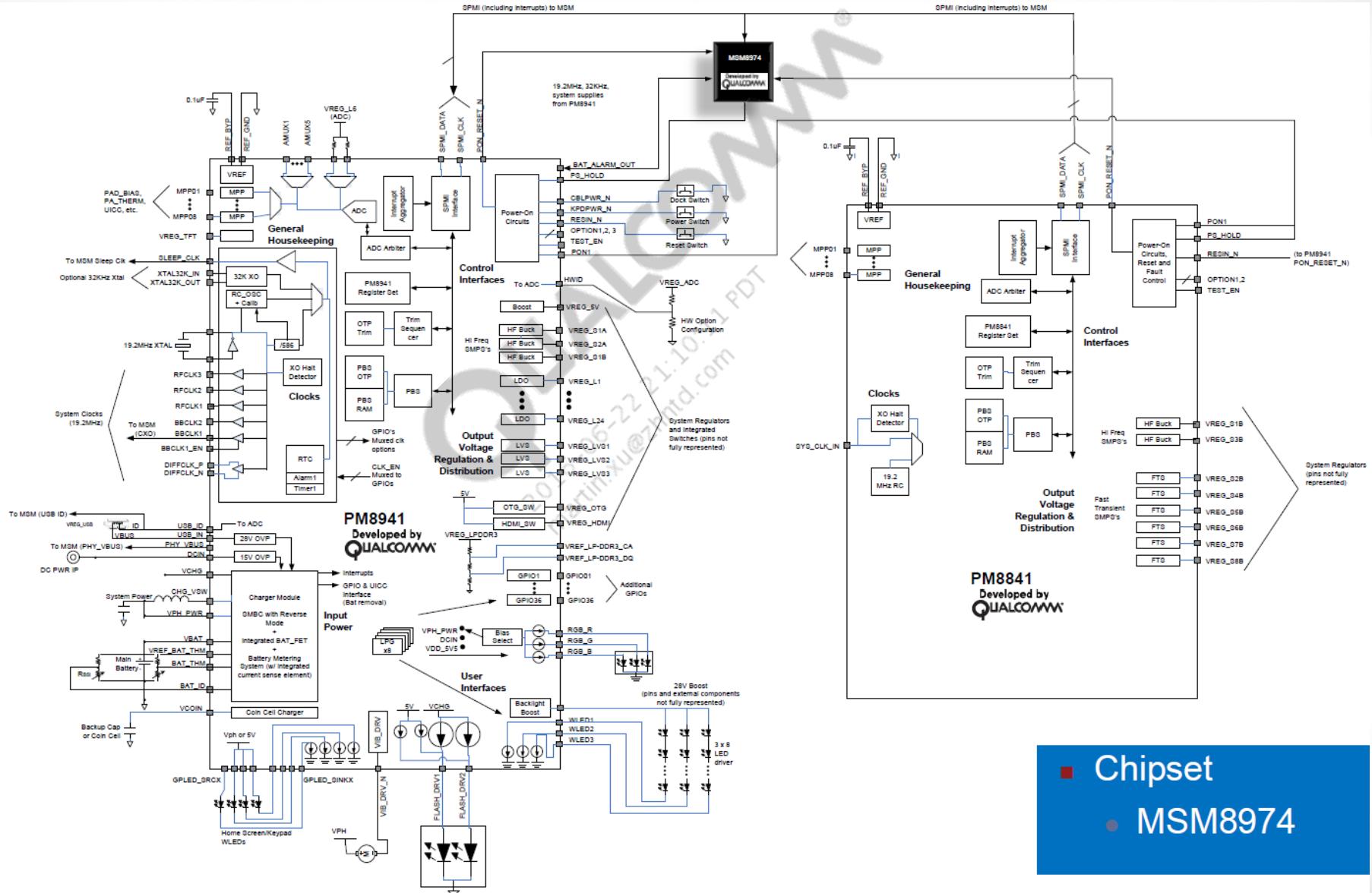
PMIC Block Diagram



PMIC Block Diagram



PMIC Block Diagram (Detailed)

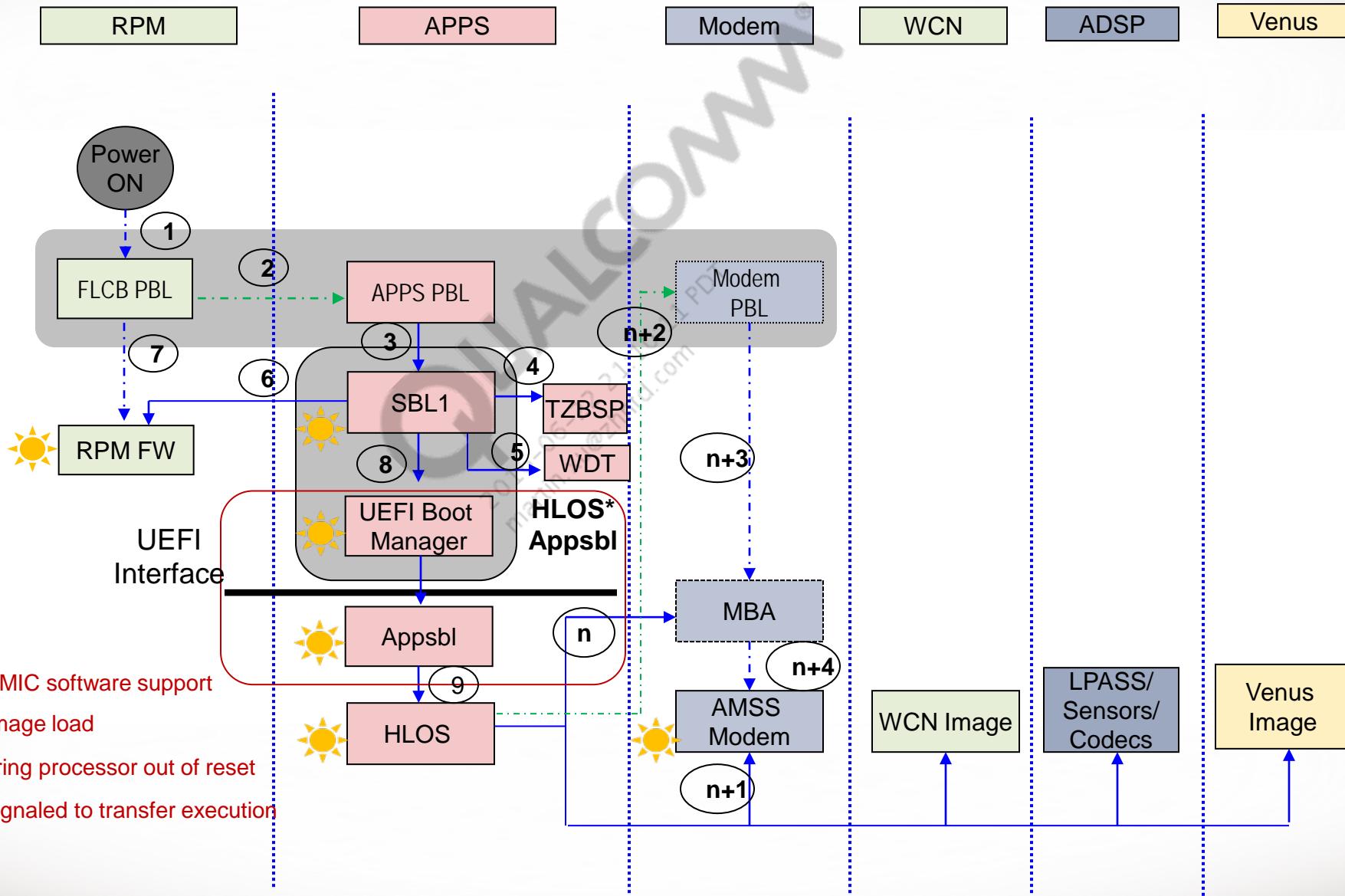




Boot Architecture



Boot Architecture



*HLOS Appsbl block is HLOS-specific, LA has only Android AppSBL whereas Windows on Snapdragon/Windows Phone 8 has UEFI and AppSBL.



Software Build Architecture

Metabuild for MSM8974 1000 (Example)

- Build components
 - Proprietary
 - M8974AAAAANLYA1000 – Android user space proprietary code and libraries
 - M8974AAAAANLYD1000 – Metabuild, contains JTAG scripts to load software
 - M8974AAAAANAZB1000 – SBL (boot loader)
 - M8974AAAAANAZM1000 – Modem subsystem
 - M8974AAAAANAZR1000 – Resource Power Manager (RPM)
 - Open source
 - M8974AAAAANLYA1000 – From codeaurora.org, contains Linux Kernel + Android Framework, and apps boot loader (little kernel) open source code



Secondary Boot Loader (SBL)

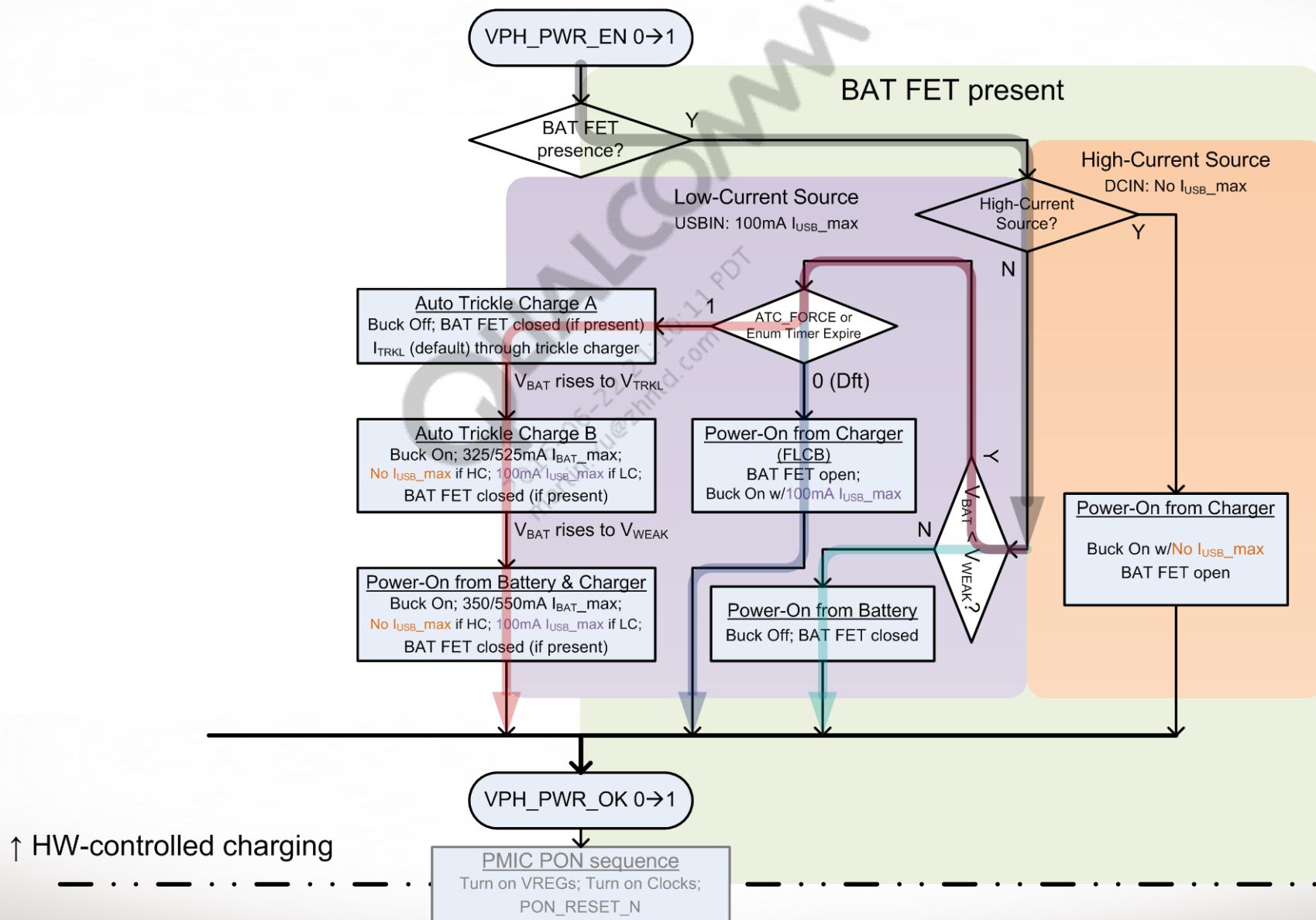


SBL1 PMIC Software Support

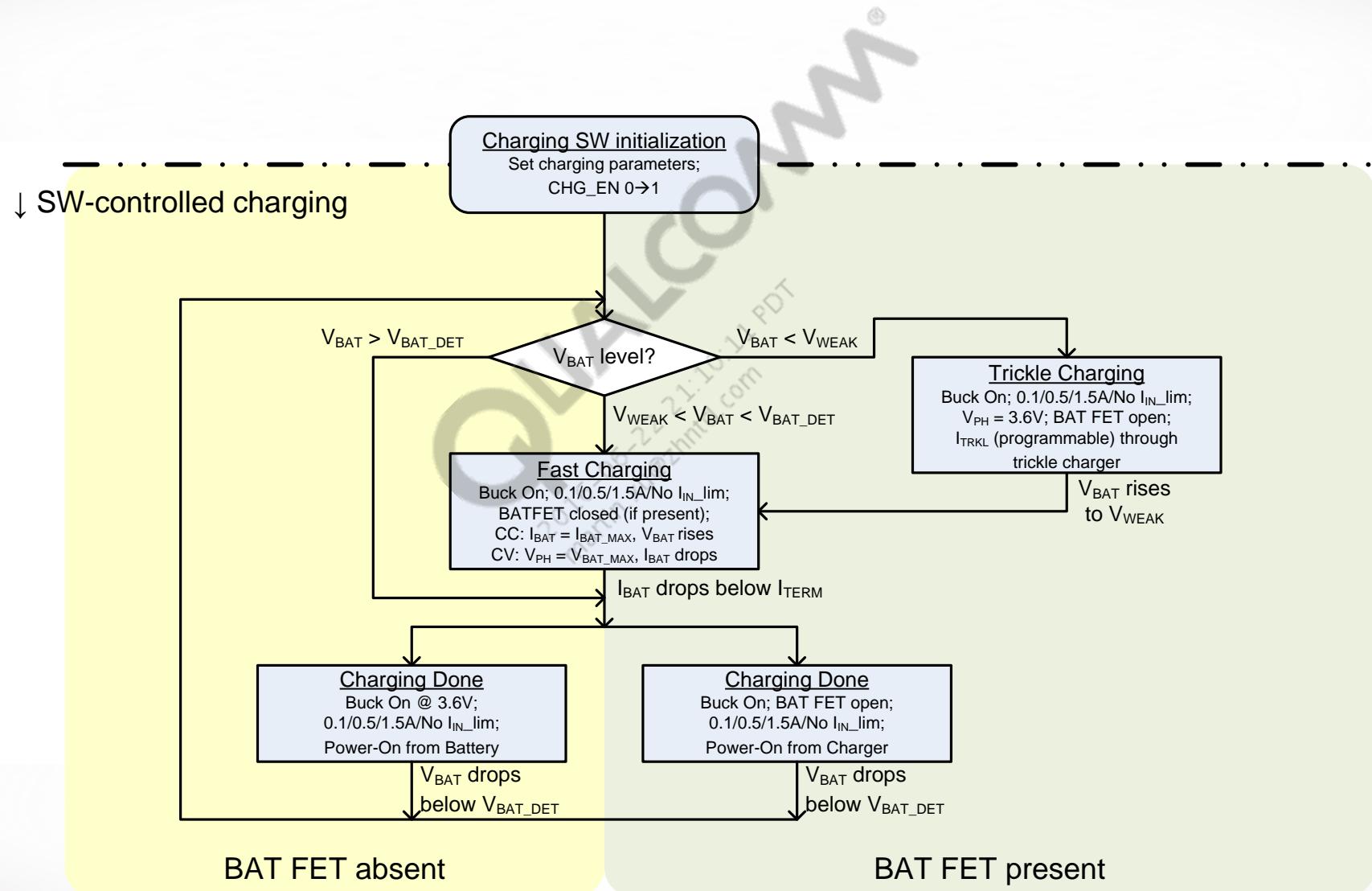
- Historically, SBL1 has hosted Dead Battery Recovery (DBR) code
- Limited PMIC software support is available
 - PMIC CHG APIs are listed in boot_images\modem\api\rfa\pm_boot_chg.h
- Code related to DBR is under boot_images\core\wiredconnectivity\qhsusb\src\al\qhsusb_al_chg.c
- All PMIC APIs can only be called after PMIC initialization is complete
 - boot_images\core\boot\secboot3\msm8974\sbl1\sbl1_hw.c

Note: For more information on DBR and Fast Low Current Boot (FLCB), see [Q2].

Pre-SBL CHG (Hardware-Controlled)



SBL CHG (Software-Controlled)



SBL1 – GPIO/MPP Configuration

- GPIO and MPP config APIs are planned to be supported in SBL1
 - GPIO
 - Digital output
 - Digital input
 - MPP
 - Digital output
 - Digital input
 - Analog output
 - Analog input
 - Current sink
- API names are still to be determined and will be provided in a future revision of this document.

Preliminary plan for VIO mapping

PMIC	MPP/GPIO group	VIN
PM8941	MPP1-8	<ul style="list-style-type: none">▪ VIN0 = VPH▪ VIN1 = L1▪ VIN2 = S3A▪ VIN3 = L6
PM8941	GPIO1-14	<ul style="list-style-type: none">▪ VIN0 = VPH▪ VIN1 = L1▪ VIN2 = S3▪ VIN3 = L6
PM8941	GPIOC15-18	<ul style="list-style-type: none">▪ VIN0 = NA▪ VIN1 = NA▪ VIN2 = S3▪ VIN3 = L6
PM8941	GPIO19-36	<ul style="list-style-type: none">▪ VIN0 = VPH▪ VIN1 = 5V▪ VIN2 = S3▪ VIN3 = L6
PM8841	MPP1-4	<ul style="list-style-type: none">▪ VIN0 = VPH (PVDD)▪ VIN1 = VPH (PVDD)▪ VIN2 = S3A (VDD_MSM_IO)▪ VIN3 = S3A (VDD_MSM_IO)

SBL1 – VREG Configuration

- Basic VREG configuration APIs will be made available
 - ON\OFF control
 - Set level
 - Pull-down configuration
 - Mode control (PWM/PFM/LPM, etc.)
- API names are still to be determined and will be provided in a future revision of this document.

SBL1 – ADC Software Support

- A FR has been filed to include ADC software support in SBL1.
- ADC reads can be used to detect proprietary charger types.
- Non-standard charger type detection is necessary for appropriate input current limiting, among other things.

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AMSS – Modem Software



AMSS – Modem Software

- AMSS has limited PMIC software support.
- Supported modules include:
 - GPIO
 - MPP
 - HKADC
- VREG and CLK configuration/control are dictated by the PMIC Arbitration Matrix (PAM)/Node Power Architecture (NPA).
- PMIC initialization occurs in `modem_proc\core\debugtools\tmc\src\tmc.c`.

Note: More information on PAM and NPA will be made available at a later date. Document number and ETA are still to be determined.

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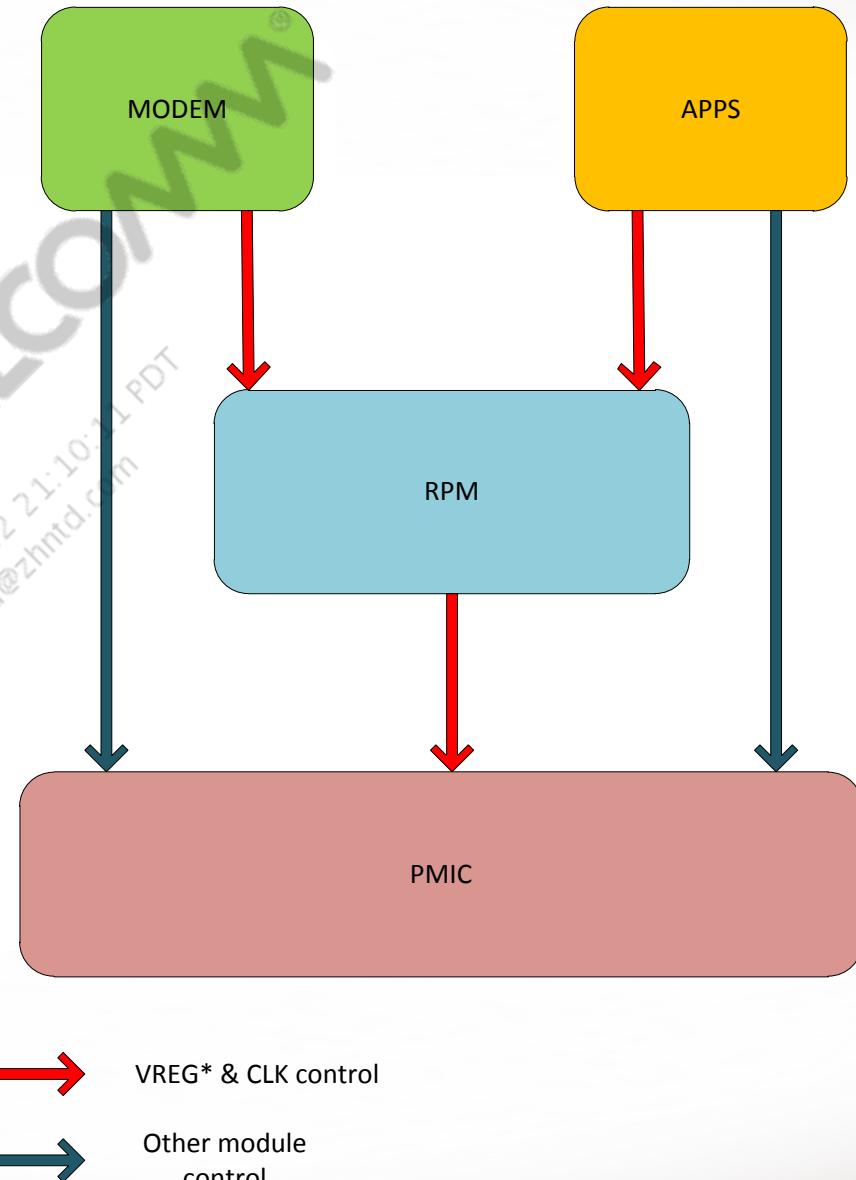
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RPM Software



RPM – PMIC

- RPM is used to control the PMIC VREGs and CLK.
- Almost all VREG and CLK requests from apps and modem are handled by the RPM.
- RPM receives incoming requests and configures the PMIC in accordance with the aggregation algorithm in RPM PMIC library software.
- There are two exposed functions in the RPM PMIC software that are called in and out of RPM-assisted sleep.
- Customers can use these functions to configure PMIC VREGs to low power settings.



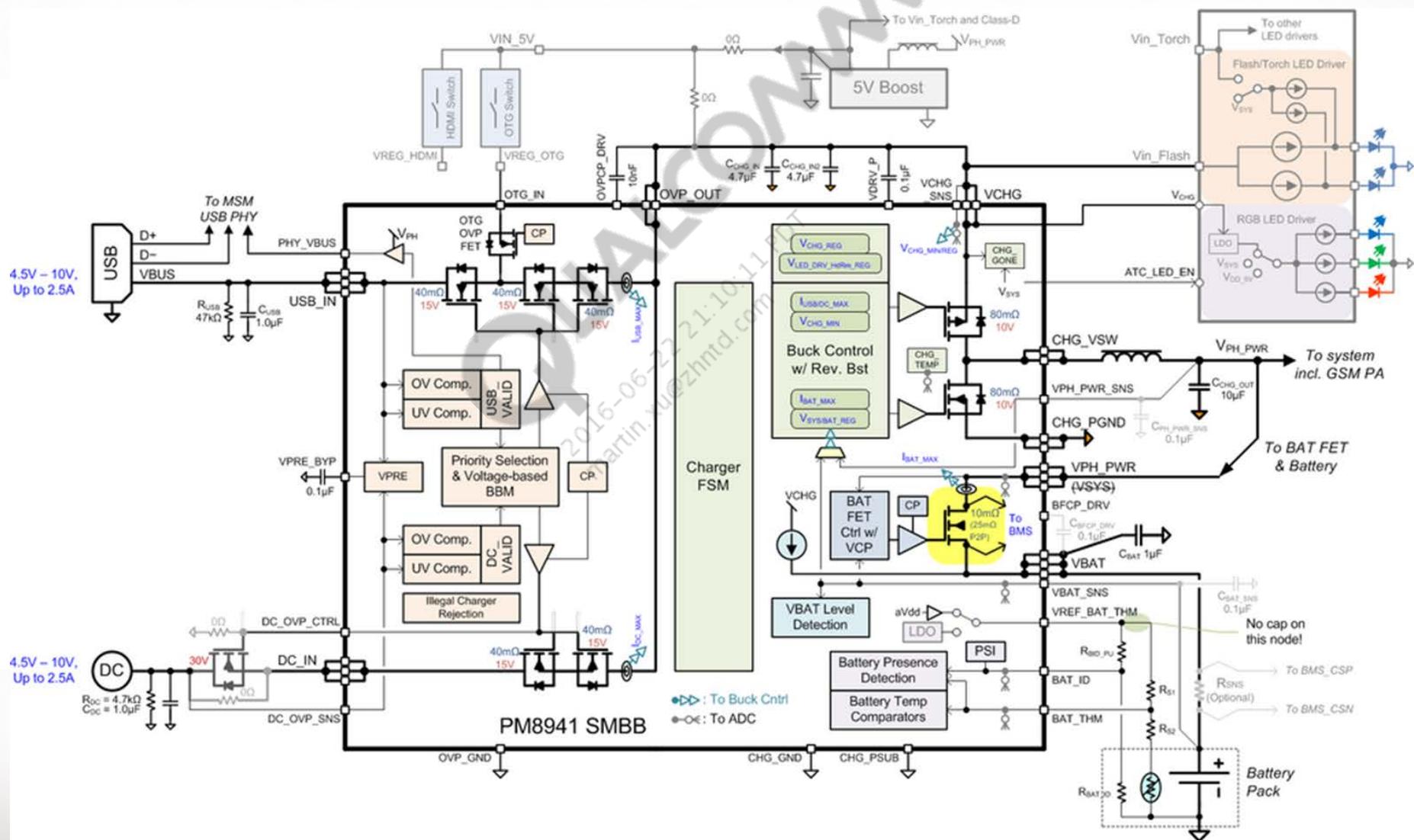
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Input Power Management Topics



SMBC Block Diagram



- Fully integrated, high efficiency switch-mode charger for single-cell Li-Ion batteries
 - Up to 3.0A current to system+battery
 - 3.2 MHz switching frequency allows small size (3225) inductor
 - Efficiency – 90% at 1.0A I_{CHG_OUT} ; 85% at 2.5A I_{CHG_OUT}
 - High-current charging IR drop compensation
- Reverse boosting mode to provide a 2A maximum to V_{chg}
 - Supports USB OTG, HDMI switch, and LED drivers (Torch, Keypad Backlight, RGB)
 - Also used for Flash LED driver in an adaptive mode to minimize the thermal generation
- Dual charging path with fast automatic charging path switching
 - Fully integrated USB charging path with +30V OVP FET; 4.5V – 10V input; USB 2.0 and USB Battery Charging Spec. 1.2 compliant
 - DC charging path with integrated +15V OVP FET for input current sensing and reverse current blocking; 4.5V – 10V input; allows an optional ext. OVP FET to support +30V OVP
- Integrated BAT FET
 - Battery current sensing across the BAT FET; eliminating the ext. RSENSE;
 - Hardware battery presence detection and temp. monitoring with JEITA spec compliance
- Charger FSM supports autonomous charging (Trickle→CC/CV→Termination→Recharge)
 - Software-initiated, hardware-managed charging; allows hardware-controlled auto trickle charge (ATC) if necessary
 - Hardware timers for battery charging safety; one-time write registers, and battery over-voltage detection
- USB support
 - Integrated USB OTG switch supporting simultaneous DC charging and USB OTG
 - USB RID detection with ACA support

CHG (cont.)

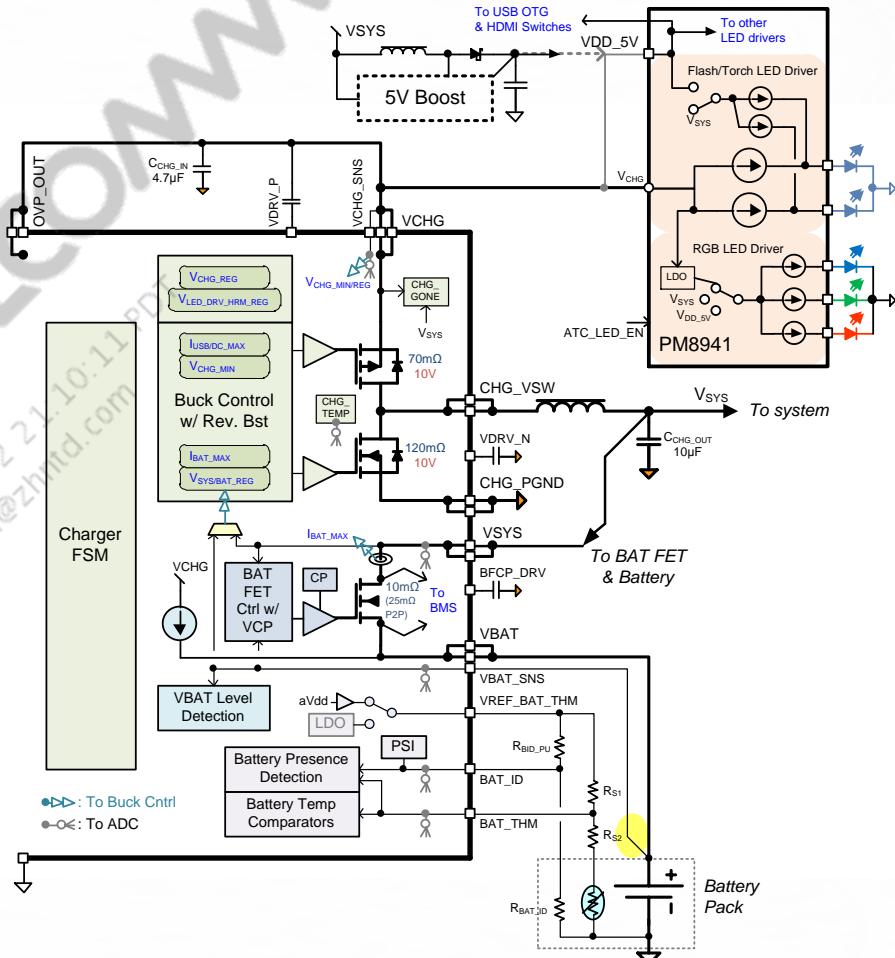
- Charging termination
 - Current into the battery is continuously monitored; when sensing $I_{BAT} < I_{TERM}$ (with deglitching), charging is terminated
 - I_{TERM} – 50 – 200 mA programmable, 10 mA steps, $\pm 2\%$ of setting ± 15 mA accuracy, 100 mA default
 - If with BAT FET, the buck remains on and supplies the system; BAT FET is open to isolate the fully charged battery
- Automatic recharge
 - When detecting V_{BAT} falls below a programmable threshold, FSM automatically recharges the battery
 - V_{BAT_DET} – 3.3 – 4.7 V programmable, 20 mV steps; ± 30 mV accuracy, 4.1 V default
- Qualcomm charger driver also supports Adaptive Input Current Limiting (AICL) wherein the current capability of a charger can be determined without being specified during initialization

CHG (Safety Features)

- Safety timers
 - Hardware timers that limit the maximum time allowed for trickle charging and the complete charging cycle
 - Stop charging (and generate interrupt) if timer times out
- Charger Watchdog timer (one-time write register)
 - Hardware timer to make sure the charging control software remains alive
 - Stops charging (and generates interrupt) if timer times out
 - 0 to 32 sec programmable
- VBAT_SAFE and IBAT_SAFE (one-time write registers)
 - To limit maximum allowed battery charging voltage/current, and prevent malware
 - Write access to these registers are enabled after power on reset, and disabled after being written once
- Battery Overvoltage Detector
 - V_{BAT_DET} comparator is reused to monitor battery overvoltage condition during fast charging
 - Interrupt is generated if battery overvoltage condition is detected
- Thermal management

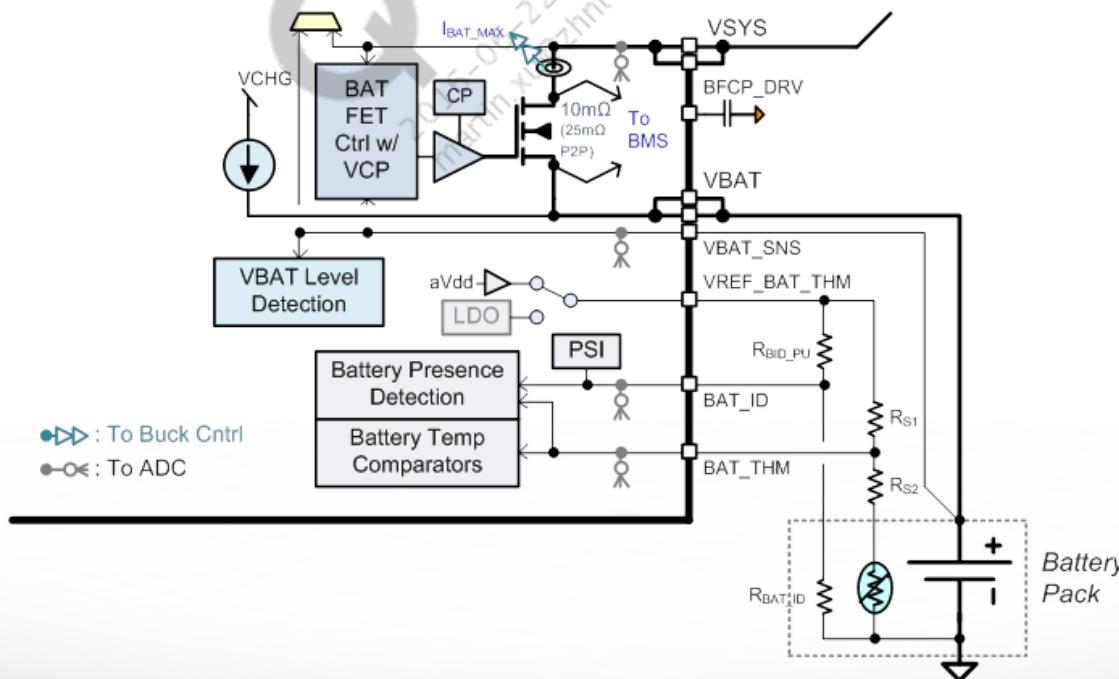
SMBC Reverse Boosting Mode (Bcharger)

- Running the SMBC buck in reverse boosting, to provide a 4v to 5v supply for:
 - Flash LED driver
 - Torch/Keypad Backlight/RGB LED drivers
 - USB OTG switch and HDMI switch
- Supports an adaptive mode that regulates the maximum headroom of the Flash LED driver
 - To minimize the voltage drop across the Flash LED driver, and its thermal consumption
- With an optional 5V LDO between VCHG and VDD_5V
 - More concurrency use cases can be supported but with thermal limitation



CHG (Battery Interface)

- Integrated NMOS BAT FET
 - Battery current sensed across BAT FET R_{ds(on)} for SMBC IBAT_MAX limiting and BMS; eliminating ext. I_{BAT} sensing resistor
 - BAT FET R_{ds(on)} regulated at 10mΩ ±2% across temp. (-30°C to 125°C) and VBAT range (2.5V to 4.5V) after trim; 25mΩ max pin-to-pin
- Hardware battery presence detection and JEITA-compliant battery temperature comparators
- PMIC Serial Interface (PSI) for digital battery interface

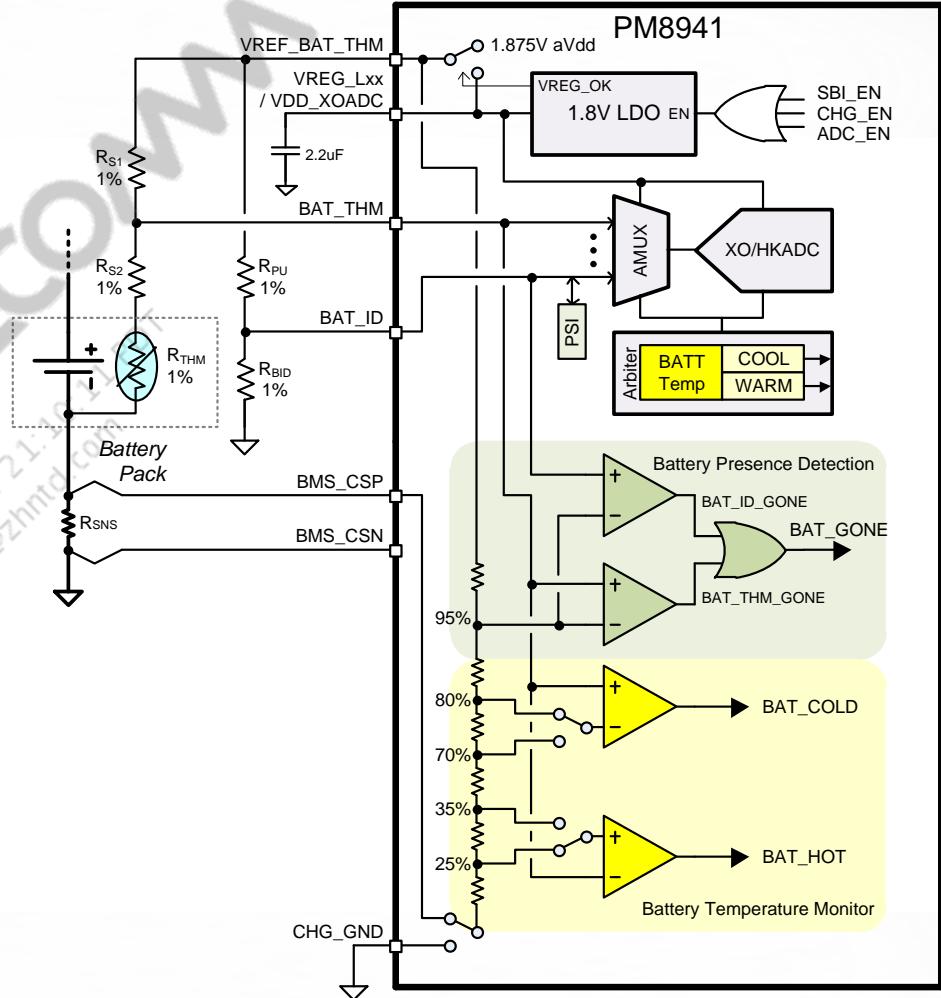


USB Support

- VBUS detection
 - USBIN_VALID window comparator outputs a '1' when USBIN (VBUS) is between UVD threshold (4.25 V rising, 3.85 V falling) and OVP threshold (6.5 V rising by default)
 - The output is level-shifted to VPH_PWR and sent to MSM USB PHY to trigger its Session_Valid comparator
- Charging port detection (SDP/CDP/DCP) and enumeration control
 - Performed by MSM USB PHY hardware and software
 - Based on charging port detection and enumeration result, USB software writes to IUSB_MAX register
 - USB OTG support
 - Reverse current blocking; blocks current in either way when turned off
 - Soft-Start – Slowly turns on the switch to prevent inrush current
 - OCP (over-current protection) – Automatically turns off the switch when detecting load current exceeds OVP threshold (1.5x IRATED typ., 2x max.), and sends an interrupt
 - Two options to connect to USB connector VBUS pin USB_ID detection and ACA support
 - A phone that supports OTG is required to detect micro-A plug insertion (USB_ID pin grounded), to act as a host and supply VBUS
 - Uses a PMIC USB_ID comparator with pull-up to detect USB_ID pin grounded
 - USB_ID also connects to PHY ID pin via an optional FET to support ACA

Battery Temperature Monitoring

- Enhanced BTM with JEITA compliance
 - Two analog BTM comparators that monitor the cold and hot conditions
 - Four thresholds generated by internal resistor ladder
 - For charging with traditional battery temp range, use 70% and 35% thresholds
 - For charging with extended battery temp range (JEITA), use 80% and 25% thresholds
 - Use R_{S1} and R_{S2} pull-up resistors to tune the trip points
 - Battery charging is paused if either comparator asserts
 - An automated digital BTM routine that monitors the cool and warm conditions
 - If enabled, battery temp is automatically measured by the ADC Arbiter periodically (programmable up to 16 sec)
 - Battery temp measurement result is compared with programmable cold and warm thresholds; interrupts are generated if either of the thresholds are exceeded
 - Charging software adjusts the VBAT_MAX and IBAT_MAX accordingly



Battery Presence Detection

- Flexible Battery Presence Detection with battery thermistor or ID resistor inputs (BPD)

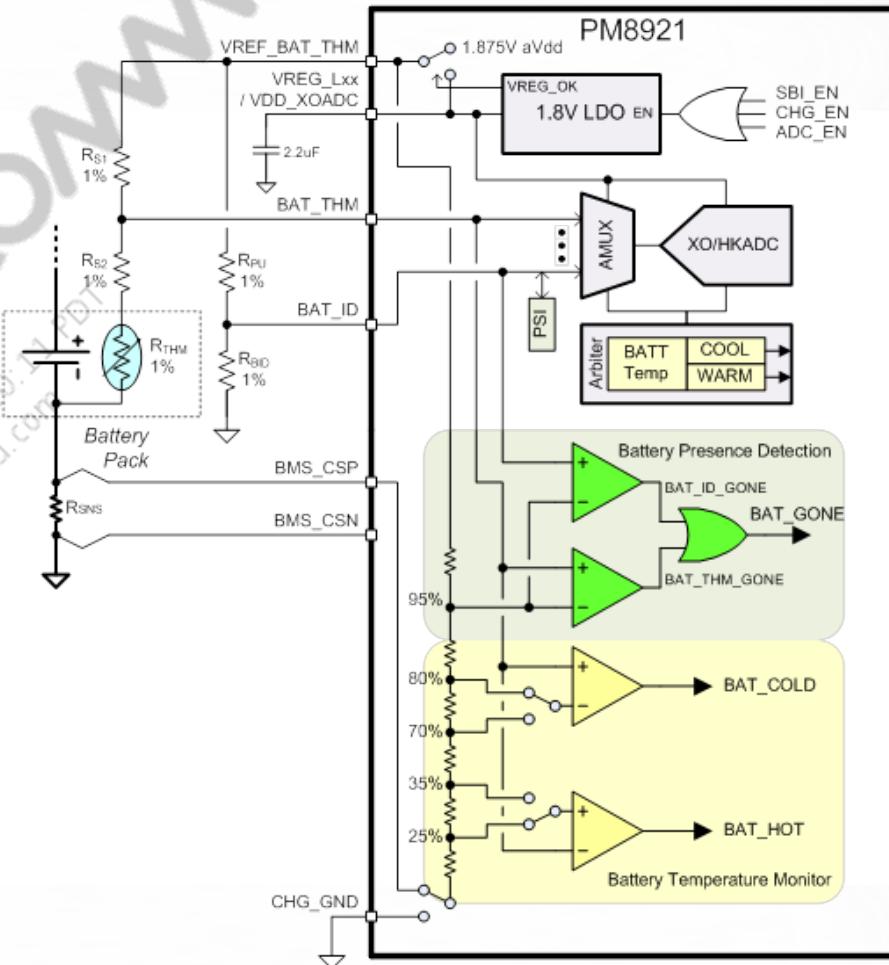
- Battery presence is detected by sensing the presence of battery thermistor or ID resistor, whichever is inside the battery pack
 - If battery is absent, the pull-up resistors will pull BAT_THM and/or BAT_ID high
- Two dedicated comparators for BPD
 - Battery is considered as “gone” if BAT_THM or BAT_ID is above 95% of $V_{REF_BAT_THM}$
 - Interrupts are generated (after deglitching) when detecting battery insertion or removal
 - Charging shall be stopped upon battery removal

- Battery Identification

- BAT_ID is sent to PMIC AMUX/HKADC for battery ID resistor (R_{BID}) measurement

- PMIC Serial Interface (PSI)

- A low-speed serial communication on the battery ID line, to transfer battery size/voltage/age information
- BAT_ID line driven/listened to by the PSI block when not measuring R_{BID}

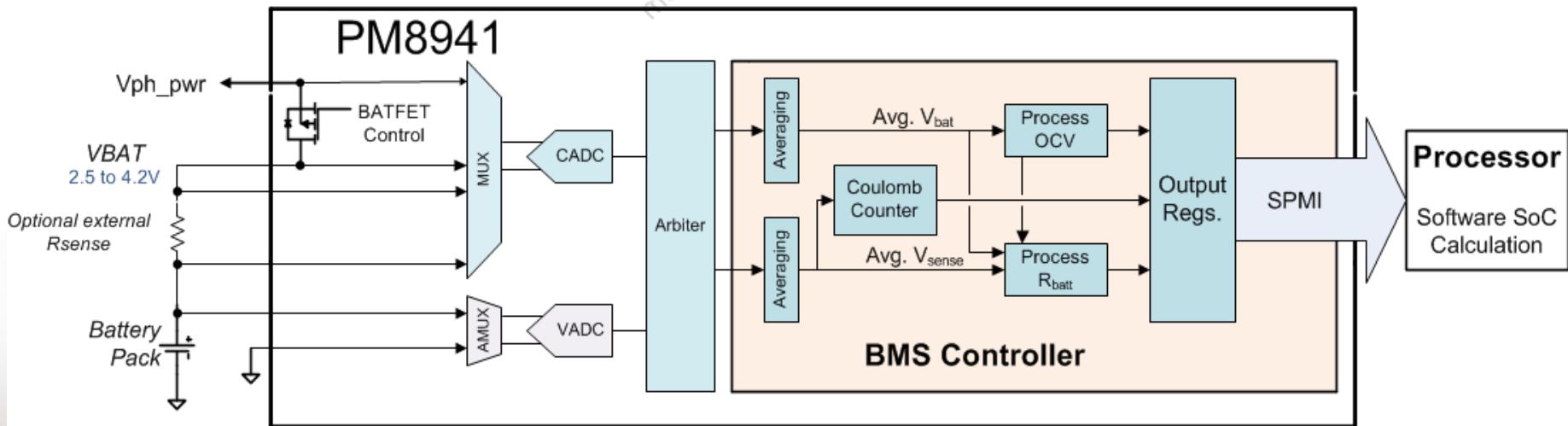


BMS

- PM8941 BMS builds on the success of the PM8921 BMS design
- PM8941 BMS change summary (relative to PM8921)
 - Internal Rsense→Voltage sensed across BATFET
 - BATFET Rds is kept constant
 - Eliminates larger and expensive component (Rsense)
 - Option for external Rsense is still available
 - Master band gap settling time is reduced→Improved PON Open Circuit Voltage (OCV) measurement
 - Selectable hardware-based or software-based Coulomb counter reset
 - Selectable range for ignoring OCV updates→Flat portion of battery profile
 - Ibat→threshold interrupt (if system current peaks are large, we generate and interrupt so that HLOS can mitigate the situation)

BMS (cont.)

- CADC samples V_{sense} generated across BATFET ($10 \text{ m}\Omega$)→current measurement
- VADC samples V_{bat} →OCV measurement
 - Shared use with other housekeeping functions
- BMS Controller autonomously manages ADCs and key measurements
 - Controls measurement frequency, averaging, coulomb counting, and CC resets
 - All data for SoC calculations stored, read as desired by software→No periodic software intervention
 - BMS Controller utilizes Qualcomm-proprietary algorithm
- PMIC software reads stored data, executes software algorithms, and calculates SoC



BMS (cont.)

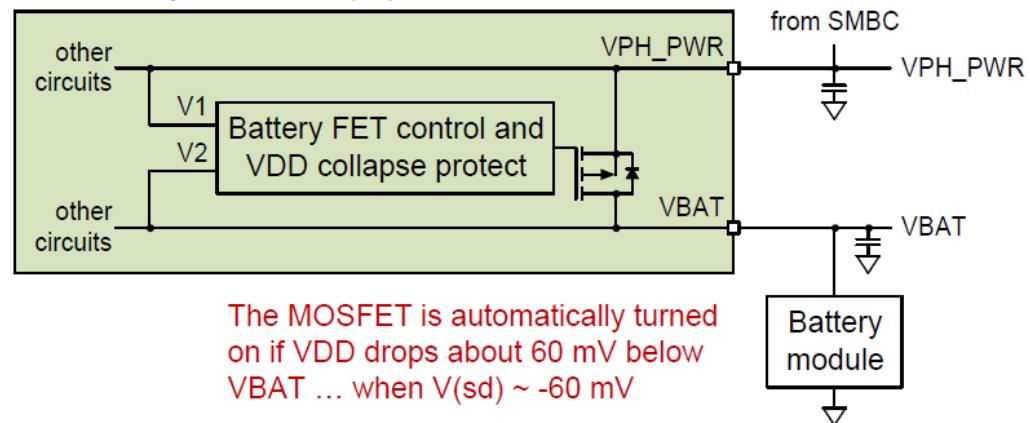
- PM8941 BMS architecture provides flexibility
 - Existing Qualcomm software/algorithms can be used
 - Custom fuel gauging solutions with unique algorithms can be used
- Software and algorithms are continually being updated
 - New algorithms being added to meet customer demands
 - Existing software is being optimized as test results dictate

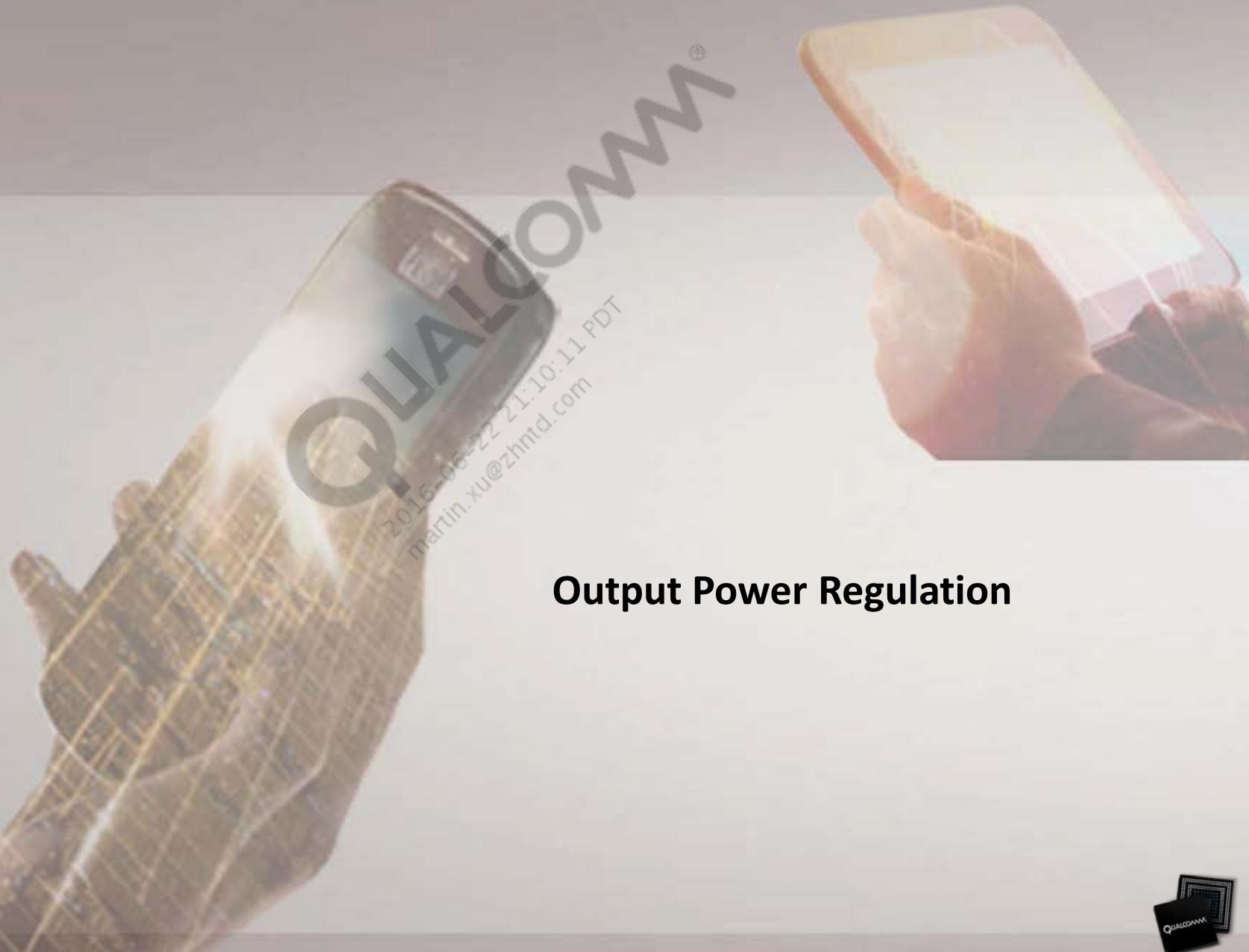
VDD Collapse Protection

- When a valid external charger is connected, and the battery is either fully charged or too hot or too cold to be charged, the battery FET is opened and the system runs off the external charger
- If the external charger's current limit is exceeded. Voltage Collapse Protection (VCP) is executed
 - If VPH_PWR drops 60 mV below VBAT, VCP is activated.
 - The battery FET is turned on, allowing the battery to supplement the external source.
 - Turn-on is a single step, not a linearly regulated process.
 - With the added battery current, the system's high current does not cause VDD to collapse
 - The battery FET is turned off when the excessive current condition ends.
 - When > 100 mA flows into the battery, or
 - When 0 to 5 mA flows into the battery for at least one sec
 - Battery FET turn-on time is fixed at 5 μ s max; the turn-off time is 1 μ s by default, but can be increased to 10 μ s via SPMI

The PMIC prevents a sudden load from inadvertently collapsing the VDD voltage as discussed here.

PMIC monitors the voltage across the battery MOSFET $V_{(sd)} = V_1 - V_2$

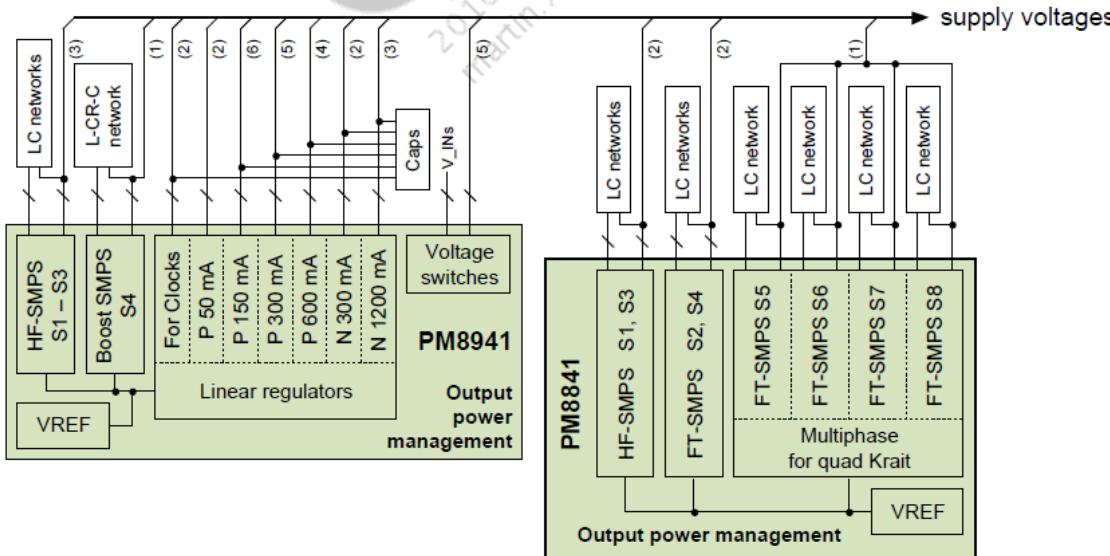




Output Power Regulation

Output Power Management Content

- Summary of OPM functions
- MSM8974 power grid
- Buck vs Buck/Low Dropout (LDO)
- HF_SMPs circuits
 - Operation
 - Efficiency plot
 - Schematic and layout
- Multiphase FT_SMPs circuits
 - Krait power delivery
 - Bimodal functional modes
 - Schematic and layout
- Boost SMPS circuits
 - Operation
 - Schematic and layout
- SMPs switching loops and components
- LDO linear regulators
 - Pseudo-capless LDOs
- Regulator low-power modes
- Internal regulator connections
- External regulator connections and subregulation
- Voltage switches
- Need for external boost bypass



Voltage Regulator Summary

Function	Circuit type	Default voltage (V)	Specified range (V)	Programmable range (V)	Rated current (mA)	Default on	Expected use
S1	HF-SMPS	1.400	1.200 – 1.500	0.375 – 3.050	2000	Y	Source for L1 & L3, L4 & L11; external connections
S2	HF-SMPS	2.150	1.800 – 2.250	0.375 – 3.050	1000	Y	WCD plus source for L5 & L7, L6 & L12 & L14 & L15; external connections
S3	HF-SMPS	1.800	1.750 – 1.850	0.375 – 3.050	2000	Y	Modem IC pad group 3, option 4 & 7; L2 and LVS; chipset and other I/Os
S4 or '5V'	Boost SMPS	5.000	4.000 – 5.500	4.000 – 5.500	1300	–	WCD spkr driver & source for 5VS1, 5VS2; option for kypd, RGB drivers
L1	NMOS LDO	1.225	1.200 – 1.250	0.750 – 1.525	1200	Y	Modem IC pad group 1, option 4, & 7; DDR memory; eMMC
L2	NMOS LDO	1.200	1.100 – 1.450	0.750 – 1.525	300	–	MIPI_DSI - analog
L3	NMOS LDO	1.200	1.100 – 1.450	0.750 – 1.525	300	–	MIPI_CSI
L4	NMOS LDO	1.300	1.150 – 1.400	0.750 – 1.525	1200	–	RFIC low-V; modem IC analog low-V
L5	Low noise LDO	1.800	1.700 – 2.200	–	On-chip only	–	PMIC low noise XO buffers
L6	PMOS LDO	1.800	1.700 – 1.900	0.750 – 3.050	150	Y	USB; WCN XO; PMIC low power XO output buffers
L7	Low noise LDO	1.800	1.700 – 2.200	–	On-chip only	–	PMIC XO circuits
L8	PMOS LDO	1.800	1.700 – 1.900	0.750 – 3.050	50	–	PMIC HKADC
L9	PMOS LDO	1.800	1.700 – 3.050	0.750 – 3.050	150	Y	Modem IC pad group 5, dual-voltage UIM1 (1.8 / 2.95 V)
L10	PMOS LDO	1.800	1.700 – 3.050	0.750 – 3.050	150	–	Modem IC pad group 6, dual-voltage UIM2 (1.8 / 2.95 V)
L11	NMOS LDO	1.300	1.200 – 1.400	0.750 – 1.525	1200	–	WCN; modem IC ADC/DAC
L12	PMOS LDO	1.800	1.700 – 1.900	0.750 – 3.050	300	–	Modem IC PLLs, MIPI_DSI, MIPI_CSI, HDMI, EDP; MIPI_DSI I/Os
L13	PMOS LDO	2.950	2.750 – 3.000	0.750 – 3.050	150	Y	Modem IC pad group 2
L14	PMOS LDO	1.900	1.700 – 2.100	0.750 – 3.050	150	–	Modem IC analog - high V
L15	PMOS LDO	2.050	2.000 – 2.100	0.750 – 3.050	600	–	RFICs - low voltage
L16	PMOS LDO	2.750	2.600 – 3.000	0.750 – 3.050	150	–	Qualcomm front-end, RF switches, GPS LNA
L17	PMOS LDO	2.800	2.700 – 3.000	0.750 – 3.050	300	–	3D cameras - analog

Voltage Regulator Summary (cont.)

Function	Circuit type	Default voltage (V)	Specified range (V)	Programmable range (V)	Rated current (mA)	Default on	Expected use
L18	PMOS LDO	2.850	2.400 – 3.300	0.750 – 3.050	300	–	Sensors; touchscreen
L19	PMOS LDO	2.900	2.600 – 3.300	0.750 – 3.050	600	–	WCN
L20	PMOS LDO	2.950	2.750 – 3.000	0.750 – 3.050	600	Y	eMMC memory
L21	PMOS LDO	2.950	2.700 – 3.000	0.750 – 3.050	600	Y	SD/MMC card
L22	PMOS LDO	3.000	2.600 – 3.300	0.750 – 3.050	300	–	MIPI_DSI1
L23	PMOS LDO	3.000	2.600 – 3.300	0.750 – 3.050	300	–	MIPI_DSI2 or MIPI_CSI
L24	PMOS LDO	3.075	3.000 – 3.300	0.750 – 3.050	50	Y	HS-USB high-voltage
LVS1	Low V switch	1.800	–	–	300	–	Sensors; touchscreen
LVS2	Low V switch	1.800	–	–	300	–	Available
LVS3	Low V switch	1.800	–	–	300	–	3D cameras
5VS1	5 V switch	5.000	–	–	500	–	USB-OTG
5VS2	5 V switch	5.000	–	–	55	–	HDMI

1) Default voltages and power-on states may depend upon option pin (OPT_x) settings.

2) S1 and S3 current ratings assume V_{out} is less than or equal to 1.8 V. Duty-cycle limitations reduce the rated current to TBD mA for $1.8 \text{ V} < V_{out} < 2.4 \text{ V}$.

3) S3 powers internal circuitry and must be kept at its default setting.

4) L6 and L8 power internal circuits that are limited to 1.8 V operation; they should not exceed the maximum stated in their programmable ranges.
L6 is used as the internal V_{DD} source after power-up; its programmed voltage should not be changed, and it should not be turned off.

5) Rated current for S4, the 5V boost circuit, depends upon the input voltage: 1.3 A for V_{IN} 3.6 to 4.2 V; 0.9 A for 3.0 to 3.6 V; 0.6 A for 2.5 to 3.0 V.

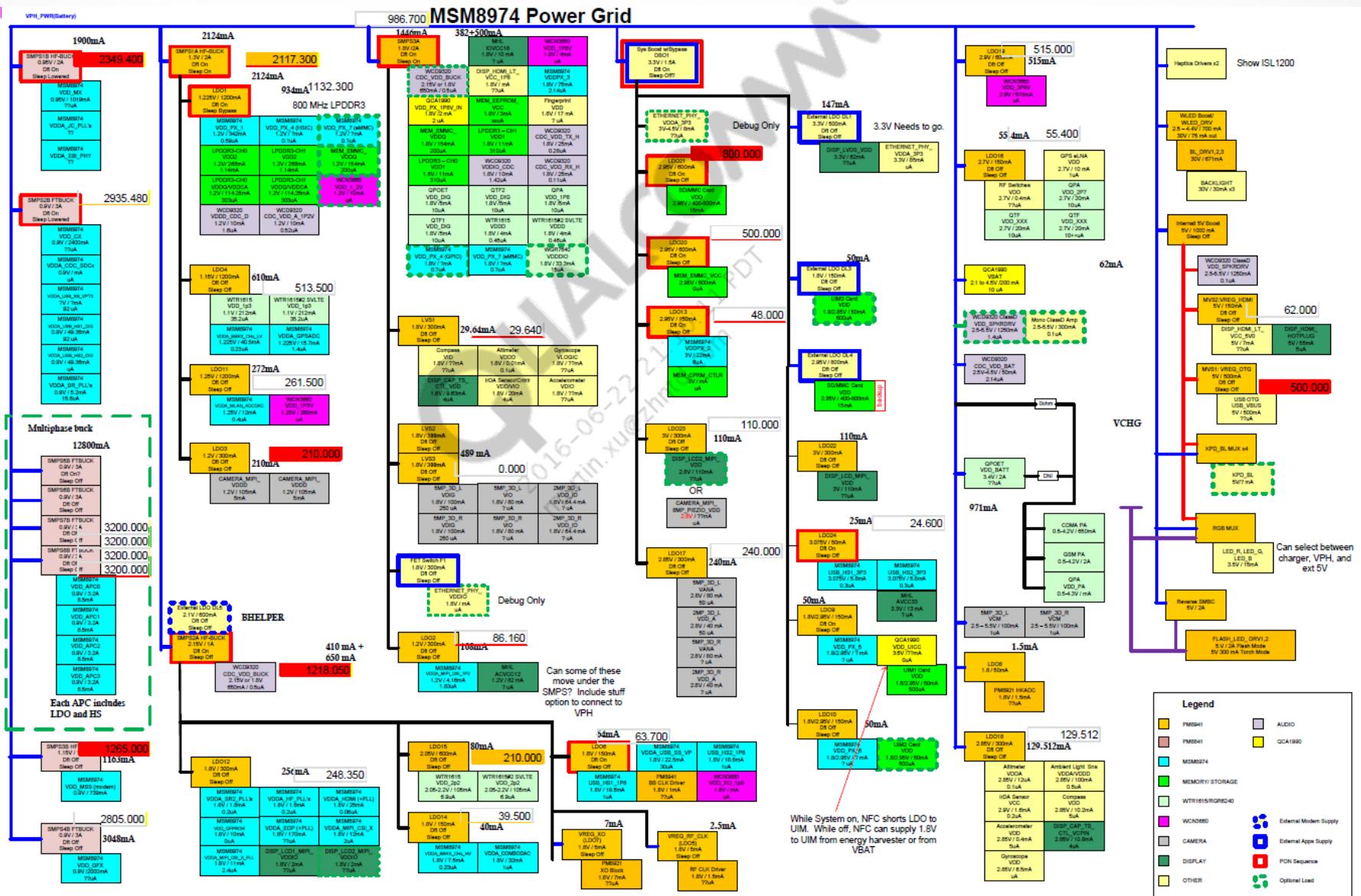
6) L24 is a conventional PMOS, 150 mA LDO that is powered off V_{PH_PWR} and is used for USB. Its dropout voltage is reduced by a factor of three when its output current is limited to 50 mA.

Voltage Regulator Summary (cont.)

Function	Circuit type	Default voltage (V)	Specified range (V)	Programmable range (V)	Rated current (mA)	Default on	Expected use
S1	HF-SMPS	0.950	0.500 – 1.400	0.375 – 3.050	2000	Y	Modem IC memory and PLLs
S2	FT-SMPS	0.900	0.500 – 1.250	0.350 – 3.300	3000	Y	Modem IC core, SDC, and USB
S3	HF-SMPS	1.150	0.500 – 1.400	0.375 – 3.050	1000	–	Modem IC modem system
S4	FT-SMPS	0.900	0.500 – 1.250	0.350 – 3.300	3000	–	Modem IC graphics
S5	FT-SMPS	0.900	0.500 – 1.250	0.350 – 3.300	3000	–	Modem IC quad Krait microprocessors
S6	FT-SMPS	0.900	0.500 – 1.250	0.350 – 3.300	3000	–	
S7	FT-SMPS	0.900	0.500 – 1.250	0.350 – 3.300	3000	–	
S8	FT-SMPS	0.900	0.500 – 1.250	0.350 – 3.300	3000	–	

1) Default voltages and poweron states may depend upon option pin (OPT_x) settings.

MSM8974 Power Grid



HFSMPS Operational Details

- PM8941 and PM8841 have second-generation HF-SMPS (PM8921 had first-generation)
- The second-generation HF-SMPS supports all features of the first-generation HF-SMPS
 - Better transient response
 - Slow start feature
 - Current limiting
 - Operating modes
 - Pulse Width Modulation (PWM)
 - Current-mode constant-frequency PWM control
 - Delivers the specified rated current to the load
 - Pulse skipping
 - Pulse Frequency Modulation (PFM)
 - The power switch is only turned on when the output voltage dips below a threshold
 - Main advantage— Maintains high efficiency even at light loads
 - Auto mode
 - Automatic switching between PFM and PWM modes, based upon load current
 - Programmable threshold
- In addition, the second-generation HF-SMPS has improved auto-PFM/PWM operation
 - Reduced PFM ripple
 - Reduced PFM/PWM transients
 - Improved output stages
 - Improved isolation and biasing
- RF rails use subregulated LDOs to improve noise and efficiency
 - Allows RF bucks to use auto-mode
 - LDOs set for minimal headroom clean up any ripple

Regulator Low Power Mode

- All SMPS and linear regulators, except for the RF_CLK and XO LDOs (L5 and L7), support low-power modes that reduce their quiescent currents. This is especially useful during the handset Sleep mode, enabling maximum standby time. Different regulator types implement their low-power modes differently, as described below:
- Linear regulator – Implements its low-power mode by reducing the current of its feedback loop. During low-power operation, the regulator performance is degraded, e.g., lower PSRR, less output current capability, etc. If the load is greater than 10 mA, the output voltage is likely to be out of specification.
- Buck SMPS – Two control modes: pulse frequency modulation (PFM) control for low-power operation, and pulse width modulation (PWM) control for normal operation. For best efficiency, the buck regulator switches automatically between PFM and PWM, but it can be switched manually via software as well (depending upon sleep or active operation).
 - In PFM mode, the controller shuts down except for a comparator that monitors the output voltage. Starting with the pass device off, eventually the output dips below the programmed output voltage. The pass device is then turned on (a single pulse) until the output voltage slightly exceeds the programmed voltage, and then it is turned off. The on/off process repeats. If the buck SMPS is loaded too heavily in PFM mode, the output ripple is degraded
 - During PFM operation, the pulse frequency varies with load current, while the ripple stays constant at about 30 to 50 mV peak-to-peak. Depending upon the load, the pulse frequency can drop into the audio range and could become audible if it couples into the audio system
 - For normal (active) phone operation, the PWM mode should be used
- Boost SMPS – Very similar to Buck modes, except low power operation uses Pulse Burst Modulation (PBM).

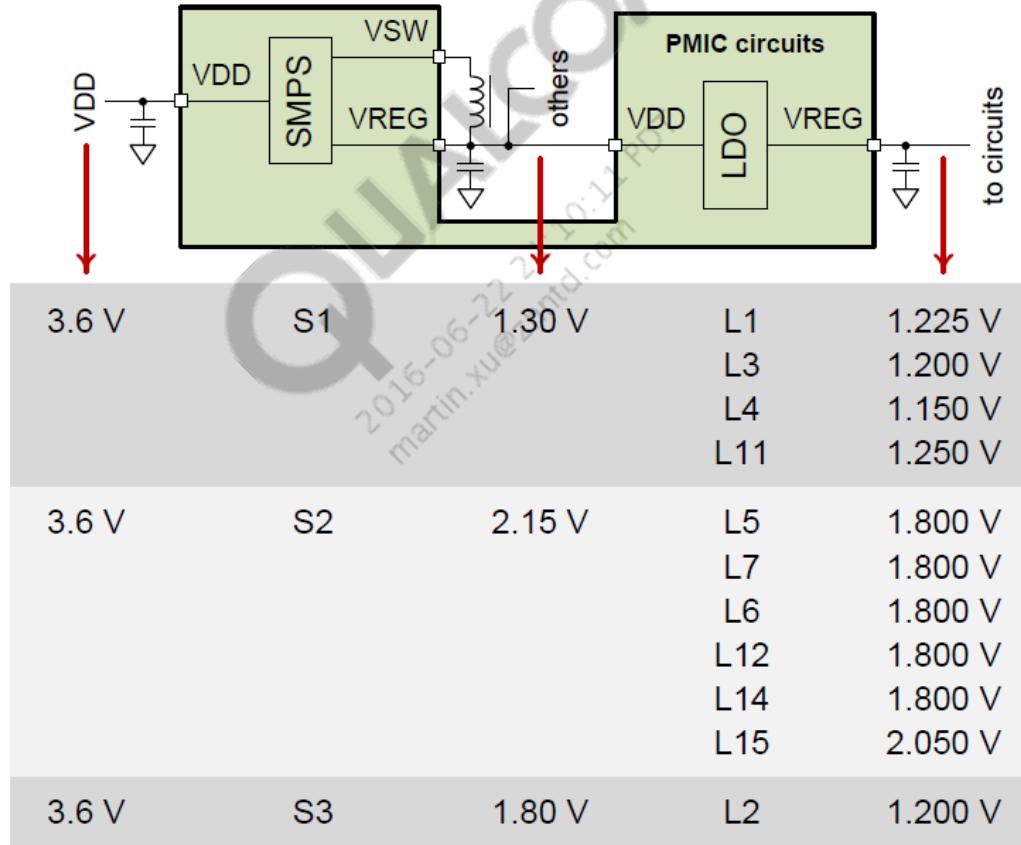
Internal Regulator Connections

- Some regulator input voltages and several regulated outputs are used to power internal PM8974 circuits. The regulators must be enabled and set to their default values for proper PMIC operation.

Regulator pin	Default voltage	Connected internal circuits
VDD_L2_LVS1_2_3 or VDD_MSM_IO	VREG_S3 (1.8 V)	Sleep clock pad, PON circuit I/Os, SPMI pads, various internal circuits, and miscellaneous I/Os
VREG_L1	1.225 V	Selectable GPIO supply Selectable MPP I/O supply
VREG_RF_CLK (L5)	1.8 V	RF clock circuits Low-noise XO outputs (XO_OUT_Ax)
VREG_L6	1.8 V	Selectable GPIO supply Selectable MPP I/O supply Low-power XO outputs (XO_OUT_Dx)
VREG_XO (L7)	1.8 V	XO core
VREG_L8	1.8 V	VREF_BAT supply HK/XO ADC
VREG_S3	1.8 V	Selectable GPIO supply Selectable MPP I/O supply
VREG_S4	5 V	Selectable GPIO supply

Sub-regulated Regulator Connections

- All MSM8x74 reference design sub-regulation implementations are described below.

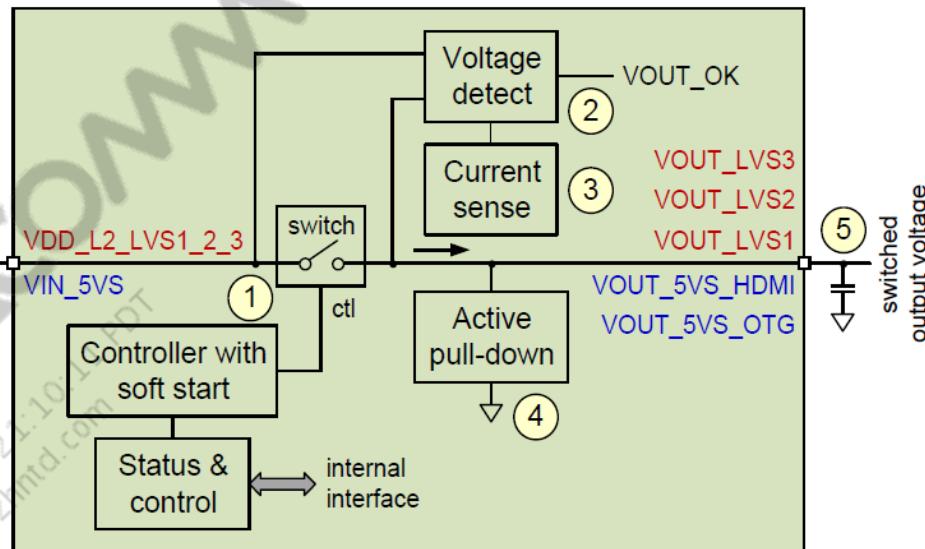


Voltage Switches

A low-voltage switch (LVS) or 5 V switch (5VS) can be used to gate a supply voltage to functions that do not support phone operation – functions such as sensors and OTG.

Switch features include:

- Soft start – prevents in-rush current from causing a voltage dip at the source regulator's output
- Output voltage verification
- Over-current protection – automatically turns off the switch and sends an interrupt
- Non-floating output – active pull-down during power-down
- Low-power mode – switch remains closed but all control functions are turned off



- 1) The switch is turned on slowly (by ramping its gate voltage) to limit in-rush current.
- 2) The output voltage is deemed “okay” when it is about 10% less than the input voltage.
- 3) The current-protection threshold is $2 \text{ to } 6 \times I_{\text{rated}}$ current; switch is opened and an interrupt is generated if the current goes above $3 \times I_{\text{rated}}$ value.
- 4) When opened, output is pulled down to ground.
- 5) External components are not required. If an output capacitor is used, do not exceed $1.0 \mu\text{F}$.

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General Housekeeping



Clock Architecture

Clock drivers have 50 Ω output impedance

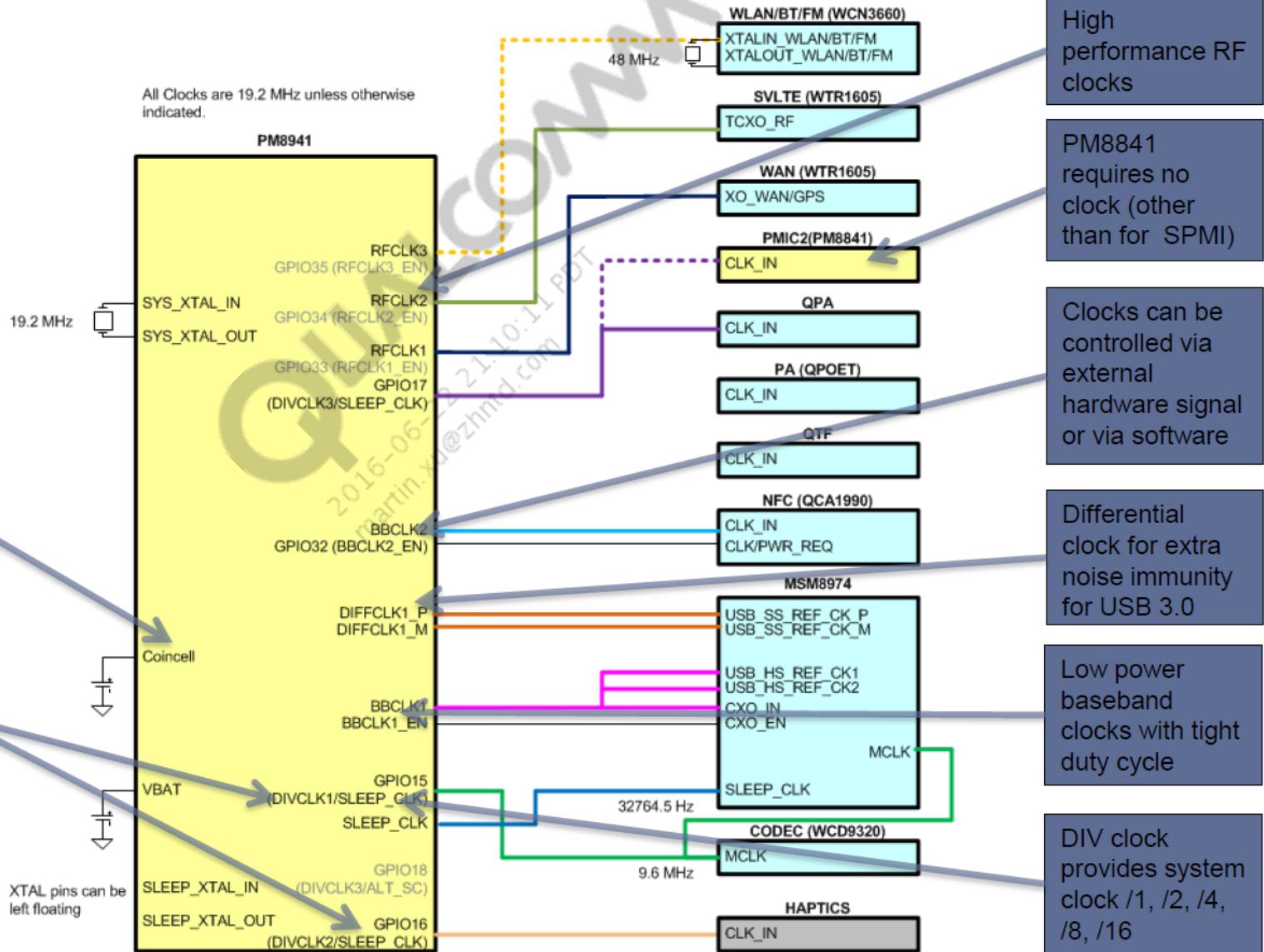
Single 19.2 MHz XTAL can act as the source for all clocks in the system

RTC backed up with a coincell/coincap even with no 32 kHz XTAL

Additional sleep clocks and DIVCLKs hidden behind GPIOs

32 kHz RTC/ Sleep clock not required

All Clocks are 19.2 MHz unless otherwise indicated.



High performance RF clocks

PM8841 requires no clock (other than for SPMI)

Clocks can be controlled via external hardware signal or via software

Differential clock for extra noise immunity for USB 3.0

Low power baseband clocks with tight duty cycle

DIV clock provides system clock /1, /2, /4, /8, /16

System Clocks

- Several clocks and clock outputs are used for general housekeeping functions and elsewhere throughout the system.
- 19.2 MHz crystal oscillator (XO) circuit; the system's master clock
- Five sets of XO controller and buffer circuits
- Differential XO output
- 19.2 MHz RC oscillator for power-up and emergency backup
- Divided and buffered clock for MP3 support
- 32.768 kHz XO – or calibrated low-frequency RC oscillator – for sleep and for the Real-Time Clock (RTC)
- Multiple buffered Sleep clock outputs
- SMPS clocks

System Clocks – Block Diagram

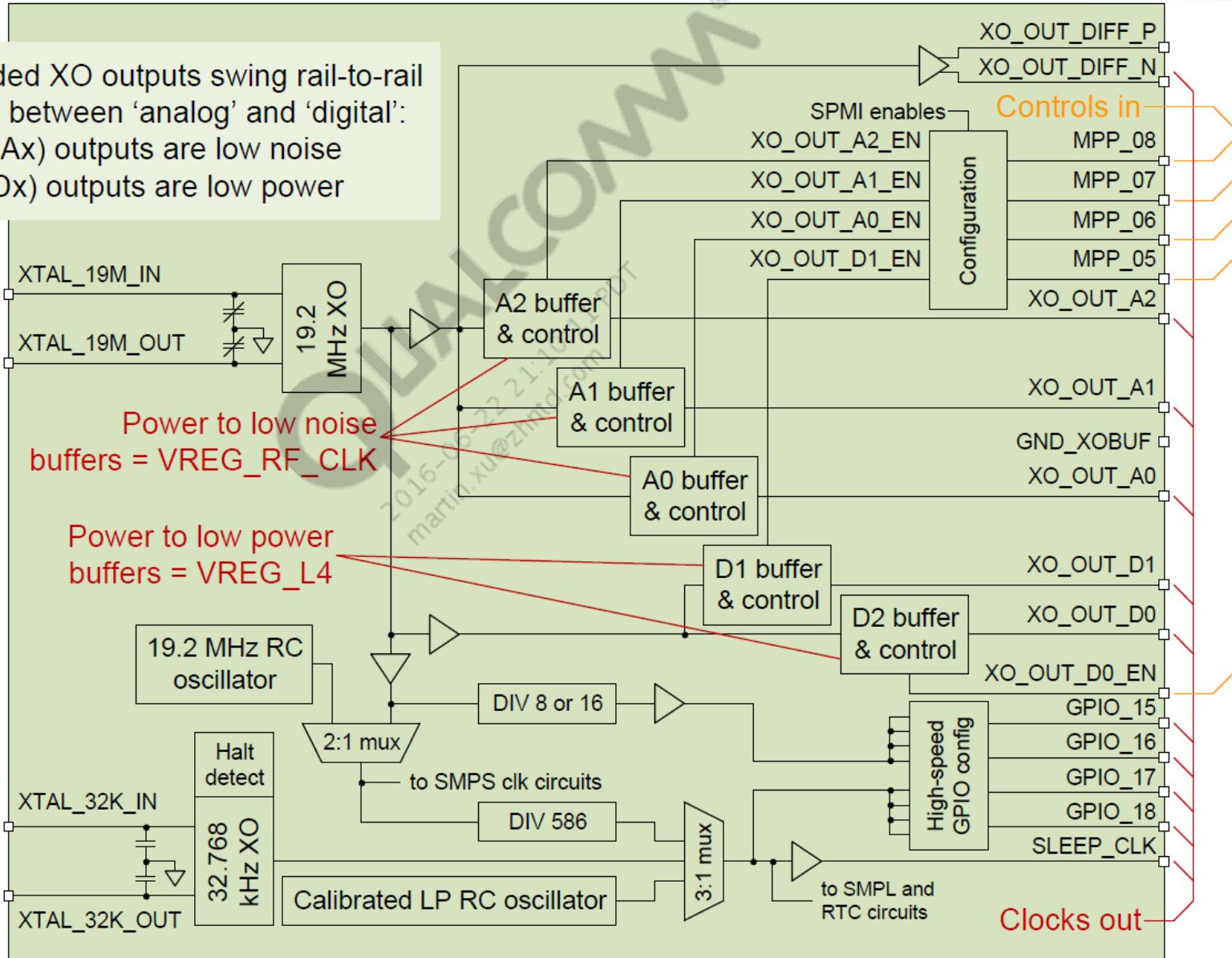
Single-ended XO outputs swing rail-to-rail
Difference between 'analog' and 'digital':
– Analog (Ax) outputs are low noise
– Digital (Dx) outputs are low power

Required
19.2 MHz
crystal

Power to low noise
buffers = VREG_RF_CLK

Power to low power
buffers = VREG_L4

Optional
32.768 kHz
crystal



SLEEP_CLK\RTC Generation and Outputs

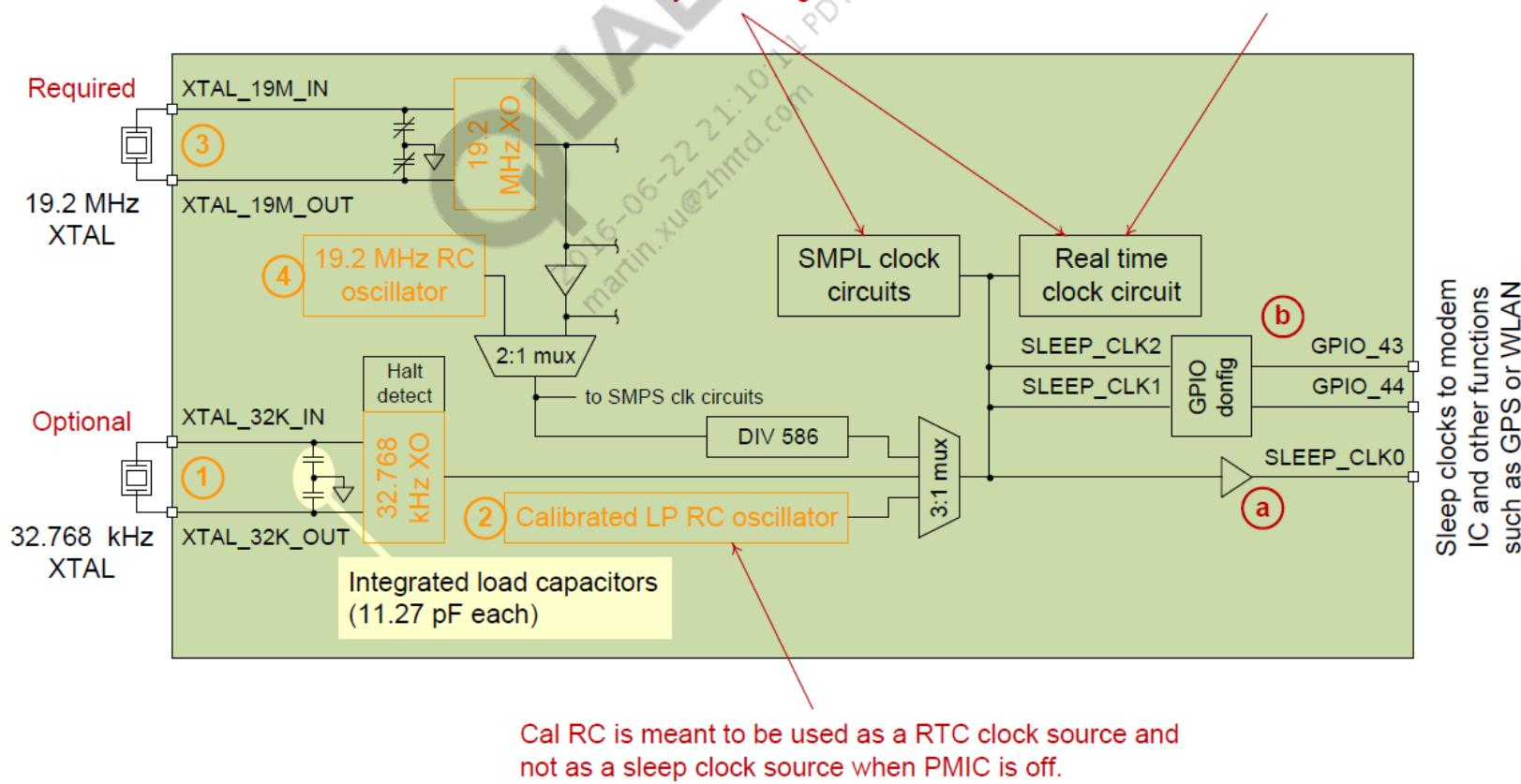
- Further discussion on the next slide:

- Source options (orange)
- Switchover
- Output options (red)

- SMPL is supported even if the only power source is a keep-alive capacitor at VCOIN.
- RTC is not supported by keep-alive capacitor; requires qualified coin cell/super capacitor when the main battery is missing.

RTC input clock source

- Uses XO/586 when the device is in active and sleep mode
- Uses calibrated low-frequency RC oscillator when the device is off



SLEEP_CLK\RTC Generation and Outputs (cont.)

- Source options
 1. A 32.768 kHz crystal source – This low-power source can have high accuracy and stability, depending upon the external crystal; the 32.768 kHz oscillator circuit is disabled by default in hardware.
 2. Calibrated low-frequency RC oscillator
 - a. Used as a source of RTC clock when PMIC is off; requires a qualified coin cell or super cap to support RTC when battery is removed
 - b. Periodically uses the XO signal for calibration, achieving accuracy suitable for RTC without an external crystal
 - c. Eliminates the external 32.768 kHz crystal, but increases the sleep mode current consumption; the 32.768 kHz oscillator consumes about 1 μ A average current, while this solution consumes about 5.5 μ A average current
 3. The 19.2 MHz XO divided by 586 (32.7645 kHz nominal) – This is the source of sleep clock and RTC clock when the device is in active and sleep mode.
 4. The 19.2 MHz RC oscillator divided by 586 (32.7645 kHz nominal) – 19.2 MHz RC oscillator is a on-chip circuit with coarse frequency accuracy:
 - a. Used during PMIC powerup until software switches over to XO/586
 - b. Used in active or sleep mode only if other sources are unavailable

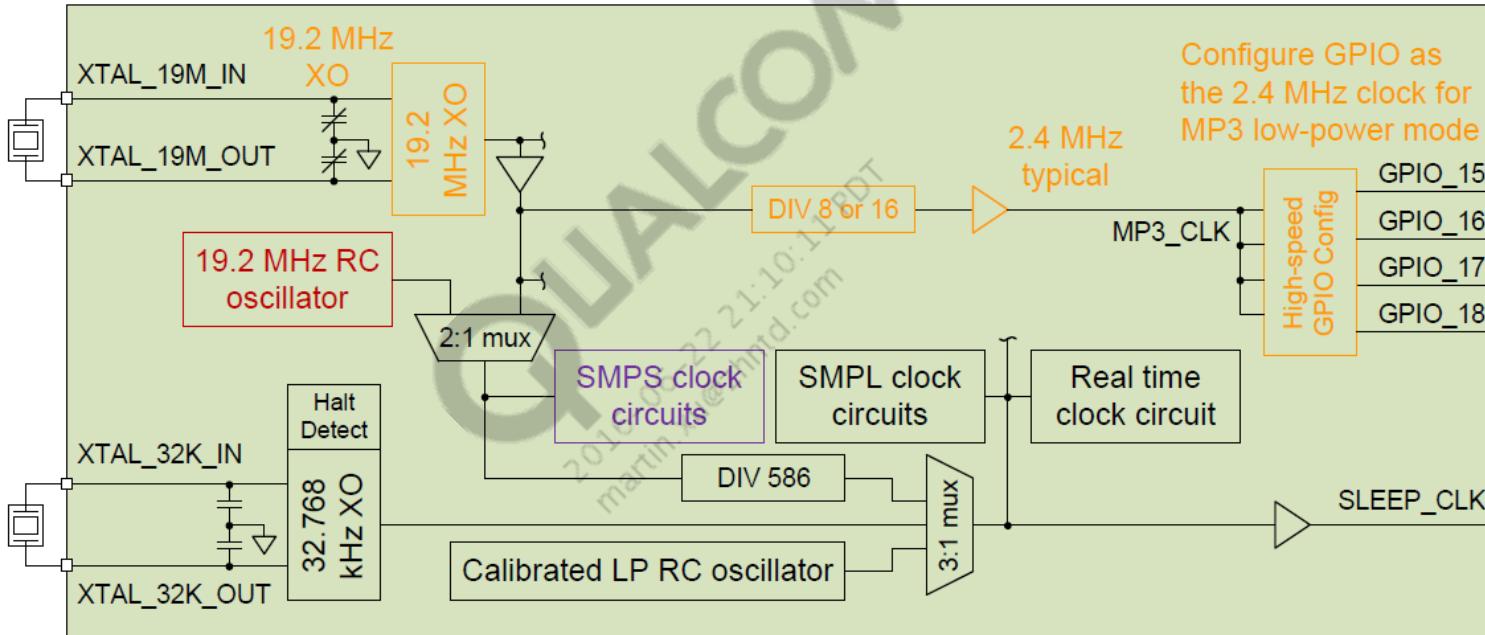
SLEEP_CLK\RTC Generation and Outputs (cont.)

- Swithchover
 - The 32.768 kHz signal is monitored to ensure continuous oscillation. If the 19.2 MHz XO oscillator source stops oscillating, a multiplexer automatically switches to the 19.2 MHz RC signal, and an interrupt is generated. Narrow pulses at the SLEEP_CLK output may occur during this switchover.
- Output options
 - A dedicated output pin (SLEEP_CLK) for the modem IC and others; toggles only when the PMIC is on and stays low when the device is off, even though the crystal oscillator continues to run.
 - GPIO_15, GPIO_16 and GPIO_17 can be configured as sleep clock outputs to support other functions

Other Clock Topics

1) MP3 clock

- 19.2 MHz XO source
- Divide by 8 for 2.4 MHz
- Configure high-speed GPIO for external routing



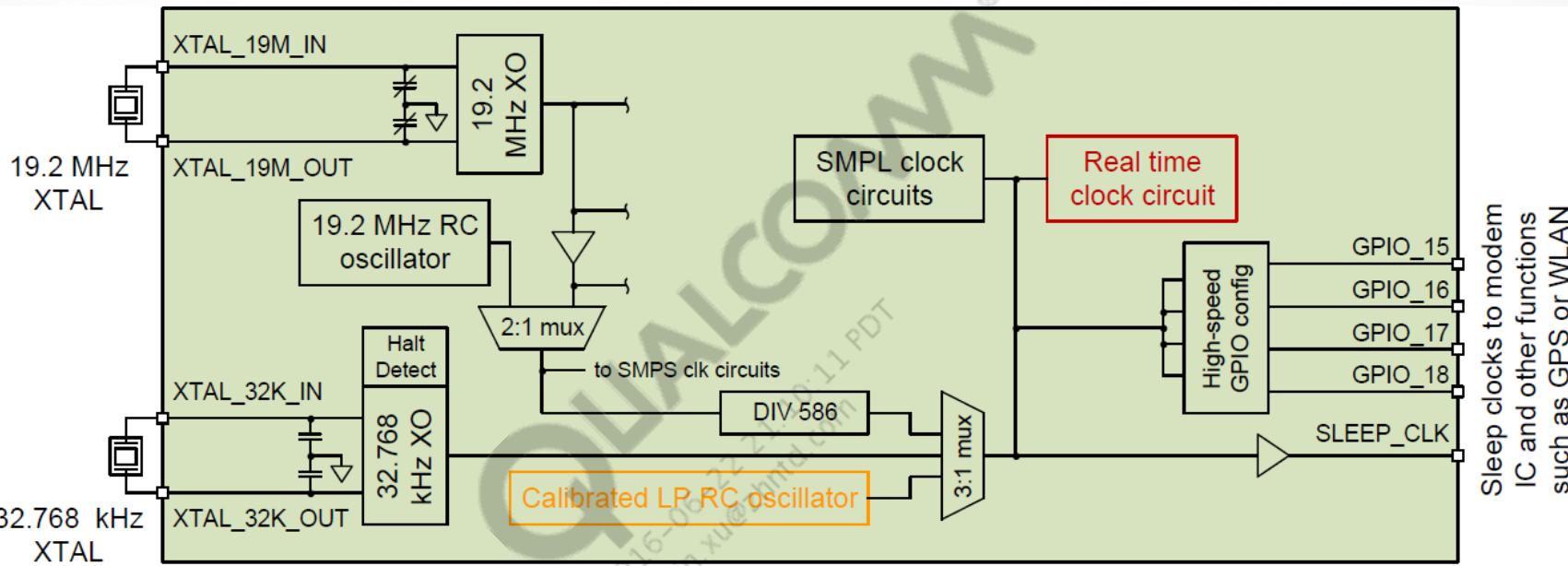
2) 19.2 MHz RC oscillator

- Default clock source during power-up
- Modem IC clears interrupts that allow switchovers to 32.768 kHz XTAL and 19.2 MHz XO sources
- Transitions synchronized, glitch-free
- RC oscillator powered down when not used to reduce power consumption; draws too much current for keep-alive battery – PMIC must be on
- Restarts if XTAL or XO halts

3) SMPS clocks

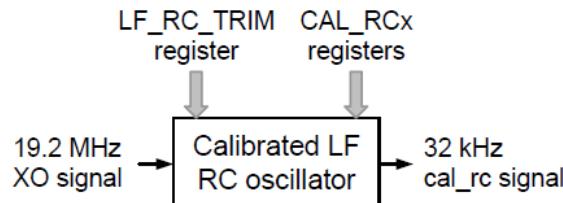
- The switched-mode power supplies are driven by one of two clock sources: 1) RC oscillator or 2) XO source (both 19.2 MHz nominal).
- Programmable and variable divide-by-3 creates 6.4 MHz
- Capable of skipping pulses; allows adjustments so that spectra due to transients can be shifted to minimize RFI

Other Clock Topics (cont.)



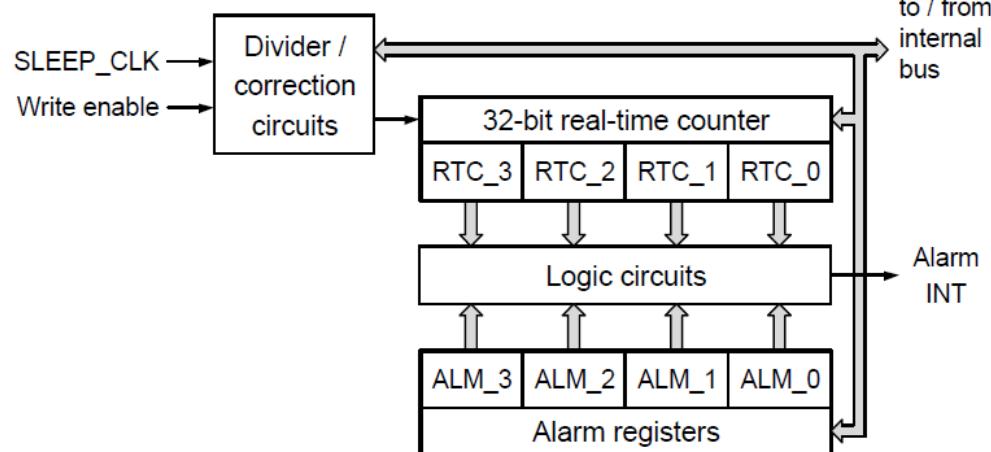
4) Calibrated low-frequency RC oscillator

- Periodically uses XO signal for calibration, achieving accuracy suitable for RTC without external crystal
- Eliminates the external 32.768 kHz crystal, but increases the sleep mode current consumption; the 32.768 kHz oscillator consumes about 1 μ A average current, while this solution consumes about 5.5 μ A average current



5) Real-time clock (RTC)

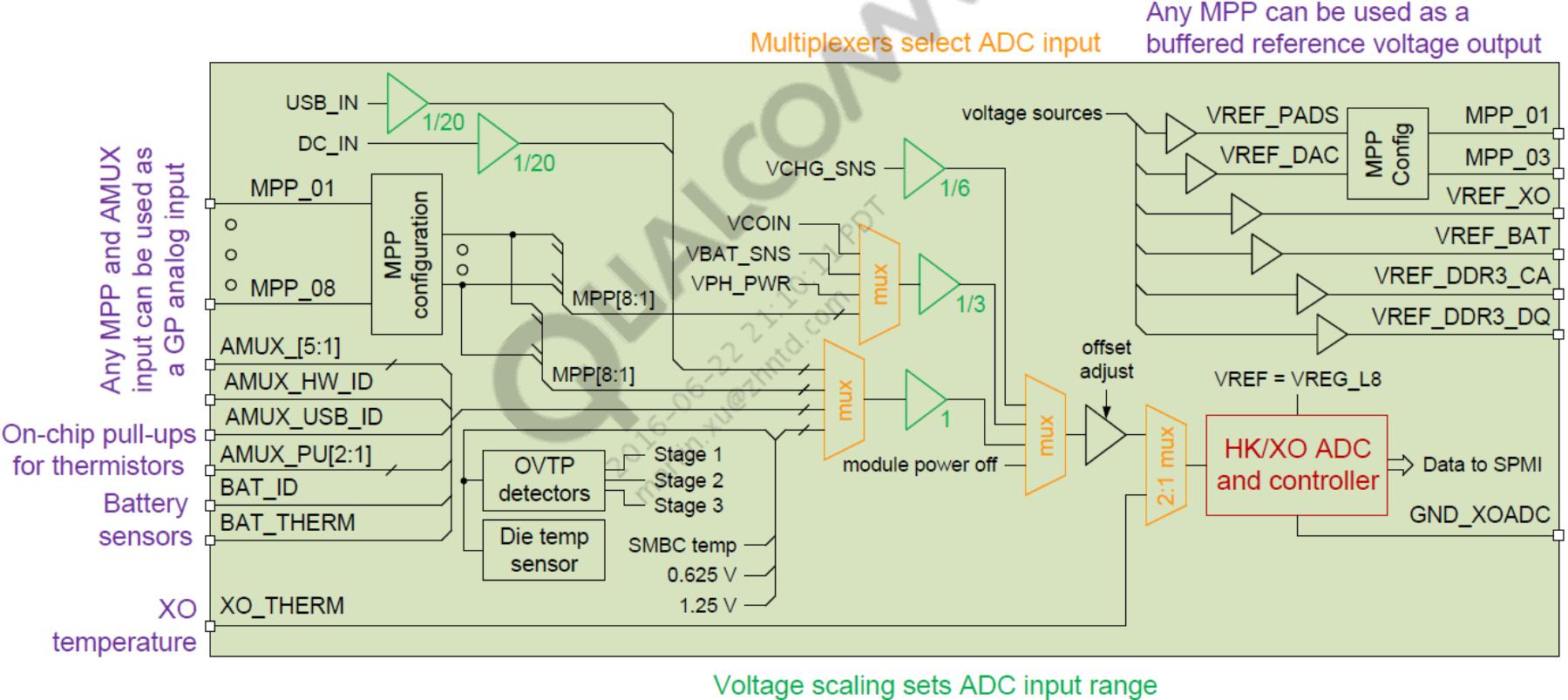
- For calendar and alarm functions



HKADC\AMUX

- Several analog switches and multiplexers select one signal for ADC conversion.
- Nestled within the multiplexers are voltage scaling circuits that condition the signals to best utilize the ADC's dynamic range.
- The selected signal allows handset software to monitor various voltage nodes, auxiliary inputs, and the die temperature using a single ADC.
- The ADC input cannot reliably go below 0.05 V or above $V_{REG_L8} + 0.05$ V; do not exceed this range.
- Gain and offset errors vary between multiplexer channels; calibration values apply to the specific channel being calibrated only. Calibrate each channel separately.
- A functional block diagram is provided on the next slide.

HKADC\AMUX (cont.)



HKADC\AMUX (cont.)

- As implied by its name, the HK/XO ADC circuit supports two modes:
 - General HK operation, where the signal selected by the analog multiplexer is routed to the ADC
 - A direct path for crystal oscillator (XO) thermal monitoring

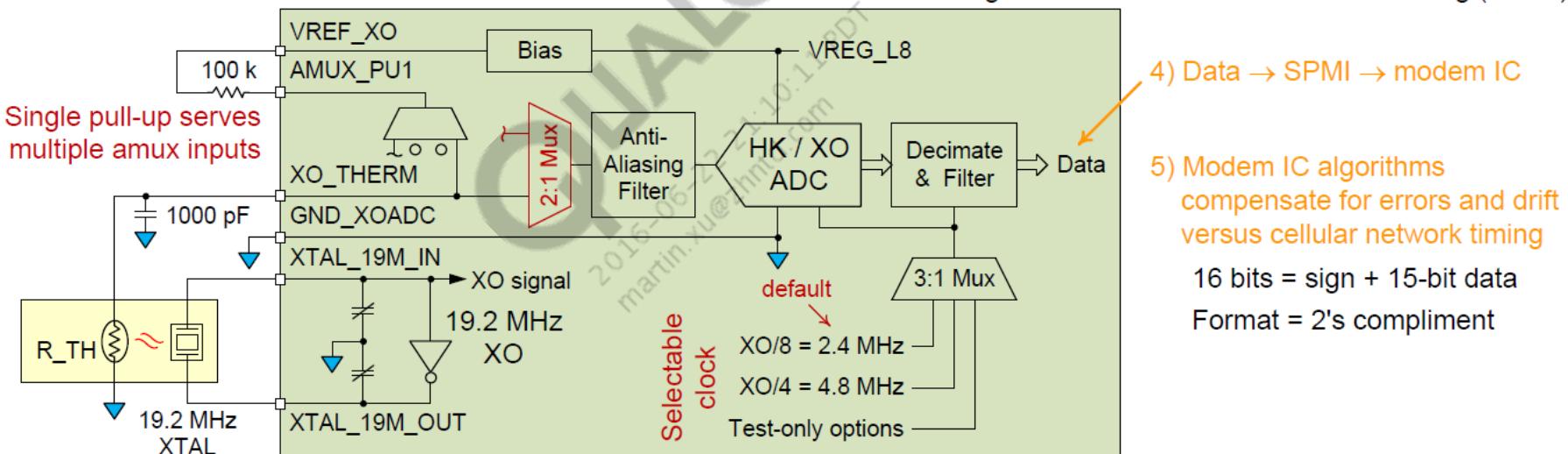
ADC input from AMUX circuits (ADC in HK mode) or XO circuits (ADC in XO mode); XO details are shown

2) Analog voltage into PMIC is proportional to crystal temperature

3) Filter and convert to digital domain

- Sigma-Delta ($\Sigma\Delta$) type ADC
- High accuracy
- Slow conversion and filtering

Programmable decimation rate and filtering (below)



1) Thermistor detects crystal temp Clock rate, decimation rate, and conversion time

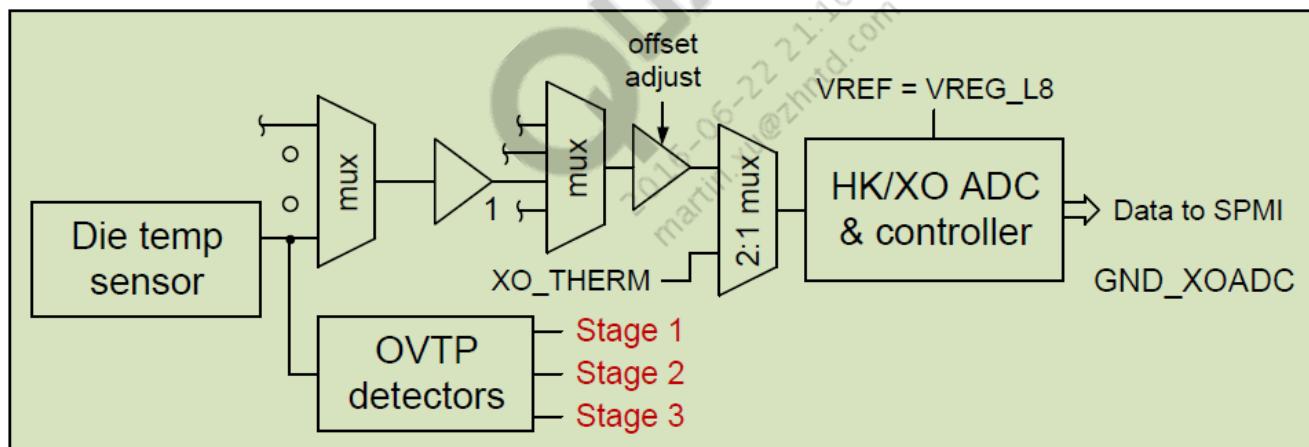
↓ = Isolated (island) ground for XO circuits only

The decimation filter can be enabled (Sinc1 & Sinc2) or disabled; the examples given at right are with the filter enabled

CLK	Decimation Ratio	Update Rate	Conversion Time	CLK	Decimation Ratio	Update Rate	Conversion Time
2.4 MHz	512	2.26 kHz	442 μ s	4.8 MHz	512	4.38 kHz	228 μ s
	1024	1.15 kHz	868 μ s		1024	2.26 kHz	442 μ s
	2048	580 Hz	1.722 ms		2048	1.15 kHz	868 μ s
	4096	290 Hz	3.428 ms		4096	580 Hz	1.722 ms

Over Temperature Protection

- The PMIC provides over-temperature protection in stages, depending upon the level of urgency as the die temperature rises.
 - Stage 0 – Normal operating conditions (less than 110°C); no interrupt is generated.
 - Stage 1 – 110°C to 130°C; interrupt sent to modem IC without shutting down any PM circuits.
 - Stage 2 – 130°C to 150°C; an interrupt is sent to the modem IC, and high-current drivers (LED drivers, backlight drivers, etc.) are shut down.
 - Stage 3 – Greater than 150°C; an interrupt is sent to the modem IC, and PM functions are completely shut down.



- Temperature hysteresis is incorporated such that the die temperature must cool significantly before the device can be powered on again.
 - If any start signals are present while at stage 3, they are ignored until stage 0 is reached.
 - When the device cools enough to reach stage 0 and a start signal is present, the PM circuits will power up immediately.

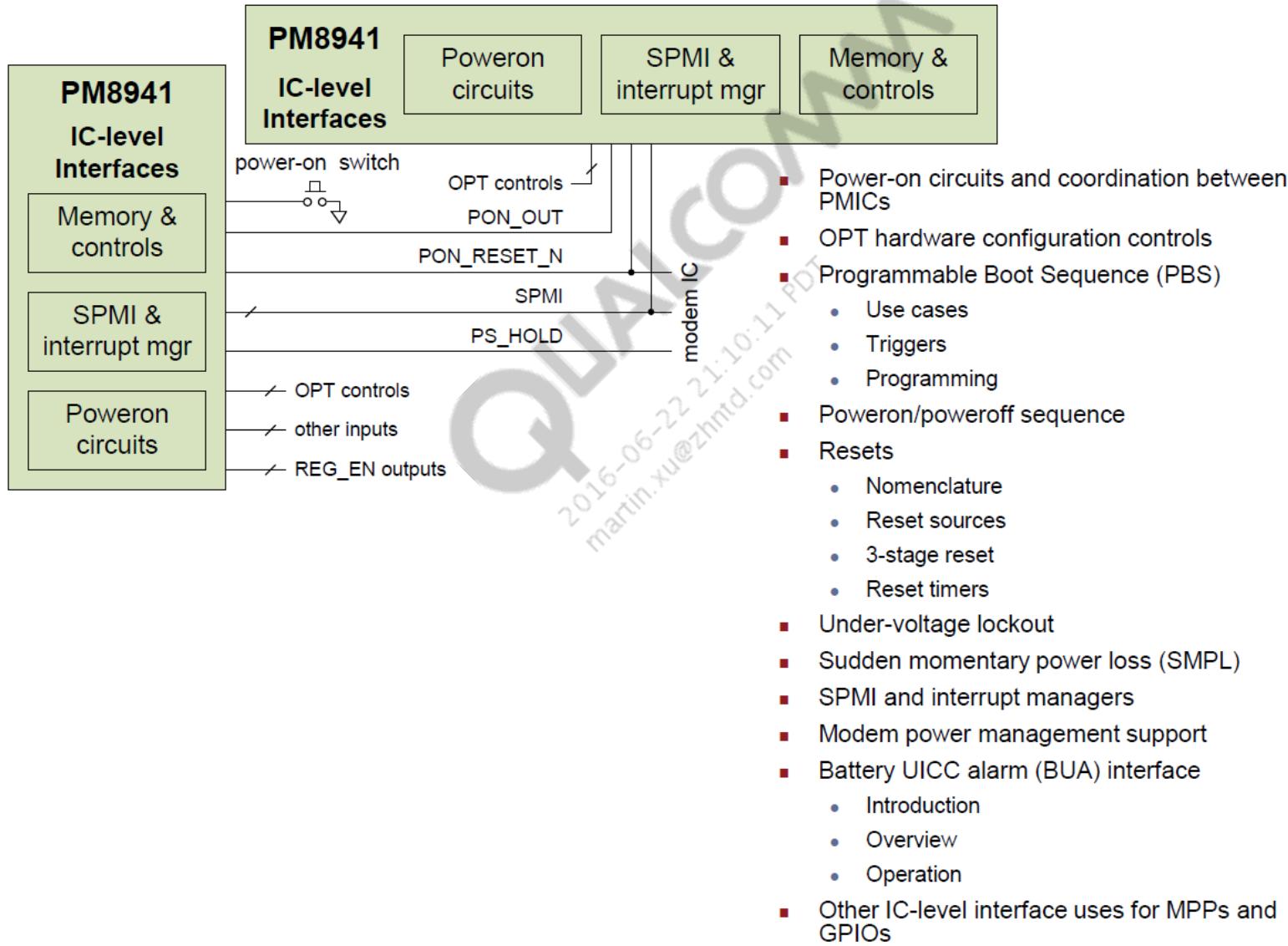
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IC Level Interface

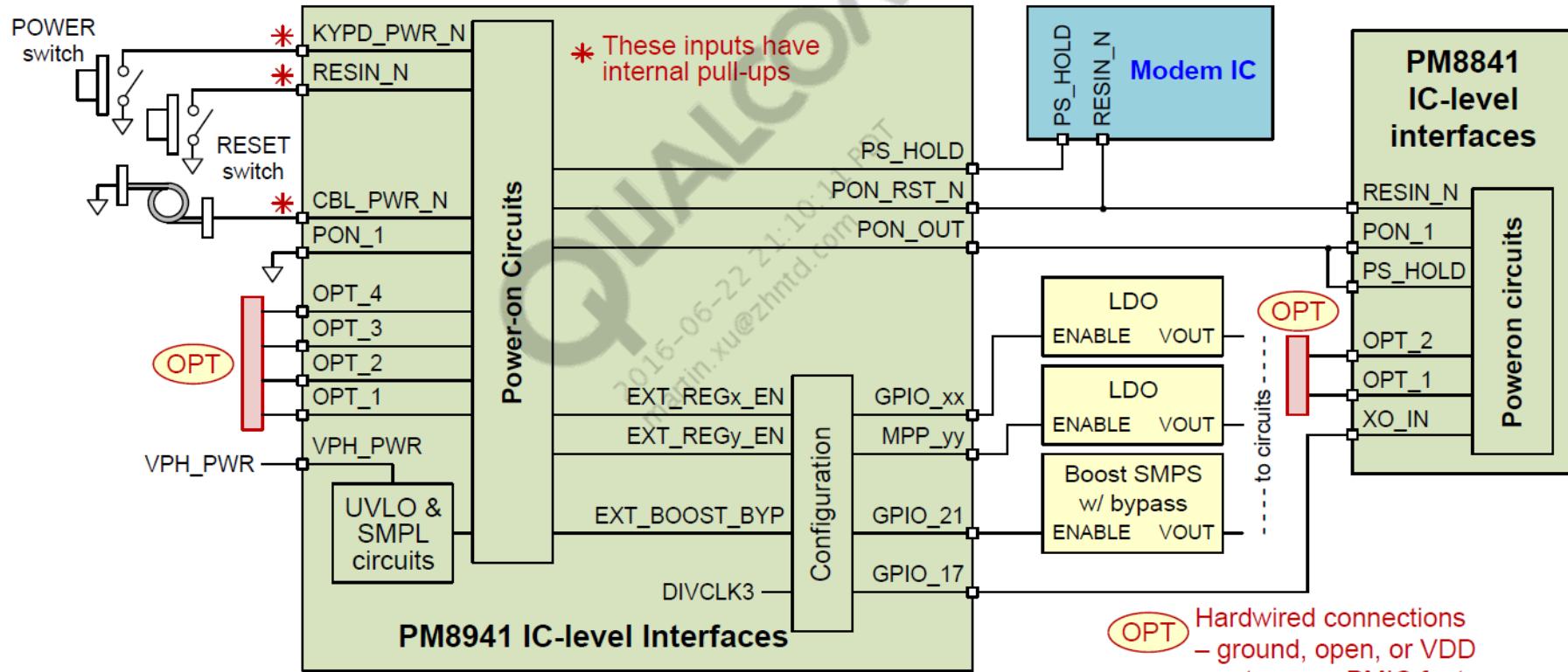


IC Level Interface



Power ON Circuits

- Dedicated PM8941 circuits continuously monitor events that might trigger a poweron sequence
- If an event occurs, these circuits power on the IC, determine the handset's available power sources, enable the correct source, enable the PM8841, and take the modem IC out of reset



- To power up immediately upon battery insertion, tie **KYPD_PWR_N** or **CBL_PWR_N** to ground
- In this case, the PMIC is always on and the modem IC should clear the **xxxPWR_PU** bit to turn-off the internal pull-up resistor, thereby reducing the PMIC quiescent current.

OPT Hardwired connections
– ground, open, or VDD

– sets some PMIC features
– see the following slides for more information

PM8941 OPT Hardware Configuration Controls

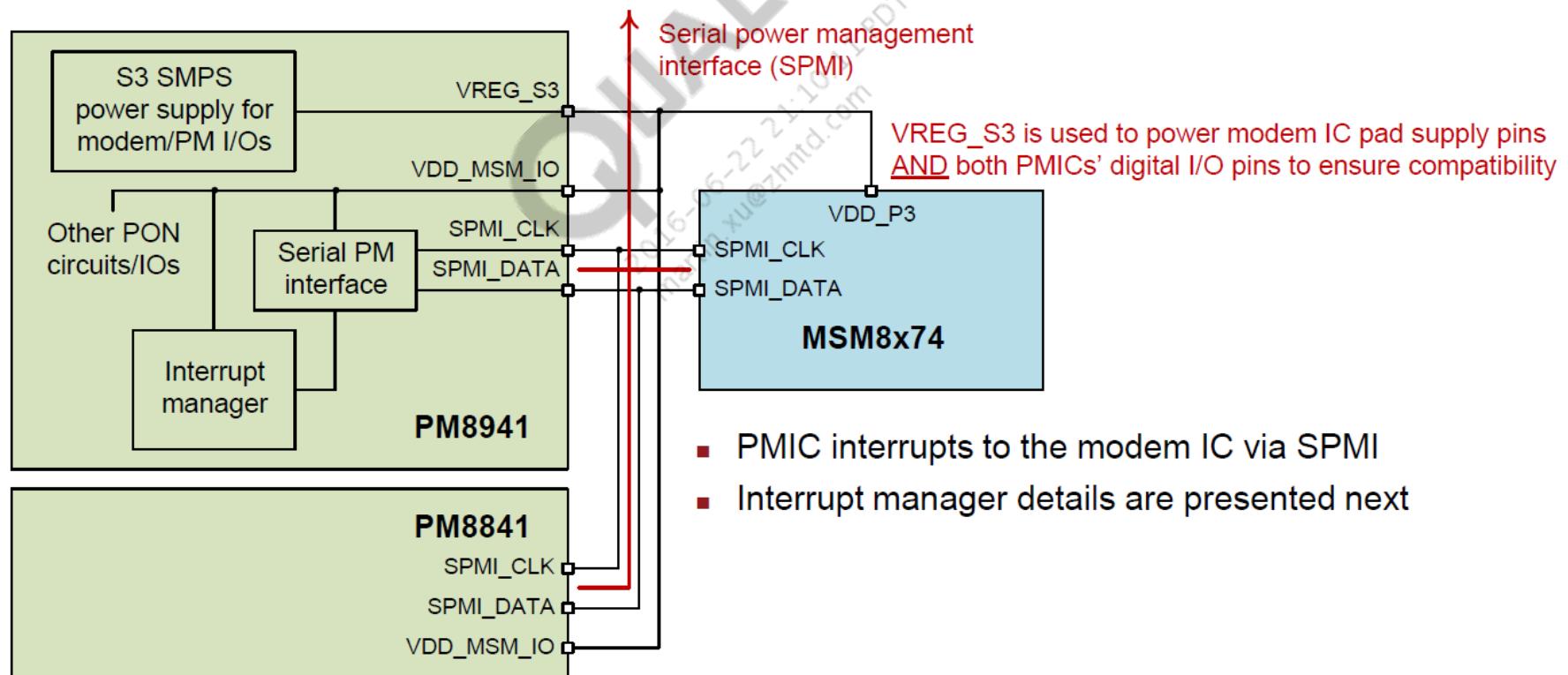
- Four PM8941 pins – OPT_[4:1] – must be hardwired to ground or VDD, or be left open (in a high-impedance state or Hi-Z); the settings of these four pins defines or influences the following PM8941 parameters:
- Each chipset that uses the PM8941 must set the OPT pins correctly for their particular application; the MSM8x74-based reference designs use these settings: OPT_[4:1] = GND, GND, GND, GND

OPT_1	External reset configuration
GND	KYPD_PWR_N + RESIN_N
Hi-Z	RESIN_N
VDD	KYPD_PWR_N

OPT_2	Chipset support
GND	MSM8974
Hi-Z	Reserved
VDD	Reserved

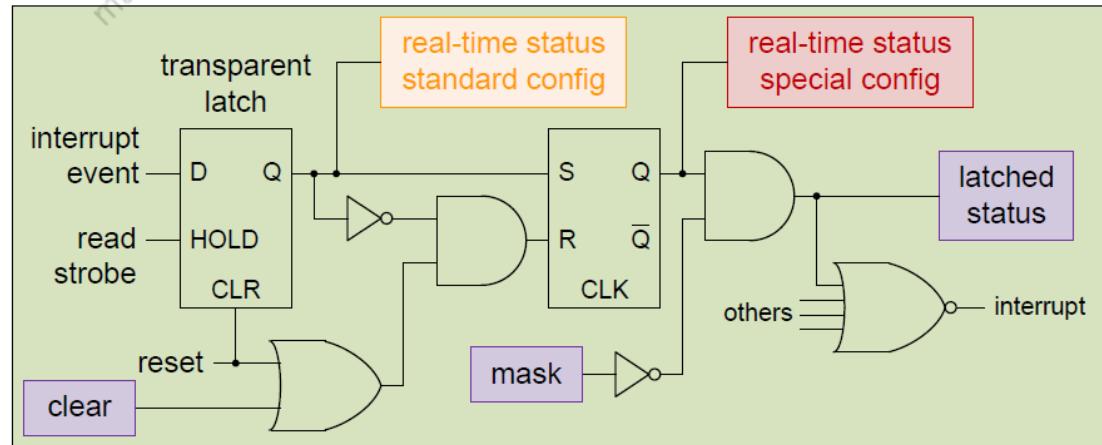
SPMI and Interrupt Manager

- SPMI – primary IC-level interface for efficient initialization, status, and control communications
- Application programming interface (API) is used to program PMICs, indirectly exercising SPMI
- The coin cell backs up several SPMI registers; at powerup, SPMI defaults are restored except bits backed up by the coin cell – they are only restored to default values if the coin cell expired



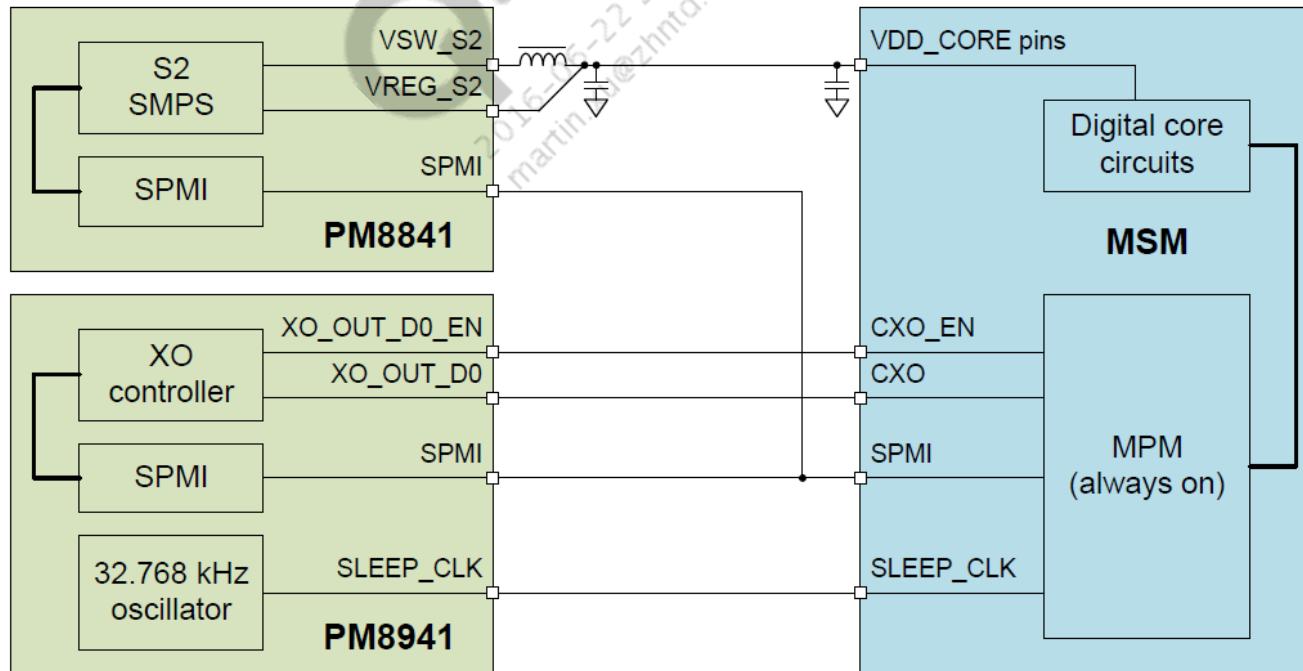
Interrupt Manager Details

- An interrupt manager receives internal reports on numerous functions and conveys status signals to the modem device, supporting its interrupt processing.
- Each interrupt event has the following associated SPMI bits:
 - Interrupt mask (read/write) – allows modem IC to ignore event; latched status hidden and interrupt is not asserted.
 - Interrupt real-time status (read only) – follows real-time interrupt status (active or inactive) for standard configuration interrupts; special configuration interrupts are highlighted in red and defined further below.
 - Interrupt latched status (read only) – set when event is active and interrupt mask bit is cleared; stays set until clear bit is set.
 - Interrupt clear (read/write) – clears latched status automatically after latched status is read.
- Unmasked interrupts notify the modem device that at least one interrupt has occurred.
- Upon powerup, software should check the RTCRST interrupt – if set, the coin cell voltage is too low, and the RTC and SRAM contents and the SMPL and WDOG interrupts are unreliable.
- Most interrupts are 'standard' (orange), but four are 'special' (red) interrupts:
 - Real-time clock reset (RTCRST)
 - Sudden momentary power loss (SMPL)
 - MDM watchdog timeout (WDOG)
 - Die over-temperature (OVERTEMP)
- These are not real-time readable – they occur only when the PMIC is reset or when they cause a PMIC reset. They are latched and backed up via coin cell. Upon a PMIC restart, latched interrupts inform the modem device why they were triggered.

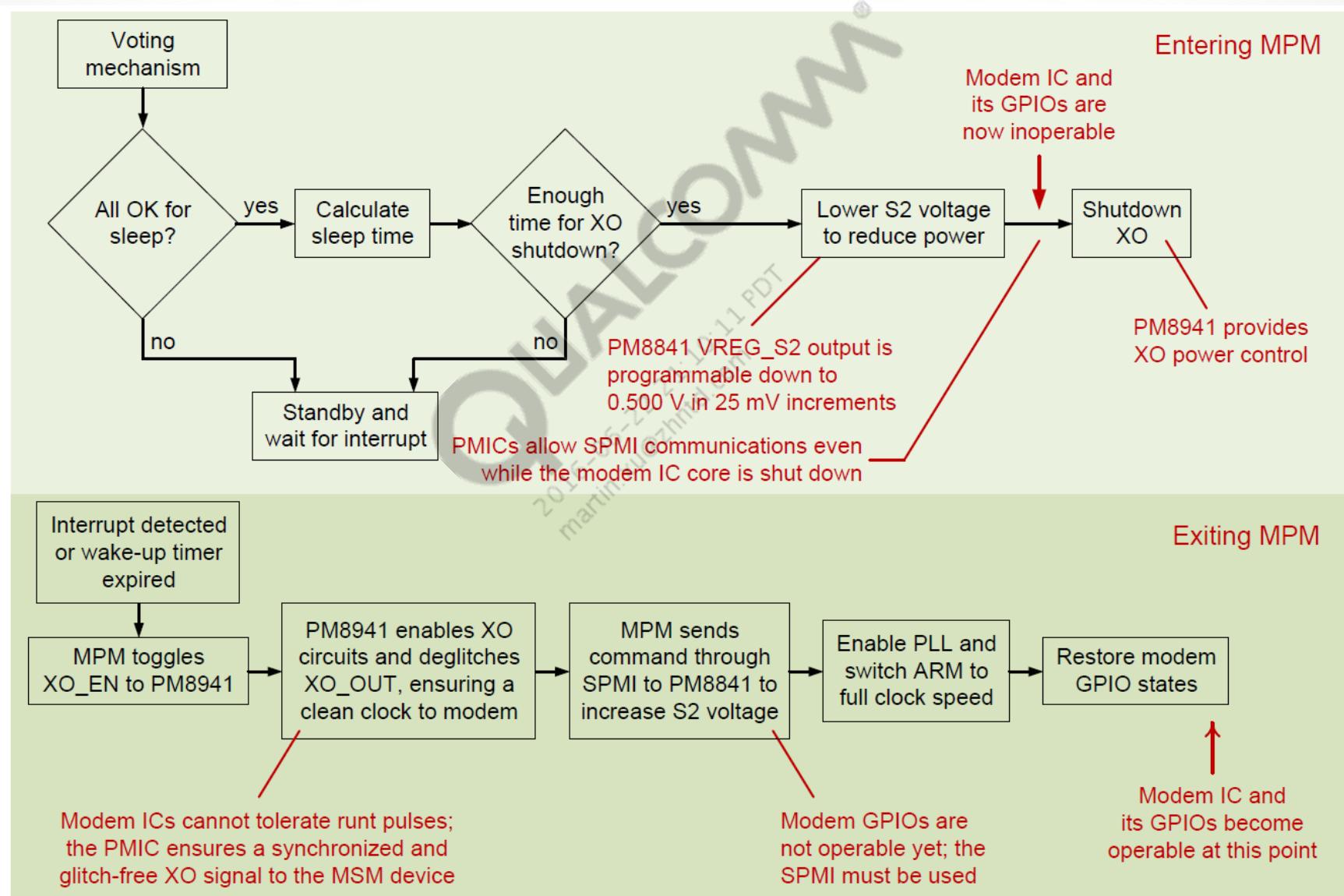


Modem Power Manager (MPM) Support

- SPMI is able to communicate with the modem IC, even while its core circuits are powered down. PMIC features necessary to support MPM:
 - Key regulator outputs programmable to 750 mV
 - SPMI continues modem communications, even while the modem IC core is powered down
 - The PMIC controls the XO power supply
 - The PMIC ensures a synchronized and glitch-free XO signal for the modem device
- Connections required for MPM support are illustrated below.



Modem Power Manager (MPM) Support (cont.)



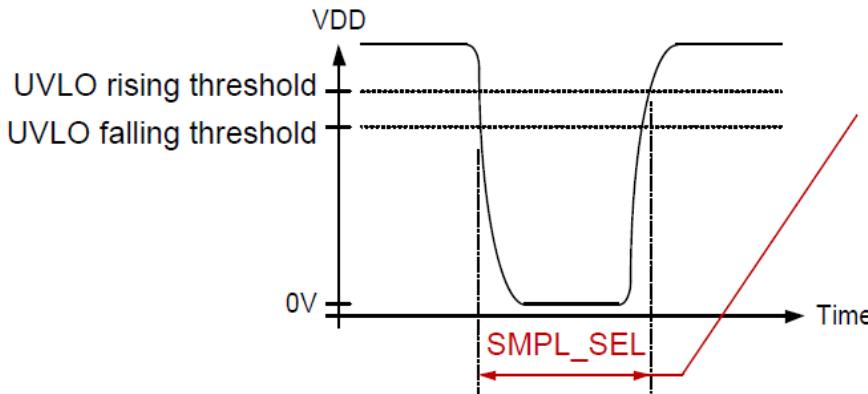
SMPL

When enabled by software → immediate and automatic recovery from a momentary PM8941 power loss

- If VDD drops out of range (< 2.475 V nominal), then it returns in-range within a programmable interval of between 0.5 and 2.0 seconds, and the recovery is executed.

Some operational details:

- UVLO event clears PON_RST_N; PMIC is powered down
- Super capacitor or coin cell takes over as SMPL power source
- If VDD returns to its valid range before timeout, a poweron sequence is initiated without software intervention, and an interrupt is sent to the modem IC indicating: 1) Power was momentarily lost, 2) RTC is corrupted due to insufficient voltage, and 3) Current PMIC actions are not a normal power sequence.
- If SMPL times out without VDD returning to its valid range – the handset must undergo normal poweron sequence whenever the next initializing event occurs.
- SMPL operation must be enabled by software and requires a coin cell or keep-alive capacitor (values listed below) at VCOIN.
- For a normal powerdown, SMPL must be disabled via software before de-asserting PS_HOLD to avoid an inadvertent SMPL override.



If VDD recovers within this programmed interval a poweron sequence is immediately and automatically initiated by power management circuits without software intervention.

If RTC support is not needed when battery is removed, a backup capacitor can be used on VCOIN pin. A ceramic capacitor with an effective capacitance of 10 μ F can support SMPL for up to 2 seconds.

UVLO

The UVLO circuit automatically turns off the PM8941 at severely low VDD conditions (2.475 V nom).

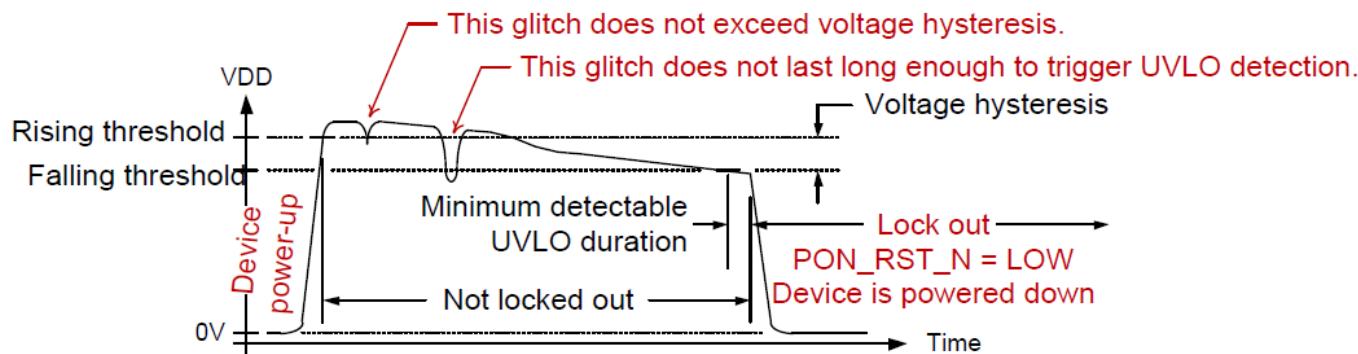
Although UVLO is a hardware feature, it allows for software interaction to realize additional features, such as SMPL recovery, poweron sequence abort, and watchdog timeout soft reset.

Operation

- As the IC powers up, VDD must exceed a rising threshold (2.775 V, default) to initiate the poweron sequence.
- Voltage hysteresis (300 mV, default) and delays prevent minor glitches from being detected as UVLO events.
- If VDD drops below the falling threshold (UVLO rising threshold minus voltage hysteresis) for sufficient duration, a valid UVLO event is detected.
 - PON_RST_N is cleared (LOW) and the device is powered down.

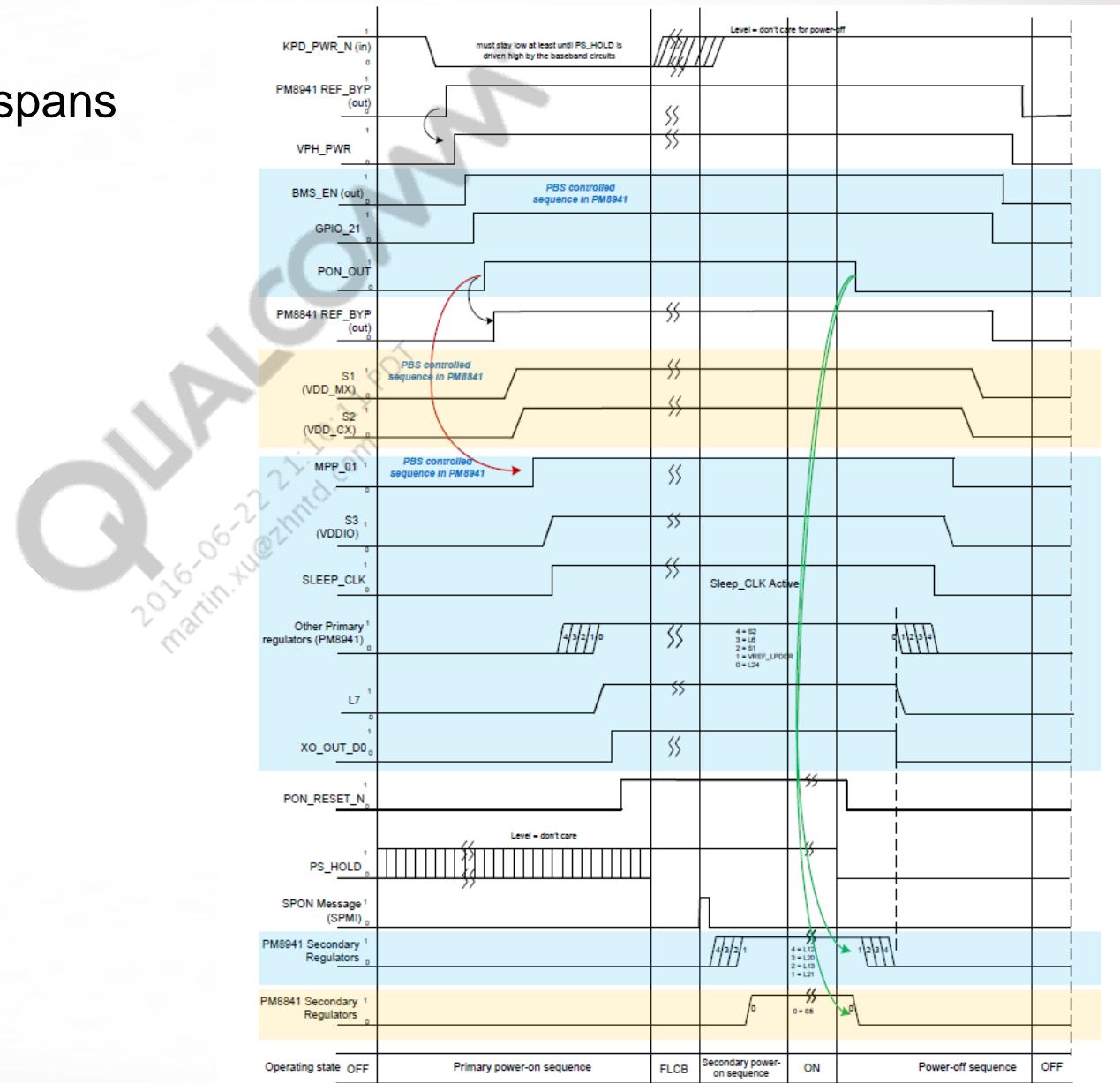
The UVLO rising threshold voltage is programmable

- 1.675 V to 3.225 V in 50 mV increments (2.775 V, default)
- Other than this programmable threshold, software is not involved in UVLO detection.
- Hysteresis and time delays are not programmable, and UVLO events do not generate interrupts; they are reported to the modem IC via PON_RST_N as part of powerdown.



Power On/Off Sequence

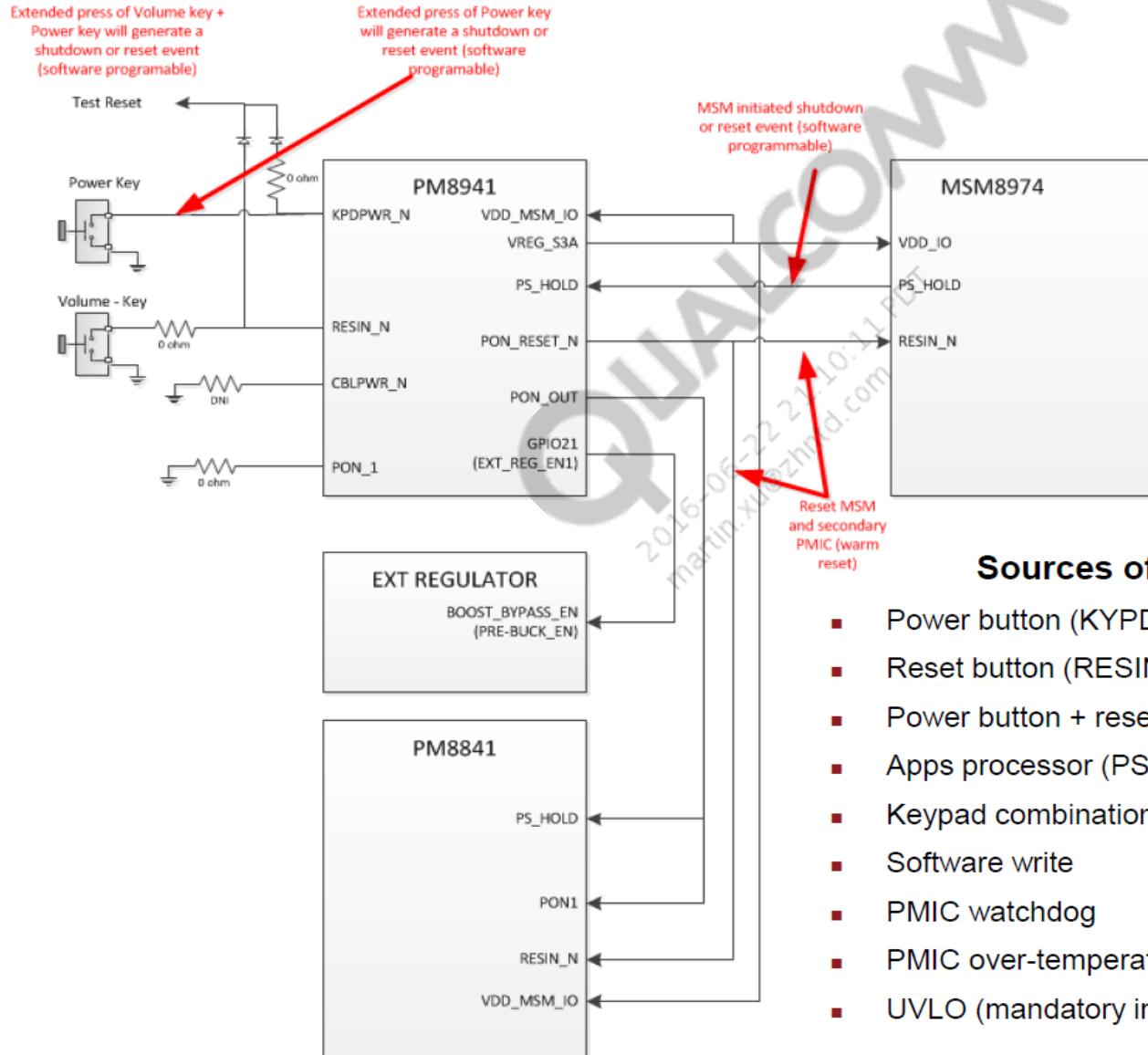
- Power On sequence spans PM8941 and PM8841



Reset – Nomenclature

- Reset triggers
 - Internal and external triggers that are routed to the PMIC's power-on module. The power-on module decides what action should be taken, based on these triggers (e.g., over-temperature stage 3, KYPD_PWR_N, RESIN_N, PS_HOLD)
- Reset types
 - Describes the behavior of the PMIC during a reset or shutdown event (e.g., warm reset or hard reset event)
 - The type of reset event is determined by configuration registers in the power-on module and broadcast throughout the PMIC using reset signals
- Reset signals
 - Signals that are generated in the power-on module and broadcast throughout the PMIC (e.g., xVdd_rb, dVdd_rb, global_soft_rb, shutdown1_rb)
- (Register) reset domains
 - Several reset domains exist to allow some PMIC registers to maintain state throughout certain reset events
- Reset stages
 - Three stages of resets – Software configurable bark, software configurable reset, failsafe reset

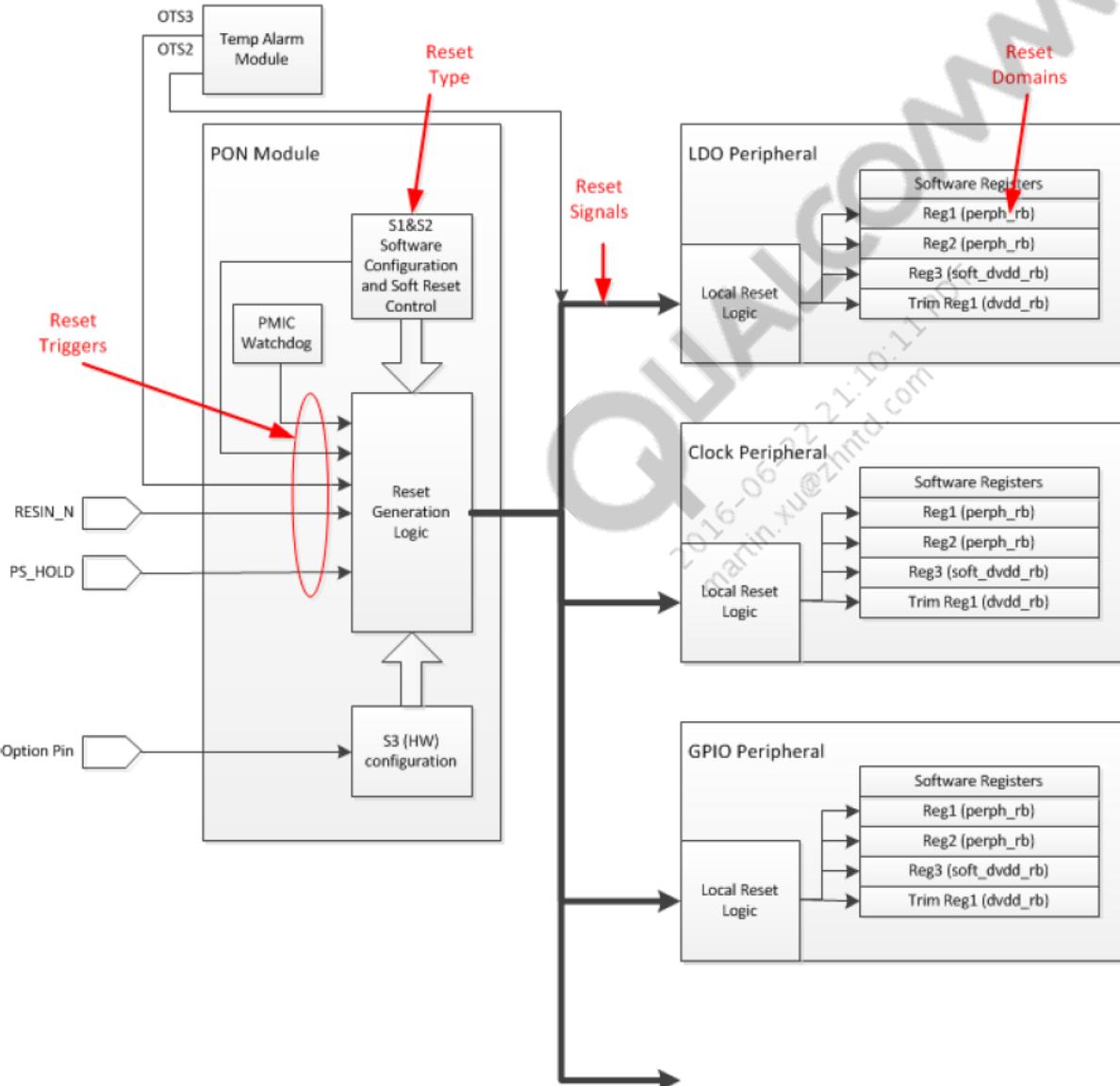
External Reset Block Diagram



Sources of reset (programmable)

- Power button (KYPD_PWR_N)
- Reset button (RESIN_N)
- Power button + reset button
- Apps processor (PS_HOLD)
- Keypad combination (upto 3 keys)
- Software write
- PMIC watchdog
- PMIC over-temperature sensor
- UVLO (mandatory immediate shutdown)

Peripheral/Module Resets and Internal Reset Block Diagram



- PMIC supports multiple triggers for reset
 - (i.e., Poweron button, Overtemp, PS_HOLD (apps processor), dedicated reset button)
 - By default all peripherals will follow all resets
 - Software can individually configure each peripheral to ignore each reset trigger individually according to mask.
 - Maintain core rails during watchdog reset (for debug)
 - Maintain LCD backlight during reset (maintain LCD content through reset)

3 Stage Reset

■ Stage 1 (Bark)

- PMIC generates interrupt, giving the MSM opportunity to fix the problem or gracefully reset the system. Example events that can cause a bark:
 - ◆ Overtemperature indicates system is getting too hot
 - ◆ PMIC watchdog indicates that it has not kicked

■ Stage 2 (Software-configurable Bite)

- If reset is ignored, PMIC will force a reset event (selectable by software)

■ Stage 3 (Hardware-mandatory Bite)

- User can generate a mandatory reset by long key press of RESIN_N, KYPD_PWR_N or RESIN_N and KYPD_PWR_N in combination (selectable via OPT_1 pin setting as shown below).
 - ◆ Cannot be disabled by software
 - ◆ Resets PMIC back to factory default
 - ◆ Only intended as a backup option if Stage 1 and Stage 2 fail

OPT_1 pin connection

VDD → KYPD_PWR_N

Hi-Z → RESIN_N

GND → RESIN_N + KYPD_PWR_N

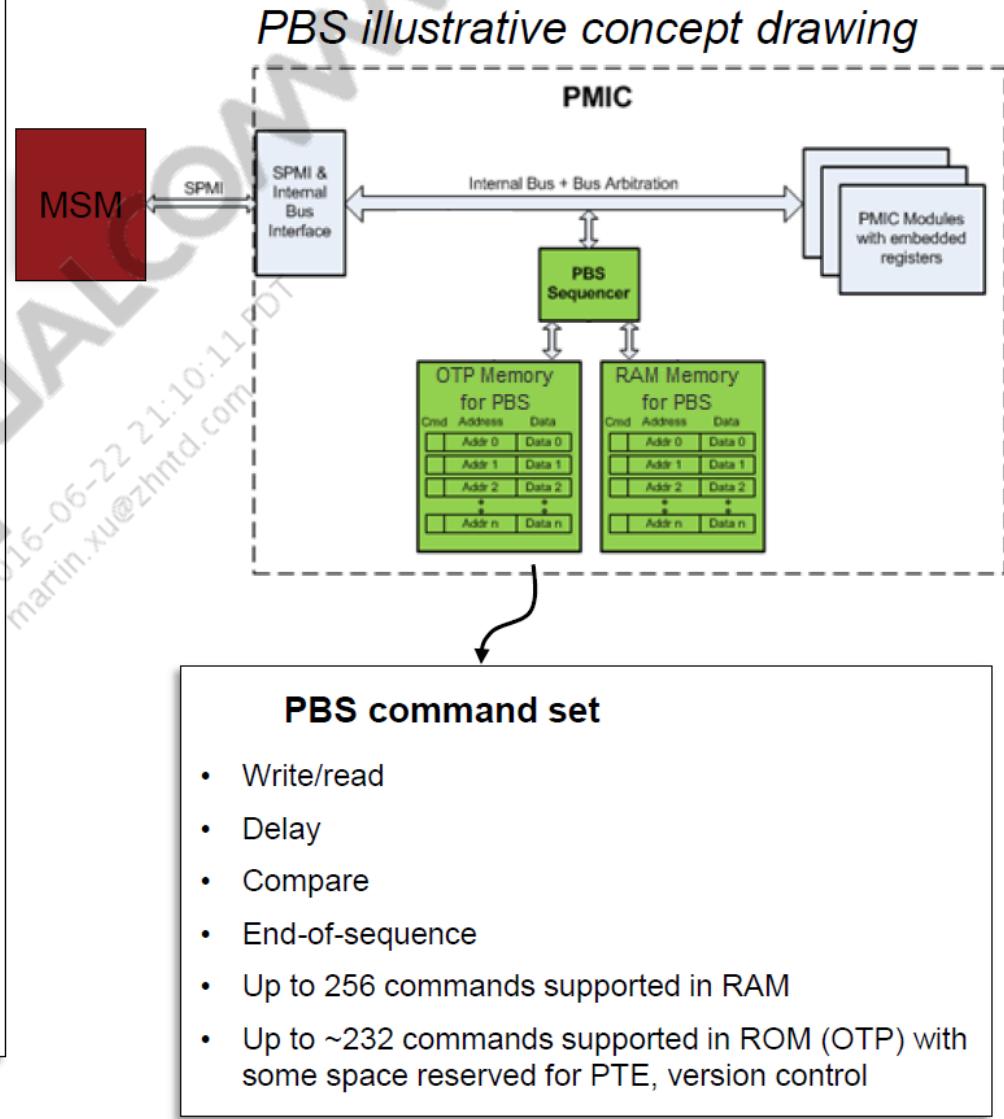
Reset Timers

#	Reset trigger	Stage 1 reset (debounce) timer	Stage 2 reset (delay) timer	Stage 3 reset timer
1	KYPD_PWR_N ^a	0 - 10.256 sec	0 – 2 sec	
2	RESIN_N ^a	0 - 10.256 sec	0 – 2 sec	0 sec
3	KYPD_PWR_N + RESIN_N ^a	0 - 10.256 sec	0 – 2 sec	2 – 128 sec
4	Keypad press ^a	0 - 10.256 sec	0 – 2 sec	
5	PMIC watchdog ^b	0 – 127 sec	0 -127 sec	N/A
6	PS_HOLD	N/A	N/A	N/A
7	Global reset	N/A	N/A	N/A
8	Over-temperature reset	N/A	N/A	N/A

- a. Each reset trigger has individual debounce and delay timers. The default value of the debounce and delay timers are 10.256 sec and 2 sec, respectively. The reset triggers share the same stage 3 reset timer.
- b. The default value of the debounce and the delay timers for the PMIC watchdog reset is 31 sec and 32 sec.

Key features:

- Custom **programmable boot sequences** configured with OTP and RAM
- Implemented as a series of address + data transactions which mimic normal software control
- Programmable control of any PMIC resource in any order with any available programmable configuration
- Support for **API-like routines** are implemented with OTP-defined sequences. Initiate via SPMI write to address pointer or via hardware trigger
- Support for a **limited command set** of executable functions



PBS Use Cases

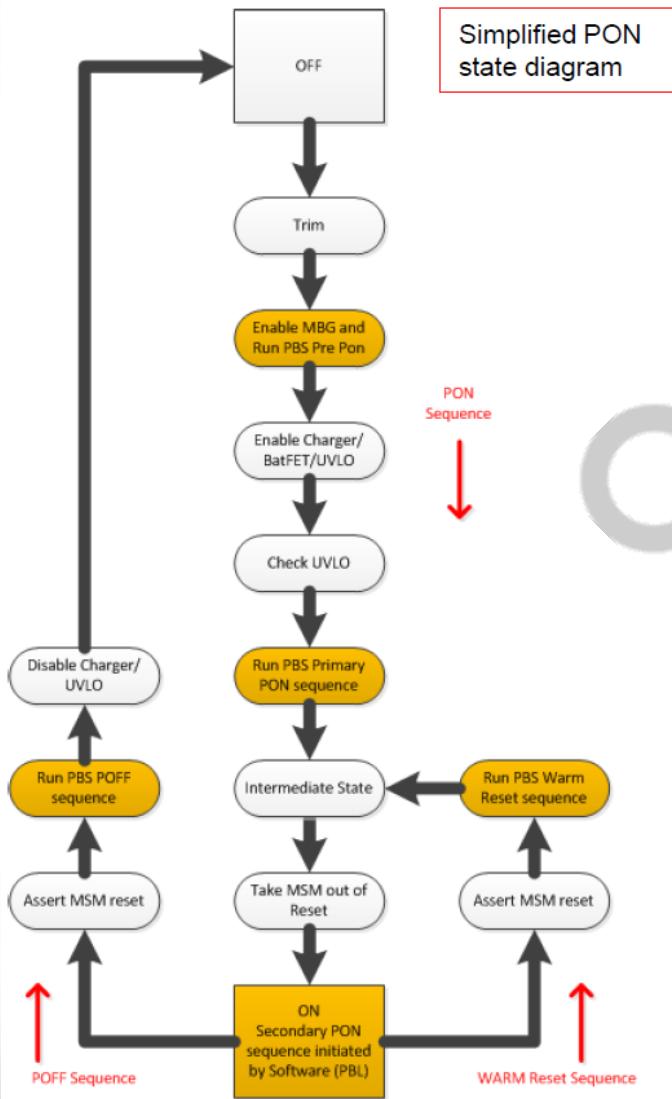
- Power-on sequence (OTP)
 - Make decisions based on the state of option pins or other registers
 - Enable regulators, change GPIO/MPP states
 - Wait for event to occur (register to change state, timer to expire)
 - Change register defaults (e.g., charger limits) prior to enabling module
- Power-off sequence (OTP)
 - Custom power-off sequence (RAM)
 - Blink LED, toggle vibrator motor, etc., as handset shuts down
- Battery UICC alarm (RAM)
 - Disables LDOs based on hardware triggers (battery removal, UICC card removal)
- Sleep/wake batch sequence
 - Several writes can done quickly when entering/exiting sleep to reduce software workload.
 - Can vibrate the VIB motor before initiating shutdown operation

PBS Triggers

- There are 16 different PBS clients in PM8941 and 8 in PM8841
- Each client can be programmed to point to any address with OTP or RAM
- Each client can trigger a sequence via software (e.g., register write) or hardware trigger (see list below)
- PM8941 triggers
 - Trigger 1 – Secondary power-on
 - Trigger 2 - – Primary power-on
 - Trigger 3 – Warm reset
 - Trigger 4 – Shutdown
 - Trigger 5 – XO_OUT_D0_EN
 - Trigger 6 – XO_OUT_D1_EN
 - Trigger 7 – Batter UICC alarm
 - Trigger 8 – Reserved
 - Trigger 9 – Prepower-on
 - Trigger 10 – Sleep
 - Trigger 11 – RTC alarm
 - Trigger 12 – RTC timer
 - Trigger 13 – DTEST1
 - Trigger 14 – DTEST2
 - Trigger 15 – DTEST3
 - Trigger 16 – DTEST4
- PM8841 triggers
 - Trigger 1 – Secondary power-on
 - Trigger 2 - – Primary power-on
 - Trigger 3 – Warm reset
 - Trigger 4 – Shutdown
 - Trigger 5 – DTEST1
 - Trigger 6 – DTEST2
 - Trigger 7 – DTEST3
 - Trigger 8 – DTEST4

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Power On\Off and Warm Reset Sequence



- PBS is run three times during poweron
 1. Configure features (i.e. charging) prior to enabling anything in the system
 2. Enable the minimum infrastructure required to boot MSM and start fast low current boot image (FLCB)
 3. Enable Krait, eMMC, etc., once it is established that the battery is sufficient, or a charger is available.
- PBS runs once during shutdown for regulator sequencing
 - Can also support shutdown indication (e.g., flash LED)
- PBS runs once during warm reset

PBS Programming

■ PBS OTP

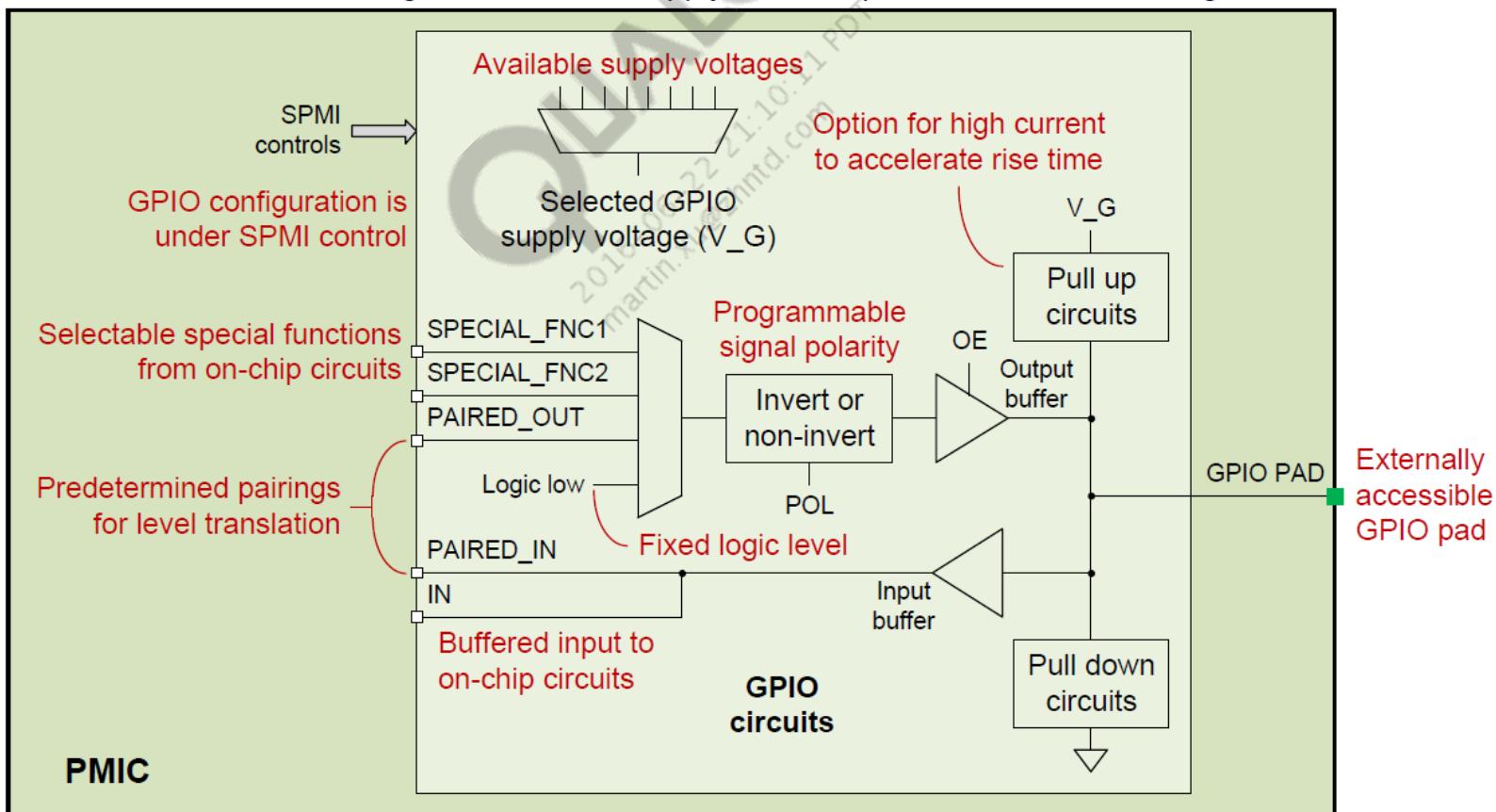
- Programmed during ATE by Qualcomm; customers can't modify it.
- Option pins allow for adjustment of the sequences or to set certain features within the PMIC
- Some area needs to be reserved for future enhancement or workarounds

■ PBS RAM

- For bring up, programmed during SBL
- Can be reprogrammed at anytime by software
- PBS programming must be handled by trusted software
- Some space will be reserved by Qualcomm during development, but these sequences can potentially be moved into OTP prior to CS
- Note: RAM sequences can “prepend” some ROM sequence (e.g., during POFF sequence, customer specific POFF sequence is run and then calls the OTP POFF sequence

GPIO

- 36 GPIOs are available, all on the PM8941 (none on PM8841)
- Some likely GPIO applications, which are discussed elsewhere: clock outputs; external current driver control; external LDO, SMPS, or power gate controls; status bit; XO controller input; and level translator
- GPIO pairs
 - Each GPIO pin is assigned as a member of a pair
 - Each pair is a combination of sequential odd and even GPIO pins (GPIO_1 is paired with GPIO_2, etc)
 - Each member can be assigned a different supply, so each pair can be used as a digital level translator



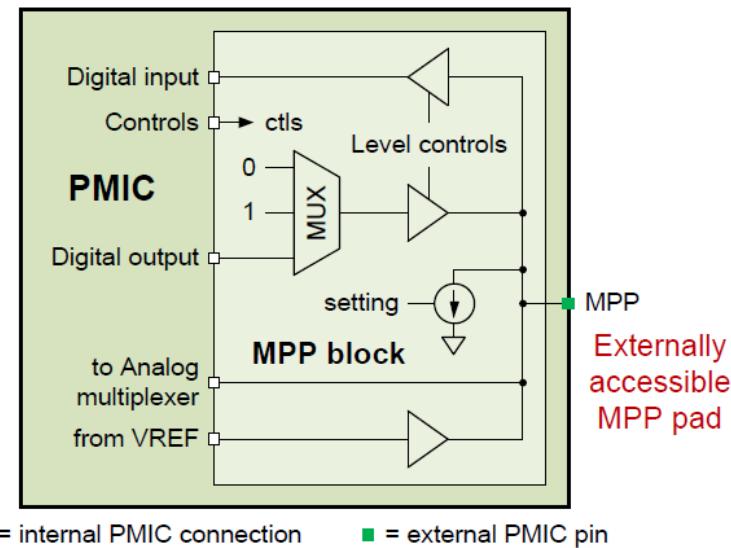
MPP

12 MPPs are available: 8 on the PM8941, 4 on the PM8841. All can be programmed to any of the following configurations.

- Digital input – Digital inputs applied to the pin can be read via software, can trigger an interrupt, or can be routed to another MPP (making this pin the input side of a level translator or current sink controller). The logic level is programmable, providing compliance between I/Os running off different power supplies.
- Digital output – The output signal can be set via software to logic LOW or HIGH, can come from this pin's complementary MPP (making this pin the output side of a level translator), or can be tri-stated for use as a switch. The logic level is programmable, providing compliance between I/Os running off different supplies.
- Bidirectional I/O – The two MPPs making up a complementary pair can be jointly configured as a bidirectional, level-translating pair.
- Analog input – Inputs are routed to the analog multiplexer switch network; if selected, that analog voltage is routed to the HK/XO ADC for digitization.
- Analog output – Buffered version of on-chip voltage reference (VREF).
- Programmable current sink – for driving LEDs.

Each MPP can be used independently or paired with its complement and used as a level translator or bidirectional, level-translating path.

- As a level translator, either side (odd or even) can be configured as the input or output; each side is pulled-up to a selectable power supply, and the internal I/Os are connected.
- As a bidirectional I/O, FET switches provide a path directly between the odd and even pins; each side is pulled-up to a selectable power supply using programmable resistors, and any external drivers must be open-drain.



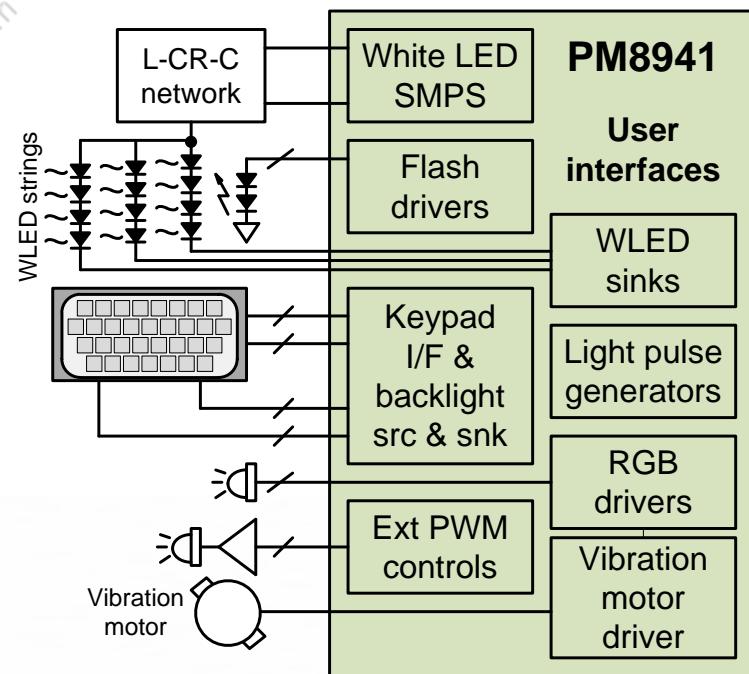


User Interfaces

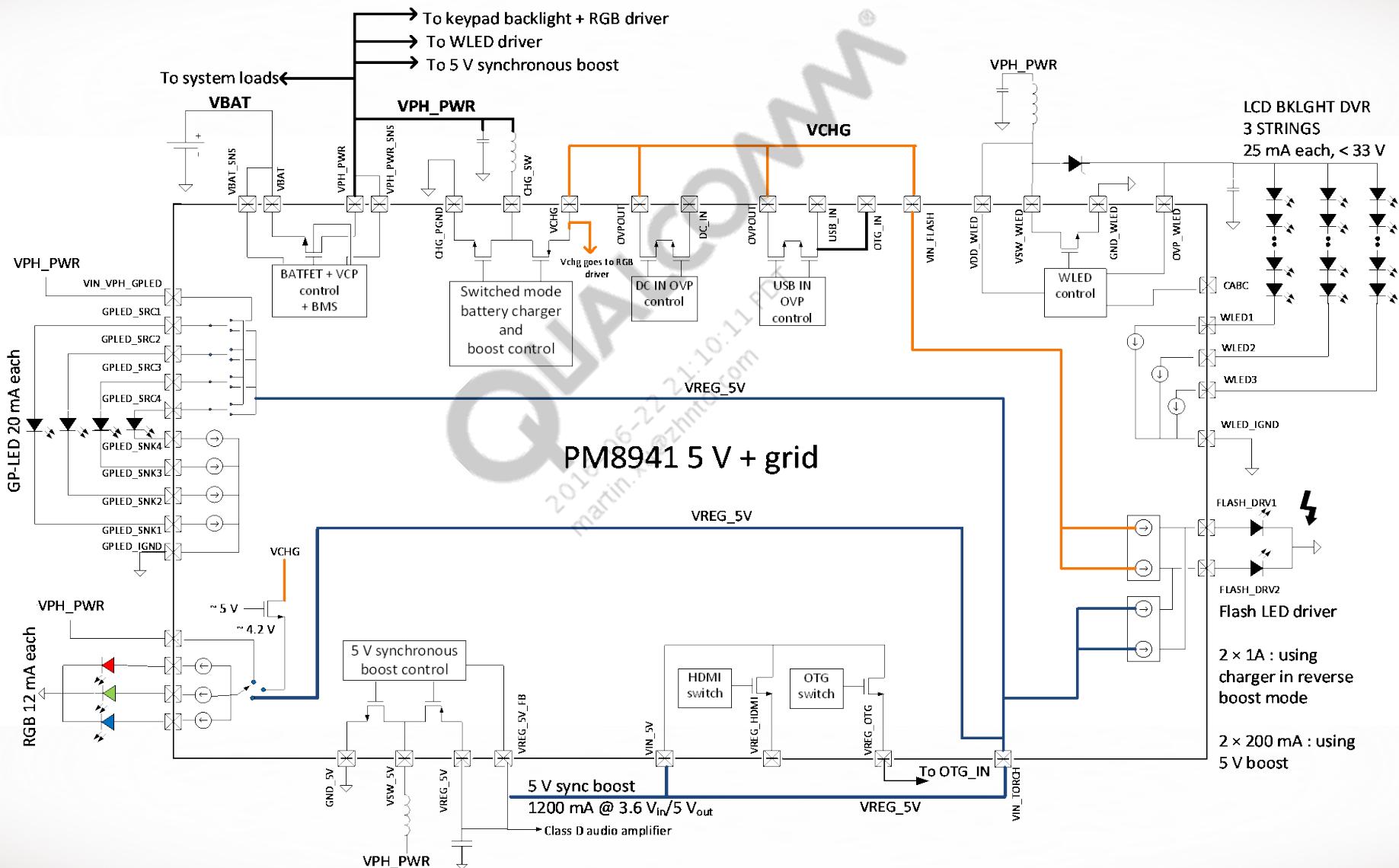
User Interfaces Content

- Lighting architecture
- Light pulse generators
 - Architecture
 - Waveforms
 - Programmable parameters and controls
- RGB LED driver
- 2x 1A Flash driver
 - Feature summary
 - VPH_PWR dip monitoring
 - Mask behavior
- White LED support
 - High-voltage SMPS
 - Schematic and layout guidelines
 - WLED string drivers
- Home row lighting/key illumination
- Keypad interface
- Vibration motor driver

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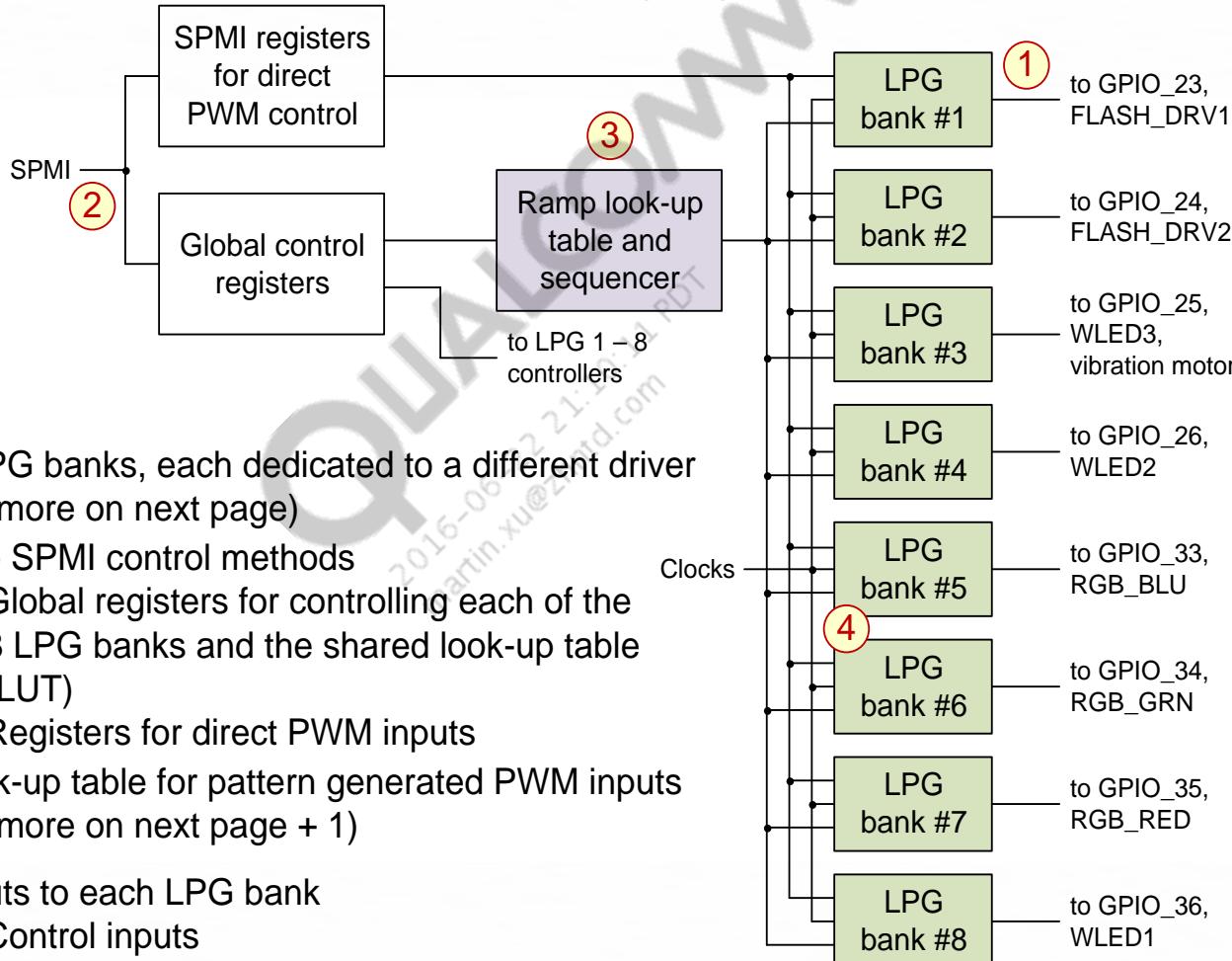


Lighting Architecture



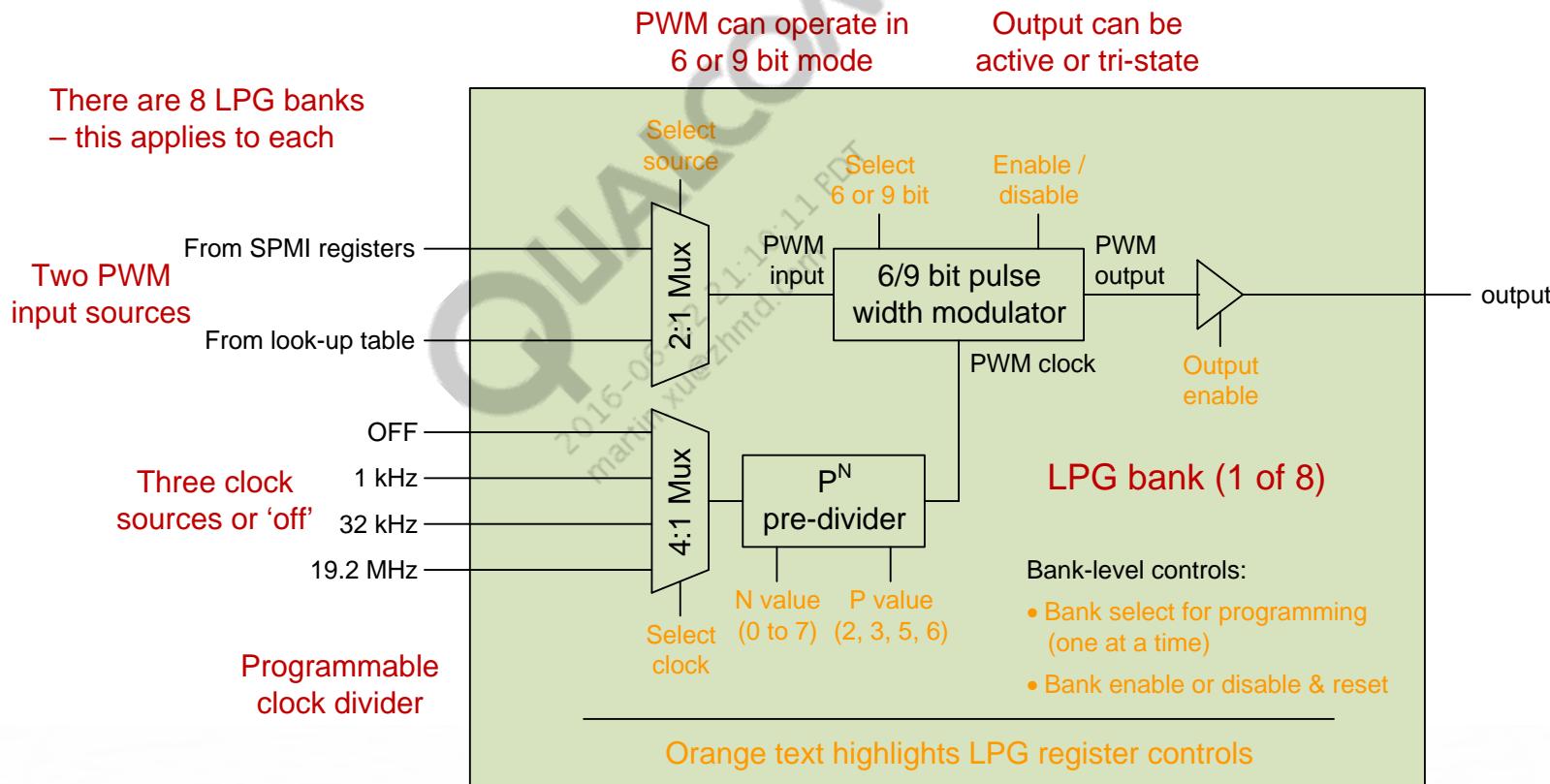
Light Pulse Generators

Two light pulse generator (LPG) circuits – one eight-channel (shown below) and one four-channel that controls the keypad backlighting (GPLED sources and drivers)



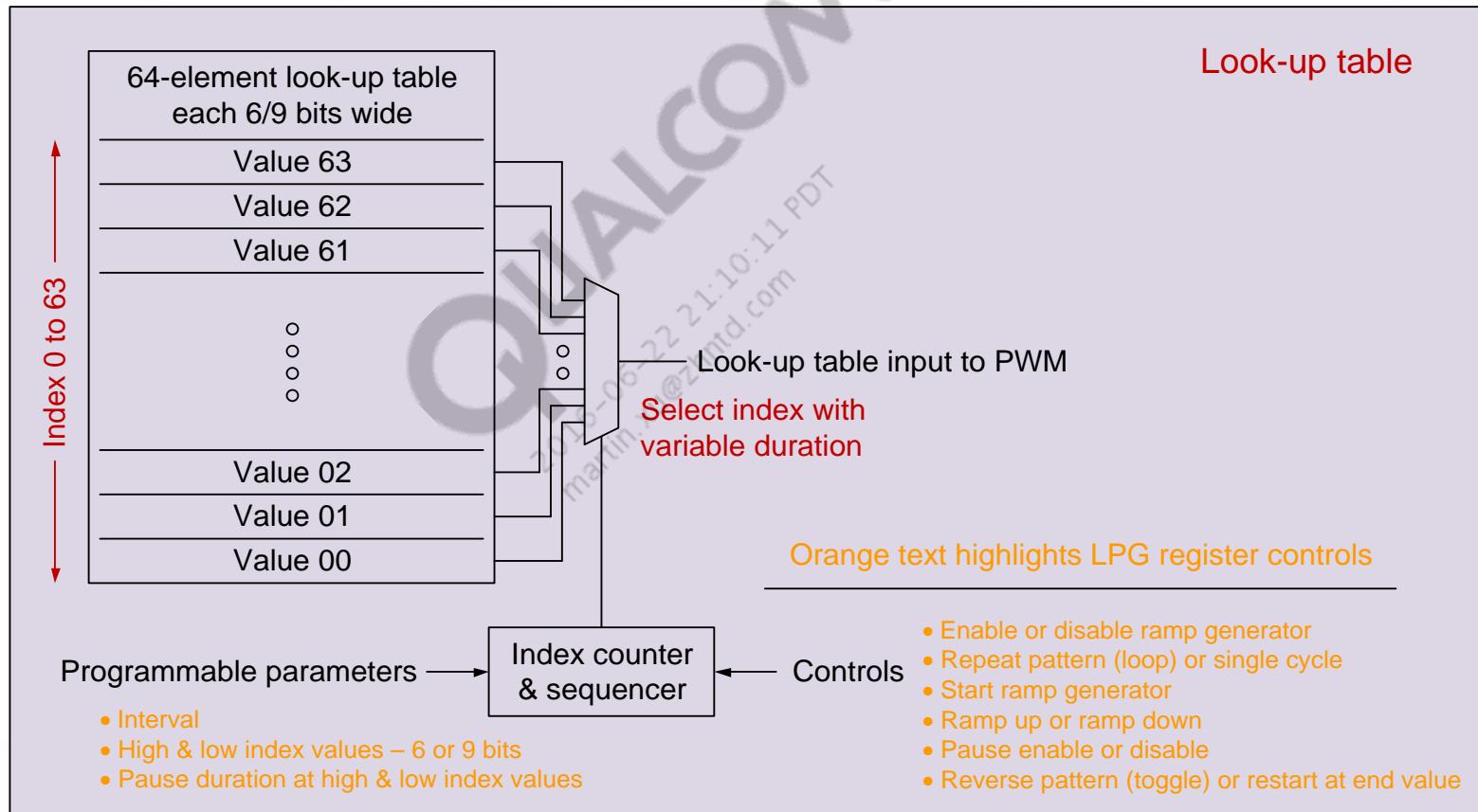
LPG Banks

Item 1 from the previous Light Pulse Generators slide – eight LPG banks, each dedicated to a different driver



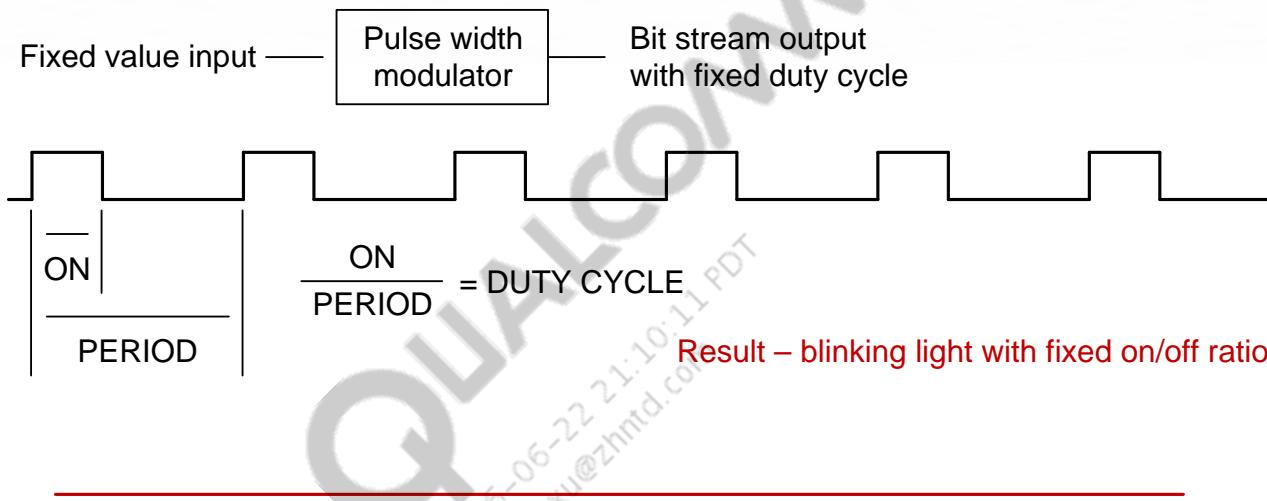
LPG Look-up Table

Item 3 from the Light Pulse Generators slide – look-up table for pattern generated PWM inputs

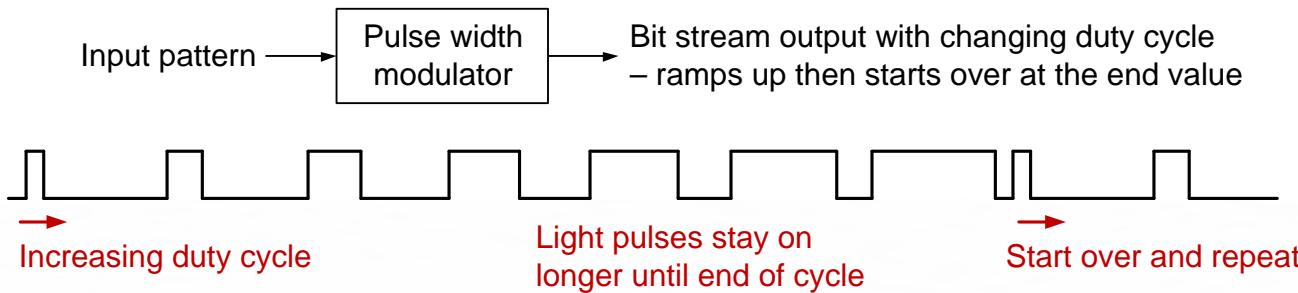


Example PWM Output Waveforms

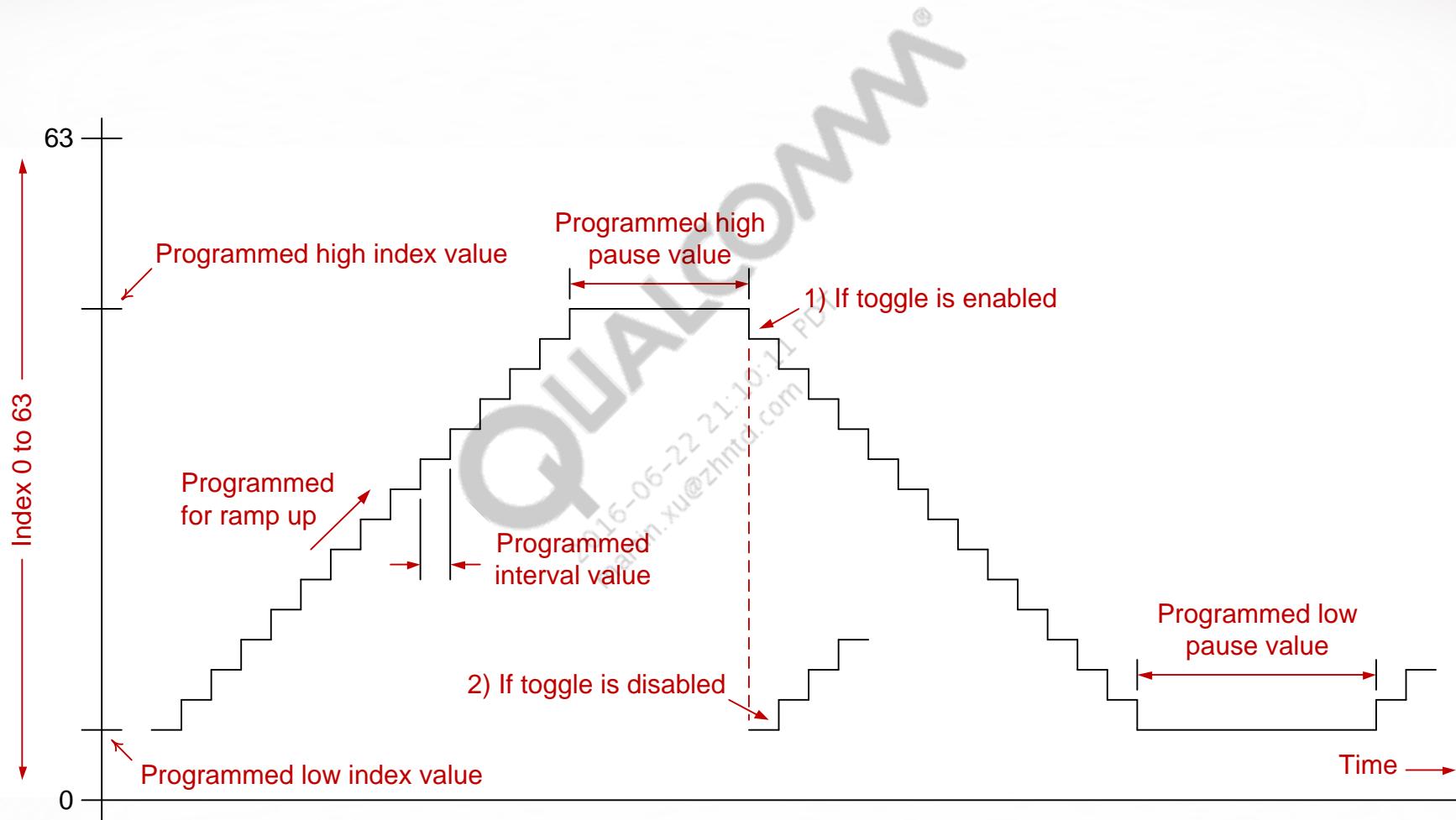
Example 1



Example 2



Example PWM Input Patterns Via Look-up Table

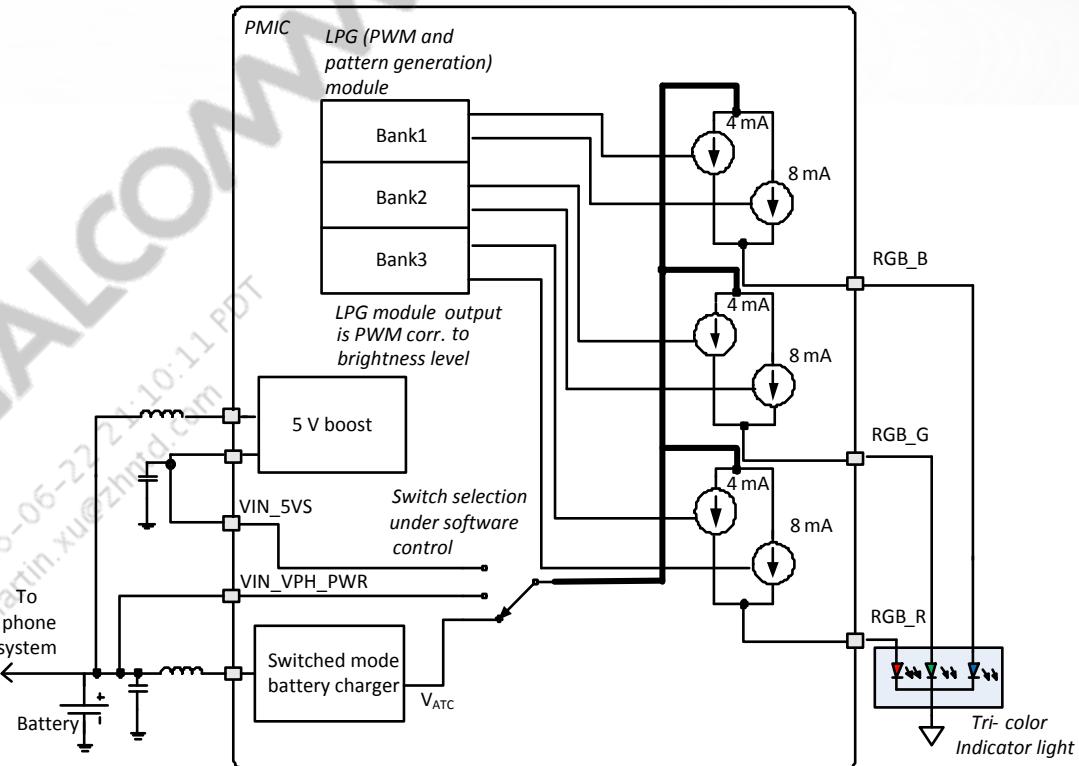


LPG Programmable Parameters and Controls

Parameter or control	Description
Interval	Time spent at each LUT value 1 ms to ~ 1/2 sec; divided down from 1 kHz
Loop	Repeat the pattern or a single cycle
Ramp direction	Up – start low index value, end high value Down – start high value, end low value
Enable ramp generator	Enable or disable
Start LPG ramp	Ramp starts when set; cleared at ramp starts
End value toggle or restart	Toggle – reverse direction at end value Restart – return to start when end reached
High index values	6-bit or 9-bit
Low index values	6-bit or 9-bit
Enable PWM	Enable or disable
PWM input source	Directly from SPMI registers or from LUT
PWM clock source	OFF (no clock), 1 kHz, 32 kHz, or 19.2 MHz
Clock pre-divide value (P)	2, 3, 5, or 6
Clock pre-divide exponent (N)	0 to 7
Pause at low index value duration	1 to 16 (all) then 23 to 7000 (select values) – 1 kHz clock
Pause at high index value duration	1 to 16 (all) then 23 to 7000 (select values) – 1 kHz clock
Enable pause at low index value	Enable or disable
Enable pause at high index value	Enable or disable
PWM output enable	Active or tri-state mode
PWM size	6-bit or 9-bit
LPG bank select	Only one can be programmed at a time.
LPG bank enable	Each can be enabled or disabled individually; when disabled, the LUT is set to its low index value and the interval is set to 0.

RGB LED Driver

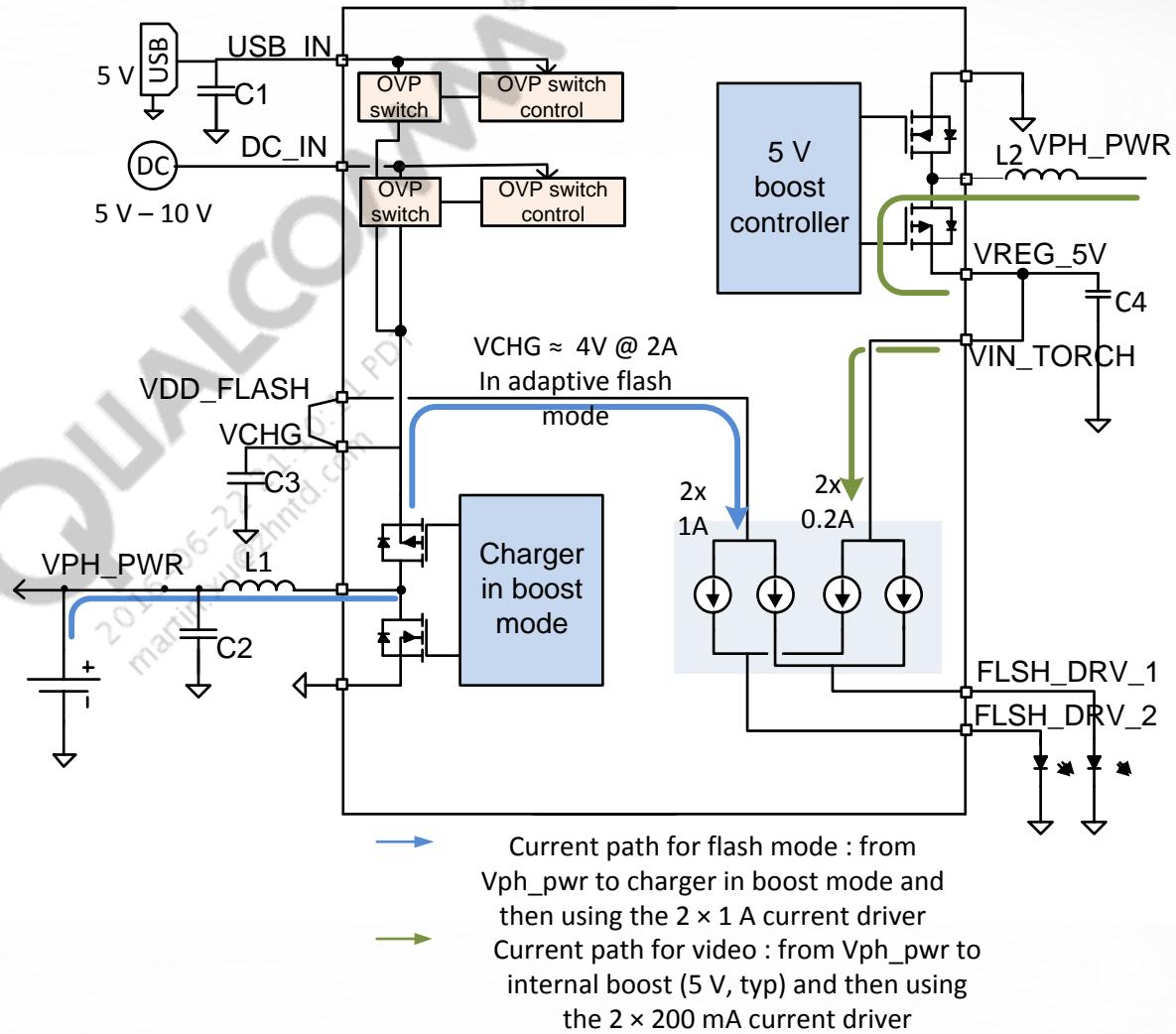
- Independent brightness control of R, G and B channels
- Independently programmable duty cycle and period via 3 LPG channels
- 8-bit resolution, digital dimming
- Software control of power source switch from VPH_PWR to VIN_5VS when operating headroom is not met in mission mode
- Constant current (4 mA/channel) during 'auto-trickle charging'. By default, the R and G LEDs are lit.



2x 1 A Flash Driver

- Flash power source – the charger module runs in reverse as boost in closed loop with the flash module to minimize internal power dissipation
- Concurrency:
 - with external DC_IN, charging is paused while the flash module and charger in reverse boost is used
- Video power sources – Uses an internal 5 V boost regulator
- Concurrency:
 - With class D audio and USB OTG, video current is managed by software

Flash	Video
2 x 1 A	2 x 0.2 A



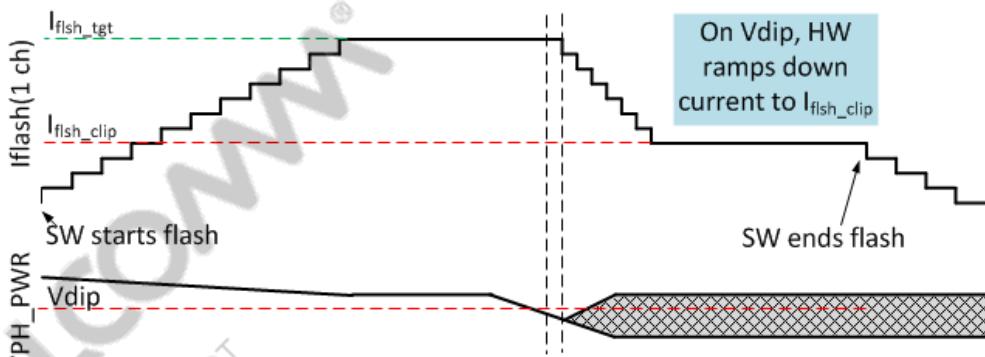
2x 1 A Flash Driver Feature Summary

- 2 LED channels, independent current control, 12.5 mA step size
- 2x 1A high side current driver for flash
 - Flash driver uses internal switched mode battery charger as a boost regulator
 - Boost adaptively regulates supply rail (VCHG) to minimum headroom of 300 mV across the two current sources.
- 2x 200 mA high side current driver for video
 - Torch driver uses internal 5 V boost regulator
- Supports hardware-controlled (GPIO) or software-controlled flash triggering
- Three mask inputs for current clipping during flash event
 - GSM_PA_ON, direct video to flash support, spare
- Low battery voltage monitoring
 - Monitors VSYS at PMIC pin and clips and/or freezes LED current if V_{dip} threshold is crossed
- During flash pulse, the actual current set by software and hardware derating can be read out
- Safety features
 - Flash timeout, video watchdog timer, Open LED/Short LED fault detection, thermal derating during flash, hot LED detection

Flash LED Battery Voltage Dip (V_{dip}) Monitoring and Response

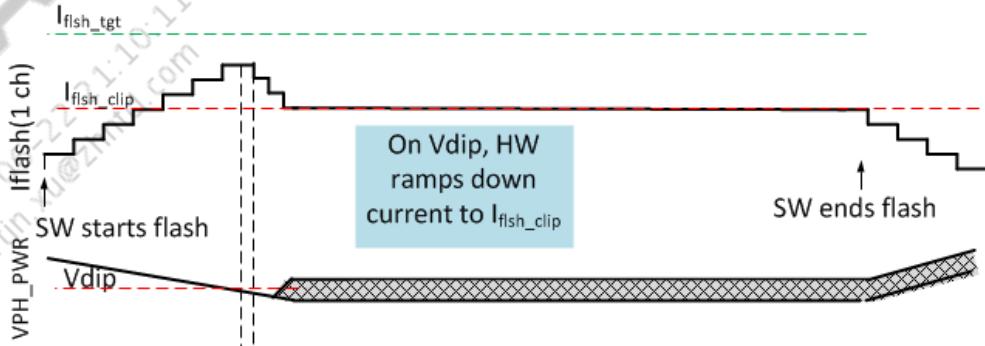
Use case 1

- Flash is at target current, when an additional load causes V_{dip}
- Hardware quickly ramps flash current down to I_{flash_clip} until flash ends



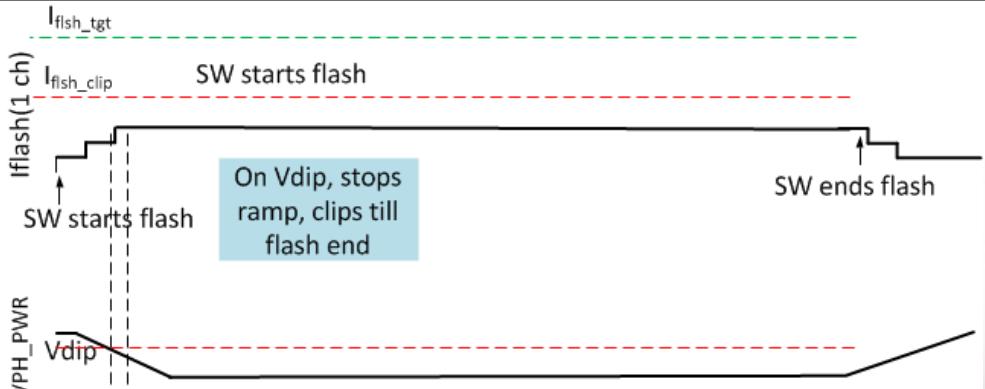
Use case 2

- Flash current is ramping up, when Battery V_{dip} threshold occurs
- Hardware will quickly ramp flash current down to I_{flash_clip} and keep it there until the flash ends



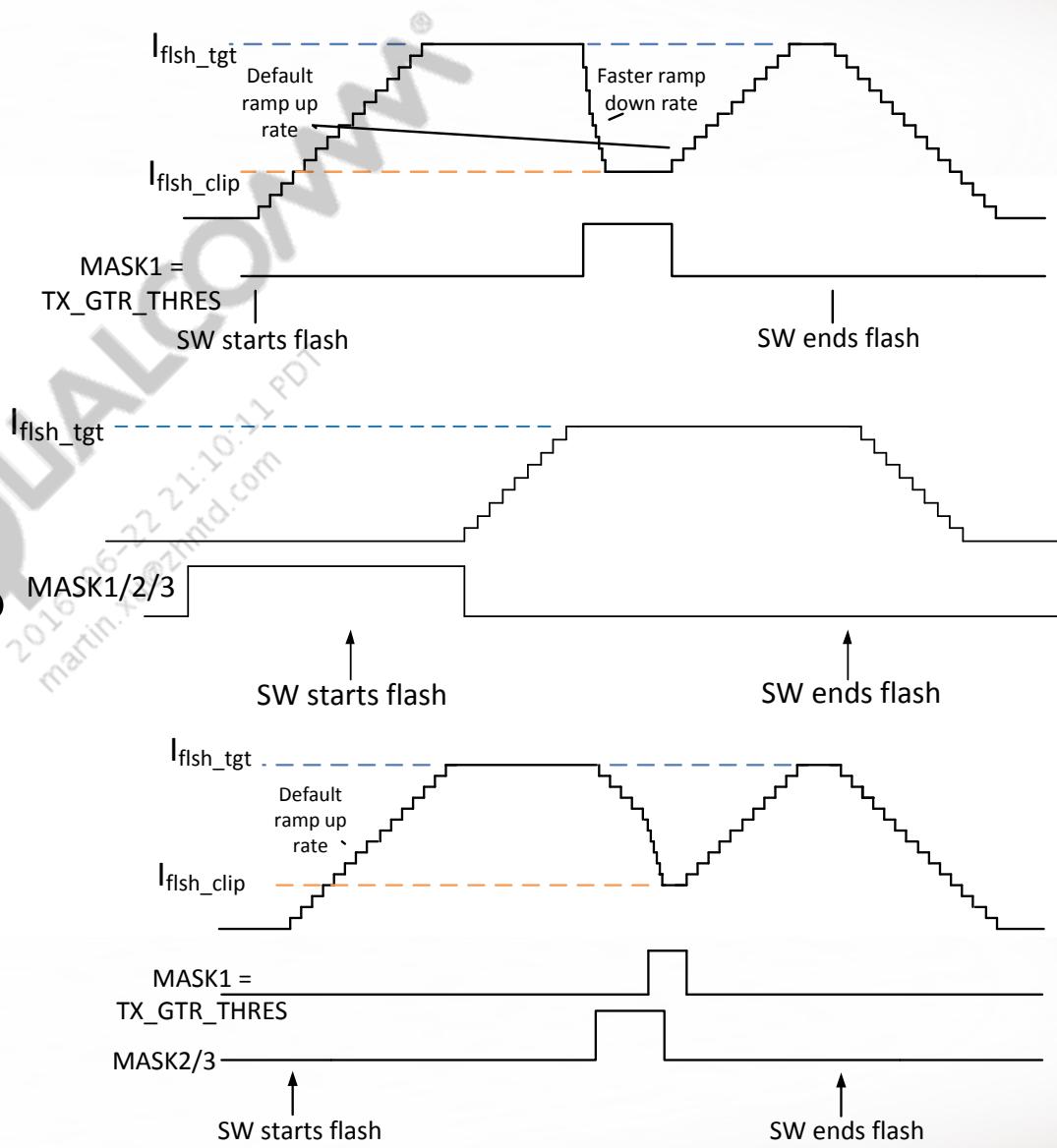
Use case 3

- Weak battery, start of flash current causes V_{dip}
- Hardware stops ramp and clips immediately, never reaching I_{flash_clip}
- Software reads out I_{actual} current



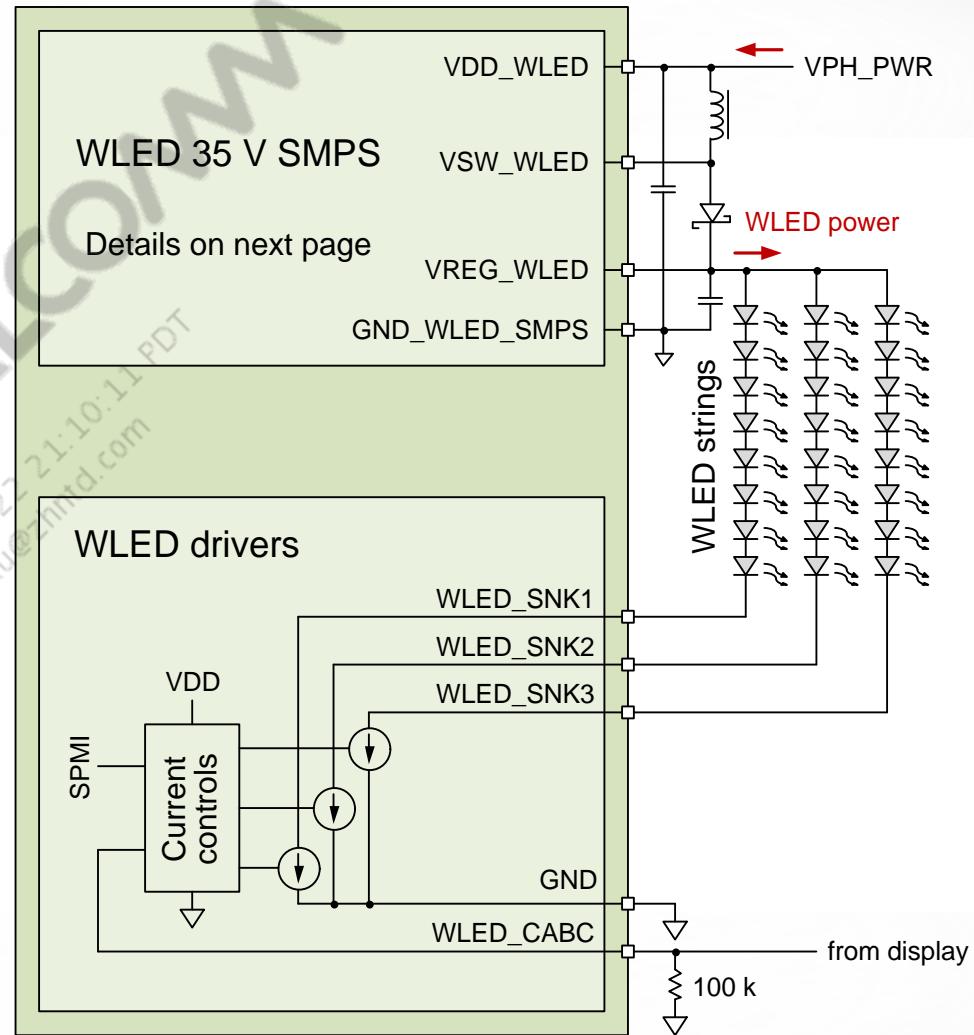
Flash LED Mask Behavior

- Mask1 is used current reduction from I_{flsh_tgt} to I_{flsh_clip} during high power GSM Tx. MSM sends `Tx_GTR_THRES` 130 μ S before PA on ramp
- Mask before software trigger disables I_{flsh_clip} ramp until the mask is removed
- Mask1 takes priority in ramp down rate over Mask2/3
- All masks share setting (programmable) for I_{flsh_clip}



White LED Support

- Integrated boost SMPS generates the high voltage needed for white LEDs
 - SMPS details on next page
- Three ground-referenced current sinks
 - Each support a string of up to eight LEDs
 - 25 mA each
 - Dedicated ground pin
- White LED Content Adaptive Backlight Control (CABC) is supported
 - Connect the WLED_CABC pin to ground through a 10 k resistor if this feature is not used



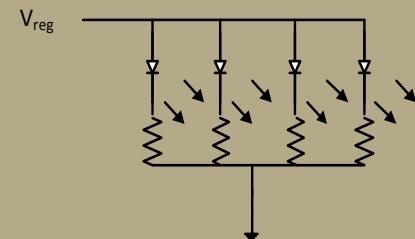
Home Row Lighting/Key Illumination



2 to 4 WLEDs

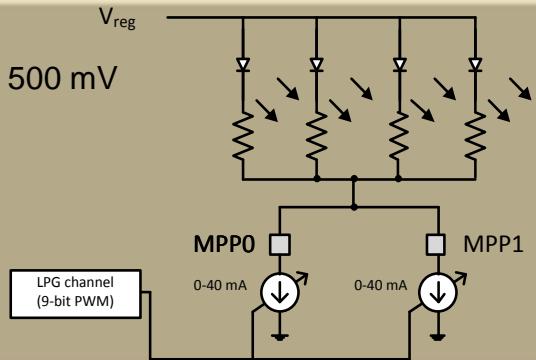
■ Option #1

- 4 ballast resistors for matching and current limiting
- Power source can be V_{sys} or regulated supply rail (see diagram at right)
- Available in most PMICs



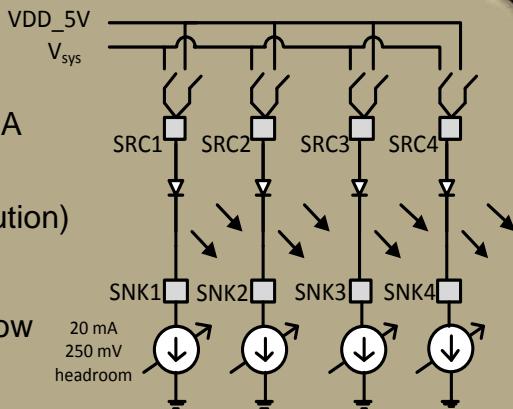
■ Option #2

- Use 1-2 MPPs as current sinks (80 mA total, 500 mV headroom)
- Uses V_{sys} or regulated rail as power source
- LED brightness is controlled via PWM (6-bit/9-bit LPG output)
- Available in most PMICs



■ Option #3

- 4 individually programmable current sinks at 20 mA each
- Each current sink controlled via PWM (8-bit resolution)
- 250 mV headroom
- Software switch to V_{bst} (5 V) when V_{sys} drops below threshold
- 2% matching, 2% accuracy



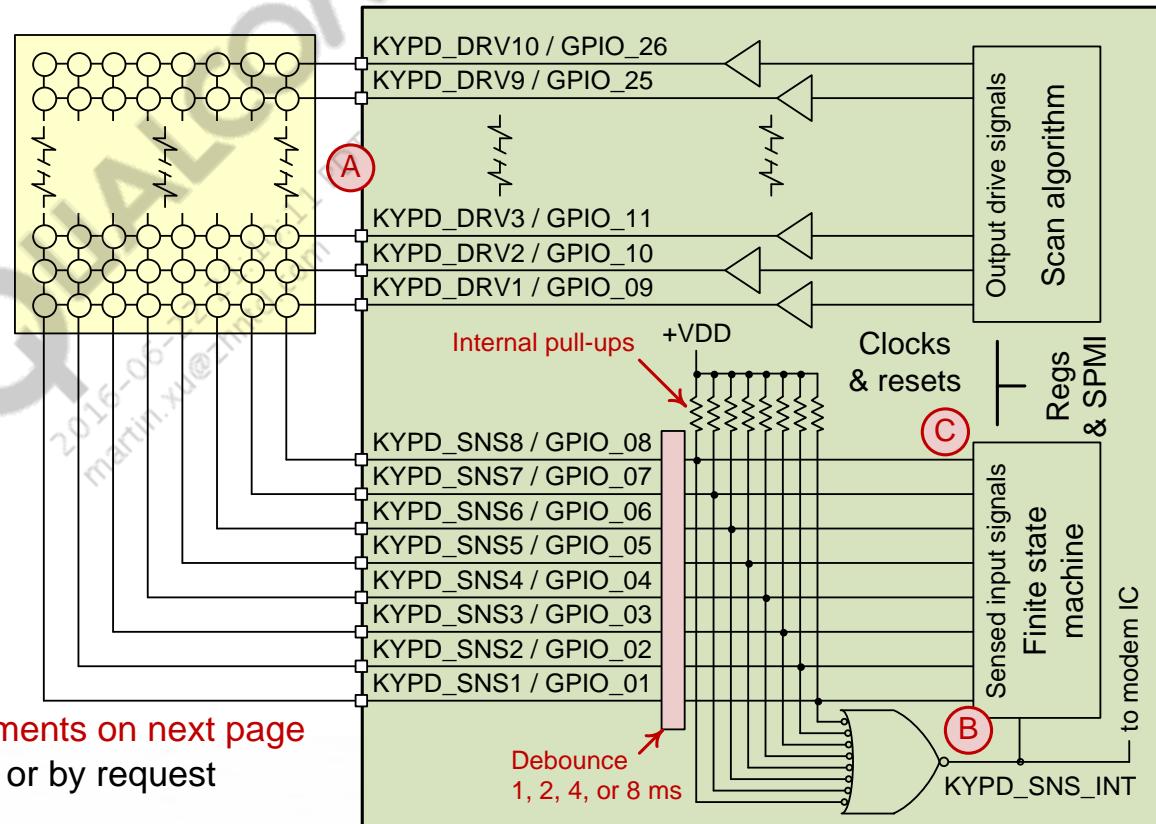
Keypad Interface

A keypad button press is detected by ORing all column signals (KYPD_SNSx) together

- Before a keypad button is pressed, all rows are driven low. (A)
- When a button is pressed, its corresponding column is pulled low (since all rows are low).
- The interrupt is asserted when any keypad button, from any column, is pressed. (B)

When the interrupt signal is received, the FSM requests the next scan.

- During a scan, each row is sequentially driven low, one at a time. (A)
- As each row is driven low, the columns are sensed. (C)
- The pressed button is identified when that button's column reads low while its row is driven low.



Other operational details – plus [enhancements on next page](#)

- A scan can be initiated by a key press or by request from FSM to get next keypad entry.
- After a scan, the FSM compares current and last data; an interrupt is generated if there was a change.
- The modem IC must read the stored key presses via SPMI.
- The delay between scans is programmable (4, 8, 16, 32, 64, or 128 ms).

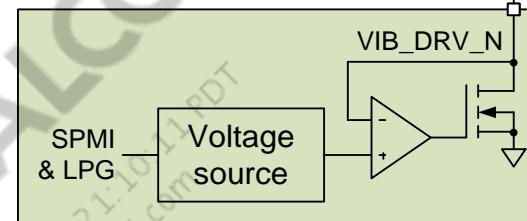
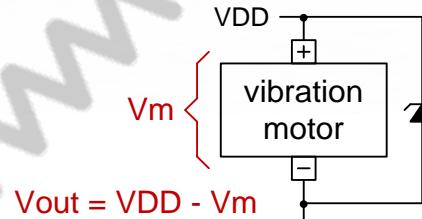
Keypad Scan Enhancements

- Up to 16 keys can be programmed to wakeup the processor, while all others are masked out; masking is bypassed when the full keypad is enabled, ensuring that all keys can generate an interrupt for normal operation.
- The wakeup can be executed in response to any of the following conditions:
 - A software-defined single key is pressed, and no other keys are pressed.
 - A software-defined two-key combination is pressed and no other keys are pressed.
 - A software-defined three-key combination is pressed and not other keys are pressed.
- The software-defined combinations are mutually exclusive – Any key used for the 1-key wakeup cannot be used in any other combination.
- Three separate wakeup combinations can be programmed:
 - One can be used to trigger a warm reset.
 - One of the remaining two can be used to trigger a hard reset.
 - The main purpose is to execute the poweron sequence.
- Warm resets include a programmable debounce time of up to 3.5 sec in 0.5 second steps.
- A hard reset can be debounced up to 15 sec in 1 second steps.
- During debounce, the keypad continues to be scanned and sampled.
- The entire key combination must be pressed during the reset debounce time, in order to generate the intended warm or hard reset.

Vibration Motor Driver

The vibration motor driver supports silent incoming-call alarms with a dedicated output pin (VIB_DRV_N).

- Programmable voltage output referenced to VDD
- When off, the output voltage is VDD
- Motor connected between VDD and VIB_DRV_N
- Voltage across motor is $V_m = VDD - V_{out}$
- V_{out} is the voltage at the PMIC pin.



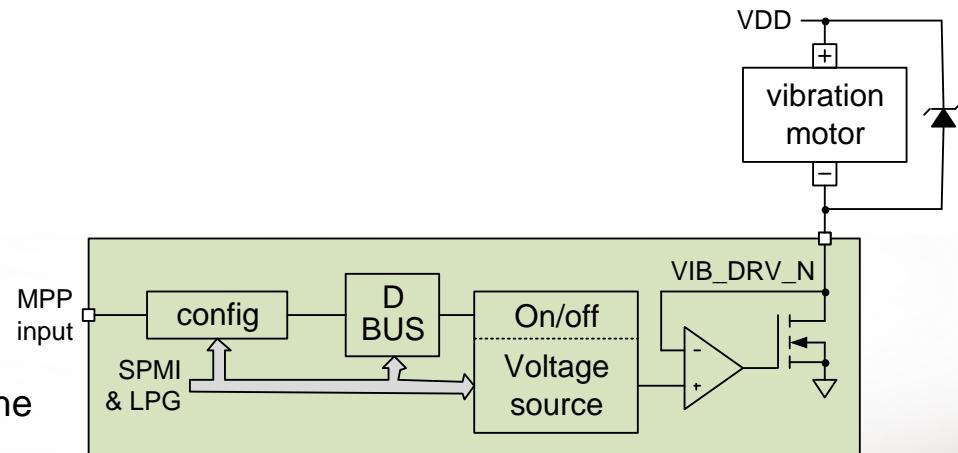
The driver is programmable for motor voltages from 1.2 to 3.1 V in 100-mV increments.

Flyback diode prevents inductive kickback during turn-off, thereby suppressing voltage transients that could damage the IC.

Short circuit current limiting protects the IC when the motor is stalled or shorted.

The PMIC provides the option to control the motor driver through an MPP, thereby providing greater flexibility in defining on and off vibration intervals. The following API software steps are required:

- Configure the MPP as a digital input
- Define that MPP to be 1 of 3 DBUS signals
- Define the polarity of the control signal
- Define the vibration motor driver on/off control to the same DBUS signal



User Interfaces

- For detailed information on user Interfaces, see [Q4]

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2016-06-22 21:10:11 PDT
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References

Ref.	Document
Qualcomm	
Q1	<i>Application Note: Software Glossary for Customers</i>
Q2	<i>Presentation: Fast Low-Current Boot (FLCB) Overview</i>
Q3	<i>Use of Super Capacitor for CAL-RC Application Note</i>
Q4	<i>PM8841 and PM8941 Training Slides</i>



Questions?

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