

# PM8841 and PM8941 Power Management

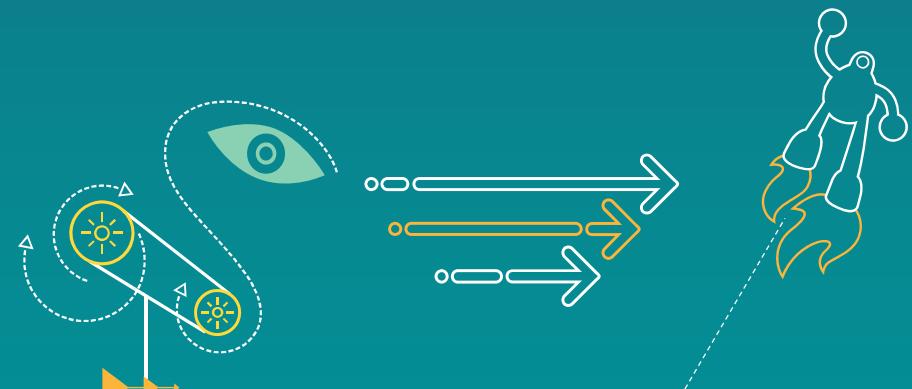


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Qualcomm Technologies, Inc.  
5775 Morehouse Drive  
San Diego, CA 92121  
U.S.A.

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## Revision History (1 of 2)

Revision	Date	Description
A	September 2012	Initial release
B	November 2013	<ul style="list-style-type: none"><li>• Updated SMBB specifications to match device spec</li><li>• Added comments to IR drop compensation</li><li>• Added measured SMBB efficiency plot</li><li>• Added slide on maximum battery charging current</li><li>• Updated voltage regulators summary</li><li>• Updated MSM8974 power grid</li><li>• Added slide on voltage reference</li><li>• Updated slides on HF SMPS; added measured efficiency plots</li><li>• Updated slides on multiphase FT SMPS; added measured efficiency plots</li><li>• Added measured efficiency plot for 5 V synchronous boost</li><li>• Updated slide on SMPS frequencies</li><li>• Updated slide on internal regulator connections</li><li>• Updated slide on input connection options</li><li>• Updated slides on external boost bypass</li><li>• Updated slides on Analog Multiplexer Channel Assignments</li><li>• Updated slide on LPG Banks</li><li>• Added measured efficiency plot of WLED</li><li>• Updated slide on keypad scan enhancements</li><li>• Updated poweron sequence slides</li><li>• Updated slide on reset timers</li><li>• Updated slide on Under-Voltage Lockout</li><li>• Added slides on PM8941 unused pin terminations</li></ul>
C	July 2014	<ul style="list-style-type: none"><li>▪ Changed S7 to S8 and removed a TBD comment on slide 57</li><li>▪ Added a clarification for the battery OCP threshold on slide 77, <i>Need for External Boost Bypass</i></li><li>▪ Modified the GPIO numbers in the figure on slide 97, <i>Other Clock Topics (2 of 2)</i></li><li>▪ Updated the pin termination for VPH_PWR pin on slide 165, <i>PM8941 Unused Pin Terminations (2 of 7)</i></li><li>▪ Added the pin termination for VDD_WLED pin on slide 169, <i>PM8941 Unused Pin Terminations (6 of 7)</i></li></ul>
D	August 2014	<ul style="list-style-type: none"><li>▪ Updated Power On sequence graphic on slide 136</li><li>▪ Added example plots of PM8x41 power-on/off sequence measured on MSM8974 CDP</li><li>▪ Clarified VDD_WLED pin termination on slide 175</li></ul>

## Revision History (2 of 2)

Revision	Date	Description
E	October 2014	<p>Slide 20: Updated input power management information</p> <p>Slide 37: Updated battery FET block diagram to show PFET pull-up. Added information about PFET pull-up</p> <p>Slides to 38 and 39: Added slides about PMIC off mode including ship/shelf mode</p> <p>Slide 44: Added reference to application notes available to customers for battery characterization</p> <p>Slides 45–56: Added slides on other charging topics like dual path charging, HVDCP charging, design example on SMB349 + PM8941 charging, and design example on SMB1357 + PM8941 charging.</p> <p>Slide 65: Added reference to application note on HF/FT SMPS</p> <p>Slide 73: Added reference to application note on LDO</p>
F	November 2014	<p>Slide 48: HVDCP Charging (1 of 4): Corrected document reference</p> <p>Slide 99: Analog Multiplexer Channel Assignments (2 of 2): Updated footnote # 1</p> <p>Slide 185: PM8941 Unused Pin Terminations (1 of 7): Added footnote #1</p> <p>Slide 186: PM8941 Unused Pin Terminations (2 of 7): Added footnote #1, and updated two entries for VBAT</p> <p>Slide 187: PM8941 Unused Pin Terminations (3 of 7): Added footnote #1</p>
G	March 2015	<p>Slide 38: Added Battery FET On Modes slide</p> <p>Slide 52: Changed “parallel” to “shorted together”</p> <p>Slide 55: Changed “dual path” to “parallel path”</p> <p>Slide 165: Changed “normal power sequence” to “user initiated power-on sequence”</p>
H	July 2015	<p>Slide 100: Changed VREG_L4 to VREG_L6</p> <p>Slides 8 to 11: Deleted (contained obsolete information about Docs and Downloads)</p>

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martin.xu@zhntd.com



## Section 1

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# Documentation Overview

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martin.xu@zhntd.com

# Design Guidelines and Training Slides

DCN	Description
<b>Topic specific design guidelines</b>	
80-NA437-5A	<i>MSM8274/MSM8674/MSM8974 Chipset Design Guidelines – Introduction</i>
80-NA437-5B	<i>MSM8x74/MSM8x74AB Design Guidelines – Digital Baseband</i>
80-N5420-5A	<i>WTR1605(L) RF Transceiver With MSM8x74/MDM9x25 Design Guidelines</i>
80-N5420-5B	<i>WTR1605-based SVD for MSM8x74/MDM9x25 Design Guidelines/Training Slides</i>
80-N5420-5C	<i>WTR1605L-based Carrier Aggregation Design Guidelines</i>
80-NA555-5	<i>PM8941 and PM8841 Power Management Design Guidelines (this document)</i>
80-N9326-5	<i>QFE1510 Tunable Front-end Design Guidelines/Training Slides</i>
80-WL300-5	<i>WLAN/BT/FM Design Guidance and Training Using WCN3660, WCN3660A, or WCN3680 Design Guidelines</i>
80-WL005-5	<i>WCN3680 + Custom FEM Layout Guidelines</i>
80-NA556-5	<i>WCD9320 Audio Codec IC Design Guidelines/Training Slides</i>
80-NA437-5C	<i>MSM8274/MSM8674/MSM8974 Chipset Design Guidelines – System Topics</i>
<b>Chipset training slides with embedded audio</b>	
AU80-NA437-21	<i>MSM8274/MSM8674/MSM8974 Chipset Overview Training Slides</i>
AU80-N5420-21	<i>WTR1605/WTR1605L Wafer-level RF Transceiver IC Training Slides</i>
AU80-TBD	<i>WTR1605-based Simultaneous Voice and Data (SVD) Training Slides</i>
AU80-N5420-25	<i>WTR1605L-based Carrier Aggregation Training Slides</i>
AU80-TBD-21	<i>QFE1100, QFE1310, and QFE1510 Training slides</i>
AU80-TBD-21	<i>WCN3680 Wireless Connectivity Training Slides</i>
AU80-TBD-21	<i>WCD9320 Audio Codec Training Slides</i>



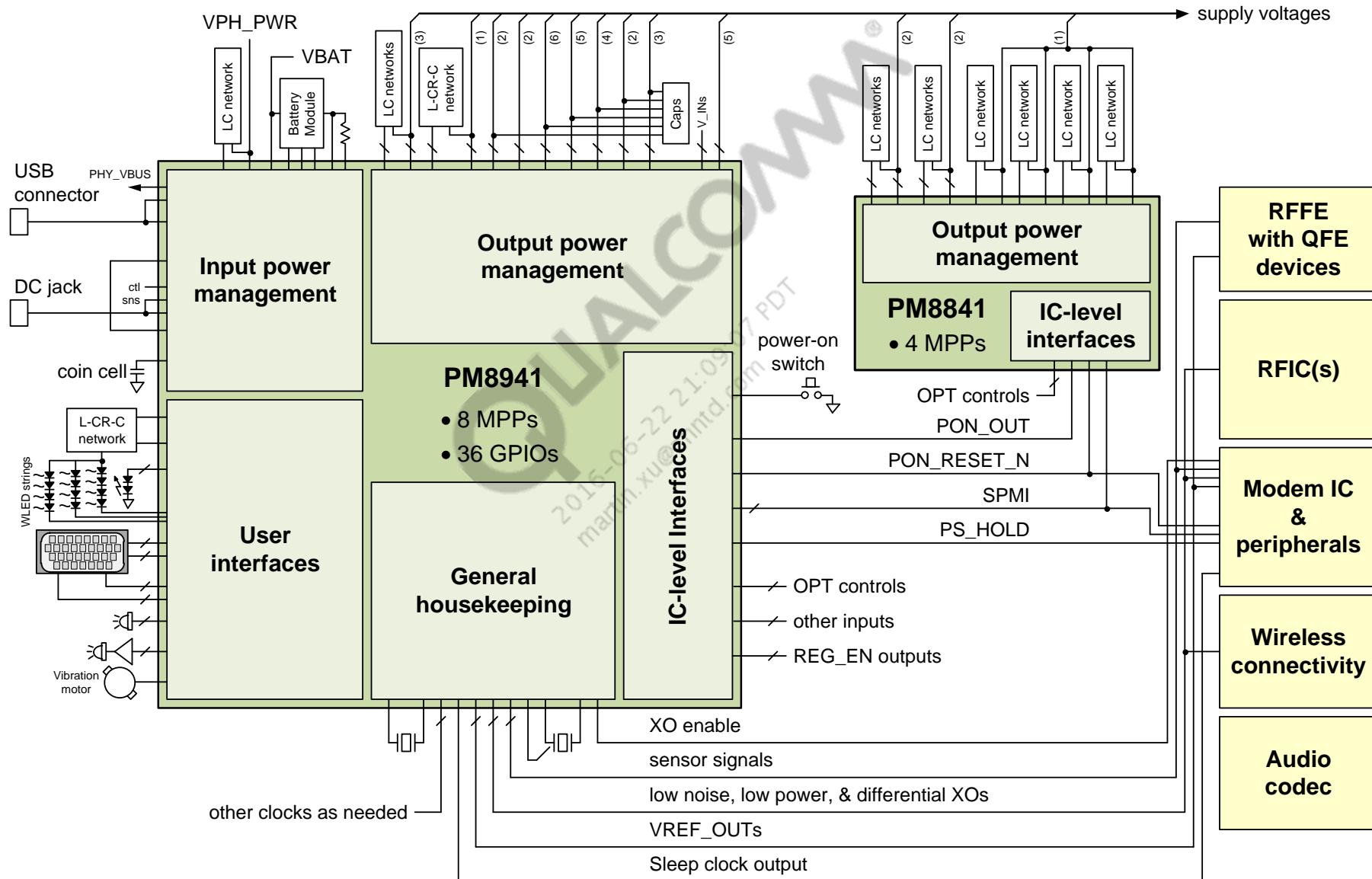
## Section 2

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# Power Management System and IC Overview

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# Power Management System Block Diagram



# PM8x41 Features (1 of 4)

	Features	PM8921	PM8038	PM8x21	PM8x41
General metrics	Process	0.18 $\mu$	0.18 $\mu$	0.18 $\mu$	0.18 $\mu$
	Package size (mm)	7.8 × 7.8 61 mm <sup>2</sup>	5.96 × 5.96 35.5 mm <sup>2</sup>	7.8 × 7.8 2.8 × 2.4 67.7 mm <sup>2</sup>	6.15 × 5.82 4.45 × 3.58 51.72 mm <sup>2</sup>
	Package type	NSP	WLP	NSP + WLP	WLP × 2
	Package I/O (non-common ground)	251	193	8921: 251 8821: 42	8941: 229 8841: 98
	PCB stackup	2N2	2N2	2N2	2N2
User interface and drivers	Keypad scanner	8 × 18	–	8 × 18	8 × 10
	MPP + AMUX channels	12	6	12 + 4	12 (8 + 4) + 8
	GPIO	44	12	44	36
	300 mA LED drivers	1	–	1	–
	40 mA LED drivers	3	3	3	–
	Matched RGB drivers	–	–	–	Yes
	LPG (light pattern generator)	8	5	8	8
	Vibrator driver	1	1	1	1
	Series white LED driver	–	Two strings Up to 32.5 V	–	Three strings Up to 32.5 V
	Camera flash driver	No	No	No	Yes: 2A

## PM8x41 Features (2 of 4)

	Features	PM8921	PM8038	PM8x21	PM8x41
Input power management	Regulation type	Switch mode 2 A	Switch mode 2 A	Switch mode 2 A	Switch mode 3 A
	OVP	30 V	30 V	30 V	30 V/15 V
	Dual path	Yes	Yes	Yes	Yes
	Number of integrated OVP FETs	1	1	1	2
	BATFET	Ext	Ext	Ext	Int
	BMS (fuel gauge)	Yes	Yes	Yes	Yes
Output power management	BMS current sense	Ext	Ext	Ext	Int
	Buck regulators	2 × 2 A FTS 6 × 1.5 A HF	2 × 2 A FTS 4 × 1.5 A HF	(2 + 2) × 2 A FTS 6 × 1.5 A HF	6 × 3 A FTS Gen2 2 × 1 A HF 3 × 2 A HF
	# LDOs	5 × 1.2 A NLDO 2 × 600 mA PLDO 4 × 300 mA PLDO 9 × 150 mA PLDO 4 × 150 mA NLDO 2 × 50 mA PLDO 2 × 10 mA LNLDLDO	6 × 1.2 A NLDO 2 × 600 mA PLDO 5 × 300 mA PLDO 1 × 300 mA NLDO 3 × 150 mA PLDO 2 × 150 mA NLDO 5 × 50 mA PLDO 2 × 10 mA LNLDLDO	5 × 1.2 A NLDO 2 × 600 mA PLDO 4 × 300 mA PLDO 9 × 150 mA PLDO 4 × 150 mA NLDO 2 × 50 mA PLDO 2 × 10 mA LNLDLDO	3 × 1.2 A NLDO 2 × 300 mA NLDO 4 × 600 mA PLDO 4 × 300 mA PLDO 7 × 150 mA PLDO 2 × 50 mA PLDO 2 × 10 mA LNLDLDO
	Power switches	6 × 100 mA LVS 1 × 300 mA LVS 1 × OTG MVS 1 × HDMI MVS	2 × 100 mA LVS	6 × 100 mA LVS 1 × 300 mA LVS 1 × OTG MVS 1 × HDMI MVS	3 × 300 mA LVS 1 × OTG MVS 1 × HDMI MVS
	5 V boost regulator	No	No	No	1.3 A Sync
	Ext. buck/boost support	Yes	Yes	Yes	Yes
	Negative charge pump	1 × 200 mA NCP	–	1 × 200 mA NCP	–

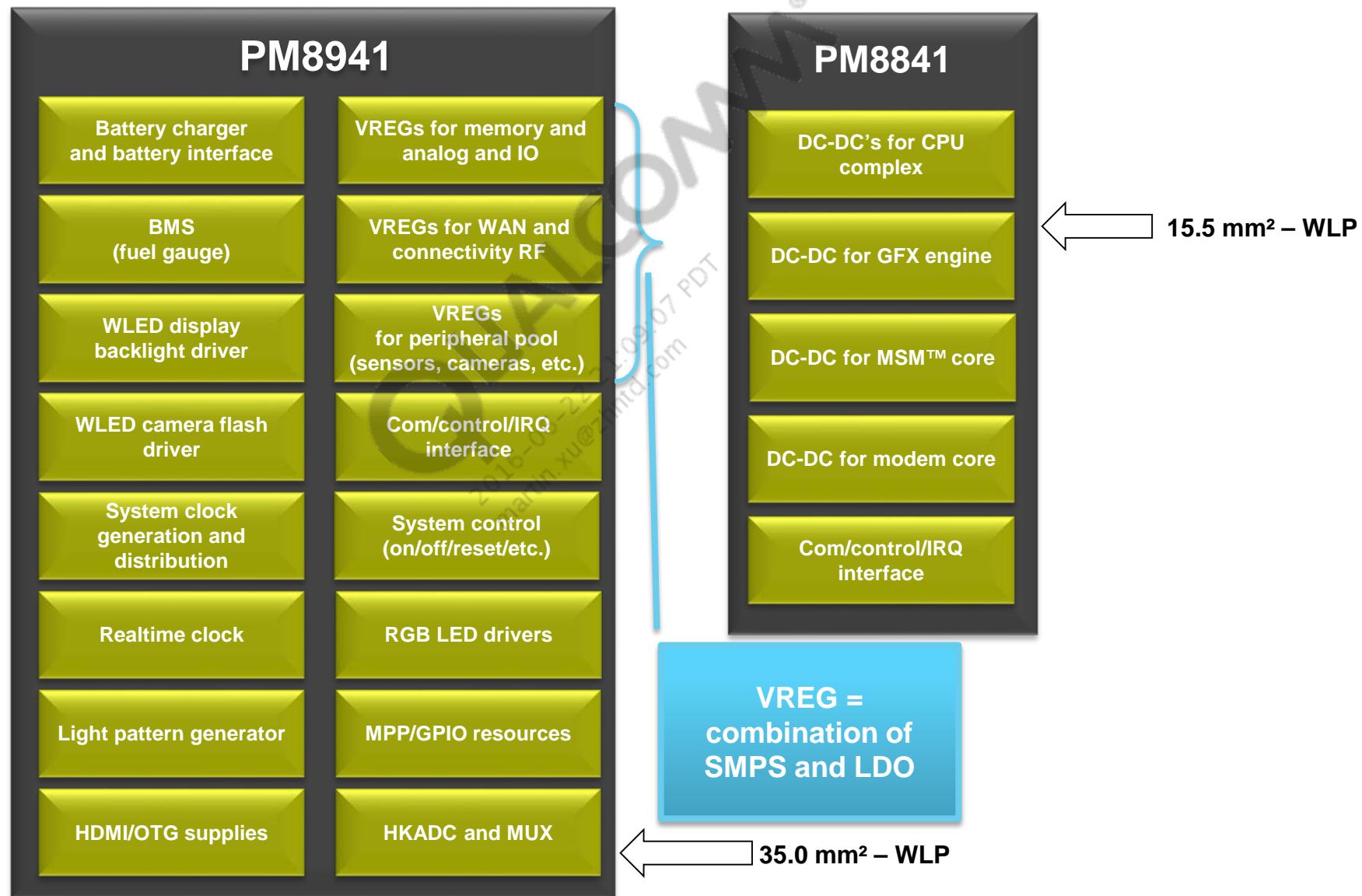
## PM8x41 Features (3 of 4)

	Features	PM8921	PM8038	PM8x21	PM8x41
Housekeeping	System clock generation	19.2 XO	19.2 XO	19.2 XO	19.2 XO
	System clock buffers	5	5	5	3 RF 2 BB 1 differential
	Sleep clock generation	XO/586	XO/586	XO/586	XO/586
	32 kHz buffers	3	3	3	3
	RTC (XO/586 when device is on, cal RC when device is off)	Yes	Yes	Yes	Yes
	MP3 slow clock buffer	Yes	Yes	Yes	Yes
	HKADC/XOADC	Yes	Yes	Yes	Yes
	UICC level translator	2	–	2	–

## PM8x41 Features (4 of 4)

	Features	PM8921	PM8038	PM8x21	PM8x41
IC interface and value added	IRQ manager	Secure	Secure	Secure	SPMI
	Serial I/F	SSBI 2.0	SSBI 2.0	SSBI 2.0	SPMI
	Plug and play compliant	–	–	–	Yes
	PBS (programmable boot sequencer)	–	–	–	Yes
	Cable detector	2	2	2	1
Audio	Loudspeaker driver	No	Mono 1W D+	No	No
	Speaker bypass	No	Yes	No	No
	OTHC (microphone bias)	3	–	3	–

# Functional Partitioning





## Section 3

# Input Power Management

### 3.1 Other Topics

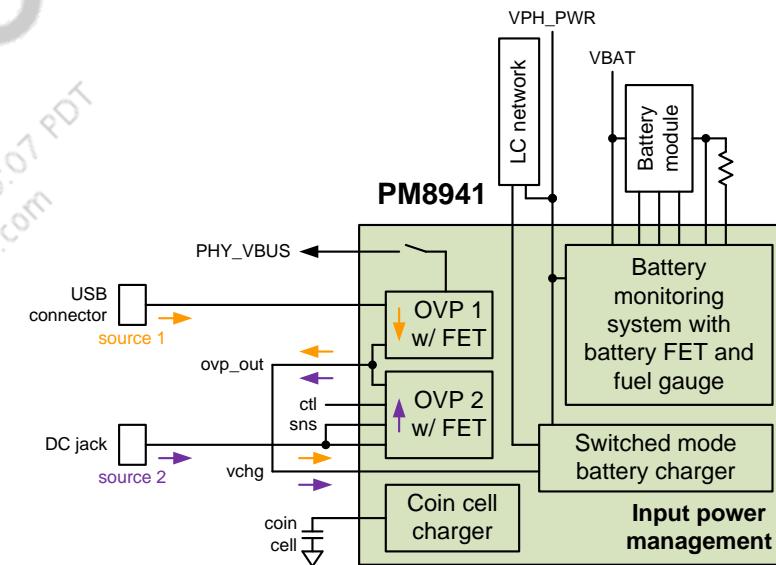
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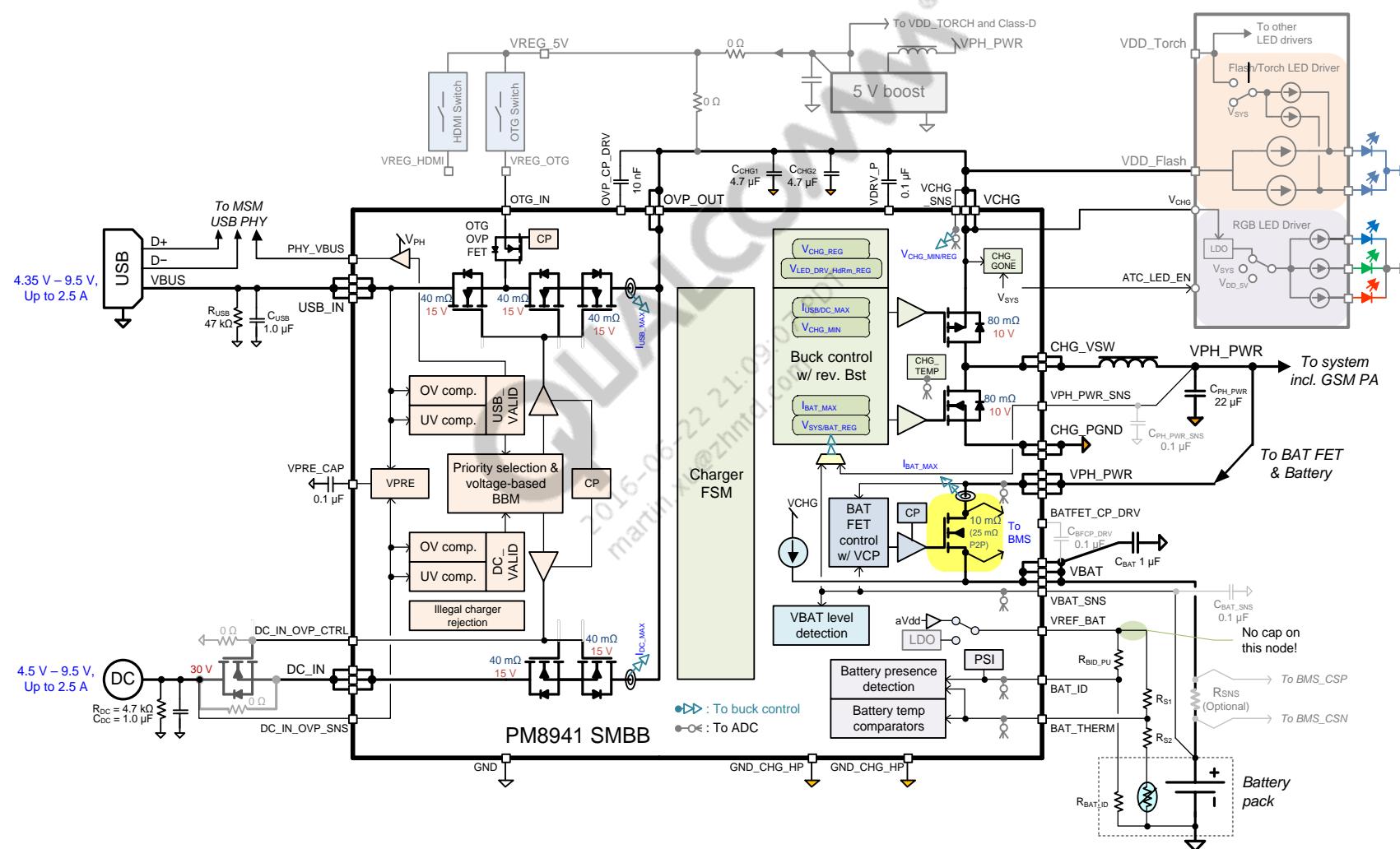
# Input Power Management Content

- Switch-mode battery charger with reverse boost (SMBB) architecture and summary
- Dual-charger support and overvoltage protection (OVP)
- Fast switching paths
- High-current IR drop compensation
- Charging flow diagram
- Autonomous charging
- Charger control loops
- Safety features
- Buck efficiency
- Reverse boost mode and efficiency
- SMBB schematic and layout
- Integrated battery FET
- Battery temperature monitoring (BTM)
- Battery presence detection (BPD)
- Voltage collapse protection (VCP)
- Battery monitoring system (BMS)
- Other topics
  - ▣ Dual path charging
  - ▣ HVDCP charging
  - ▣ Design example: SMB349 + PM8941 charging
  - ▣ Design example: SMB1357 + PM8941 charging

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# SMBB Architecture and Feature Summary (1 of 2)



## SMBB Architecture and Feature Summary (2 of 2)

Dual charging paths with fast automatic charging path switching

- Fully integrated USB charging path with +30 V OVP FET; 4.35 V–9.5 V input; USB 2.0 and USB battery charging specification 1.2-compliant
- DC charging path with integrated +15 V OVP FET for input current sensing and reverse current blocking; 4.5 V–9.5 V input; allows an optional external OVP FET to support +30 V OVP

Fully integrated, high efficiency switch-mode charger for single-cell lithium-ion batteries

- Up to 3.0 A current to system plus battery
- 3.2 MHz switching frequency allows for a small-size inductor (e.g., 3225)
- Efficiency: 88% at 1.0 A  $I_{CHG\_OUT}$ ; 79% at 2.5 A  $I_{CHG\_OUT}$
- High-current charging IR drop compensation

Reverse-boosting mode to provide a 2 A max to VCHG

- Supports USB OTG, HDMI switch, and LED drivers (torch, home row lighting, RGB)
- Also used for flash LED driver in an adaptive mode to minimize the thermal generation

Integrated BAT FET

- Battery current sensing across the BAT FET; eliminating the external  $R_{SENSE}$
- HW battery presence detection and temperature monitoring with JEITA-specification compliance

Charger FSM supports autonomous charging (trickle → CC/CV → termination → recharge)

- Software-initiated, hardware-managed charging; allows for hardware-controlled auto-trickle charge (ATC), if necessary
- Hardware timers for battery charging safety; one-time write registers, and battery overvoltage detection

USB support

- Integrated USB OTG switch supporting simultaneous DC charging and USB OTG
- USB  $R_{ID}$  detection with ACA support

# Dual Charging Support and Over Voltage Protection (OVP)

## USB charging path

- Fully integrated 30 V OVP FET and control
- Pass up to 9.5 V for high-voltage charger
- Compliant to USB specification 2.0 and USB battery charging specification 1.2

## DC charging path

- Integrated 15 V OVP FET for input current sensing and reverse current blocking for wireless charging application
- 30 V OVP with an optional external OVP FET
- If the external OVP is not used, then:
  - Float DC\_IN\_OVP\_CTRL
  - Short DC\_IN\_OVP\_SNS to DC\_IN

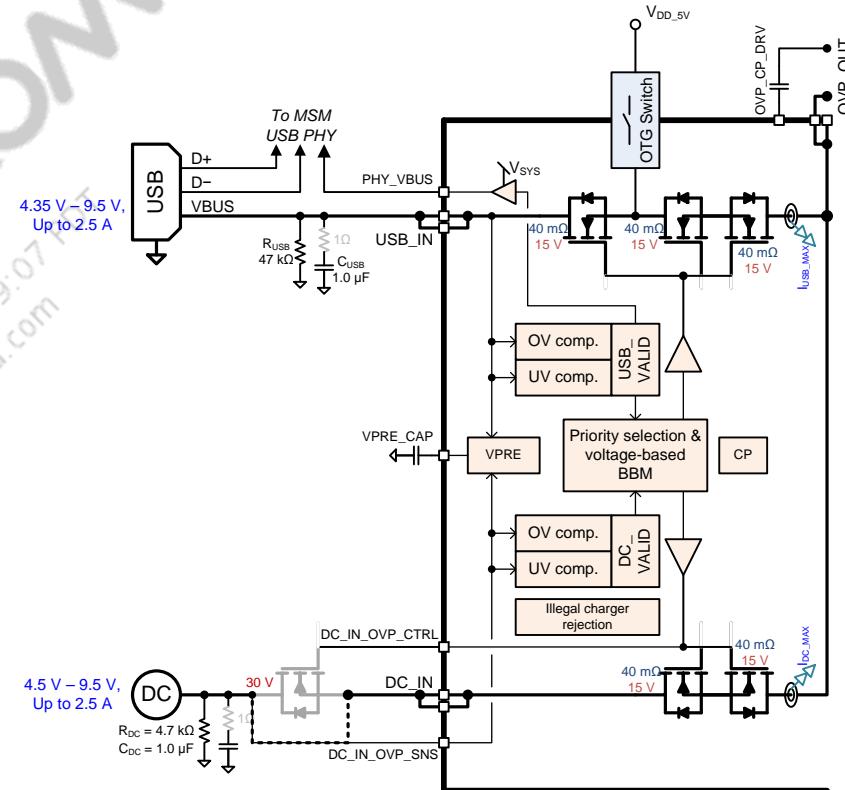
## External charger detection

- If external charger is used instead of SMBB, connect DC\_IN\_OVP\_CTRL to GND

## Automatic charging path selection with software-programmable priority

## Fast-charging path switching

- To minimize the risk of a system brownout when switching the charging path with a weak battery



## Fast Switching Between Charging Paths

SMBC hardware automatically switches between charging sources under the following conditions:

- A higher-priority source becomes available
- Software changes the priority when both sources are available
- The high-priority source is removed

This fast-switching feature uses a voltage-based break-before-make scheme:

- Addresses possible brownout (temporary system crash) when switching between sources during charging with a weak or disconnected battery

Charging source switching time

(whether from a low-voltage source to a high-voltage source or vice versa)

- Programmable from 60 to 120  $\mu$ s in 20  $\mu$ s steps
- With an 80  $\mu$ s default, 50  $\mu$ F capacitance on VPH\_PWR is needed to prevent 4.2 V from dropping below 3.2 V (default weak battery threshold), during a charging source switchover, with a 1 A system load.

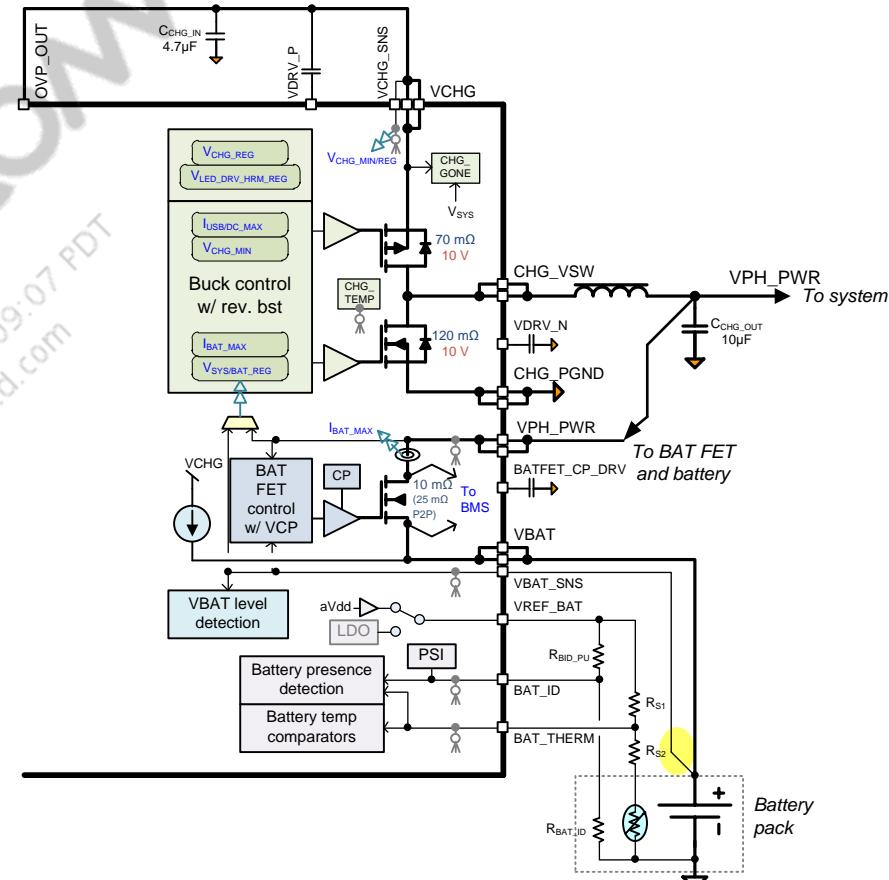
# High-current Charging IR Drop Compensation

## Issue description

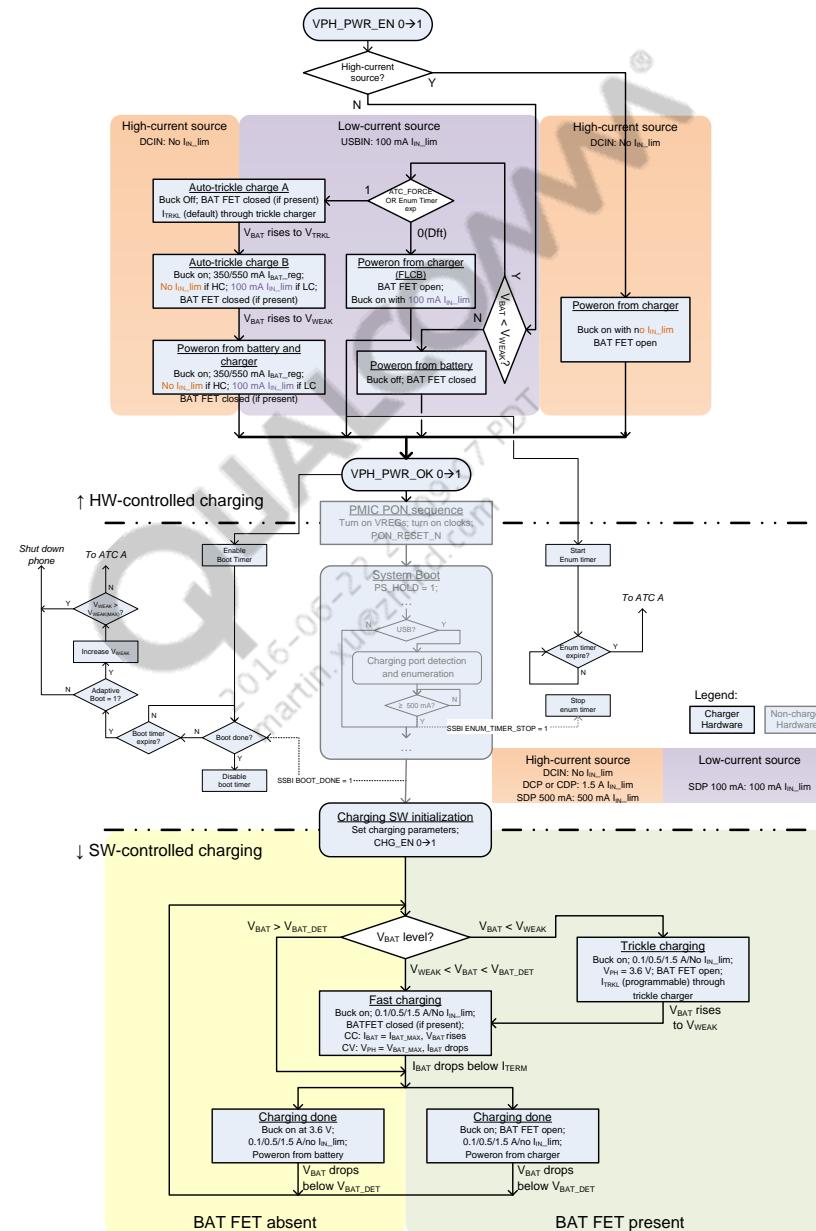
- Extra resistance from the charger output to the battery can easily add up close to 100 mΩ PCB routing, BAT FET R<sub>d(on)</sub>, current sensing resistor, contact resistance, etc.
- 3 A charging current results in a 300 mV IR drop
- Charger leaves CC charging prematurely, resulting in a longer charge time.

## PM8941 solution:

- Charger regulates V<sub>BAT</sub> (Kelvin-sensed) during CC/CV charging, instead of V<sub>SYS</sub>. This is called analog IR compensation.
- The PMIC also supports digital IR compensation where sensing is done at VPH\_PWR and the resistance between VPH\_PWR to VBAT can be fed to the PMIC.
- Analog IR drop compensation is recommended over digital IR drop compensation.



# Charging Flow Diagram



## Autonomous Charging (1 of 2)

Software-initiated, hardware-managed autonomous charging

- The charger does not start charging the battery until software initiation, unless an auto-trickle charge (ATC) is necessary.
- Once initiated, the charger FSM hardware autonomously manages the charging (trickle → CC → CV → termination → recharge) with software visibility/configurability/controllability.

Two-step ATC

- The battery voltage level (VTRKL), below which the battery has to be trickle-charged for safety reasons, is generally lower than the voltage level (VWEAK), above which the phone can boot.
- To save time spent in ATC, charge the battery with a higher current once VBAT rises above VTRKL:
  - ATC A:
    - Buck off, BAT FET closed; the trickle charger charges the battery with ITRKL to VTRKL
    - ITRKL: 50 mA–200 mA programmable, 10 mA steps,  $\pm 10\%$  of setting  $\pm 5$  mA accuracy, 50 mA default
    - VTRKL: 2.05 V–2.8 V programmable, 50 mV steps,  $\pm 50$  mV accuracy, 2.8 V default
  - ATC B:
    - Buck on, BAT FET closed; the main charger charges the battery with 300 mA/500 mA to VWEAK
    - VWEAK: 2.1 V–3.6 V programmable, 100 mV steps,  $\pm 50$  mV accuracy, 3.2 V default

## Autonomous Charging (2 of 2)

### Trickle charging

- Necessary if coming from FLCB
- Buck on, BAT FET open, system ON, and supplied by charger
- Trickle charger charges the battery with ITRKL via VBAT pin, until VBAT rises to VWEAK

### Fast charging

- Constant-current (CC) charging if VWEAK < VBAT < VBAT\_MAX
  - Charger controller regulates the maximum current (IBAT\_MAX) into the battery; VBAT rises
  - IBAT\_MAX: 200 mA–3000 mA programmable, 50 mA steps,  $\pm 5\%$  of setting  $\pm 50$  mA accuracy, 300 mA default
- Constant-voltage (CV) charging if VBAT reaches VBAT\_MAX
  - Charger controller regulates VPH\_PWR = VDD\_MAX; IBAT drops gradually
  - VDD\_MAX: 3.24 V–4.5 V programmable, 20 mV steps,  $\pm 30$  mV accuracy, 4.2 V default

### Charging termination

- The current into the battery is continuously monitored when sensing IBAT < ITERM (with deglitching) charging is terminated.
  - ITERM: 35 mA–276 mA programmable, 17.28 mA steps,  $\pm 25$  mA accuracy, 207 mA default
- With BAT FET, the buck remains on and supplies the system; BAT FET is open to isolate the fully charged battery.

### Automatic recharge

- When detecting VBAT falls below a programmable threshold, FSM automatically recharges the battery.
  - VBAT\_DET: 3.3 V–4.7 V programmable, 20 mV steps;  $\pm 30$  mV accuracy, 4.1 V default

# Charger Control Loops

## Charger control loops

- VSYS/VBAT regulation during trickle or CV charging
  - ▣ VDD\_MAX: 3.24 V–4.5 V programmable, 10 mV steps, monotonic  $\pm$  30 mV accuracy, 4.2 V default
- Maximum IBAT regulation (sensed over BAT FET) to limit the maximum current into the battery during CC charging
  - ▣ IBAT\_MAX: 200 mA–3000 mA programmable, 50 mA steps,  $\pm$  5%  $\pm$  50 mA accuracy, 300 mA default
- Minimum VIN limiting to prevent deep voltage collapse on current limited charger
  - ▣ VIN\_MIN: 3.4 V–9.6 V programmable, 50/100 mV steps,  $\pm$  2% accuracy, 4.3 V default
  - ▣ SMBB also provides support of hardware automatic input current limiting (AICL)
- Maximum IIN limiting to limit the maximum input current for USB compliance
  - ▣ IUSB\_MAX: 100/150/200/300/400 to 2500 mA programmable, 100 mA default

Each loop converts the control variable (either a voltage or a current) to a duty cycle control input that drives the PFET and NFET output stages.

Not all control loops are active at any one time, though multiple loops can be active simultaneously.

Regardless of the number of loops that are active, the loop demanding the lowest duty cycle (lowest output voltage or current) is always selected – only one control loop is closed.

The two input control loops (USB current and charger voltage) limit the charger's input current, thereby preventing input voltage collapse.

# Safety Features

## Safety timers

- Hardware timers that limit the maximum time allowed for trickle charging and the complete charging cycle
- Stops charging (and generates interrupt) if the timer times out

## Charger watchdog timer (one-time write register)

- Hardware timer to ensure the charging control software remains alive
- Stops charging (and generates interrupt) if the timer times out
- 0–32 second programmable

## VBAT\_SAFE and IBAT\_SAFE (one-time write registers)

- To limit maximum allowed battery charging voltage/current, and prevent malware
- Write access to these registers are enabled after power on reset, and are disabled after being written once

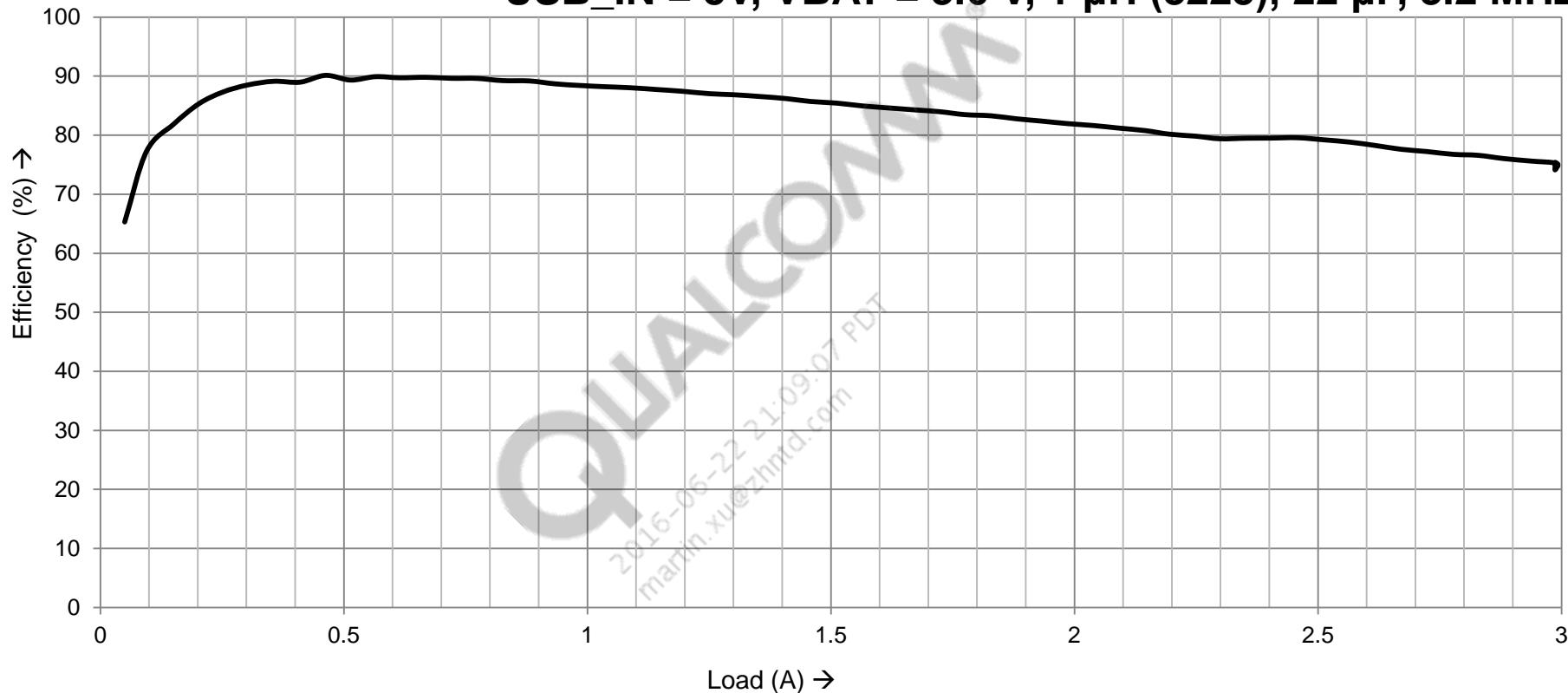
## Battery overvoltage detector

- VBAT\_DET comparator is reused to monitor battery overvoltage condition during fast charging
- Interrupt is generated if the battery overvoltage condition is detected

## Thermal management

## SMBB Buck Efficiency

**USB\_IN = 5V, VBAT = 3.6 V, 1  $\mu$ H (3225), 22  $\mu$ F, 3.2 MHz**



PM8941 SMBB efficiency:

- 80% at 100 mA  $I_{out}$
- 90% at 500 mA  $I_{out}$
- 88% at 1.0 A  $I_{out}$
- 79% at 2.5 A  $I_{out}$

## Maximum Battery Charging Current

Maximum battery charging current depends upon the impedance between TA to VBAT.

- Smaller the TA to VBAT impedance is, higher headroom available for SMBB, and higher battery charging current can be achieved.
- Although PMIC supports IBAT\_MAX up to 3000 mA, it is not possible to achieve this due to the headroom limitation and increased power dissipation across the PMIC.

Element	Typical impedance (mΩ)
TA cable + contact resistance (A)	250
USB OVP resistance (B)	190
SMBB high side FET resistance (C)	95
Inductor DCR (D)	37
Battery FET impedance (E)	15
Resistance from USB_IN to VPH_PWR (F = B + C + D)	322
Impedance from USB_IN to VBAT (G = E + F)	337
Impedance from TA to VBAT (H = A + G)	587

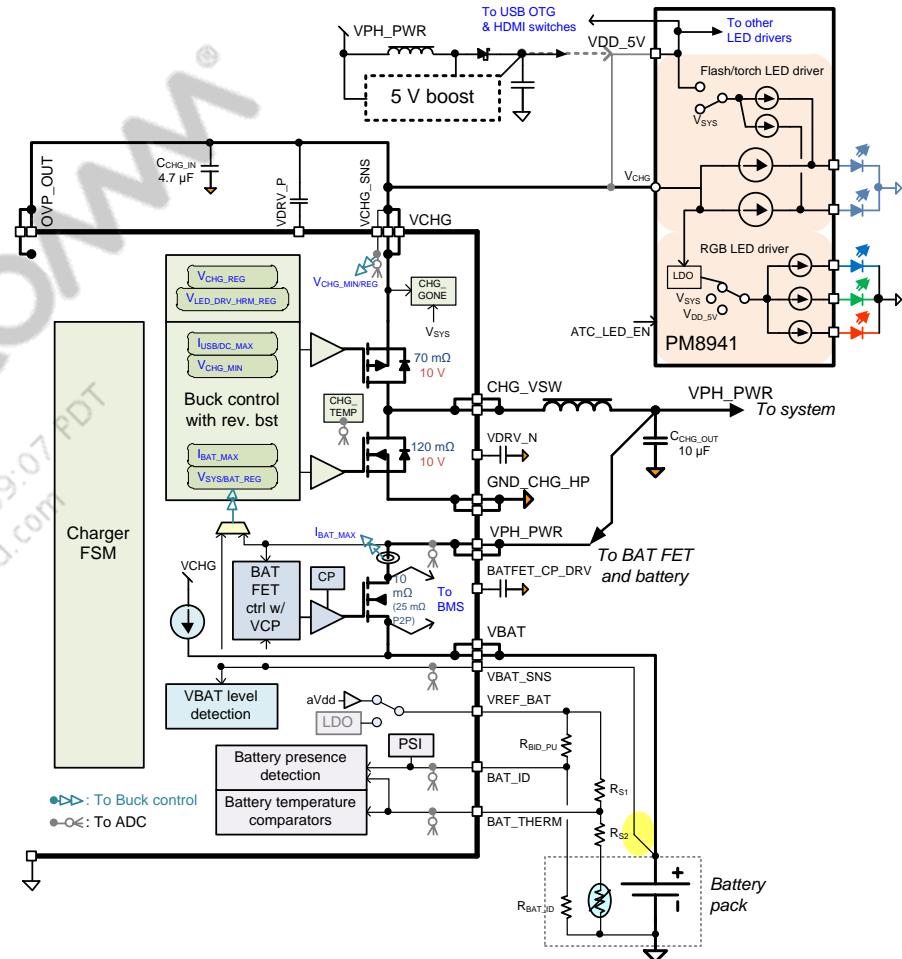
# SMBB Reverse Boost Mode

The SMBB runs in reverse boost mode to provide a 4 V to 5 V supply for:

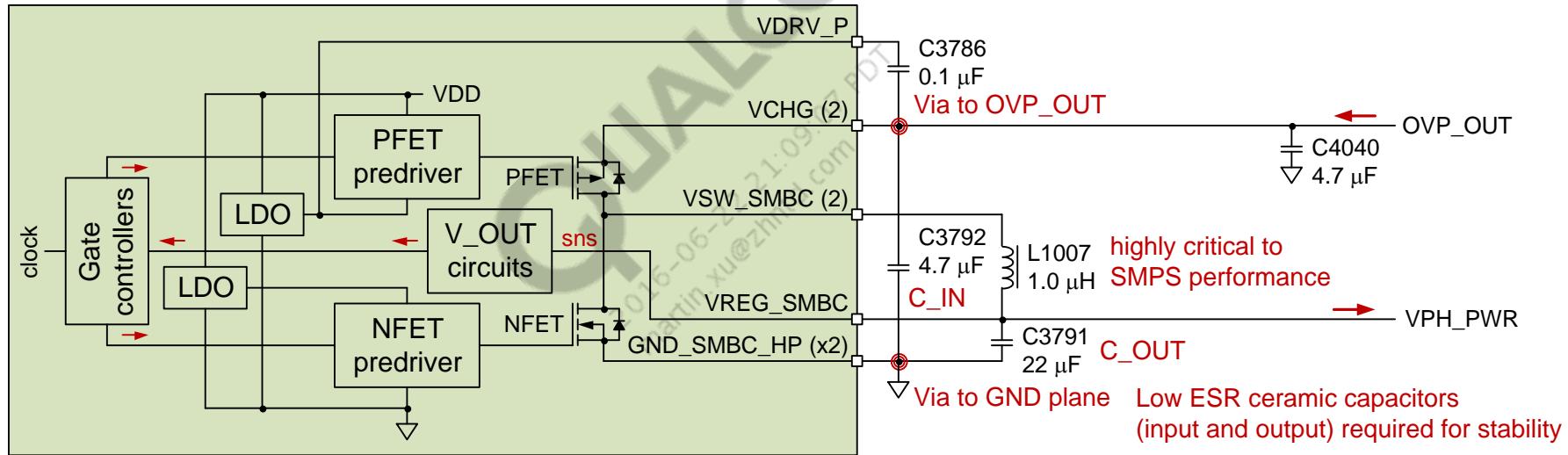
- Flash LED driver
- Torch/home row lighting/RGB LED drivers
- USB OTG switch and HDMI switch

Supports an adaptive mode that regulates the maximum headroom of the Flash LED driver

- To minimize the voltage drop across the flash LED driver and its thermal consumption



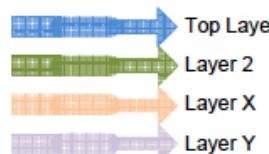
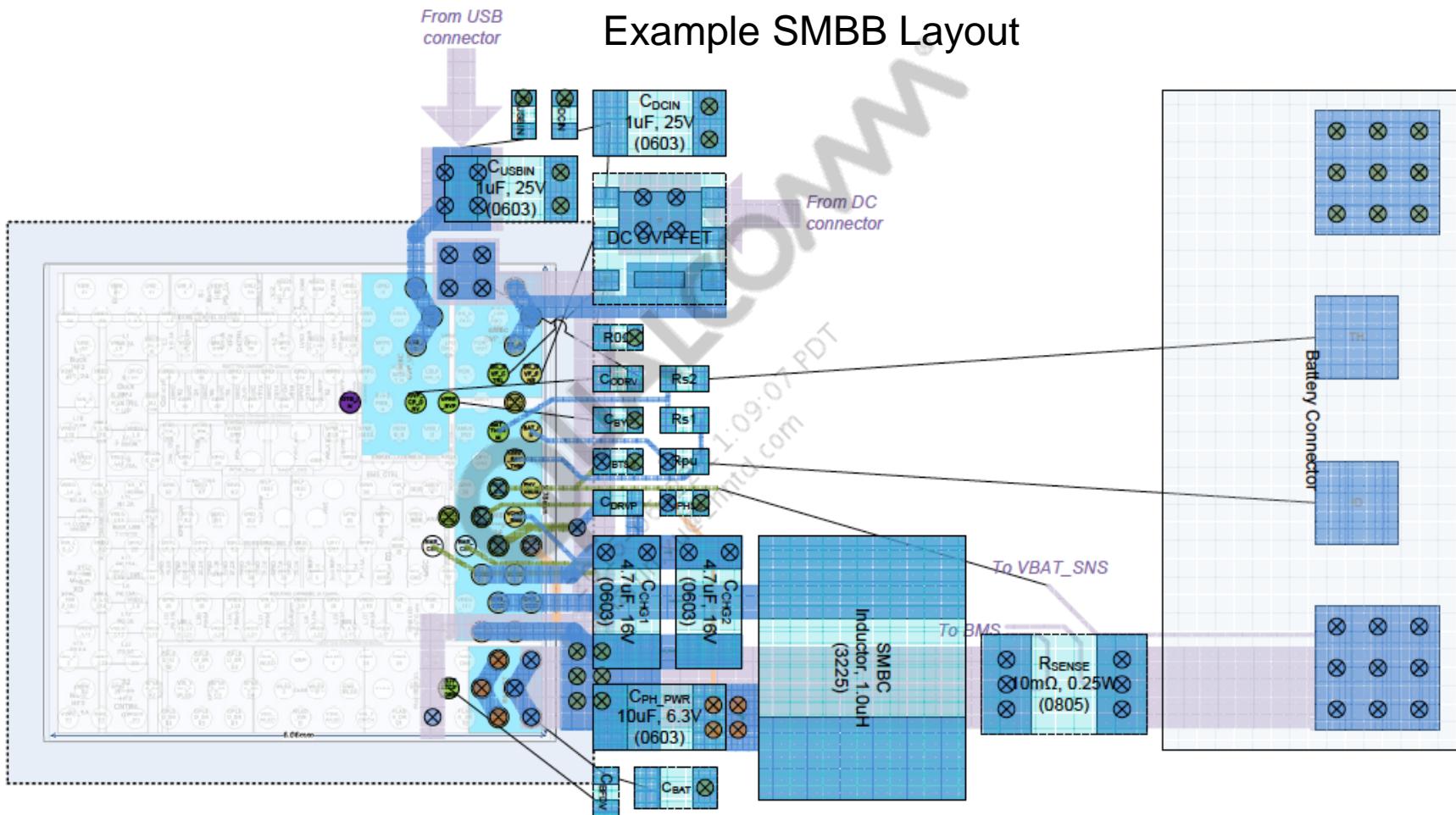
# Example SMBB Schematic



**Note:** Refer to the latest revision of the *MSM8274/MSM8274AB, MSM8674/MSM8674AB, and MSM8974/MSM8974AB Baseband Reference Schematic* (80-NA437-41) for the SMBB schematic.

# SMBB Layout Guidelines (1 of 2)

## Example SMBB Layout



- Via to GND plane
- Via to VPH plane
- Via to inner layer

## SMBB Layout Guidelines (2 of 2)

### Placement:

- Minimize switching loop. Place charger input capacitors, output capacitors, and inductor close to each other.
- Place the DRV\_P capacitor close to the charger input capacitor.

### Grounding:

- Connect GND of charger input capacitors, output capacitors, and GND\_CHG\_HP pins of PMIC together.  
Connect the common point directly to the main GND using multiple vias.
- Connect pin 185 to GND directly using a dedicated via.

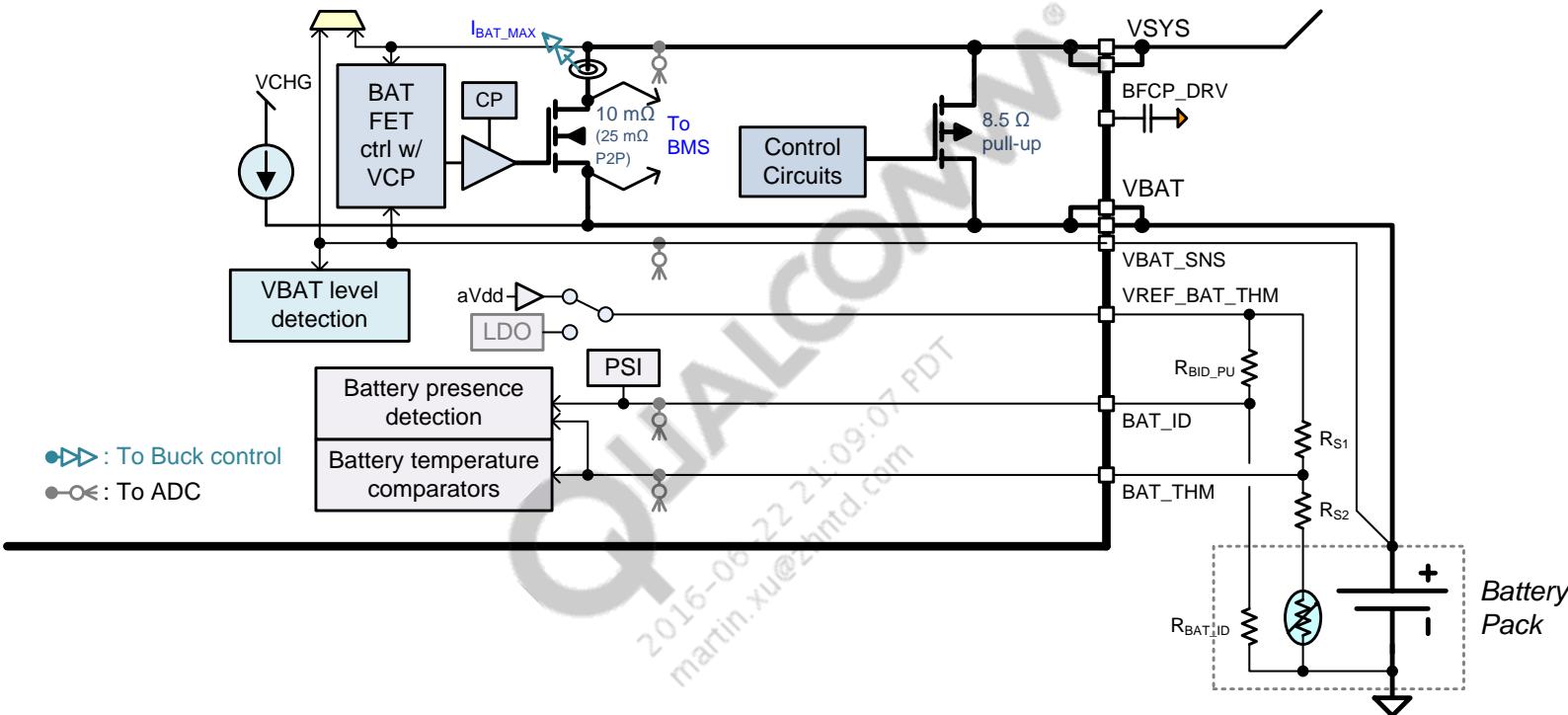
### High current paths:

- Use a thick trace from USB connector to USB\_IN pins and DC connector to DC\_IN pins of the PMIC.
- Use a thick trace from OVP\_OUT pin to VCHG pin of PMIC.
- Use a thick trace from VCHG to VDD\_FLASH pin of PMIC.
- Use a thick trace from battery connector to VBAT pin.

### Sensing:

- Connect the VBAT\_SNS pin to the battery connector using a thin trace.
- Connect the VCHG\_SNS pin to VCHG using a thin trace.
- Connect VREG\_SMBC to the output of SMBB using a thin trace.

# Integrated Battery FET



## Integrated NMOS BAT FET

- Battery current sensed across BAT FET R<sub>ds(on)</sub> for SMBC I<sub>BAT</sub>\_MAX limiting and BMS; eliminating the external I<sub>BAT</sub> sensing resistor.
- BAT FET R<sub>ds(on)</sub> regulated at  $10 \text{ m}\Omega \pm 2\%$  across temperature (-30°C to 125°C) and V<sub>BAT</sub> range (2.5 V to 4.5 V) after trim; 25 mΩ max pin-to-pin.
- In parallel with the battery NFET, there is an integrated PFET that acts as a 8.5 Ω pull-up between V<sub>BAT</sub> and V<sub>PWR</sub> when the PMIC is off (see the next slide).

Hardware battery presence detection and JEITA-compliant battery temperature comparators PMIC serial interface (PSI) for the digital battery interface.

## Battery FET On Modes

PMIC mode	Battery FET state	Battery FET charge pump mode	PFET pull-up	Clock source for charge pump	Comment
Active (with charger attached)	On/Off	HPM	Off	19.2 MHz XO/TCXO	Used when charger is connected (for charging and/or fast BATFET turning-on upon VCP event), or at least 200 $\mu$ s after charger removal (for fast turning-on of the BATFET to run system from battery).
Active (on from battery)	On	NPM	Off	1.2 MHz	Used when phone is active running off a battery, (starting 200 $\mu$ s after charger removal).
Sleep	On	LPM	Off	1.2 MHz	Used during sleep to minimize current consumption.
	On	NPM	Off	1.2 MHz	Used during sleep to provide current to a client-like WLAN chip or during BMS measurement.
	Off	Ultra LPM	On	Off	Used when system is in sleep and BMS is not taking measurement or no client-like WLAN chip is being powered via VPH_PWR.

PMIC battery FET charge pump (CP) supports the following modes:

- HPM mode → Used when charger is connected; clock source for CP is 19.2 MHz XO/TCXO.
- NPM mode → Used when PMIC is on from battery; clock source for CP is internal 1.2 MHz clock source; could also be used during sleep.
- LPM mode → Used during sleep; clock source for CP is internal 1.2 MHz clock source with more current saving optimizations.
- Ultra LPM mode → Used during sleep; battery FET and its CP are off, PFET pull-up is on.

## Battery FET Off Modes

Off modes	NFET status	PFET status	VPH_PWR discharge load	Ignores power on
AFP	Off, with body diode off	Off, with body diode off	On	Yes
Shelf/ship	Off, with body diode off	Off, with body diode off	Off	No
Normal	Off, with body diode off	On, 8.5 Ω (typical)	Off	No
Pseudo	On	Off, with body diode off	Off	No

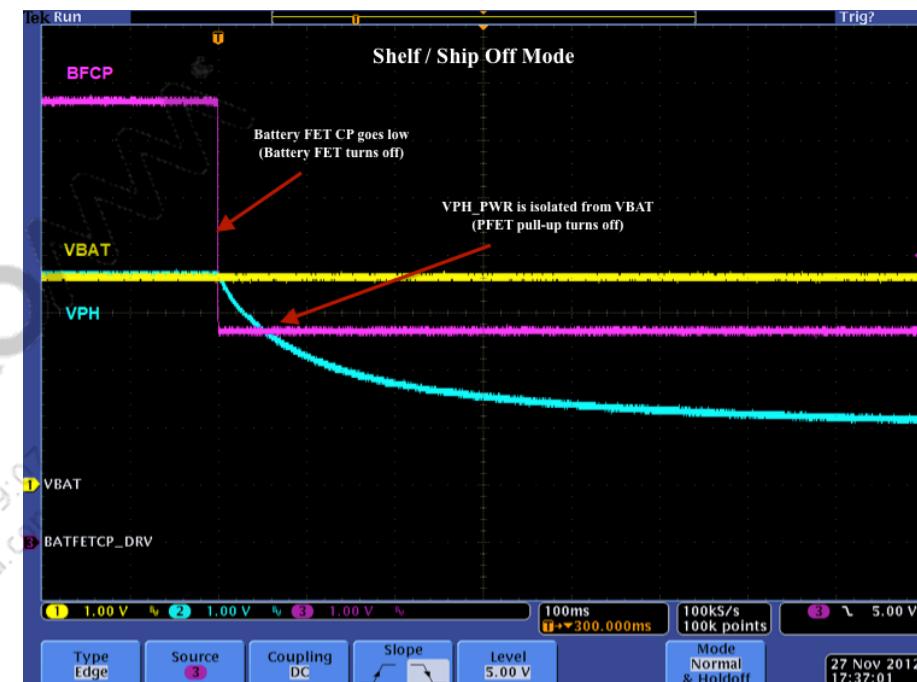
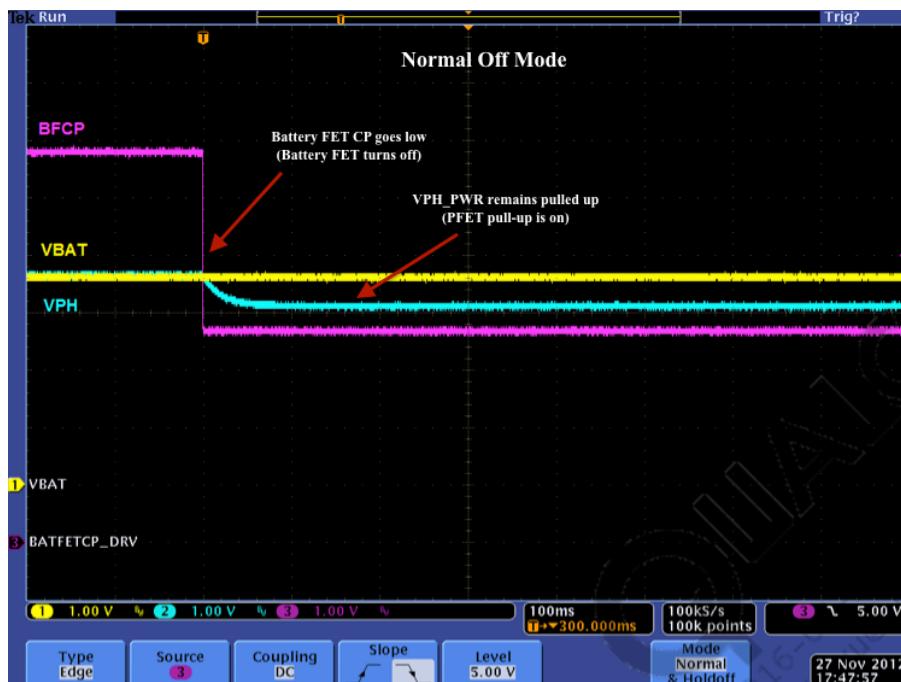
PMIC supports the following OFF modes:

- AFP off mode in which the battery FET, its body diode, and PFET pull-up are all off. VPH\_PWR discharge load (50 Ω, typical) is on → VPH\_PWR is isolated from VBAT; additionally VPH\_PWR is discharged by the 50 Ω load.
- Shelf/ship mode in which the battery FET, its body diode, and PFET pull-up are all off → VPH\_PWR is isolated from VBAT.
- Normal off mode in which the battery FET and its body diode are off but the PFET pull-up is on → VPH\_PWR is still connected to VBAT through the PFET pull-up.
- Pseudo off mode in which the battery FET is on but the PFET pull-up is off → VPH\_PWR is same as VBAT. This can be used for NFC applications when the device is off.

### Note:

- AFP mode can be exited either by removing all power sources or pressing the power key.
- Shelf/ship mode can be exited by applying any power-on trigger (power-key press, charger insertion, etc.)

# Normal Off Mode vs. Shelf/Ship Off Mode



Steps to put PMIC in ship/shelf off mode:

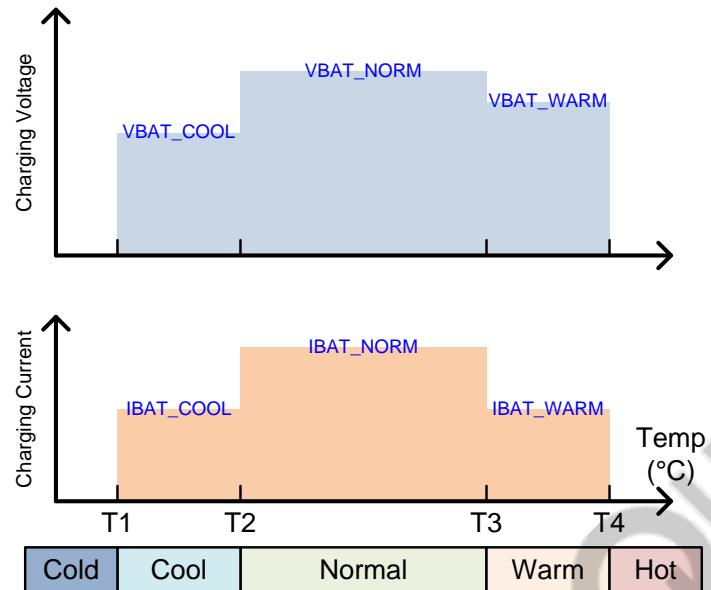
1. Before the last power-off in phone factory line, make the following register writes:

0x12D0 = 0xA5  
0x12DA = 0x08  
0x12D0 = 0xA5  
0x12E3 = 0x20

2. During power on, in SBL make the following register writes:

0x12D0 = 0xA5  
0x12DA = 0x0F  
0x12D0 = 0xA5  
0x12E3 = 0x00

# JEITA Specification – Battery Temperature-dependent Charging



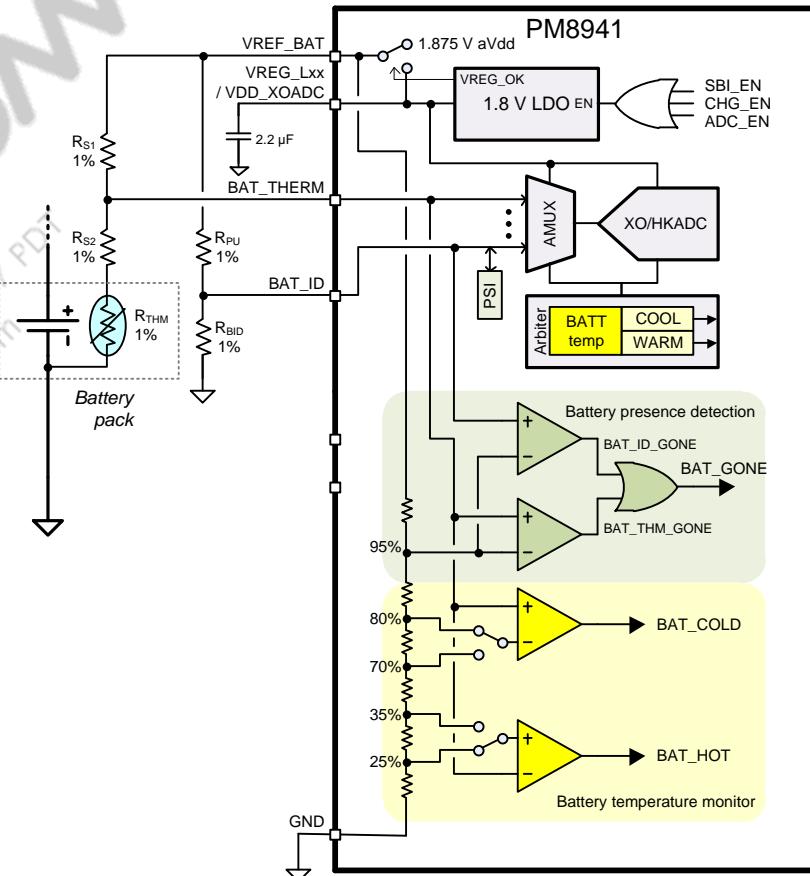
JEITA\*: A Guide to the Safe Use of Secondary Lithium Ion Batteries in Notebook-type Personal Computers

- Reduced maximum battery charging voltage and current at extended battery temperature ranges
  - NORMAL region ( $T_2 < TBAT < T_3$ ): optimal charging with  $V_{BAT\_NORM}$  and  $I_{BAT\_NORM}$
  - COOL region ( $T_1 < TBAT < T_2$ ): reduced charging with  $V_{BAT\_COOL}$  and  $I_{BAT\_COOL}$
  - WARM region ( $T_3 < TBAT < T_4$ ): reduced charging with  $V_{BAT\_WARM}$  and  $I_{BAT\_WARM}$
  - COLD region ( $TBAT < T_1$ ) or HOT region ( $TBAT > T_4$ ): charging is prohibited
- Mandatory in Japan after November 2011
- Actual T1, T2, T3, and T4 values vary by battery manufacturer.
- \* JEITA: Japan Electronics and Information Technology Industries Association

# Battery Temperature Monitoring (BTM)

Enhanced BTM with JEITA compliance

- Two analog BTM comparators that monitor the cold and hot conditions
  - Four thresholds generated by internal resistor ladder.
    - For charging with traditional battery temperature range, use 70% and 35% thresholds.
    - For charging with extended battery temperature range (JEITA), use 80% and 25% thresholds.
  - Using RS1 and RS2 pull-up resistors to tune the trip points.
  - Battery charging is paused if either comparator asserts.
- An automated digital BTM routine that monitors the cool and warm conditions.
  - If enabled, battery temperature is automatically measured by the ADC Arbiter periodically (programmable up to 16 seconds).
  - The battery temperature measurement result compared with programmable cold and warm thresholds; interrupts are generated if either of the thresholds are exceeded.
  - Charging software adjusts the VBAT\_MAX and IBAT\_MAX accordingly.
- Battery thermistor/resistor biasing
  - VREF\_BAT\_THM: 1.875 V aVdd before power on; 1.8 V LDO (L8) after poweron.



# Battery Presence Detection (BPD)

Flexible BPD with battery thermistor or ID resistor inputs

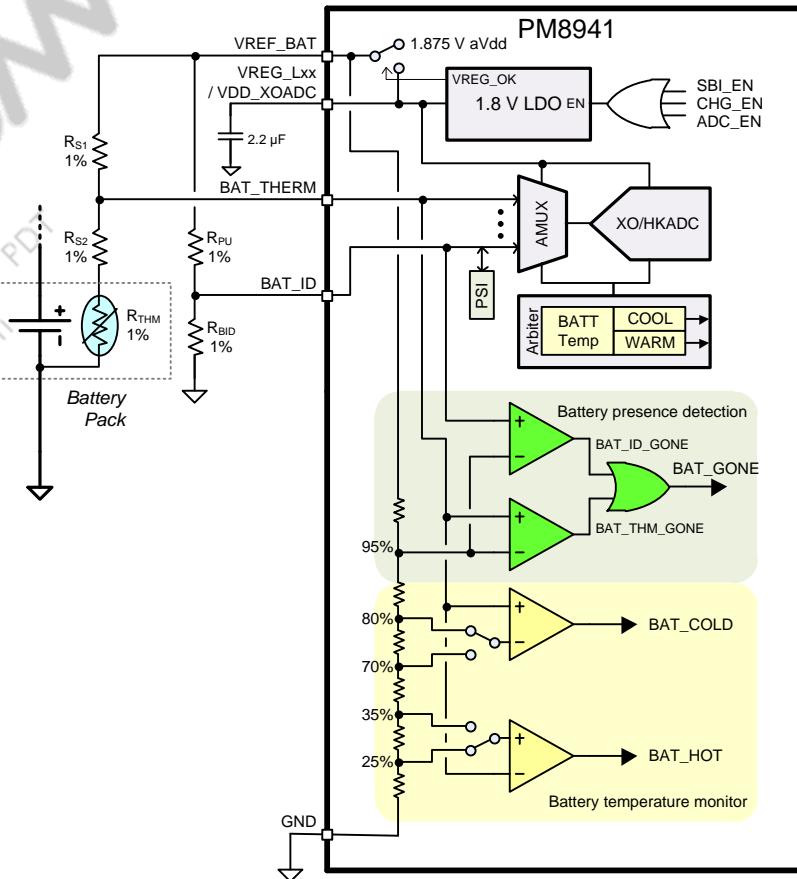
- Battery presence is detected by sensing the presence of battery thermistor or ID resistor, whichever is inside the battery pack.
  - If battery is absent, the pull-up resistors will pull BAT\_THM and/or BAT\_ID high.
- Two dedicated comparators for BPD.
  - Battery is considered as gone, if BAT\_THM or BAT\_ID is above 95% of VREF\_BAT\_THM.
  - Interrupts are generated (after deglitching) when detecting battery insertion or removal.
  - Charging shall be stopped upon battery removal.

## Battery Identification

- BAT\_ID is sent to PMIC AMUX/HKADC for battery ID resistor (RBID) measurement.

## PMIC serial interface (PSI)

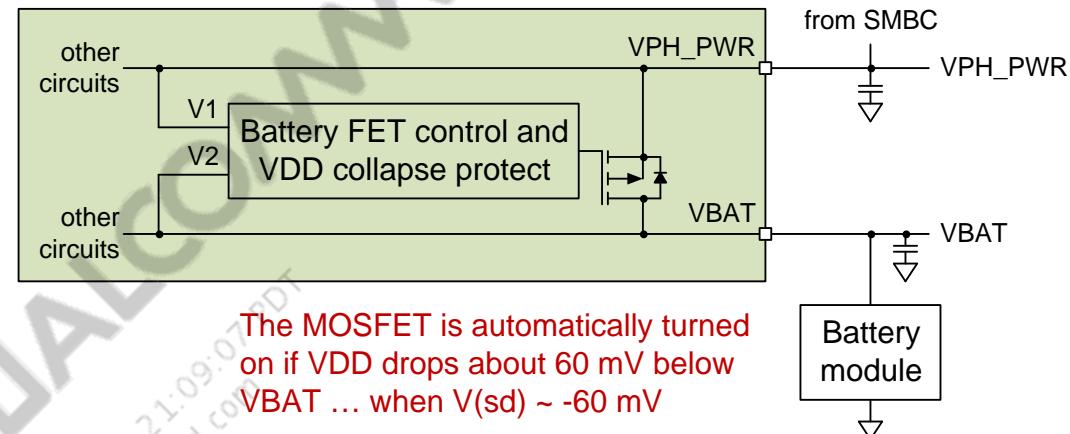
- A low-speed serial communication on the battery ID line, to transfer battery size/voltage/age information.
- BAT\_ID line driven/listened by the PSI block when not measuring RBID.



## VDD Collapse Protection

The PMIC prevents a sudden load from inadvertently collapsing the VDD voltage as discussed here.

PMIC monitors the voltage across the battery MOSFET  $V(sd) = V1 - V2$



- When a valid external charger is connected, and the battery is either fully charged or too hot or cold to be charged, the battery FET is opened and the system runs off the external charger.
- If the external charger's current limit is exceeded, voltage collapse protection (VCP) is executed.
  - ▣ If VPH\_PWR drops 60 mV below VBAT, VCP is activated.
  - ▣ The battery FET is turned on, allowing the battery to supplement the external source.
    - Turn-on is a single step, not a linearly regulated process.
  - ▣ With the added battery current, the system's high current does not cause VDD to collapse.
  - ▣ The battery FET is turned off when the excessive current condition ends.
    - When > 100 mA flows into the battery, or
    - When 0 to 5 mA flows into the battery for at least 1 second
  - ▣ Battery FET turn-on time is fixed at 5 ms max; the turn-off time is 1 ms by default, but can be increased to 10 ms via SPMI.

# Battery Monitoring System (BMS)

- Controls measurement frequency, averaging, Coulomb counting, and CC resets

PM8941 employs a high side BMS

The CADC samples Vsense generated across BATFET ( $10 \text{ m}\Omega$ ) → current measurement

The VADC samples Vbat → OCV measurement

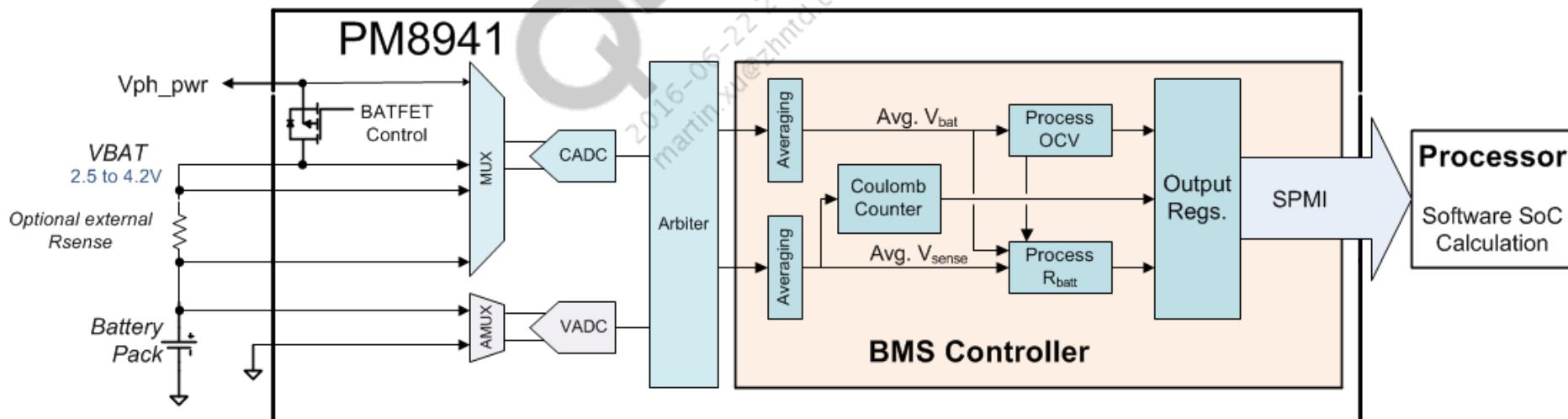
- Shared use with other housekeeping functions

The BMS controller autonomously manages ADCs and key measurements

- All data for SoC calculations are stored, read as desired by software → no periodic software intervention

- The BMS controller uses a Qualcomm Technologies, Inc. (QTI) proprietary algorithm.

The PMIC software reads stored data, executes software algorithms and calculates SoC.



## Note:

The following documents (application notes) have been released to assist customers with the battery characterization process:

- 1) *Battery Characterization Process Application Note* (80-VT310-24)
- 2) *Qualcomm Battery Characterization (QBCSW) 1.6 Software User Manual* (80-NN139-1)



## Section 3.1

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# Other Topics

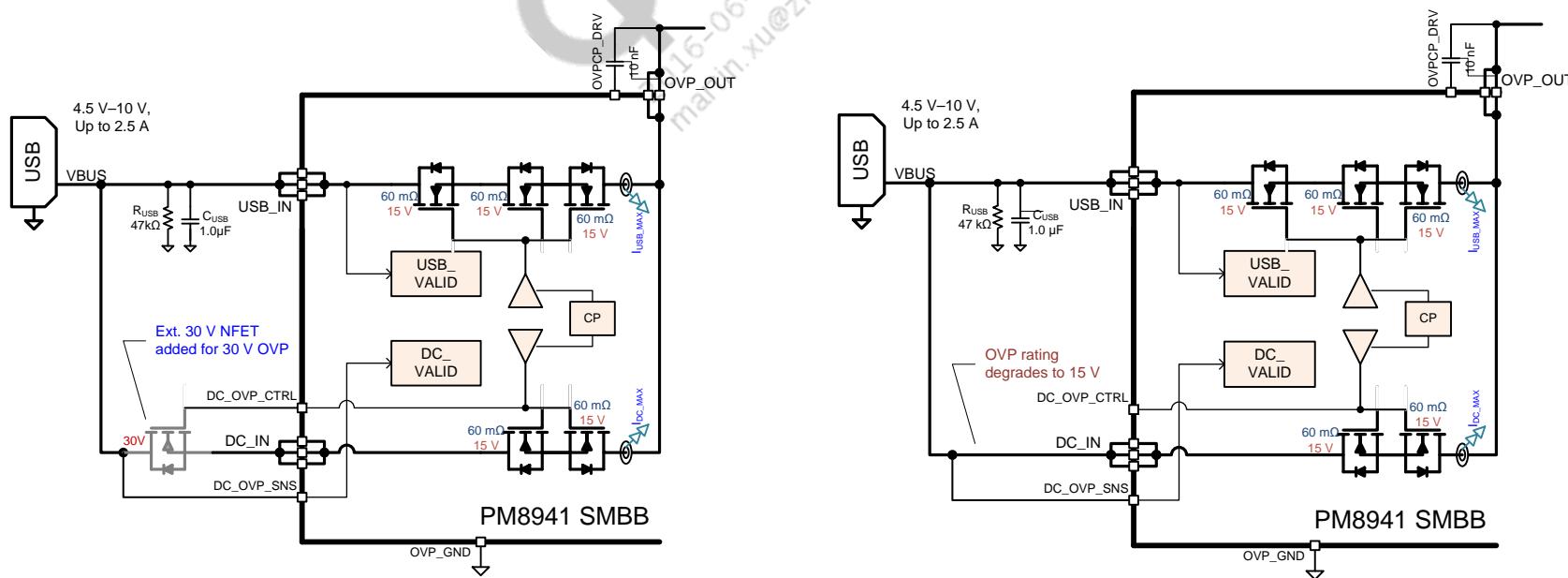
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## Dual Path Charging (1 of 2)

If the DC charging path is not used, DC OVP FET can be used for USB charging.

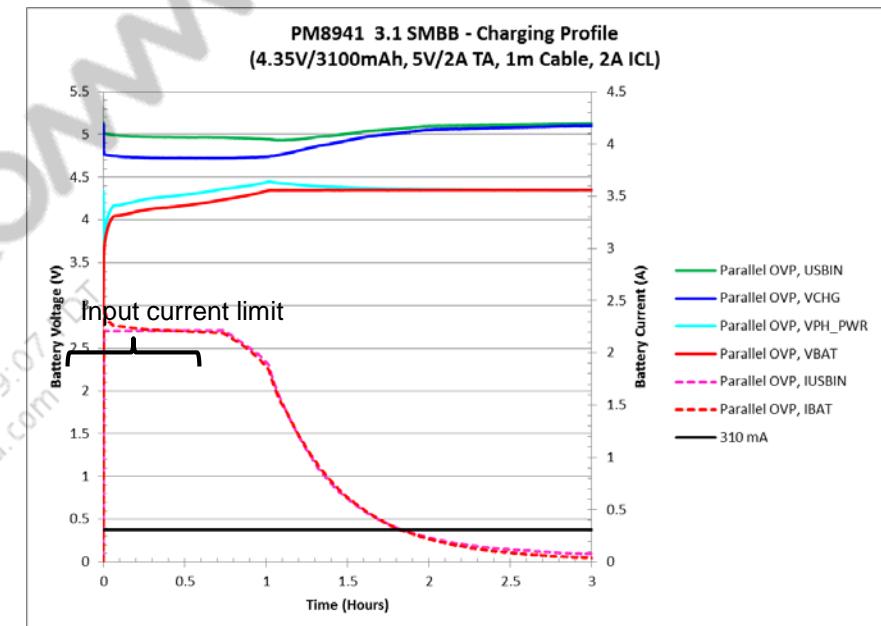
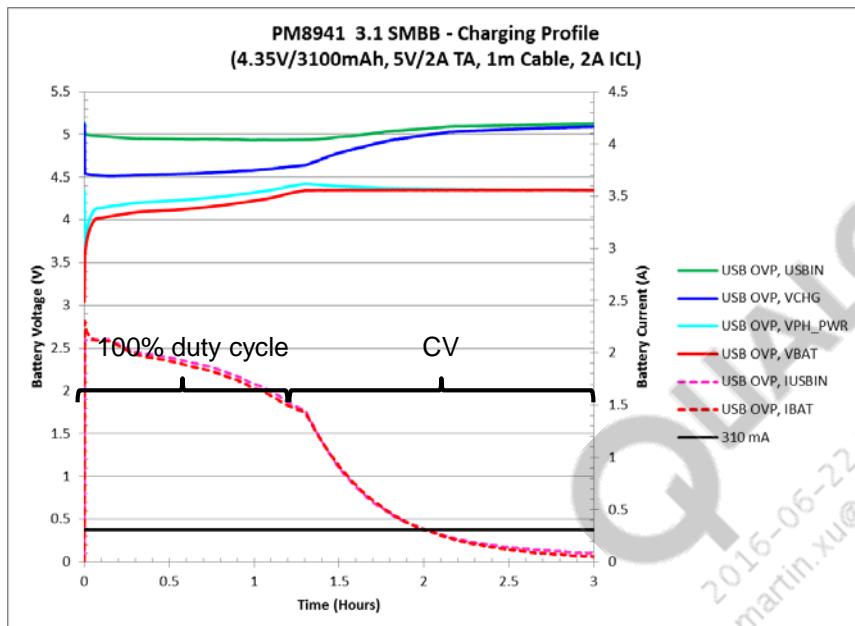
- Reduces USB charging path Rds (on); increases charging current when headroom is limited → less charge time
- Reduces heat generation; redistributes the heat over both USB and DC OVP FETs → lower PMIC die temperature during charging

If 28 V OVP (for USB) is required:	If 15 V OVP (for USB) is acceptable
<ul style="list-style-type: none"> <li>Install 30 V NFET between USB_IN and DC_IN</li> <li>DC_OVP_CTRL controls NFET gate</li> <li>DC_OVP_SNS connected to USB_IN</li> </ul>	<ul style="list-style-type: none"> <li>Short USB_IN to DC_IN</li> <li>DC_OVP_CTRL floating</li> <li>DC_OVP_SNS connected to USB_IN</li> </ul>



## Dual Path Charging (2 of 2)

Due to reduced OVP resistance, dual path charging results in reducing charging time as indicated below.



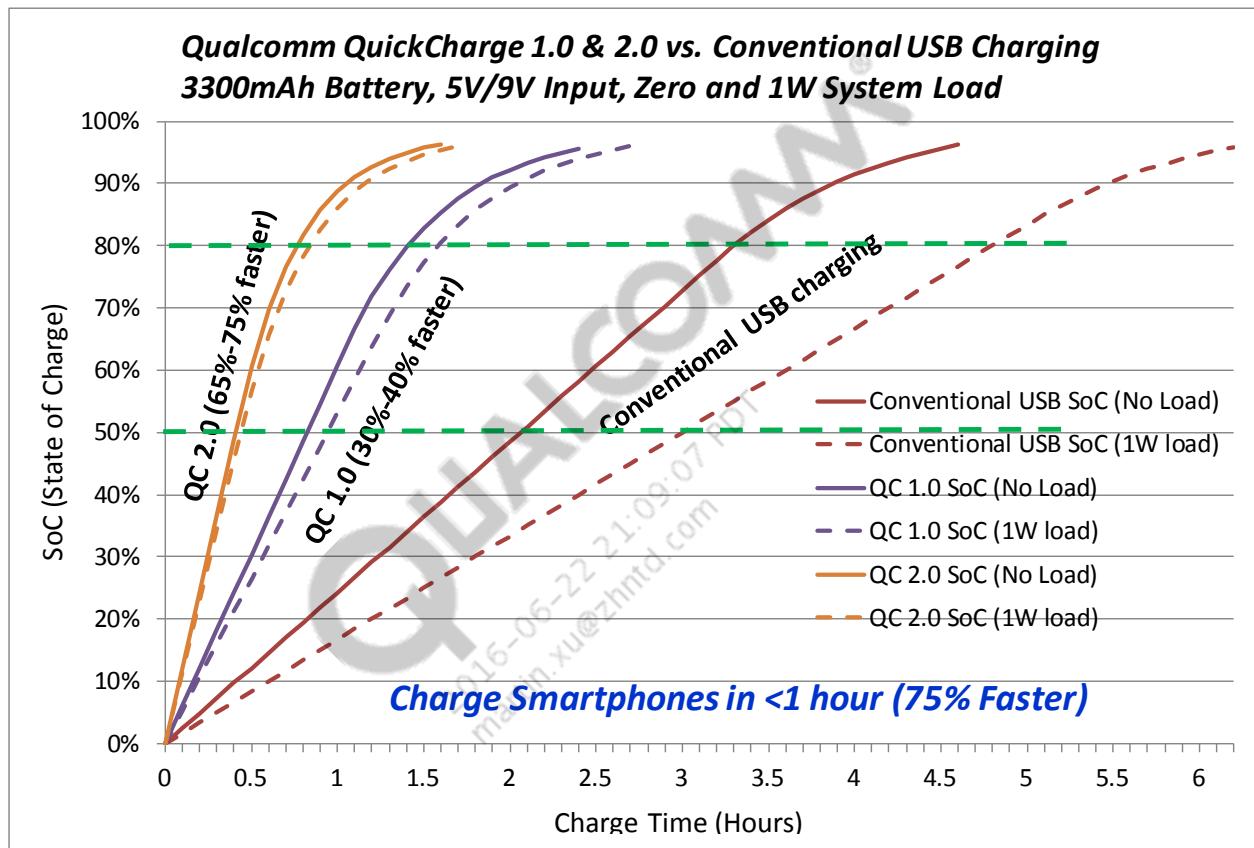
Charging method	EoC current	Battery capacity	SoC	Charging time
Single path (USB OVP)	310 mA	2.90 Ah	93.55%	120 min (2.00 hrs)
Dual path (USB OVP in parallel with DC OVP)	310 mA	2.89 Ah	93.23%	109 min (1.82 hrs)

**Note:** Software changes are required to support dual path charging on PM8941. The Linux Android platform supports this through CR565240. For other mobile OS, customers should contact the CE team for support.

## HVDCP Charging (1 of 4)

- PM8941 supports HVDCP Qualcomm® Quick Charge™ 2.0 charging.
- Quick Charge 2.0 can deliver significantly higher power to a portable device for faster charging and/or system operation:
  - Up to 60 W over standard micro-USB cables/connectors
  - Class A: 5 V/9 V/12 V for smartphones, tablets, mobile routers, digital still cameras, etc.
  - Class B: 5 V/9 V/12 V/20 V for Chromebooks, slim notebooks, etc.
  - Current capability of 500 mA to more than 3 A
  - Backwards compatible with BC 1.2 detection
  - Delivers up to 75% faster charging vs. conventional USB charging (see the next slide)\*
  - Provides high performance independent of cable quality, thickness, or length
  - Full ecosystem support and qualification enabled by QTI
  - Features UL compliancy testing/certification to ensure interoperability and high quality
- For more details about Quick Charge 2.0, refer to *Introduction to Qualcomm Quick Charge 2.0* (80-VT310-3).

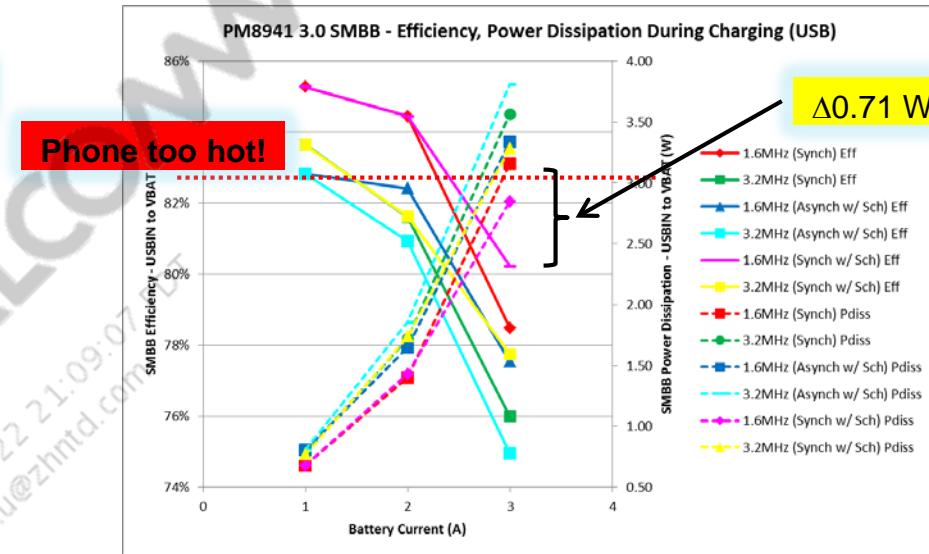
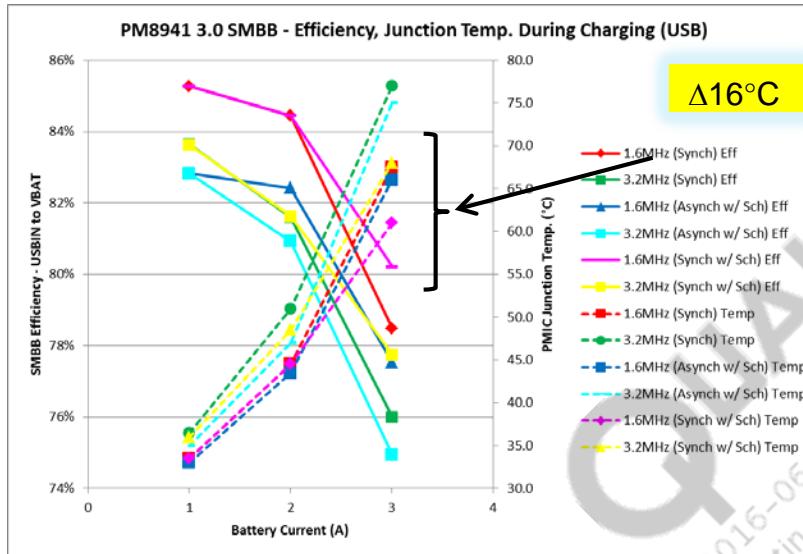
## HVDCP Charging (2 of 4)



\* Based on internal tests, charging a 3300 mAh battery using a [1] QTI 2.0 USB wall adapter (9 V, 2 A), [2] USB wall adapter (5 V, 2 A), and [3] USB wall adapter (5 V, 1 A), respectively. (February 2013)

## HVDCP Charging (3 of 4)

The plots and the table below show efficiency, power dissipation, and junction temperature with HVDCP charging along USB path.



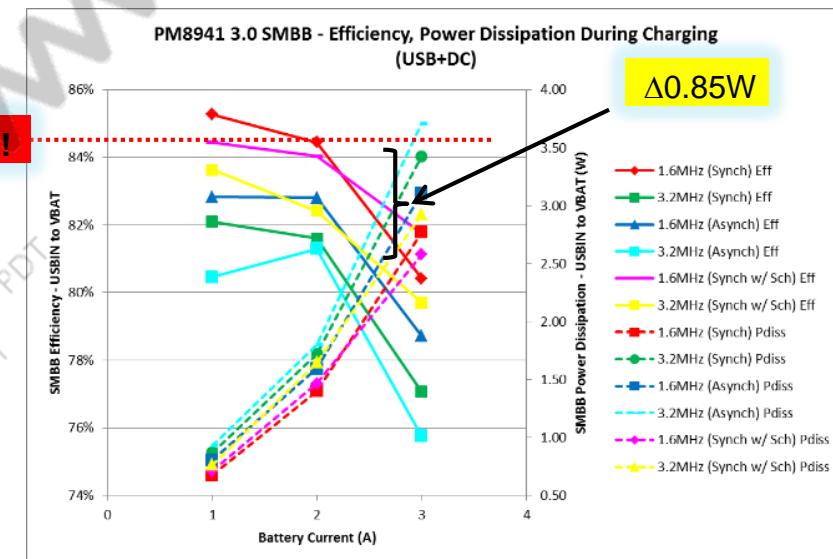
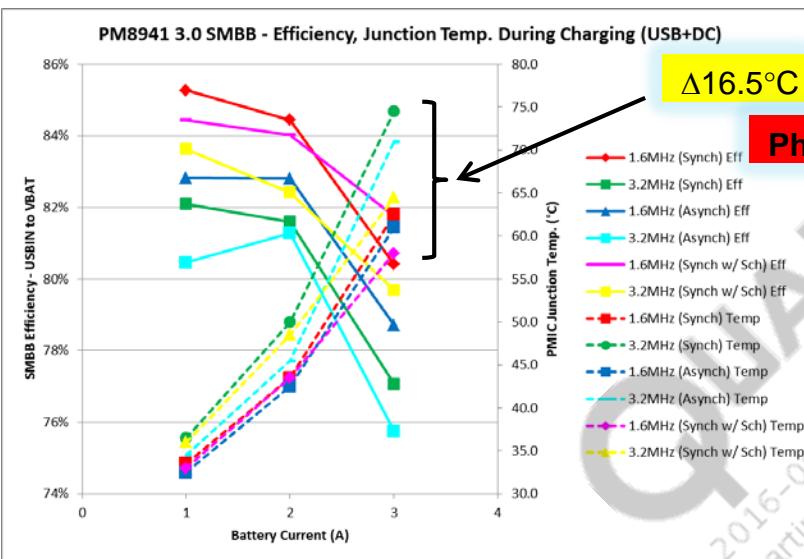
	Fsw	1A				2A				3A			
		Pdiss (W)	Efficiency	Junction Temperature (V/°C)	Junction Temperature Rise (°C)	Pdiss (W)	Efficiency	Junction Temperature (V/°C)	Junction Temperature Rise (°C)	Pdiss (W)	Efficiency	Junction Temperature (V/°C)	Junction Temperature Rise (°C)
9V	1.6MHz (Synch)	0.68	85%	0.613	33.5	6.5	1.40	84%	0.635	44.5	17.5	3.16	78%
	3.2MHz (Synch)	0.78	84%	0.619	36.5	9.5	1.72	82%	0.648	51.0	24.0	3.56	76%
	1.6MHz (Synch w/ Schottky)	0.68	85%	0.613	33.5	6.5	1.43	84%	0.635	44.5	17.5	2.85	80%
	3.2MHz (Synch w/ Schottky)	0.77	84%	0.618	36.0	9.0	1.74	82%	0.643	48.5	21.5	3.28	78%
	1.6MHz (Asynch w/ Schottky)	0.80	83%	0.612	33.0	6.0	1.65	82%	0.633	43.5	16.5	3.34	78%
	3.2MHz (Asynch w/ Schottky)	0.80	83%	0.616	35.0	8.0	1.85	81%	0.640	47.0	20.0	3.81	75%

### Note:

- Only 3.2 MHz switching frequency is supported for SMMB. 1.6 MHz in the above plot/table was used for experimentation only.
- For some cases, an external Schottky diode was placed in parallel with low side FET.

## HVDCP Charging (4 of 4)

Plots and table below show efficiency, power dissipation, junction temperature with HVDCP charging along dual path (USB and DC OVP shorted together).



	Fsw	1A				2A				3A			
		Pdiss (W)	Efficiency	Junction Temperature (V/°C)	Junction Temperature Rise (°C)	Pdiss (W)	Efficiency	Junction Temperature (V/°C)	Junction Temperature Rise (°C)	Pdiss (W)	Efficiency	Junction Temperature (V/°C)	Junction Temperature Rise (°C)
9V	1.6MHz (Synch)	0.68	85%	0.613	33.5	6.5	1.40	84%	0.633	43.5	16.5	2.77	80%
	3.2MHz (Synch)	0.87	82%	0.619	36.5	9.5	1.72	82%	0.646	50.0	23.0	3.43	77%
	1.6MHz (Synch w/ Schottky)	0.71	84%	0.612	33.0	6.0	1.47	84%	0.633	43.5	16.5	2.58	82%
	3.2MHz (Synch w/ Schottky)	0.77	84%	0.618	36.0	9.0	1.65	82%	0.643	48.5	21.5	2.92	80%
	1.6MHz (Asynch w/ Schottky)	0.80	83%	0.611	32.5	5.5	1.59	83%	0.631	42.5	15.5	3.10	79%
	3.2MHz (Asynch w/ Schottky)	0.93	80%	0.615	34.5	7.5	1.80	81%	0.637	45.5	18.5	3.71	76%

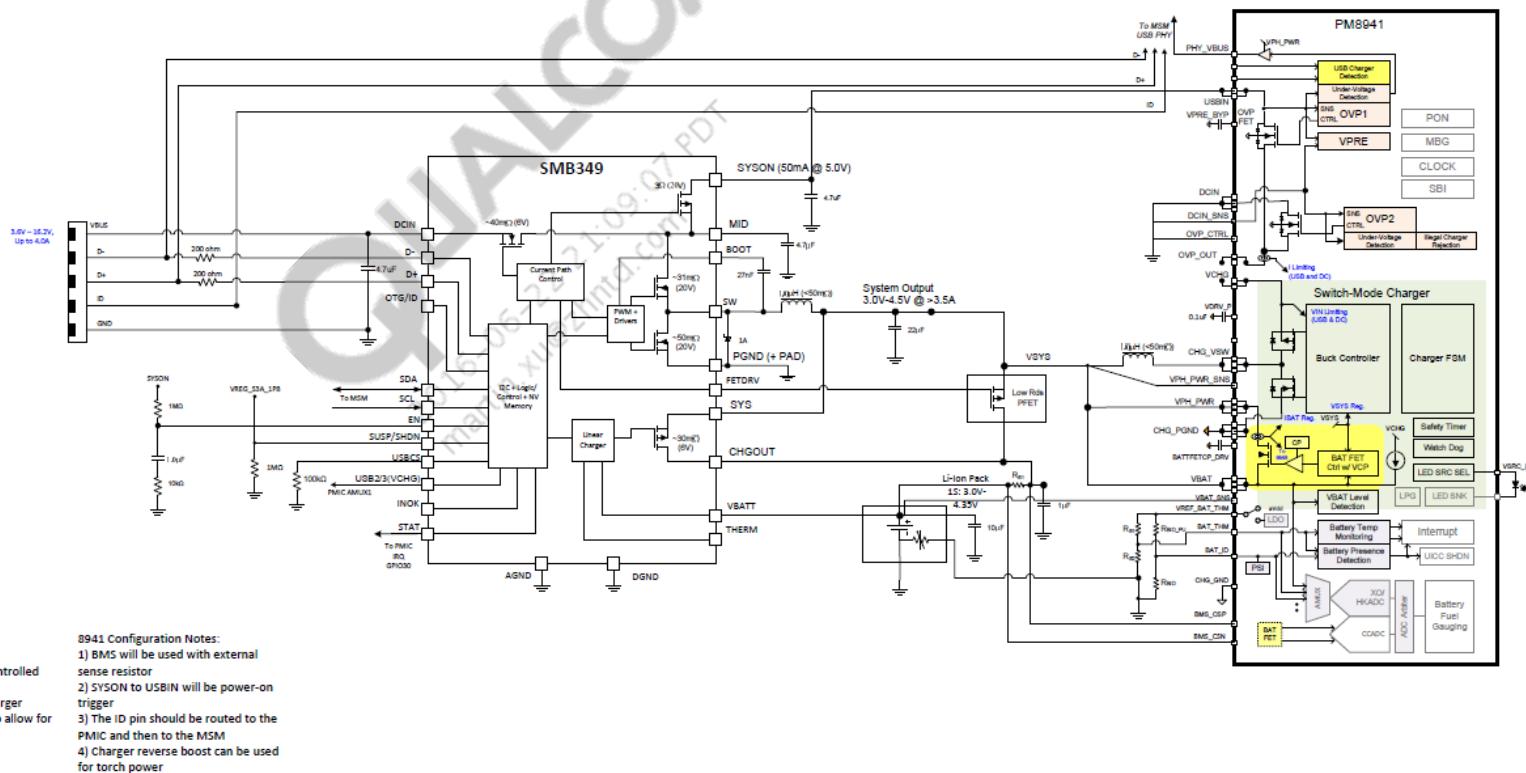
### Note:

- Only 3.2 MHz switching frequency is supported for SMBB. 1.6 MHz in the above plot/table was used for experimentation only.
- For some cases, an external Schottky diode was placed in parallel with low side FET.

# Design Example: SMB349 + PM8941 Charging (1 of 3)

Single path charging:

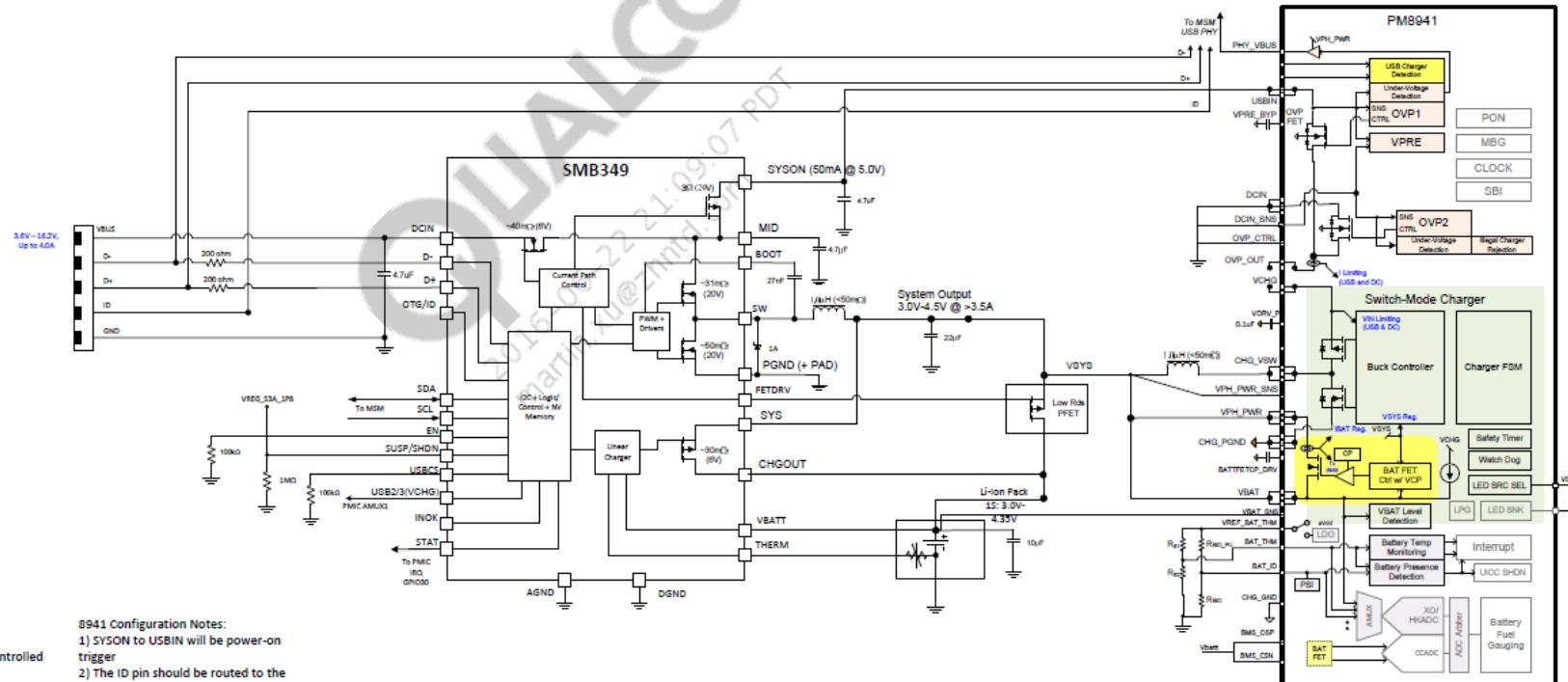
- SMB349 performs battery charging.
- PM8941 BMS is used for fuel gauging.



# Design Example: SMB349 + PM8941 Charging (2 of 3)

Single path charging:

- SMB349 performs battery charging.
- PM8941 BMS is not used for fuel gauging (external fuel gauge must be used which is not included below).



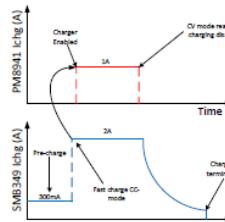
# Design Example: SMB349 + PM8941 Charging (3 of 3)

## Parallel path charging:

- SMB349 is primary charger and PM8941 is secondary.
- PM8941 BMS is not used for fuel gauging (external fuel gauge needs to be used which is not included below).

### Charging Operation:

- 1) The SMB349 will be used as the primary charger and will be enabled by default.
- 2) The PM8941 charger will only be enabled if the BC1.2 detection result is a DCP, the SMB349 AICL does not trip before 2A, and the SMB349 is in CC-mode charging.
- 3) The SMB349 will indicate CC-mode via the STAT pin I<sub>Q</sub>.
- 4) The PM8941 CV threshold will be set ~50mV below the SMB349 CV threshold. Once the PM8941 charger reaches CV-mode, it will be disabled.
- 5) The SMB349 will solely perform CV charging and termination.



### OTG Operation:

- 1) The SMB349 will provide OTG regulation.
- 2) Enabling OTG on the SMB349 will force INOK high and disable the Vbus connection to the PM8941.

### Input Current Limit:

- 1) The SMB349 will be set to 500mA, and the PM8941 will be disconnected by default until the SMB349 completes BC1.2 detection, turns on the switcher, and asserts INOK low.
- 2) If the MSM USB\_PHY detects a DCP, then the SMB349 will be set to HC mode with AICL enabled and a 2A input current limit.

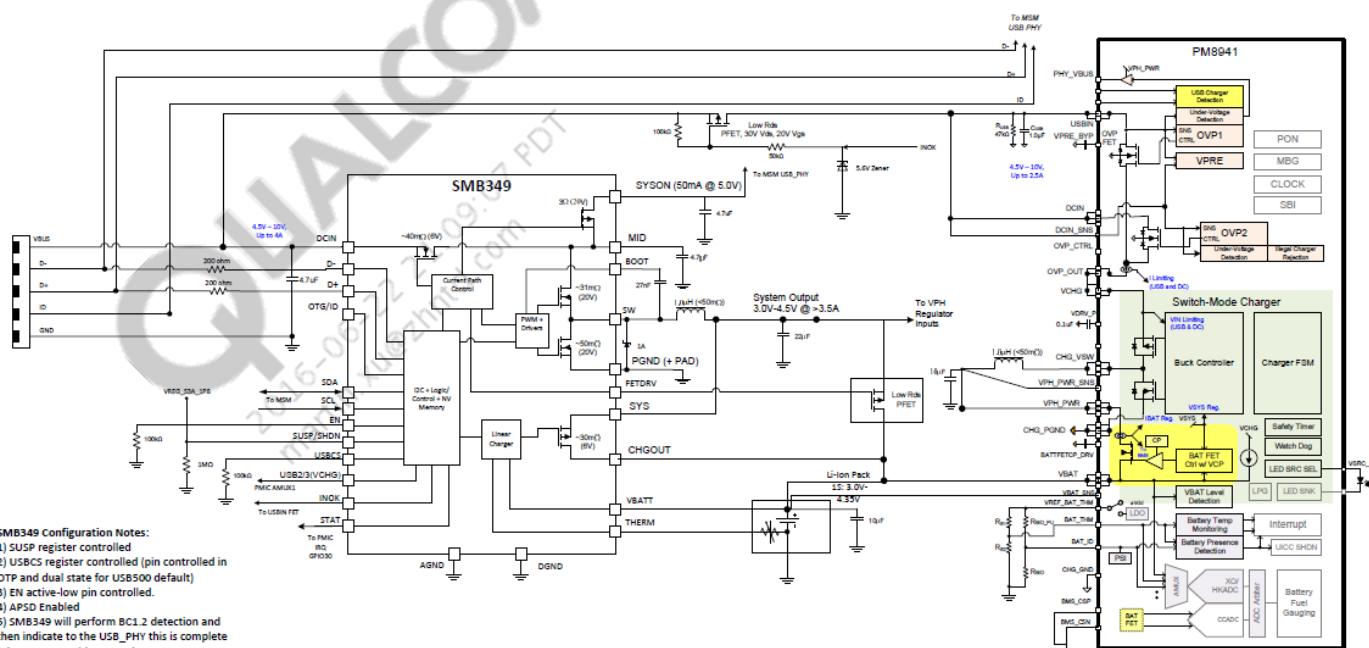
- 3) After a DCP is detected, and the SMB349 AICL does not trip before 2A, then the PM8941 will be enabled during CC charging with a 1A input current limit.
- 4) The PM8941 AICL threshold will be set higher than the SMB349, so it trips first and limits the input current through the PM8941 but not the SMB349.

**PM8941 Configuration Notes:**

- 1) USBIN will be power-on trigger, controlled by INOK of the SMB349.
- 2) Only the USBIN input will be used to take advantage of 30V OVP.
- 3) The ID pin should be routed to the PMIC and then to the MSM.
- 4) APSD Enabled.
- 5) SMB349 will perform BC1.2 detection and then indicate to the USB\_PHY this is complete (ok to power-on) by powering on SYSON after SMB349 SYSON pin goes high.
- 6) External BMS will be used.

**SMB349 Configuration Notes:**

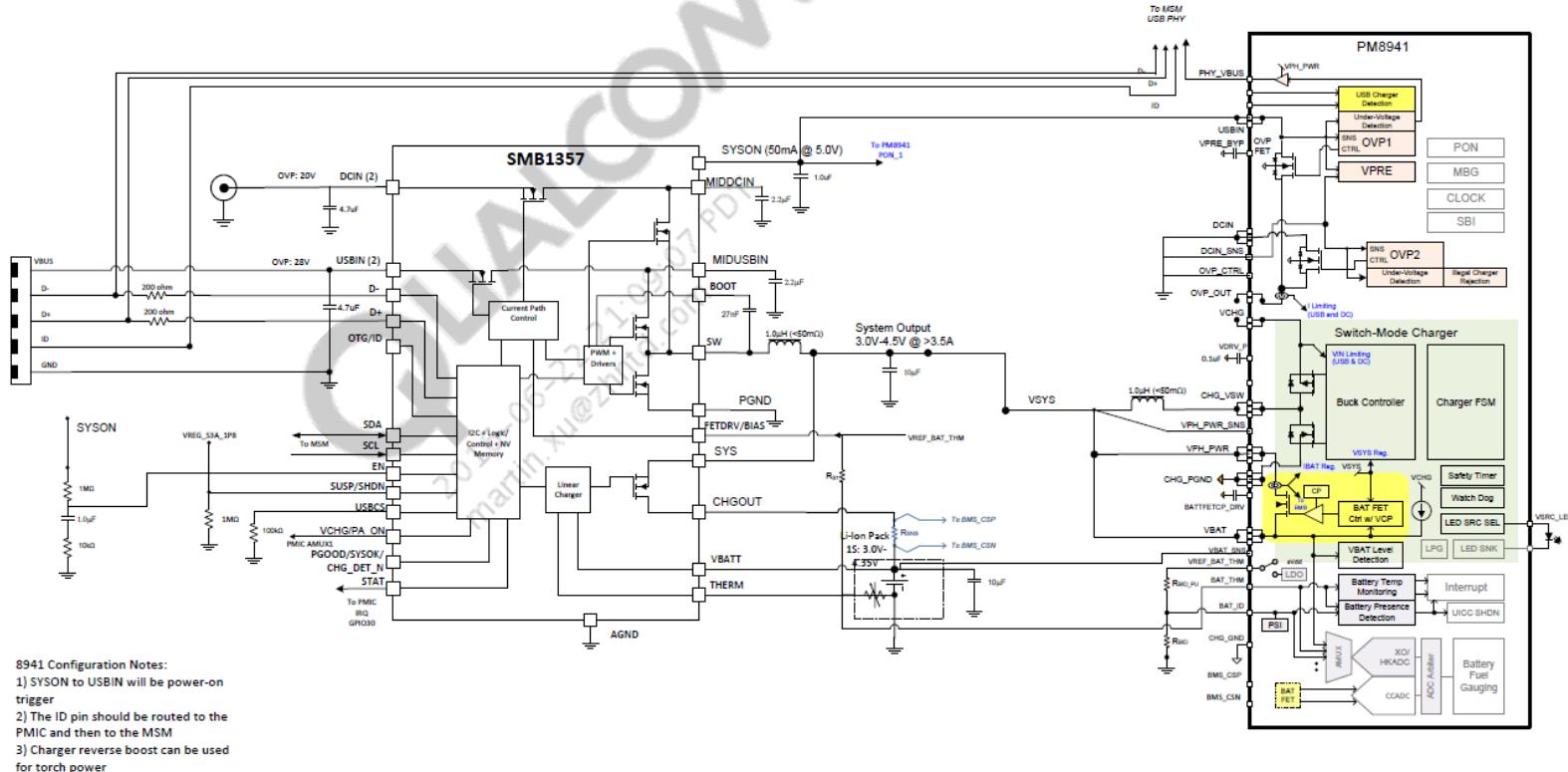
- 1) SUSP register controlled.
- 2) USBCS register controlled (pin controlled in OTP and dual state for USB500 default).
- 3) The EN pin should be routed to the PMIC and then to the MSM.
- 4) Charger reverse boost will be used for flash/torch power.
- 5) MSM USB\_PHY will perform BC1.2 detection after SMB349 SYSON pin goes high.
- 6) External BMS will be used.



# Design Example: SMB1357 + PM8941 Charging (1 of 2)

Single path charging:

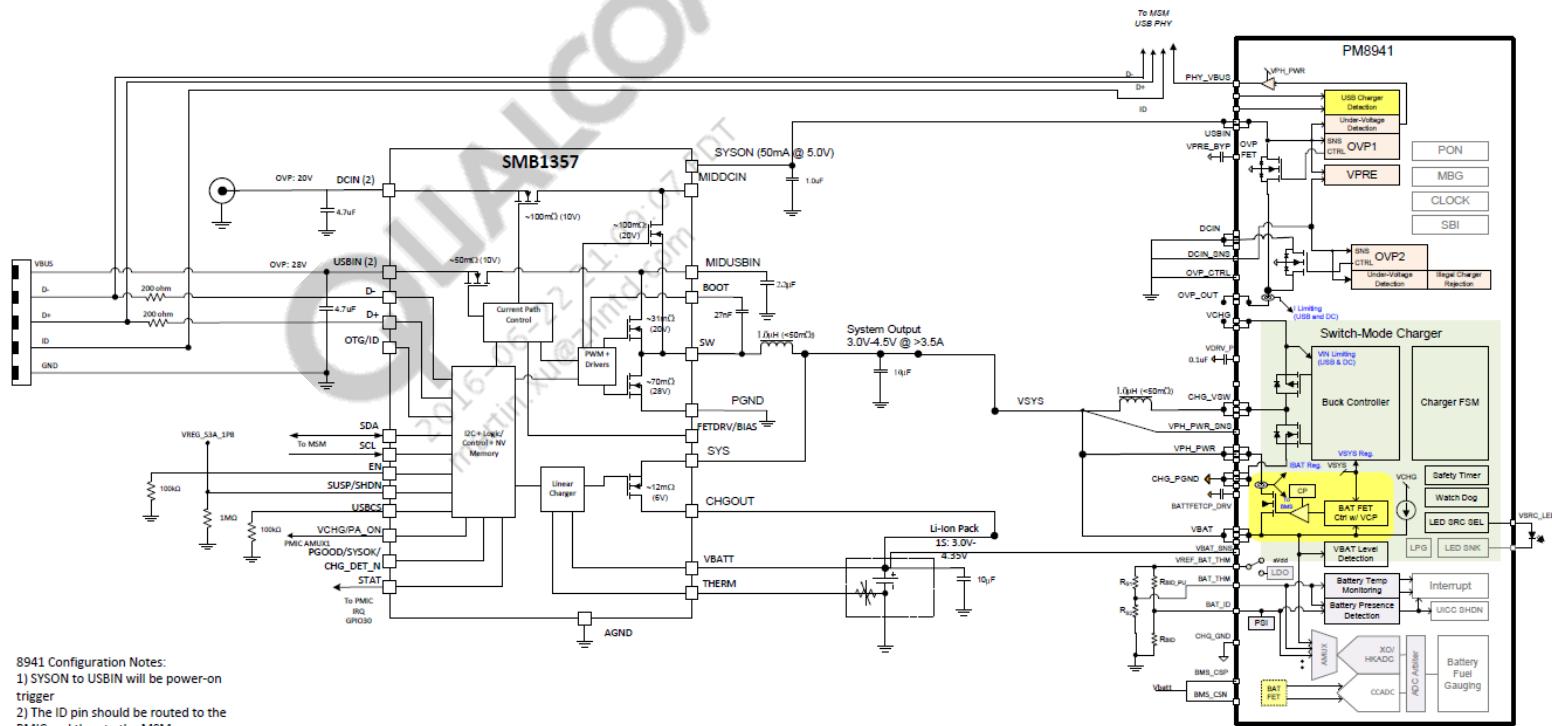
- SMB1357 performs battery charging.
- PM8941 BMS is used for fuel gauging.



# Design Example: SMB1357 + PM8941 Charging (2 of 2)

Single path charging:

- SMB1357 performs battery charging.
- PM8941 BMS is not used for fuel gauging (external fuel gauge needs to be used which is not included below).

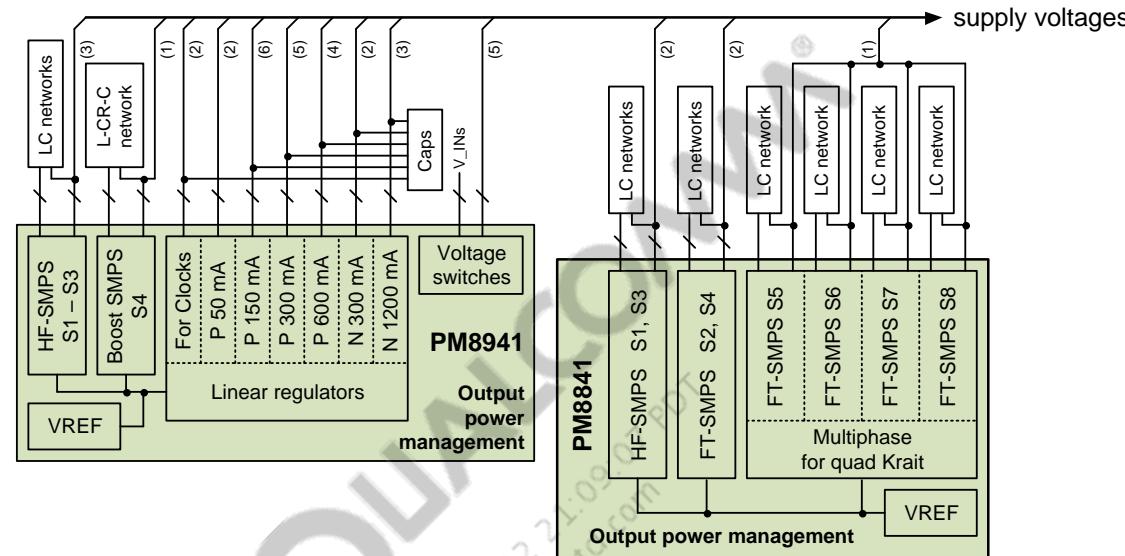




## Section 4

# Output Power Management

# Output Power Management Content



- Summary of OPM function
- MSM8974 power grid
- Buck vs. buck/LDO
- HF-SMPS circuits
  - Operation
  - Efficiency plot
  - Schematic and layout
- Multi-phase FT-SMPS circuits
  - Qualcomm® Krait™ power delivery
  - Bimodal functional modes
  - Schematic and layout
- Boost SMPS circuits
  - Operation
  - Schematic and layout
- SMPS switching loops and components
- Low dropout (LDO) linear regulators
  - Pseudo-capless LDOs
  - Regulator low-power modes
  - Internal regulator connections
  - External regulator connections and subregulation
  - Voltage switches
  - Need for external boost bypass

# Output Power Management – Summary (1 of 3)

PM8941 page 1 of 2

Function	Circuit type	Default voltage (V) <sup>8</sup>	Specified range (V)	Programmable range (V)	Rated current (mA)	Default on <sup>8</sup>	Expected use
S1	HF-SMPS	1.300	1.200–1.500	0.375–3.050	2000	Y	Source for L1 and L3, L4 and L11; external connections
S2	HF-SMPS	2.150	1.800–2.300	0.375–3.050	1000	Y	WCD plus source for L5 and L7, L6 and L12 and L14 and L15; external connections
S3 <sup>1</sup>	HF-SMPS	1.800	1.750–1.850	0.375–3.050	2000	Y	Modem IC pad group 3, option 4 and 7; L2 and LVS; chipset and other I/Os
S4 or '5V <sup>2</sup>	Boost SMPS	5.000	4.500–5.200	4.000–5.500	1300	—	WCD spkr driver and source for 5VS1, 5VS2; option for kypd, RGB drivers
L1	NMOS LDO	1.225	1.200–1.250	0.750–1.525	1200	Y	Modem IC pad group 1, option 4, and 7; DDR memory; eMMC
L2	NMOS LDO	1.200	1.100–1.450	0.750–1.525	300	—	MIPI_DSI - analog
L3	NMOS LDO	1.200	1.100–1.450	0.750–1.525	300	—	MIPI_CSI
L4	NMOS LDO	1.200	1.150–1.400	0.750–1.525	1200	—	RFIC low-V; modem IC analog low-V
L5 <sup>3</sup>	Low noise LDO	1.740	1.700–2.200	—	On-chip only	—	PMIC low noise XO buffers
L6 <sup>4</sup>	PMOS LDO	1.800	1.700–1.900	1.500 - 4.900	150	Y	USB; WCN XO; PMIC low power XO output buffers
L7 <sup>3</sup>	Low noise LDO	1.740	1.700–2.200	—	On-chip only	Y	PMIC XO circuits
L8 <sup>4,5</sup>	PMOS LDO	1.800	1.700–1.900	1.500 - 4.900	50	Y	PMIC HKADC
L9	PMOS LDO	1.800	1.700–3.050	1.500 - 4.900	150	—	Modem IC pad group 5, dual-voltage UIM1 (1.8 / 2.95 V)
L10	PMOS LDO	1.800	1.700–3.050	1.500 - 4.900	150	—	Modem IC pad group 6, dual-voltage UIM2 (1.8 / 2.95 V)
L11	NMOS LDO	1.225	1.200–1.400	0.750–1.525	1200	—	WCN; modem IC ADC/DAC
L12	PMOS LDO	1.800	1.700–1.900	1.500 - 4.900	300	Y	Modem IC PLLs, MIPI_DSI, MIPI_CSI, HDMI, EDP; MIPI_DSI I/Os
L13 <sup>6</sup>	PMOS LDO	2.950	2.750–3.000	1.500 - 4.900	150	Y	Modem IC pad group 2
L14	PMOS LDO	1.900	1.700–2.100	1.500 - 4.900	150	—	Modem IC analog - high V
L15	PMOS LDO	2.050	2.000–2.100	1.500 - 4.900	600	—	RFICs - low voltage
L16	PMOS LDO	2.750	2.600–3.000	1.500 - 4.900	150	—	Qualcomm front-end, RF switches, GPS LNA
L17	PMOS LDO	2.800	2.700–3.000	1.500 - 4.900	300	—	3D cameras - analog

# Output Power Management – Summary (2 of 3)

## PM8941 page 2 of 2

Function	Circuit type	Default voltage (V) <sup>8</sup>	Specified range (V)	Programmable range (V)	Rated current (mA)	Default on <sup>8</sup>	Expected use
L18	PMOS LDO	2.850	2.400–3.300	1.500 - 4.900	300	–	Sensors; touchscreen
L19	PMOS LDO	2.900	2.600–3.300	1.500 - 4.900	600	–	WCN
L20 <sup>7</sup>	PMOS LDO	2.950	2.750–3.000	1.500 - 4.900	600	Y	eMMC memory
L21 <sup>7</sup>	PMOS LDO	2.950	2.750–3.000	1.500 - 4.900	600	Y	SD/MMC card
L22	PMOS LDO	3.000	2.600–3.300	1.500 - 4.900	300	–	MIPI_DSI1
L23	PMOS LDO	3.000	2.600–3.300	1.500 - 4.900	300	–	MIPI_DSI2 or MIPI_CSI
L24	PMOS LDO	3.075	3.000–3.300	1.500 - 4.900	50	Y	HS-USB high-voltage
LVS1	Low V switch	1.800	–	–	300	–	Sensors; touchscreen
LVS2	Low V switch	1.800	–	–	300	–	Available
LVS3	Low V switch	1.800	–	–	300	–	3D cameras
5VS1	5 V switch	5.000	–	–	500	–	USB-OTG
5VS2	5 V switch	5.000	–	–	55	–	HDMI

1) S3 powers internal circuitry, and must be kept at its default setting.

2) Rated current for S4, the 5 V boost circuit, depends on the input voltage: 1.3 A for VDD = 3 V to 4.5 V and 600 mA for VDD = 2.5 V to 3 V.

3) VREG\_L5 (VREG\_RF\_CLK) and VREG\_L7 (VREG\_XO) power RF buffers and XO circuits respectively and must be kept at their default settings.

4) L6 and L8 power internal circuits that are limited to 1.8 V operation; they should not exceed the maximum stated in their programmable ranges. L6 is used as the internal dVdd source after power-up; its programmed voltage should not be changed, and it should not be turned off.

5) L8 is controlled by BMS during poweron.

6) L13 has been characterized at 1.8 V and meets all specifications at rated load current.

7) L20 and L21 have been characterized for 800 mA peak current capability. These regulators meet all the specifications at 800 mA except a.) Overshoot due to load transients (100 mV overshoot observed), and b.) Load regulation at high temperature, low voltage (at VBAT = 3 V and 90°C, load regulation is about 0.68% for normal power mode).

8) All regulators have output voltage default settings. Default voltage and poweron state depends on PBS configurations.

# Output Power Management – Summary (3 of 3)

## PM8841 page 1 of 1

Function	Circuit type	Default voltage (V) <sup>1</sup>	Specified range (V) <sup>2</sup>	Programmable range (V)	Rated current (mA) <sup>3</sup>	Default on	Expected use
S1 <sup>4</sup>	HF-SMPS	0.950	0.675–1.050	0.375–3.050	2000	Y	Modem IC memory and PLLs
S2	FT-SMPS	0.900	0.500–1.050	0.350–2.250	3000	Y	Modem IC core, SDC, and USB
S3 <sup>5</sup>	HF-SMPS	0.900	0.500–1.050	0.375–3.050	1000	–	Modem IC modem system
S4	FT-SMPS	0.900	0.500–1.050	0.350–2.250	3000	–	Modem IC graphics
S5	FT-SMPS	0.900	0.500–1.050	0.350–2.250	3000	Y	Modem IC quad Krait microprocessors
S6	FT-SMPS	0.900	0.500–1.050	0.350–2.250	3000	–	
S7	FT-SMPS	0.900	0.500–1.050	0.350–2.250	3000	–	
S8	FT-SMPS	0.900	0.500–1.050	0.350–2.250	3000	–	

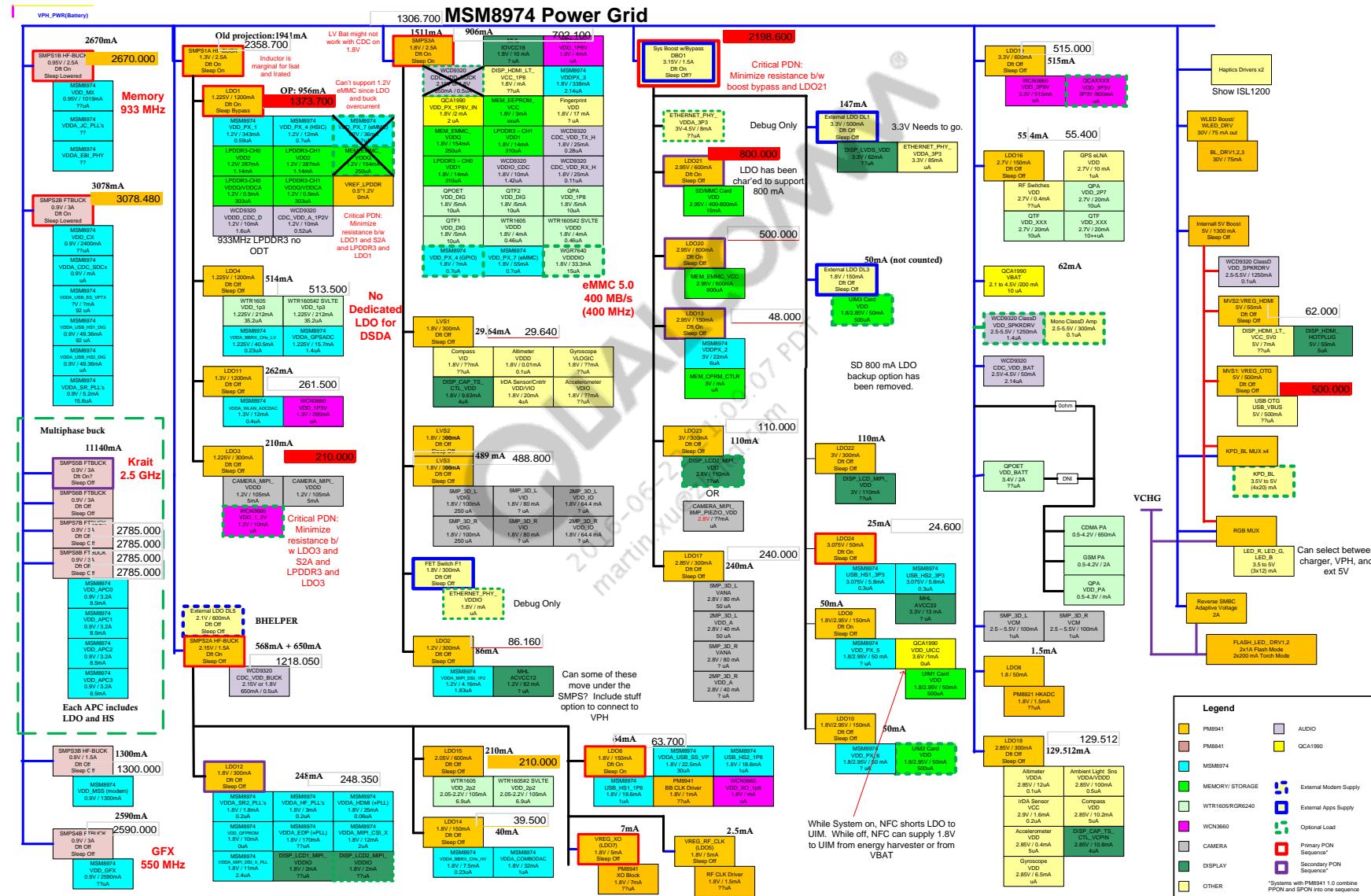
1) All regulators have output voltage default settings. The default voltage and poweron state depends on the PBS configurations.

2) The specified range corresponds to the range where performance is tested.

3) Rated current is the maximum current for which specification compliance is guaranteed unless otherwise stated.

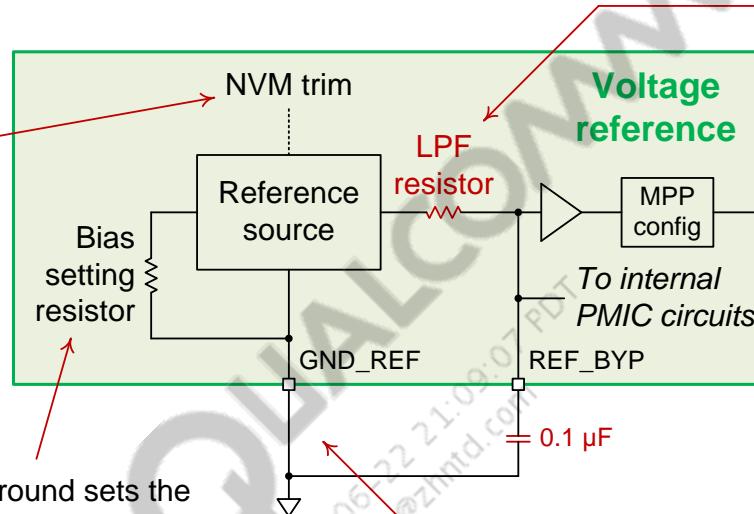
4) S1 has been specifically characterized for peak current capability up to 2500 mA. It meets all performance specifications at this load current.

# MSM8974 Power Grid



# Voltage Reference

The reference voltage is trimmed in final IC test and the optimal setting is permanently stored in nonvolatile memory (NVM).



An internal shunt resistor to ground sets the reference circuit's bias current.

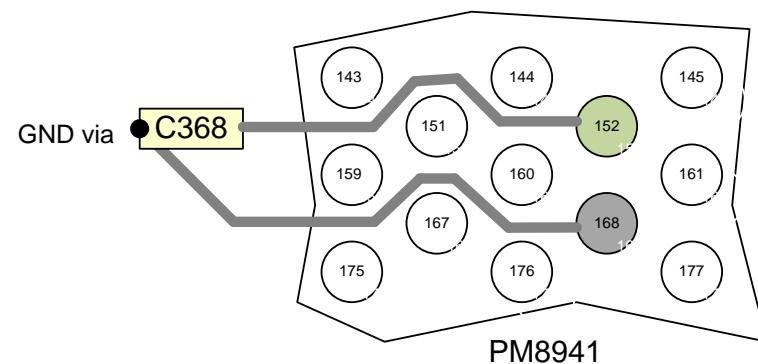
The on-chip series resistor supplements off-chip  $0.1 \mu\text{F}$  ceramic capacitor at the REF\_BYP pin to lowpass-filter the reference voltage that is distributed throughout the device.

any MPP

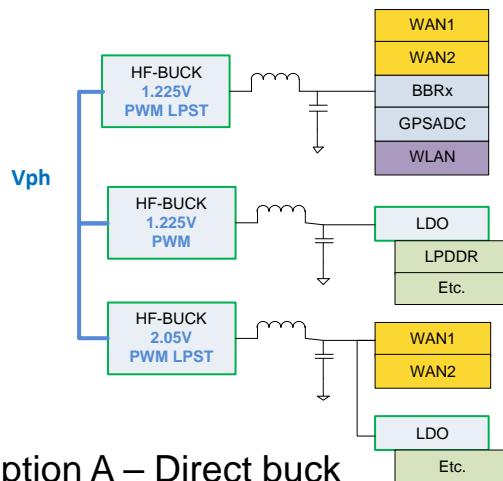
The internal VREF node is buffered and available as an output via correctly configured MPPs.

This circuit's ground is brought off-chip at GND\_REF. This ground is isolated from others until they converge on the main ground plane.

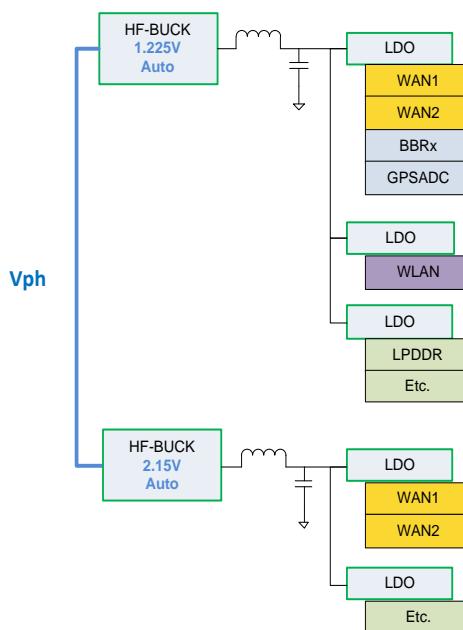
- 1) Locate the capacitor near PMIC pin REF\_BYP.
- 2) Use short, direct traces between the PMIC and capacitor.
- 3) The capacitor and PMIC circuits must be referenced to the same 0 V ground (GND\_REF pin). Ground via
- 4) Keep GND\_REF separate from all other grounds except where it vias to the PCB ground plane. The via to ground could be placed near PMIC pin or at the capacitor.



# Bucks vs. Buck/LDO – Example Analysis



## Option B – LDO subregulation



Item	Option A	Option B	Comment
Bucks	+1	+0	
BOM	+1 Ind +10 mm <sup>2</sup>	+0	LC for additional buck
$I_{Bat\_Wasted}$ – GSMTalk (mA)	4.9	2	$I_{Load} = 30$ mA
$I_{Bat\_Wasted}$ - CDMA Talk (mA)	7.5	6.5	$I_{Load} = 100$ mA
$I_{Bat\_Wasted}$ - LTE (CAT2) (mA)	10.3	12.3	$I_{Load} = 200$ mA
$I_{Bat\_Wasted}$ - SV-LTE (mA)	14	17.3	$I_{Load} = 300$ mA
$I_{Bat\_Wasted}$ – GPS (mA)	3.8	1.3	$I_{Load} = 20$ mA
$I_{Bat\_Wasted}$ – WLAN (mA)	3.2	1.1	$I_{Load} = 15$ mA
Noise – GSM ( $mV_{RMS}$ )	0.25	0.35	BW: 0-100 kHz, $I_{Load} = 30$ mA
Noise - CDMA Talk ( $mV_{RMS}$ )	0.72	1.4	BW: 0-2 MHz, $I_{Load} = 100$ mA
Noise - LTE (CAT2) ( $mV_{RMS}$ )	3.1	2.1	BW: 0-10 MHz, $I_{Load} = 200$ mA
Noise - SV-LTE ( $mV_{RMS}$ )	3.2	2.4	BW: 0-10 MHz, $I_{Load} = 300$ mA
Noise – GPS ( $mV_{RMS}$ )			BW: 0-1 MHz, $I_{Load} = 20$ mA
Noise – WLAN ( $mV_{RMS}$ )	2.8	1	BW: 0-10 MHz, $I_{Load} = 15$ mA

- With a LDO subregulated RF, the system can work with a single 1.3 V buck instead of two. This results in reduction of die area, PWB area, and BOM cost.
- The LDO subregulation provides sufficient suppression of buck noise and spurs to allow running buck in auto mode. This results in significantly better buck efficiency below ~100–150 mA load current.
- Improving RF noise sensitivity and buck/LDO output noise can now be turned into power savings by reducing LDO headroom.
- Provides flexibility to tradeoff power and RF performance post silicon, reducing need for re-spin.
- $I_{bat}$  wasted based only on WAN loads.

## HF-SMPS – Operational Details

PM8941 and PM8841 have second-generation HF-SMPS (PM8921 had first-generation).

The second-generation HF-SMPS supports all features of the first-generation HF-SMPS:

- Better transient response
- Slow start feature
- Operating modes
  - ▣ Pulse width modulation (PWM)
    - Current-mode constant-frequency PWM control
    - Delivers the specified rated current to the load
    - Pulse skipping
  - ▣ Pulse frequency modulation (PFM)
    - The power switch is only turned on when the output voltage dips below a threshold.
    - Main advantage: maintains high efficiency even at light loads
  - ▣ Auto mode
    - Automatic switching between PFM and PWM modes, based upon load current
    - Programmable threshold

In addition, the second-generation HF-SMPS has improved auto-PFM/PWM operation:

- Reduced PFM ripple
- Reduced PFM/PWM transients
- Improved output stages
- Improved isolation and biasing

RF rails use subregulated LDOs to improve noise and efficiency

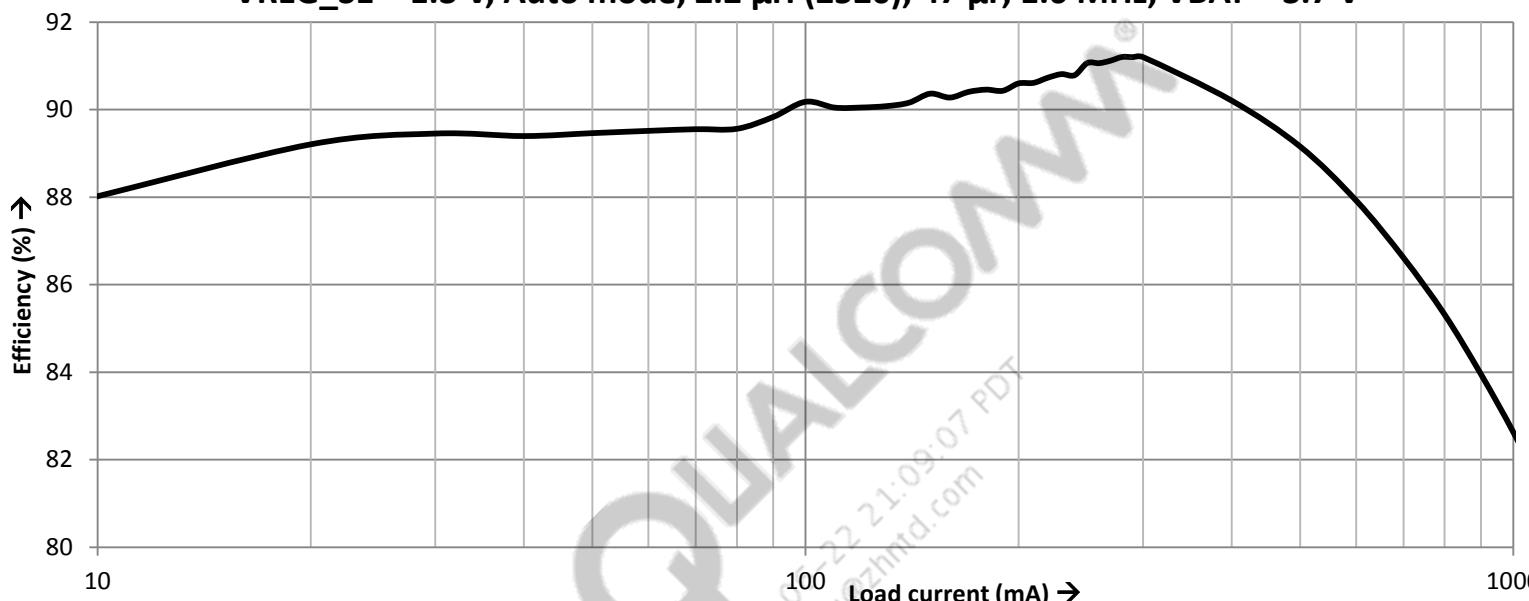
- Allows RF bucks to use auto-mode
- LDOs set for minimal headroom clean up any ripple

**Note:** All HF SMPS are turned ON in PWM mode during poweron and are configured in SBL for auto mode.

Refer to *Understanding High-frequency and Fast-transient Switched Mode Power Supplies Application Note* (80-VT310-124) for general details about SMPS operation.

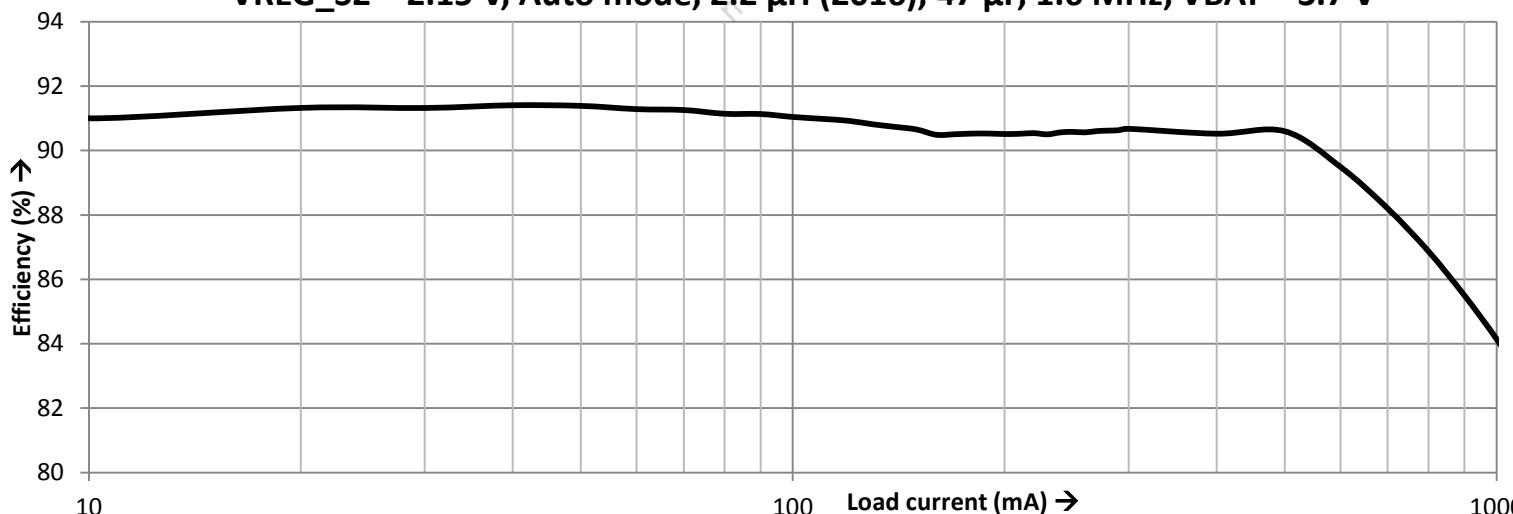
## HF-SMPS Efficiency Plots (1 of 3)

VREG\_S1 = 1.3 V, Auto mode, 2.2  $\mu$ H (2520), 47  $\mu$ F, 1.6 MHz, VBAT = 3.7 V



PM8941  
S1 buck

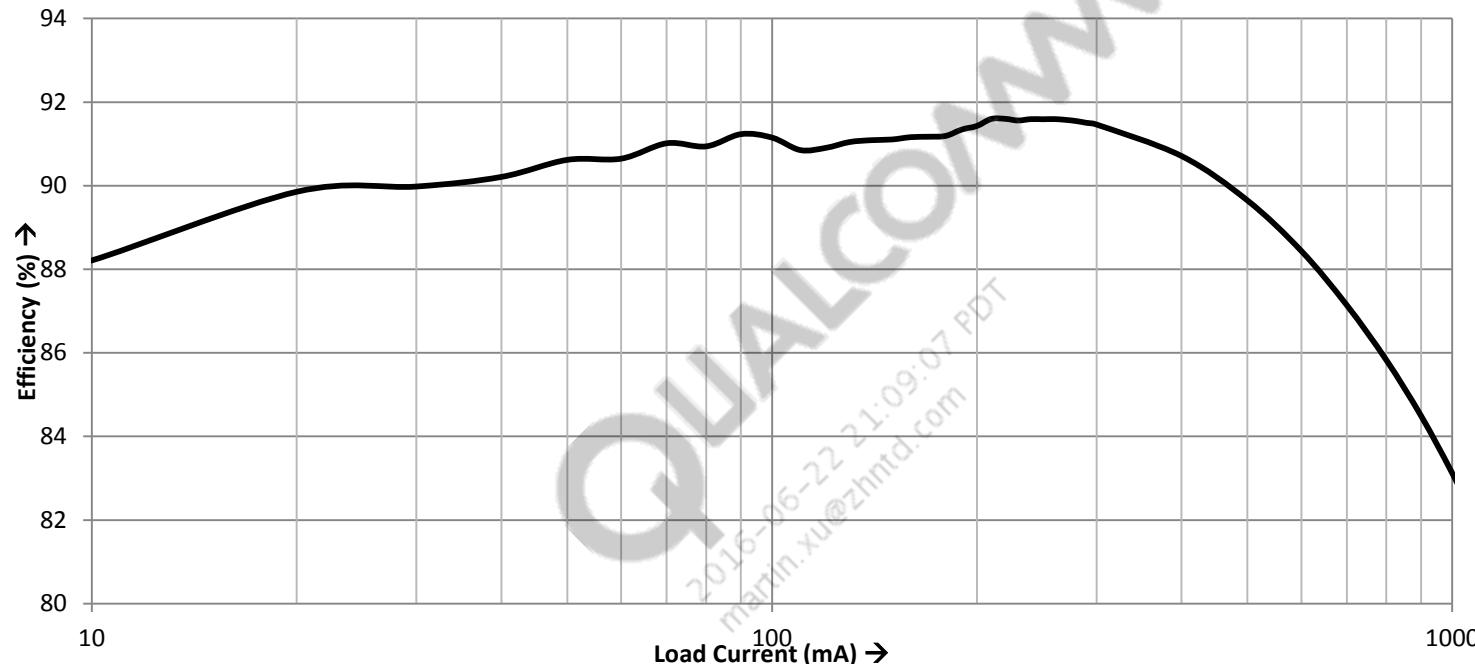
VREG\_S2 = 2.15 V, Auto mode, 2.2  $\mu$ H (2016), 47  $\mu$ F, 1.6 MHz, VBAT = 3.7 V



PM8941  
S2 buck

## HF-SMPS Efficiency Plots (2 of 3)

VREG\_S3 = 1.8 V, Auto mode, 2.2  $\mu$ H (2016), 47  $\mu$ F, 1.6 MHz, VBAT = 3.7 V



PM8941  
S3 buck

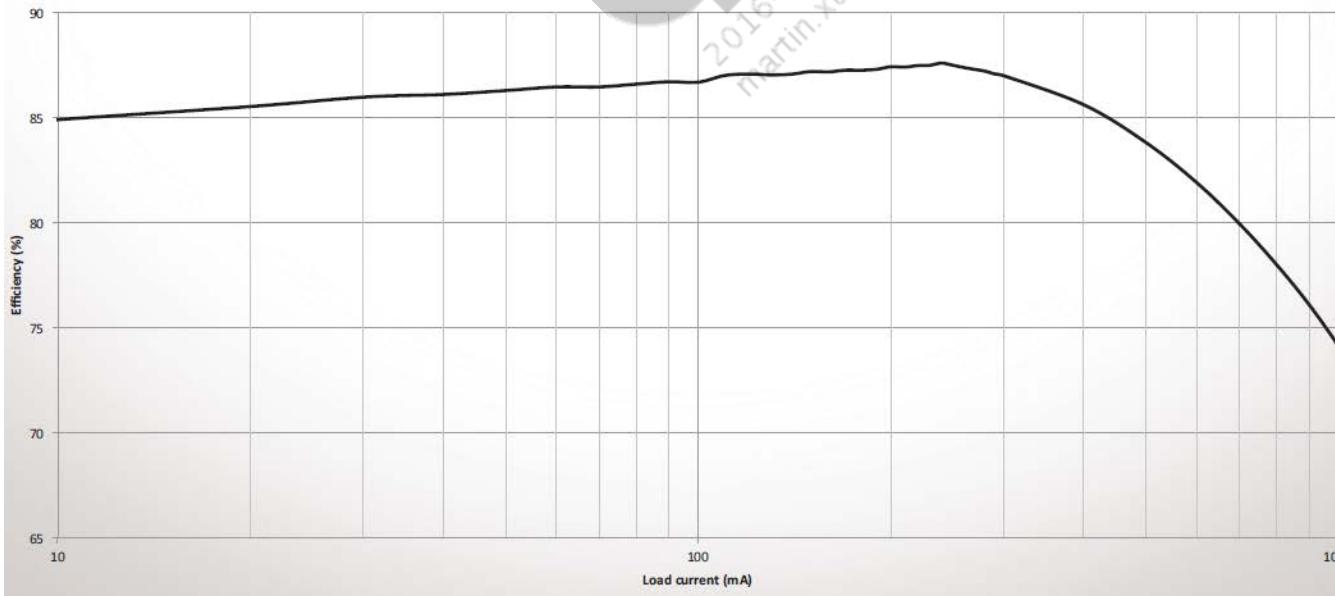
## HF-SMPS Efficiency Plots (3 of 3)

VREG\_S1B = 1.05 V, Auto mode, 0.47  $\mu$ H (2016), 2 x 47  $\mu$ F, 3.84 MHz, VBAT = 3.8 V



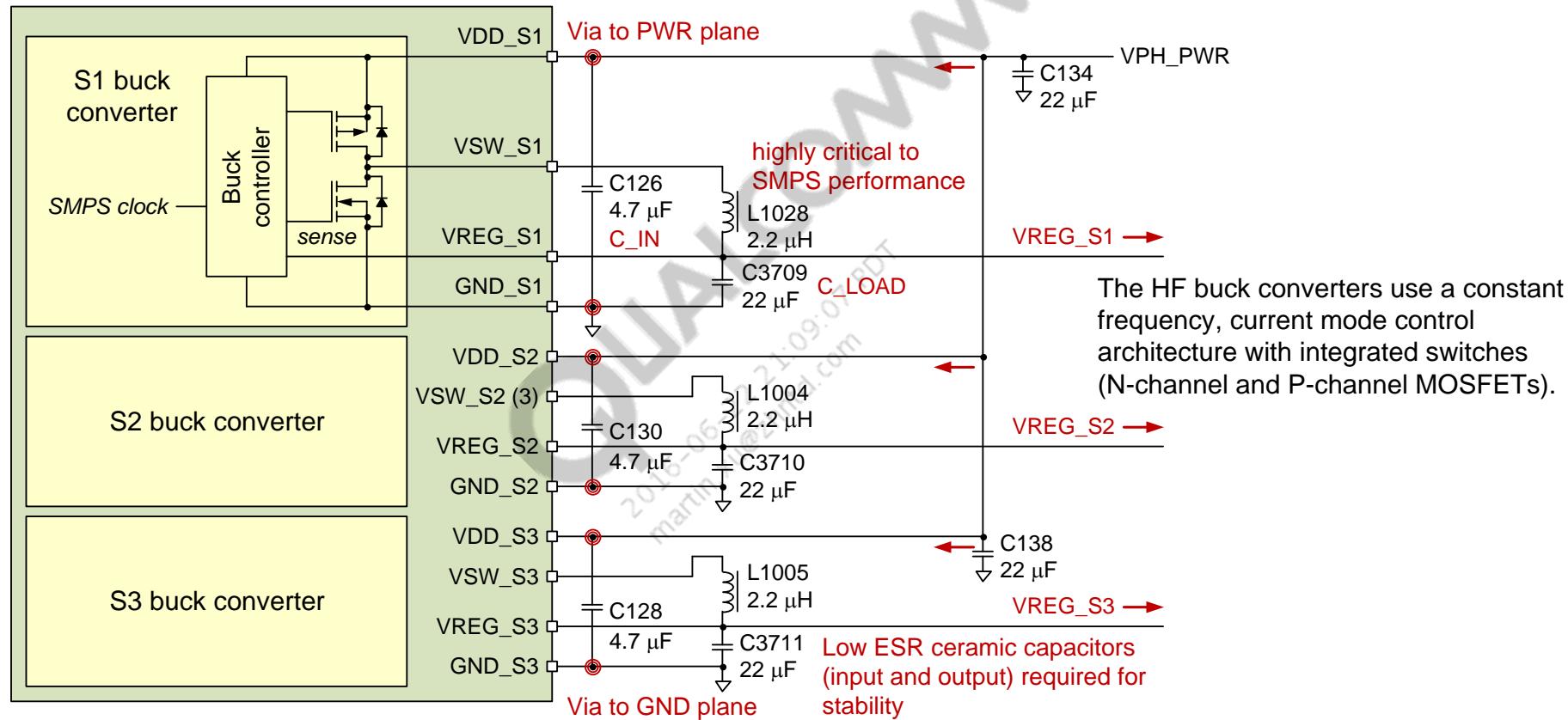
PM8841  
S1 buck

VREG\_S3B = 1.05 V, Auto mode, 2.2  $\mu$ H (2016), 47  $\mu$ F, 1.6 MHz, VBAT = 3.7 V



PM8841  
S3 buck

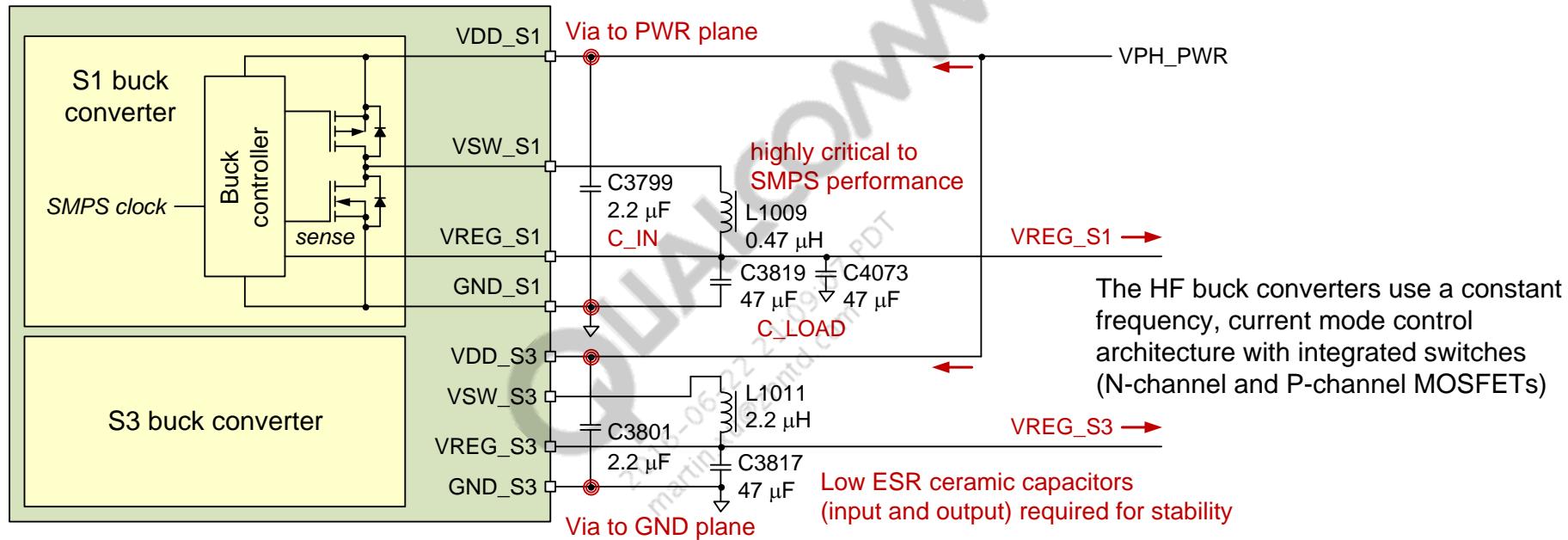
# Example PM8941 HF-SMPS Schematic



## Note:

Refer to the latest revision of the *MSM8274/MSM8274AB*, *MSM8674/MSM8674AB*, and *MSM8974/MSM8974AB Baseband Reference Schematic* (80-NA437-41) for the HF-SMPS schematic.

# Example PM8841 HF-SMPS Schematic



## Note:

Refer to the latest revision of the *MSM8274/MSM8274AB, MSM8674/MSM8674AB, and MSM8974/MSM8974AB Baseband Reference Schematic* (80-NA437-41) for the HF-SMPS schematic.

# PM8941 and PM8841 HF-SMPS – Layout Guidelines

## Placement:

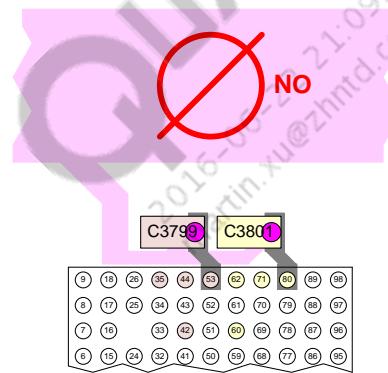
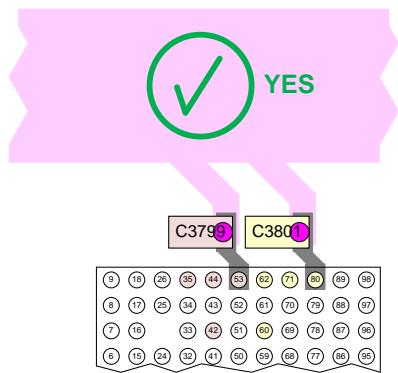
- Minimize switching loop. Place HF-SMPS input cap, output cap, and inductor close to each other.

## Grounding:

- Connect GND of HF-SMPS input caps, output cap, and GND\_Sx pins of PMIC together. Connect the common point directly to main GND.

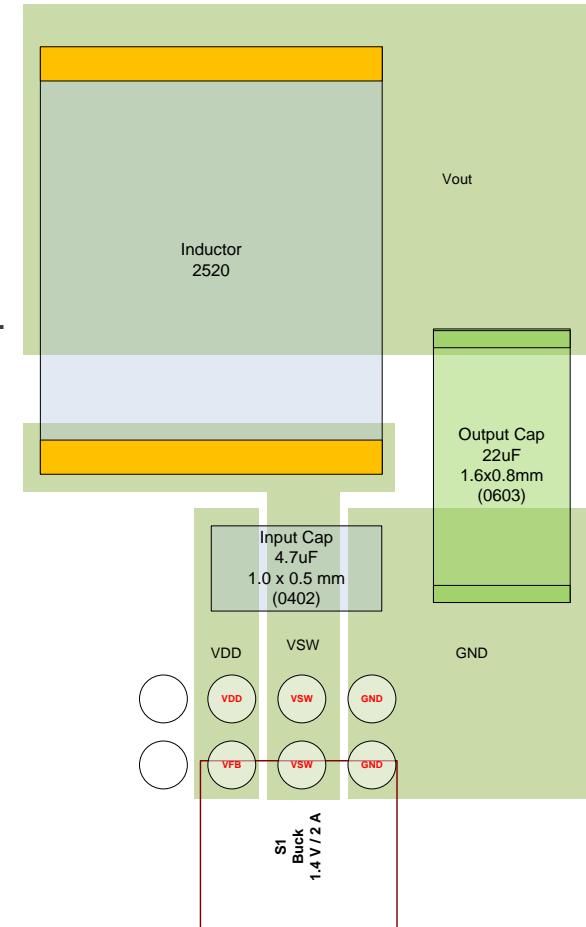
## High current paths:

- Use thick and short trace from VSW\_Sx pin to inductor.
- Use star routing from main power plane to VDD\_Sx pins as shown below.



## Sensing:

- Connect VREG\_Sx pin to output of the SMPS using a thin trace.

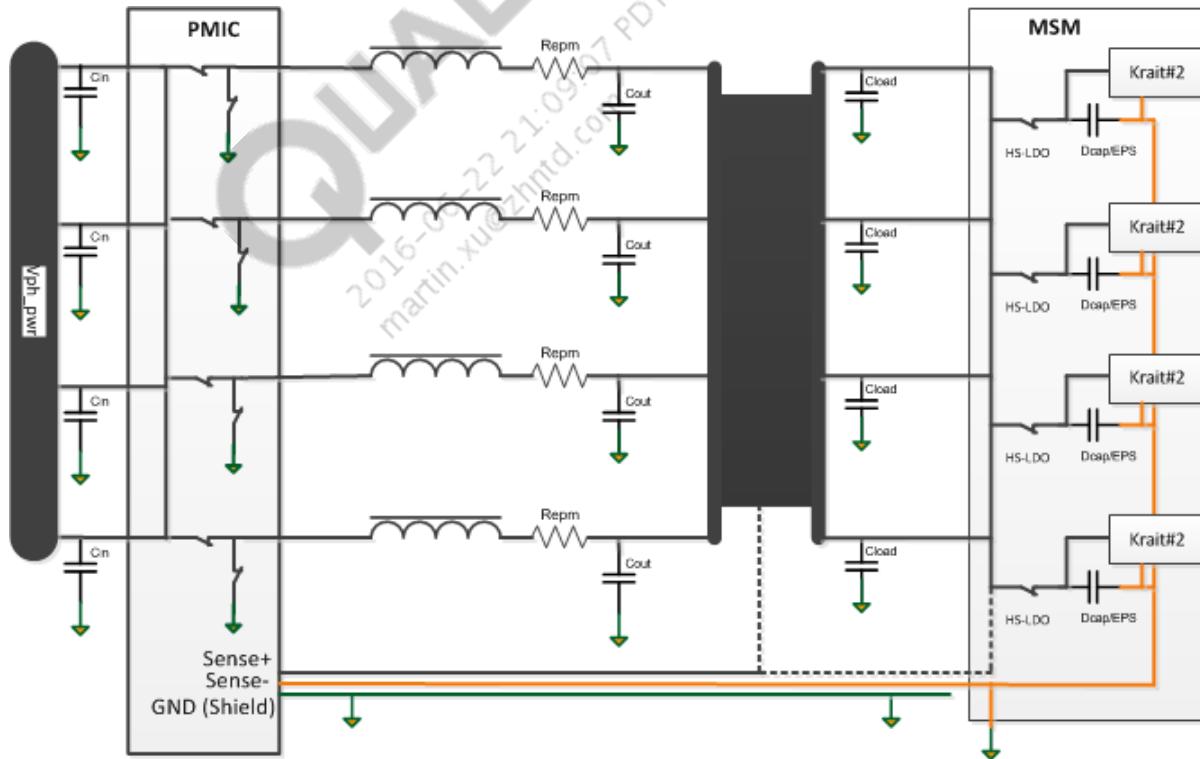


## Multiphase FT SMPS

PM8841 has a second-generation FT-SMPS that employs multiphase operation to extend efficiency on a wider load range.

FT SMPS S5 through S8 are ganged together to form the multiphase FT SMPS that power the application processors.

- Outputs of the FT SMPS are tied together.
- S5 is the gang leader; S6 through S8 follow S5.



## App Processor Bimodal Functional Modes Support

Single core mode: full DCVS (1.1 V–0.5 V)

- Maximum power efficiency

Multicore symmetric mode: full DCVS (1.1 V–0.5 V)

- Good power efficiency, could support running higher PMIC setpoint for same performance

Multicore asymmetric mode: HS (1.1 V–0.85 V) and LDO (0.75 V–0.5 V)

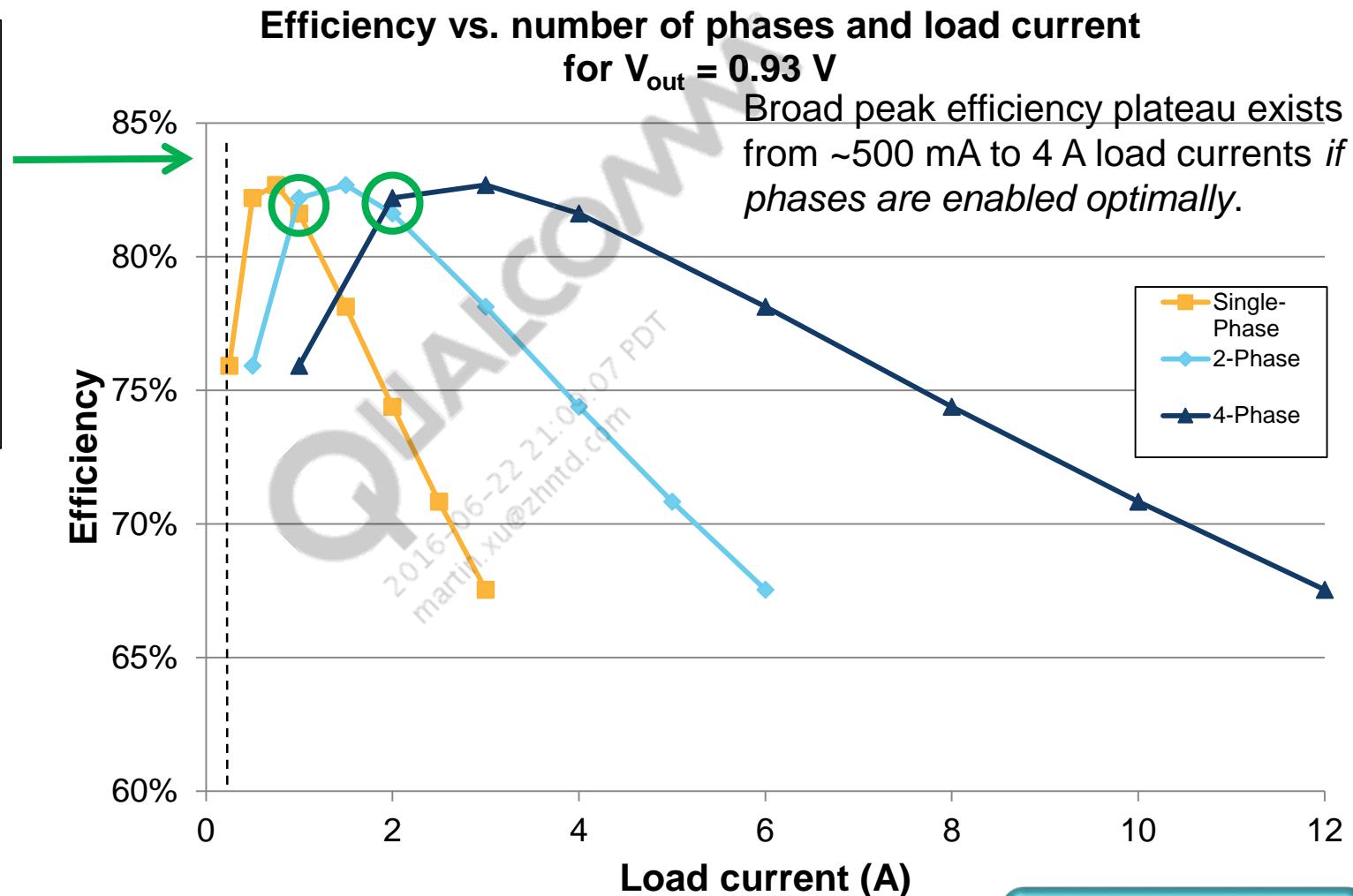
- PMIC DCVS through HS but limited to maximum setpoint of all core voltages
- Need software/hardware aggregation to maintain PMIC at the common mode maximum

### Note:

Refer to the *Understanding High-frequency and Fast-transient Switched Mode Power Supplies Application Note* (80-VT310-124) for general details about SMPS operation.

## Efficiency vs. Multiphases

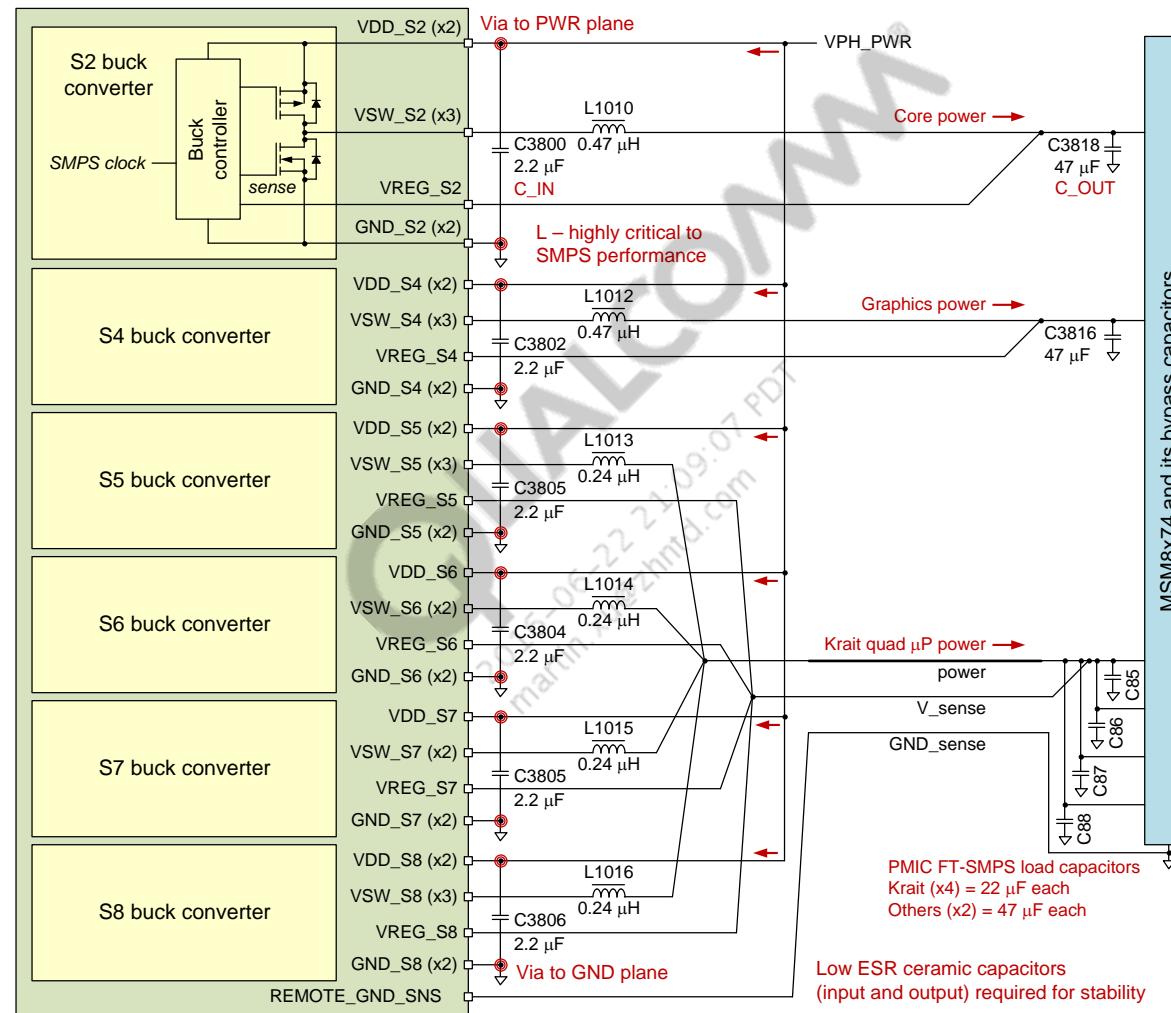
Optimum transition points are at 1 A from one to two phases and at 2 A from two to four phases.



**Note:** PFM (low current mode) not shown

Software selects the number of phases

# Example PM8841 FT-SMPS – Schematic



## Note:

Refer to the latest revision of the **MSM8274/MSM8274AB**, **MSM8674/MSM8674AB**, and **MSM8974/MSM8974AB** **Baseband Reference Schematic** (80-NA437-41) for the FT-SMPS schematic.

# PM8841 FT-SMPS – Layout Guidelines

## Placement:

- Place the SMPS output capacitor closer to the MSM device. This is required for reduced IR drops and best transient performance.
- Place SMPS input capacitor and inductor close to the PMIC.
- Place the bulk input capacitor closer to the PMIC.

## Grounding:

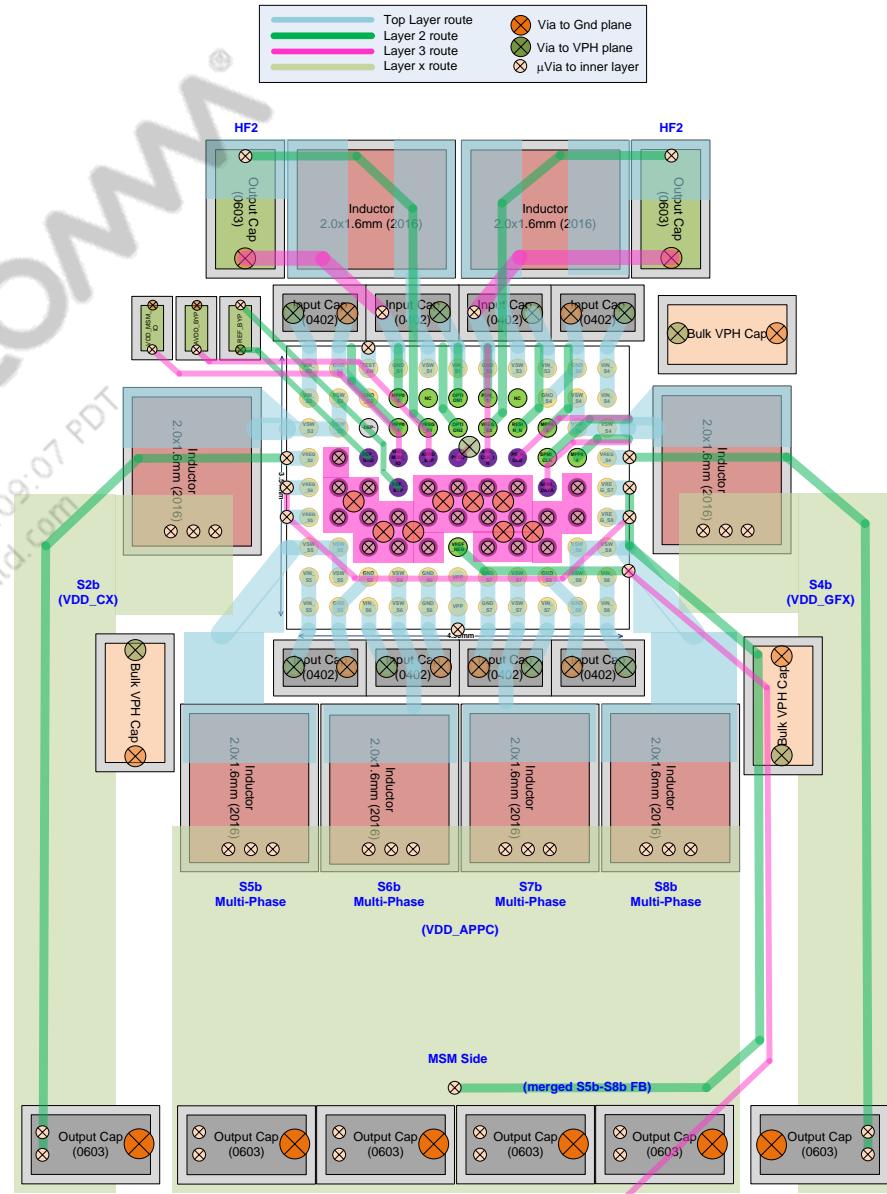
- Connect the GND of SMPS input capacitor and GND\_Sx pins of PMIC together. Connect the common point directly to the main GND.
- Connect GND of SMPS output capacitor directly to the main GND.
- Connect GND of the bulk input capacitor directly to the main GND.

## High current paths:

- For multiphase FT SMPS (S5-S8), ensure that all the inductors are connected together to the output capacitors via large area fill as shown in the adjacent figure.
- For S2, S4 FT SMPS, ensure that there is a thick trace from the inductor to output capacitor.

## Sensing:

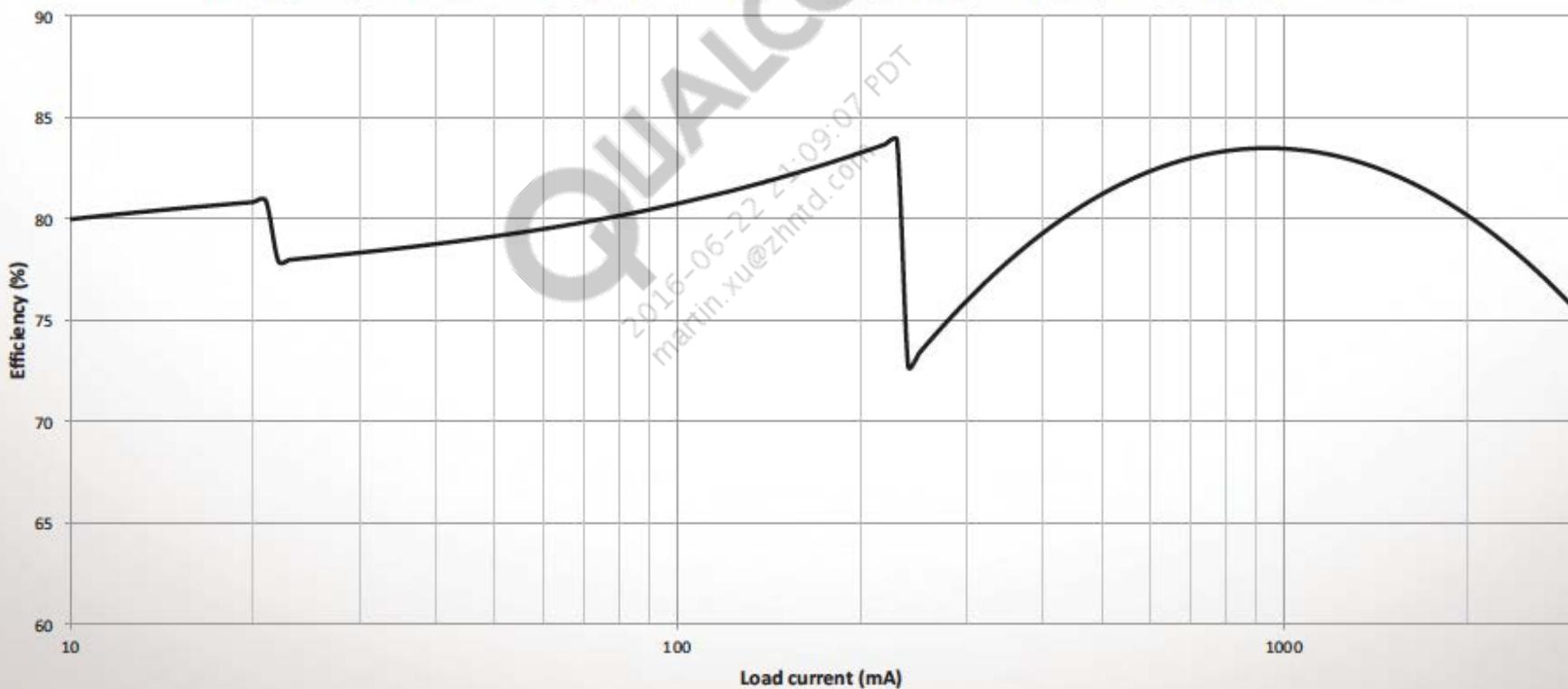
- Connect VREG\_Sx directly to remote output capacitors, as shown in adjacent figure.



# FT-SMPs Efficiency Plot

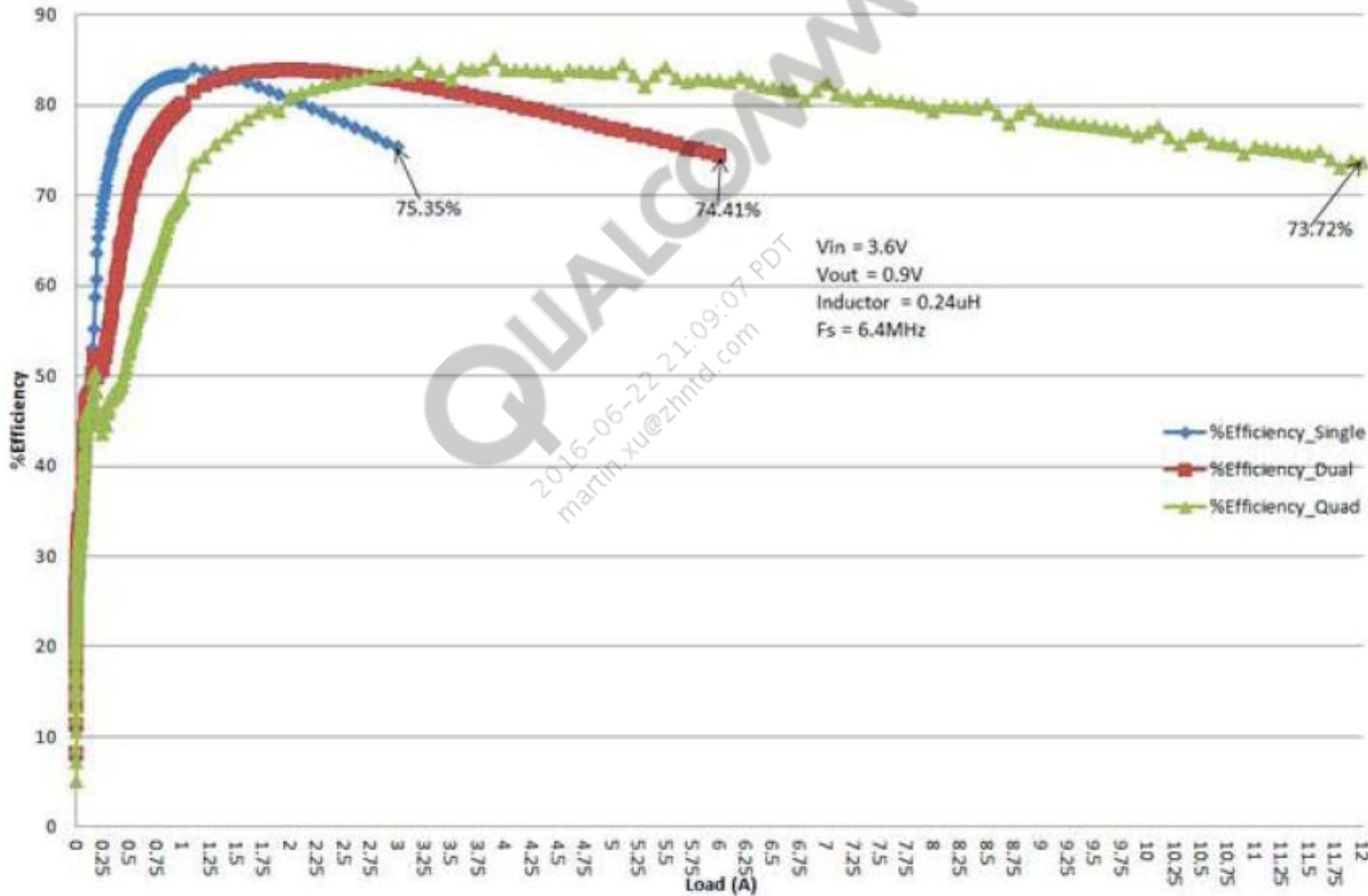
PM8841 S2/S4 buck

VREG\_S2B / VREG\_S4B = 1 V, Auto mode, 0.47  $\mu$ H (2016), 2 x 47  $\mu$ F, 6.4 MHz, VBAT = 3.7 V

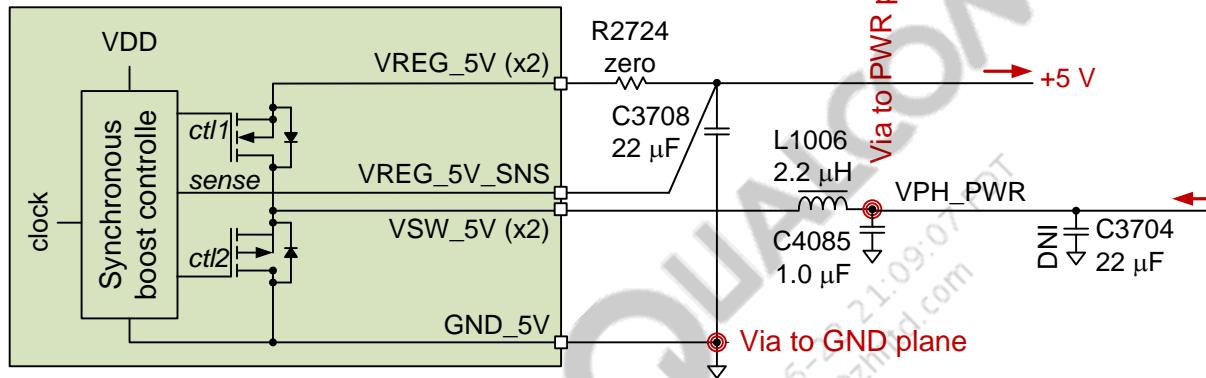


# Multiphase FT-SMPS Efficiency Plot

PM8841 S5 – S8 bucks



# PM8941 Synchronous Boost SMPS – Schematic and Layout Guidelines



L – highly critical to SMPS performance

Low ESR ceramic capacitors (input and output) required for stability

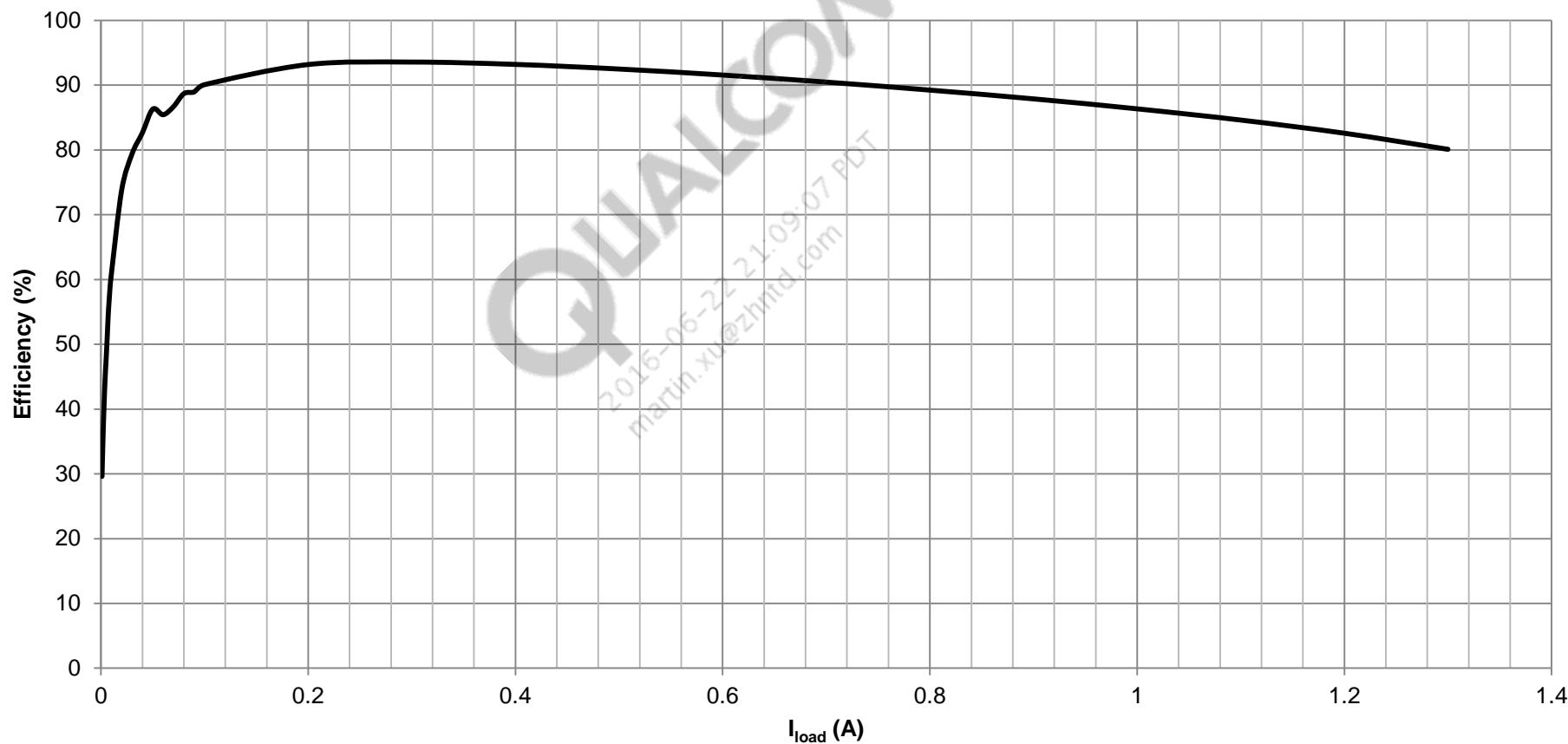
Earlier discussion of high-frequency switching loops also applies to the Boost SMPS.

Same placement and layout guidelines apply to the 5 V synchronous boost SMPS as HF SMPS. Example placement and layout can be seen in the top-level design topics section later in the slides.

# Synchronous Boost Efficiency Plot

PM8941 S4 boost

**VREG\_S4 = 5.1 V, 2.2  $\mu$ H (2016), 22  $\mu$ F, 1.6 MHz, VBAT = 3.6 V**



## SMPs Switching Frequencies

SMPS*	Type	L ( $\mu$ H)	F <sub>sw</sub> (MHz)
S1A	HF	2.2	1.6
S2A	HF	2.2	1.6
S3A	HF	2.2	1.6
S4A	HF	2.2	1.6
S1B	HF	0.47	3.84
S2B	FT	0.47	6.4
S3B	HF	2.2	1.6
S4B	FT	0.47	6.4
S5B – S8B	FT	0.24	6.4

\* A = PM8941, B = PM8841

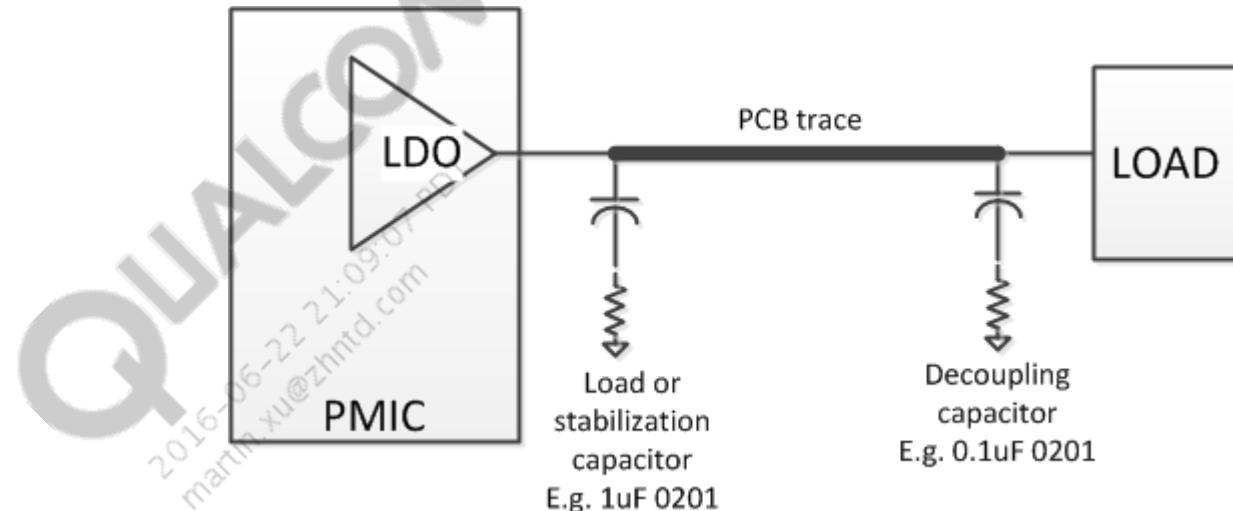
- The SMPS inductors are especially critical to performance, and should be selected in accordance with the guidelines given in *Switched-Mode Power Supply (SMPS) Inductor Selection Application Note* (80-VC603-9).
- Designers should select inductors that have the same or better specifications as the inductors used in the QTI reference designs.

## Low-dropout Linear Regulators – Pseudo-capless PMOS LDOs (1 of 2)

PM8941 eliminates the need to have load capacitor for certain PMOS LDOs. These LDOs are called the Pseudo-capless LDOs. These LDOs have been identified in the *MSM8274/MSM8274AB*, *MSM8674/MSM8674AB*, and *MSM8974/MSM8974AB Baseband Reference Schematic* (80-NA437-41), with DNI load capacitors.

Present situation:

- Load capacitor at LDO output
- Decoupling capacitor at load

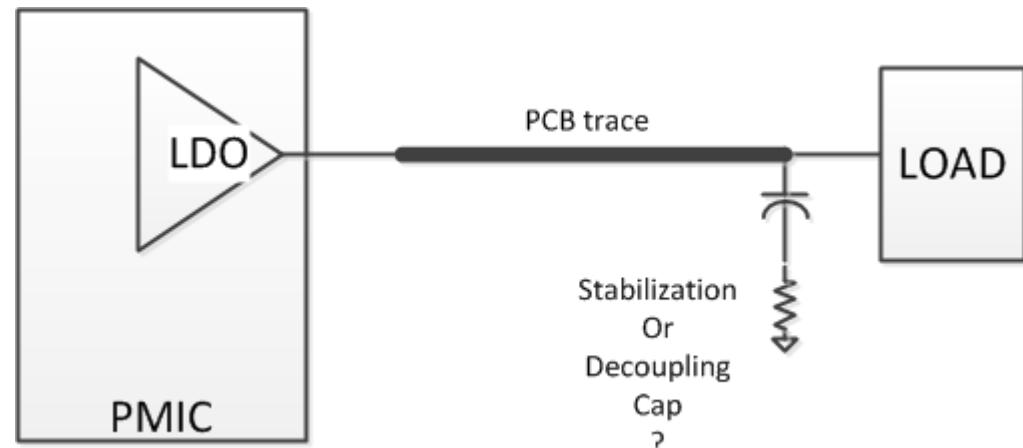


Want to eliminate the LDO load capacitor:

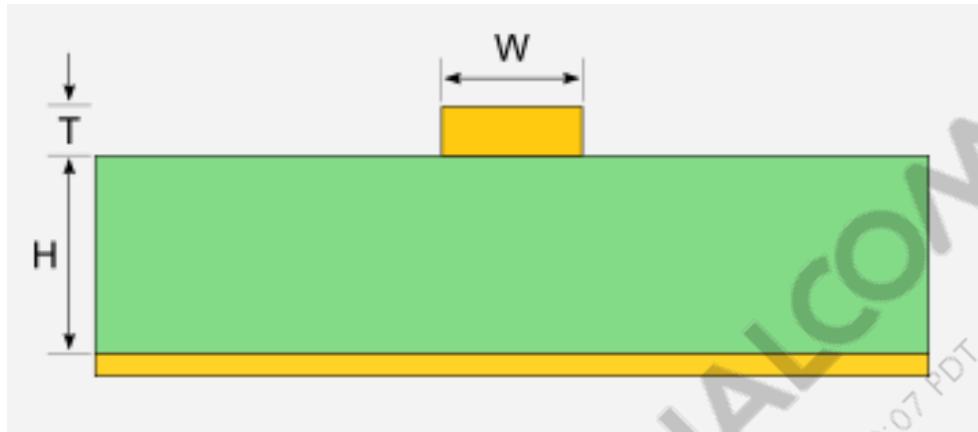
- Reduce BOM cost
- Reduce board area

### Note:

Refer to the *Understanding Low-dropout (LDO) Regulators Application Note* (80-VT310-125) for general details about LDO operation.



## Low-dropout Linear Regulators – Pseudo-capless PMOS LDOs (2 of 2)



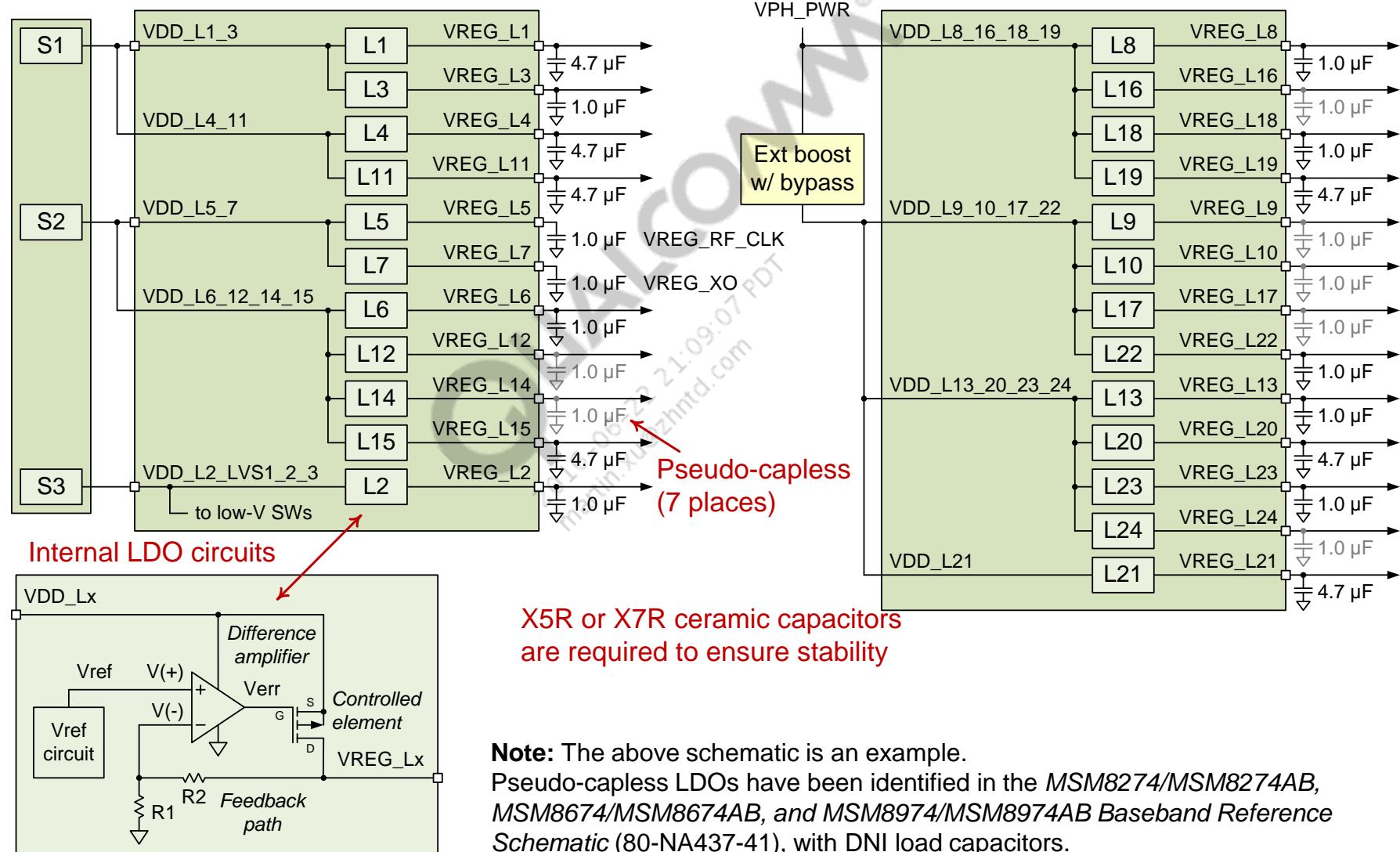
W = width of the trace  
L = length of the trace  
T = thickness of the trace  
H = height of the substrate

Rough guidelines – use worst case CAD extraction	W ( $\mu\text{m}$ )	H ( $\mu\text{m}$ )	T ( $\mu\text{m}$ )	L (cm)	Trace inductance (nH)	Trace resistance ( $\text{m}\Omega$ )
Long trace carrying 600 mA	1600	90	17	5	4.6	< 30
Long trace carrying 300 mA	1000	90	17	5	5.7	40
Long trace carrying 200 mA	800	90	17	5	7.05	60
Long trace carrying 100 mA	400	90	17	5	14.1	120
Long trace carrying 25 mA	100	90	17	5	56.5	480

### Recommendation:

For PMOS LDOs with load within 5 cm of the PMIC LDO pin, combine the PMIC load capacitor and load bypass capacitor, and place at the load.

# Example Low-dropout Linear Regulators – Schematic



# Low-dropout Linear Regulators – Layout Guidelines

## Pseudo-capless LDO

- The trace from LDO output pin to the load capacitor must meet the inductance and resistance requirements quoted in the previous slides.

## Other LDO

- The trace from LDO output pin to the output capacitor must have inductance and resistance less than 5 nH and 5 mΩ, respectively.

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martin.xu@zhntd.com

## Regulator Low-Power Modes

All SMPS and linear regulators, except for the RF\_CLK and XO LDOs (L5 and L7) and the 5 V synchronous boost, support low-power modes that reduce their quiescent currents. This is especially useful during the handset sleep mode, enabling maximum standby time. Different regulator types implement their low-power modes differently, as described below:

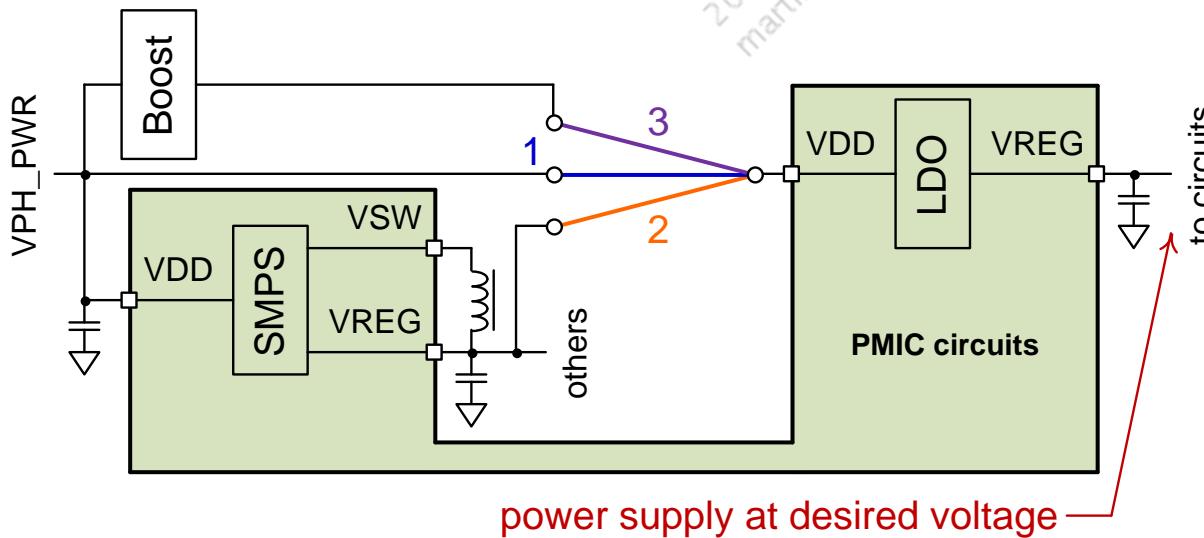
- Linear regulator: implements its low-power mode by reducing the current of its feedback loop. During low-power operation, the regulator performance is degraded – lower PSRR, less output current capability, etc. If the load is greater than 10 mA, the output voltage is likely to be out of specification.
- Buck SMPS: has two control modes: pulse frequency modulation (PFM) control for low-power operation and pulse width modulation (PWM) control for normal operation. For best efficiency, the buck regulator switches automatically between PFM and PWM, but it can be switched manually via software as well (depending upon sleep or active operation).
  - ▣ In PFM mode, the controller shuts down, except for a comparator that monitors the output voltage. Starting with the pass device off, eventually the output dips below the programmed output voltage. The pass device is then turned on (a single pulse) until the output voltage slightly exceeds the programmed voltage, and then it is turned off. The on/off process repeats. If the buck SMPS is loaded too heavily in PFM mode, the output ripple is degraded.
  - ▣ During PFM operation, the pulse frequency varies with load current, while the ripple stays constant at about 30 to 50 mV peak-to-peak. Depending upon the load, the pulse frequency can drop into the audio range and could become audible if it couples into the audio system.
  - ▣ For normal (active) phone operation, the PWM mode should be used.
- Boost SMPS: is very similar to Buck modes, except no low-power mode exists.

# External Connection Options and Subregulation

Linear regulators are powered by one of three sources (see below):

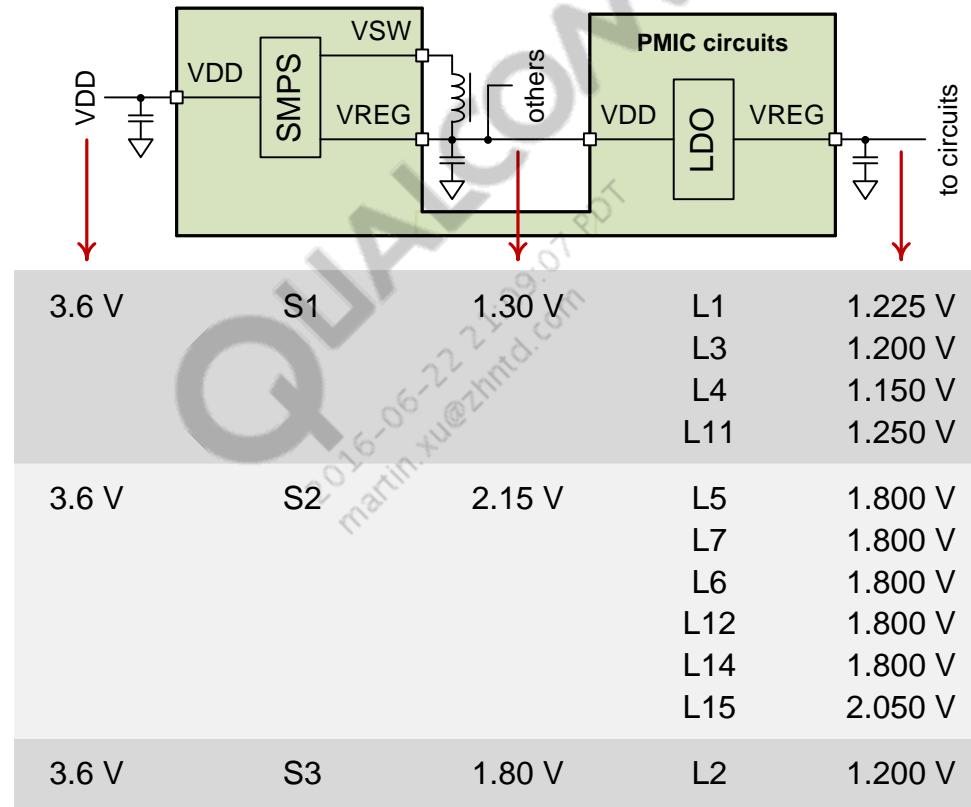
1. An SMPS output: this option implements subregulation (see the next slide)
2. The primary phone power supply node (VPH\_PWR; see the LDO Regulator Supplies – Other than Subregulation slide)
3. An external boost SMPS with optional bypass mode (see the LDO Regulator Supplies – Other than Subregulation slide)

- 1) Select VPH\_PWR for single-stage, direct regulation
- 2) Select PMIC SMPS output for two-stage, subregulation
- 3) Select external boost SMPS output for two-stage, subregulation when higher final output voltages are needed; if the SMPS has a bypass option, it can be placed in its bypass mode if the primary voltage (VPH\_PWR) is high enough (boost not required)



## LDO Regulator Supplies – Those Using Subregulation

All of the MSM8x74 reference designs subregulation implementations are described below.



# Internal Regulator Connections

Some regulator input voltages and several regulated outputs are used to power internal PM8941 circuits. The regulators must be enabled and set to their default values for proper PMIC operation.

Feature	Regulator / Connection	Default	Notes
GPIO_01-14 supplies	VREG_L6	1.8 V	
	VDD_L2_LVS1_2_3	1.8 V	Same as VREG_S3
	VREG_L1	1.225 V	
	VDD_L8_16_18_19	3.6 V	Same as VPH_PWR
GPIO_15-18 supplies	VREG_L6	1.8 V	
	VDD_L2_LVS1_2_3	1.8 V	Same as VREG_S3
	VREG_L6	1.8 V	
GPIO_19-36 supplies	VDD_MSM_IO	1.8 V	Same as VREG_S3
	VDD_TORCH	5.0 V	Same as VREG_5V
	VDD_GPLED	3.6 V	Same as VPH_PWR
MPP_01-04	VREG_L6	1.8 V	
	VDD_L2_LVS1_2_3	1.8 V	Same as VREG_S3
	VREG_L1	1.225 V	
	VDD_L8_16_18_19	3.6 V	Same as VPH_PWR
MPP_05-08	VREG_L6	1.8 V	
	VDD_MSM_IO	1.8 V	Same as VREG_S3
	VREG_L1	1.225 V	
	VDD_GPLED	3.6 V	Same as VPH_PWR
Clocks	VDD_MSM_IO	1.8 V	Sleep clock pad (Vio)
	VREG_XO	1.8 V	XO core
	VREG_RF_CLK	1.8V	Low noise output buffers (XO_OUT_Ax)
	VREG_L6	1.8 V	Low power output buffers (XO_OUT_Dx) The XO_OUT_Dx buffer supply VREG_L6 is forced on by XO_OUT_Dx EN
Power-on	VDD_MSM_IO	1.8 V	PAD IO (Vio)
	VREG_SMB	3.6 V	UVLO detect
SPMI	VDD_MSM_IO	1.8 V	SPMI pad (Vio)
AMUX, XO/HKADC supply	VREG_L8	1.8 V	
BMS	VREG_L8	1.8 V	BMS IADC supply VREG_L8 is forced on by BMS for OCV measurement
SMBB	VREG_L8	1.8 V	VREF_BAT supply
RGB supply	VDD_RGB	3.6 V	Same as VPH_PWR
	VDD_TORCH	5.0 V	Same as VREG_5V
GPLED supply	VDD_GPLED	3.6 V	Same as VPH_PWR
	VDD_TORCH	5.0 V	Same as VREG_5V
Flash supply	VCHG	5.0 V	Flash mode
	VDD_TORCH	5.0 V	Torch mode
WLED supply	VDD_GPLED	3.6 V	Same as VPH_PWR
Vibrator driver supply	VDD_L8_16_18_19		Same as VPH_PWR
dVdd regulator	VDD_L2_LVS1_2_3	1.8 V	Same as VREG_S3
	VREG_L6	1.8 V	

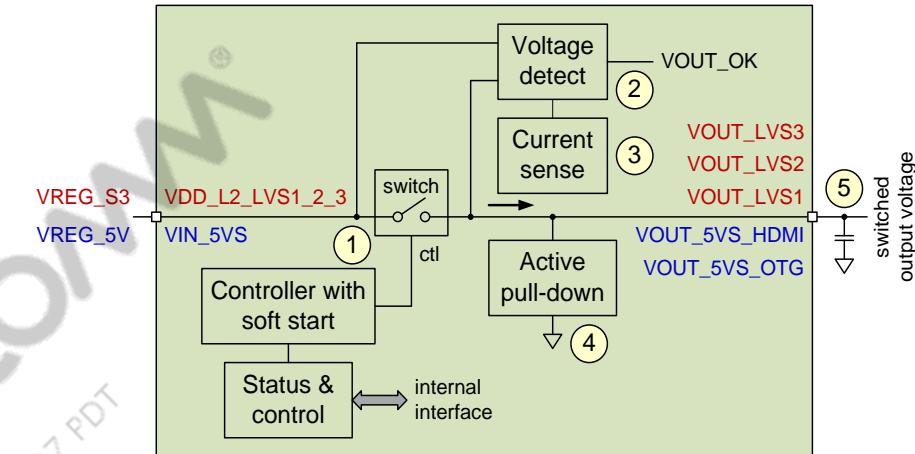
# Input Connection Options

Voltage regulator input	Input connection options
VDD_L1_3	VREG_S1
VDD_L4_11	VREG_S1
VDD_L5_7	VREG_S2 or VPH_PWR
VDD_L6_12_14_15	VREG_S2
VDD_L8_16_18_19	VPH_PWR
VDD_L9_10_17_22	Boost bypass output (VREG_BOOST_BYPASS)
VDD_L13_20_23_24	Boost bypass output (VREG_BOOST_BYPASS)
VDD_L21	Boost bypass output (VREG_BOOST_BYPASS)
VDD_L2_LVS1_2_3	VREG_S3

# Voltage Switches

A low-voltage switch (LVS) or 5 V switch (5VS) can be used to gate a supply voltage to functions that do not support phone operation, such as sensors and OTG. Switch features include:

- Soft start: prevents in-rush current from causing a voltage dip at the source regulator's output.
- Output voltage verification.
- Over-current protection: automatically turns off the switch and sends an interrupt.
- Non-floating output: active pull-down during powerdown.
- Low-power mode: switch remains closed but all control functions are turned off.



1. The switch is turned on slowly (by ramping its gate voltage) to limit in-rush current.
2. The output voltage is deemed okay when it is about 10% less than the input voltage.
3. The current-protection threshold is 2 to  $6 \times I_{\text{rated}}$  current; switch is opened and an interrupt is generated if the current goes above  $3 \times I_{\text{rated}}$  value.
4. When opened, the output is pulled down to ground.
5. External components are not required. If an output capacitor is used, do not exceed  $1.0 \mu F$ .

## Need for External Boost Bypass

Battery impedance could be as high as 250 mΩ. For a 4 A transient current consumption:

- 4 A × 250 mΩ = 1 V drop

With 4 A of transient current drawn from the battery, a fully charged battery is on the verge of browning out the eMMC and SD card.

- 4.2 V → 3.2 V

Peripheral	Battery cutoff voltage
HS USB Phy 3.3 V	3.15 V
SD card	3.16 V
eMMC	3.16 V
LCD (typical)	3.01 V
Camera (typical)	3.0 V
UIM card	2.99 V
Sensors (typical)	3.02 V (moving to 2.5 V)

The external boost bypass (FAN48630UC315X) boosts the system voltage and powers critical rails like eMMC, SD, etc., during high current events.

**Important:** For the MSM8974 platform, it is recommended to use a battery with sufficiently high OCP threshold (5 A to 6 A in 12 msec.) so that OCP is not triggered during high current consumption use cases.

## External Boost Bypass Operation

The mode of external boost bypass and its output voltage depends upon the input voltage and status of EN, BYP\_N, VSEL pins as indicated in the table below.

EN	BYP_N	VSEL	Vout
0	x	x	Boost bypass disabled
1	1	0	For Vin < 3.15 V, Vout = 3.15 V (boost mode) For Vin > = 3.15 V, Vout = Vin (bypass mode)
1	1	1	For Vin < 3.3 V, Vout = 3.3 V (boost mode) For Vin > = 3.3 V, Vout = Vin (bypass mode)
1	0	x	Vout = Vin (forced bypass mode)

EN pin of boost bypass is tied to VPH\_PWR; the boost bypass is always enabled

BYP\_N pin of the boost bypass is connected to GPIO\_21.

- During PMIC powerup GPIO\_21 is driven high
- During sleep GPIO\_21 is driven low

VSEL pin of the boost bypass is connected to TX\_GTR\_THRES pin of MSM.

- The MSM device drives Tx\_GTR\_THRES high 130  $\mu$ s before PA on ramp

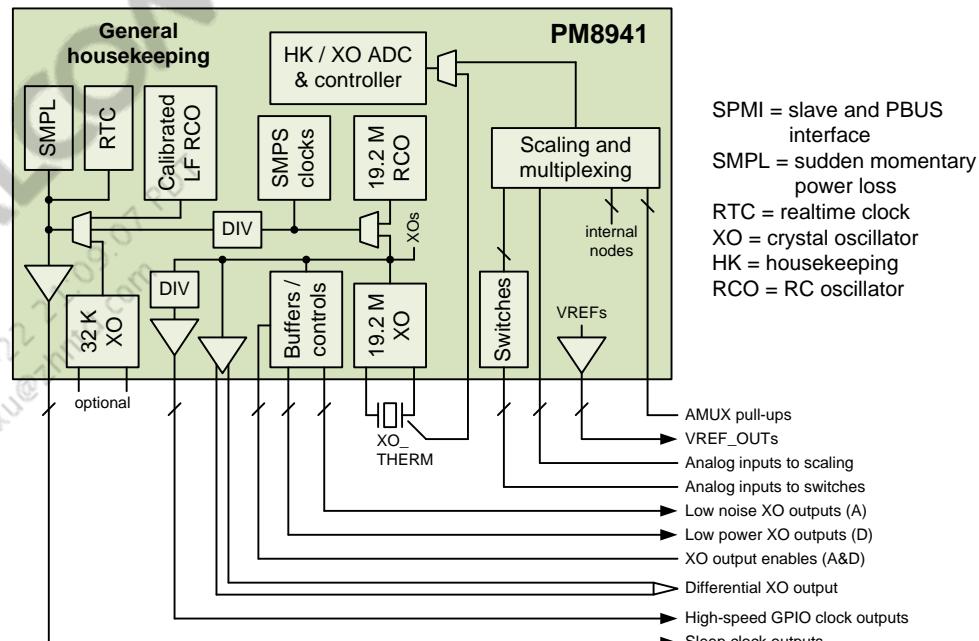


## Section 5

# General Housekeeping

# General Housekeeping Content

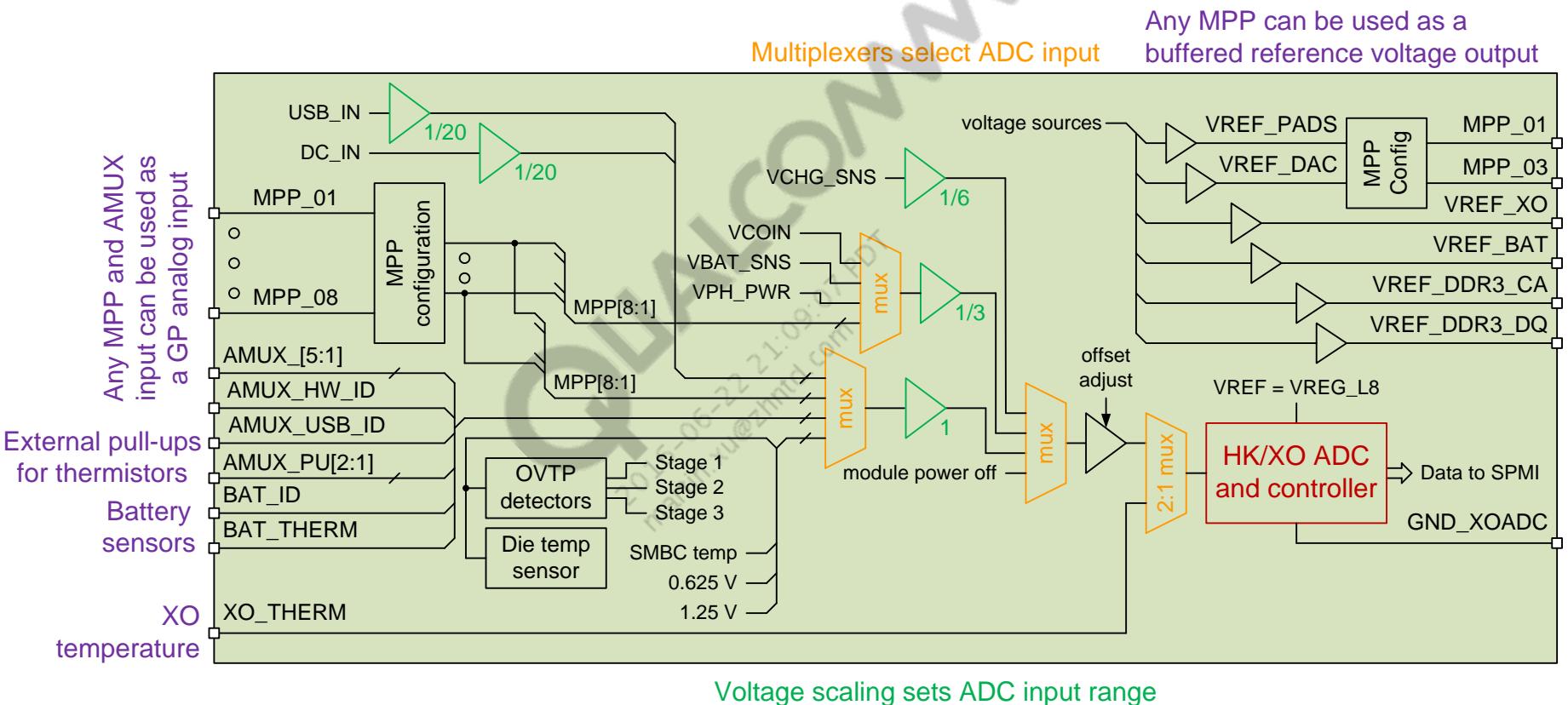
- Analog multiplexer and scaling circuits
- HK/XO ADC circuits
- Clock architecture
- System clocks – 19.2 MHz XO
  - 19.2 MHz XO source
  - XO buffers and controllers
  - Low-noise, low-power, and differential outputs
- System clocks – sleep clock
- Other clock topics
  - MP3 and other alternate clocks
  - SMPS clock circuits
  - Realtime clock
  - 19.2 MHz RC oscillator
  - Calibrated low-frequency RC oscillator
  - External components
  - RTC accuracy
- Over-temperature protection
- Automatic fault protection (AFP)



## Analog Multiplexer and Scaling Circuits (1 of 2)

- Several analog switches and multiplexers select one signal for ADC conversion.
- Nestled within the multiplexers are voltage scaling circuits that condition the signals to best use the ADC's dynamic range.
- The selected signal allows handset software to monitor various voltage nodes, auxiliary inputs, and the die temperature using a single ADC.
- The ADC input cannot reliably go below 0.05 V or above  $V_{REG\_L8} + 0.05$  V; do not exceed this range.
- Gain and offset errors vary between multiplexer channels; calibration values apply to the specific channel being calibrated only. Calibrate each channel separately.
- A functional block diagram is provided on the next slide.

## Analog Multiplexer and Scaling Circuits (2 of 2)



## Analog Multiplexer Channel Assignments (1 of 2)

Ch #	Description	Typical input range (V)	Scaling	Typical output range (V)
0	USB_IN pin (divided by 20)	0.15 to 0.50	1	0.15 to 0.50
1	DC_IN pin (divided by 20)	0.15 to 0.50	1	0.15 to 0.50
2	VCHG_SNS	3 to 10	1/6	0.50 to 1.67
3	–	–	–	–
4	AMUX_USB_ID pin (MV)	0.3 to 3 * (VL8 - 0.10)	1/3	0.10 to (VL8 - 0.10)
5	VCOIN pin	2.0 to 3.25	1/3	0.67 to 1.08
6	VBAT_SNS pin	2.5 to 4.5	1/3	0.83 to 1.50
7	VPH_PWR pin	2.5 to 4.5	1/3	0.83 to 1.50
8	Die-temperature monitor	0.4 to 0.9	1	0.4 to 0.9
9	0.625 V reference voltage	0.625	1	0.625
10	1.25 V reference voltage	1.25	1	1.25
11	Charger temperature	0.10 to (VL8 - 0.10)	1	0.10 to (VL8 - 0.10)
12, 13	–	–	–	–
14, 15	GND_REF, VDD_ADC	–	–	–
16 to 23	MPP_01 to MPP_08 pin	0.10 to (VL8 - 0.10)	1	0.10 to (VL8 - 0.10)
24 to 31	–	–	–	–

## Analog Multiplexer Channel Assignments (2 of 2)

Ch #	Description	Typical input range (V)	Scaling	Typical output range (V)
48	BAT_THERM pin	0.05 to (VL8 – 0.05)	1	0.05 to (VL8 – 0.05)
49	BAT_ID pin	0.05 to (VL8 – 0.05)	1	0.05 to (VL8 – 0.05)
50	XO_THERM pin direct	0.05 to (VL8 – 0.05)	1	0.05 to (VL8 – 0.05)
51 to 53	AMUX_1 to AMUX_3 pin	0.05 to (VL8 – 0.05)	1	0.05 to (VL8 – 0.05)
54	AMUX_HW_ID pin	0.05 to (VL8 – 0.05)	1	0.05 to (VL8 – 0.05)
55, 56	AMUX_4, AMUX_5 pin	0.05 to (VL8 – 0.05)	1	0.05 to (VL8 – 0.05)
57	AMUX_USB_ID pin	0.05 to (VL8 – 0.05)	1	0.05 to (VL8 – 0.05)
58, 59	AMUX_PU1, AMUX_PU2 pin	0.05 to (VL8 – 0.05)	1	0.05 to (VL8 – 0.05)
60	XO_THERM pin through amux	0.05 to (VL8 – 0.05)	1	0.05 to (VL8 – 0.05)
61, 62	–	–	–	–
63	Module power off	–	–	–

- 1) Amux circuits include switches that allow signals from off-chip thermistors to use one of two external pull-up resistors (at AMUX\_PU1 or AMUX\_PU2), thereby reducing the number of resistors in the thermistor networks. AMUX\_PU1/PU2 can be applied to the following PMIC pins: BAT\_THERM, BAT\_ID, XO\_THERM, AMUX\_1, AMUX\_2, AMUX\_3, AMUX\_4, AMUX\_5, AMUX\_HW\_ID, and AMUX\_USB\_ID.
- 2) Channel 63 should be selected when the amux is not being used; this prevents the scalers from loading the inputs.
- 3) Input voltages must not exceed the highest of the following supply voltages: VCOIN, VBAT, VCHG, or VPH\_PWR. The term 'VL8' is the VREG\_L8 output voltage (connected internally).

# HK and XO ADC Circuits

As implied by its name, the HK/XO ADC circuit supports two modes:

- General HK operation, where the signal selected by the analog multiplexer is routed to the ADC.
- A direct path for crystal oscillator (XO) thermal monitoring.

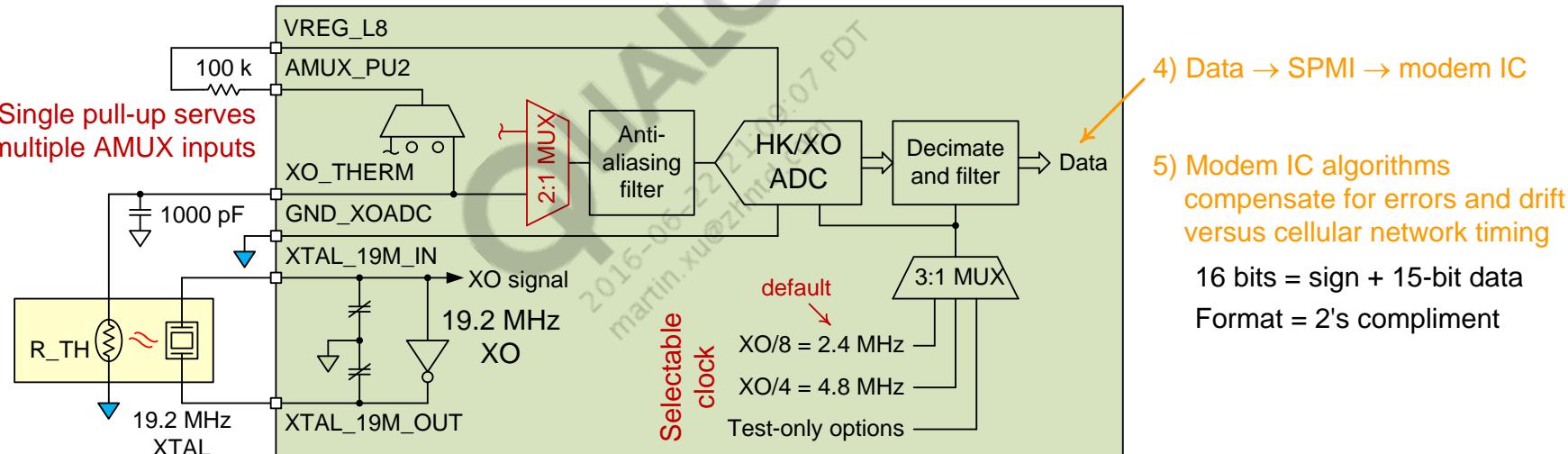
ADC input from AMUX circuits (ADC in HK mode) or  
XO circuits (ADC in XO mode); XO details are shown

2) Analog voltage into PMIC is  
proportional to crystal temperature

3) Filter and convert  
to digital domain

- Sigma-Delta ( $\Sigma\Delta$ ) type ADC
- High accuracy
- Slow conversion and filtering

Programmable decimation rate and filtering (below)



1) Thermistor detects crystal temp      Clock rate, decimation rate, and conversion time

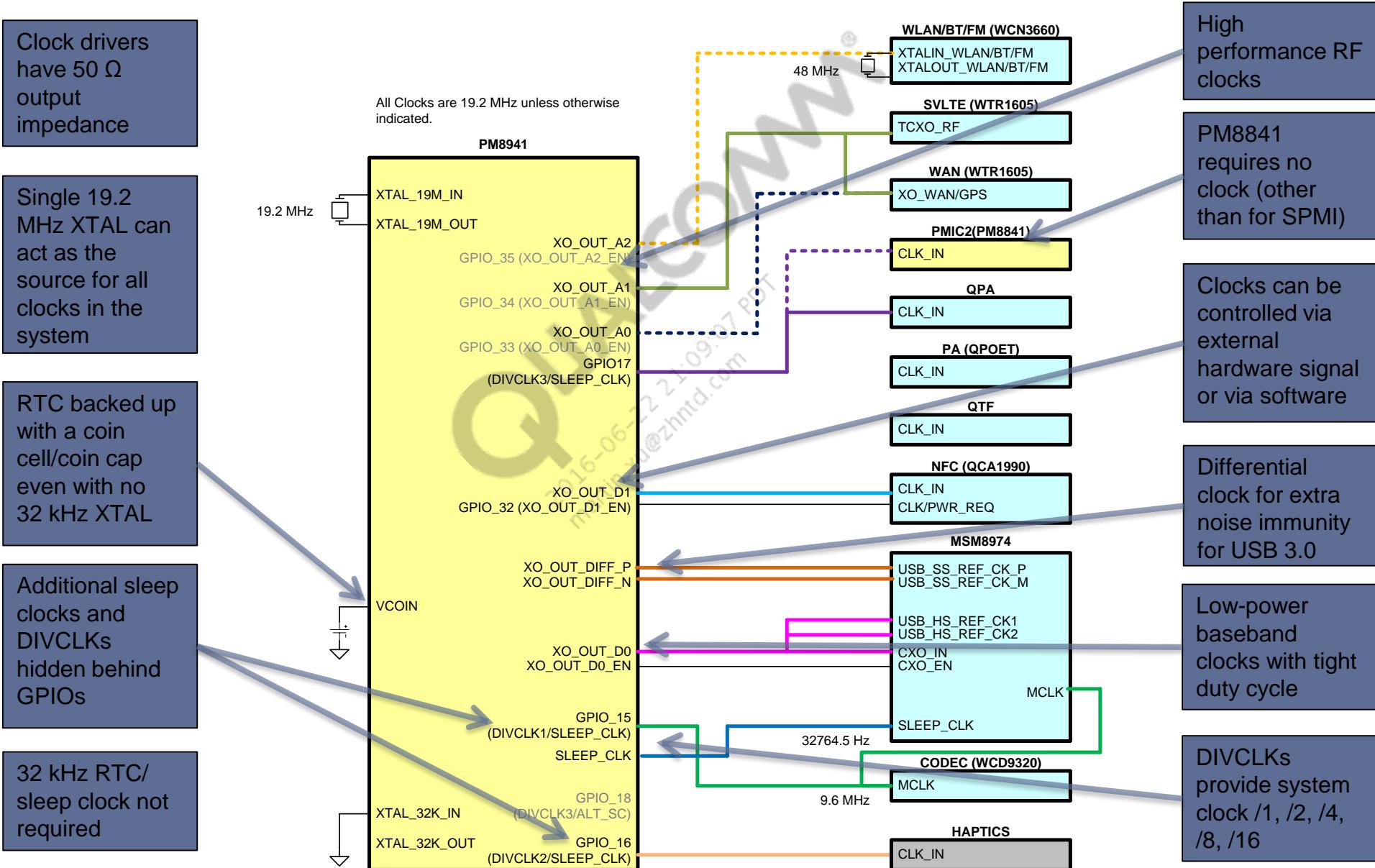
$\downarrow$  Isolated (island) ground  
for XO circuits only

The decimation filter can be  
enabled (Sinc1 & Sinc2) or  
disabled; the examples given at  
right are with the filter enabled.

CLK	Decimation ratio	Update rate	Conversion time
2.4 MHz	512	2.26 kHz	442 $\mu$ s
	1024	1.15 kHz	868 $\mu$ s
	2048	580 Hz	1.722 ms
	4096	290 Hz	3.428 ms

CLK	Decimation ratio	Update rate	Conversion time
4.8 MHz	512	4.38 kHz	228 $\mu$ s
	1024	2.26 kHz	442 $\mu$ s
	2048	1.15 kHz	868 $\mu$ s
	4096	580 Hz	1.722 ms

# Clock Architecture

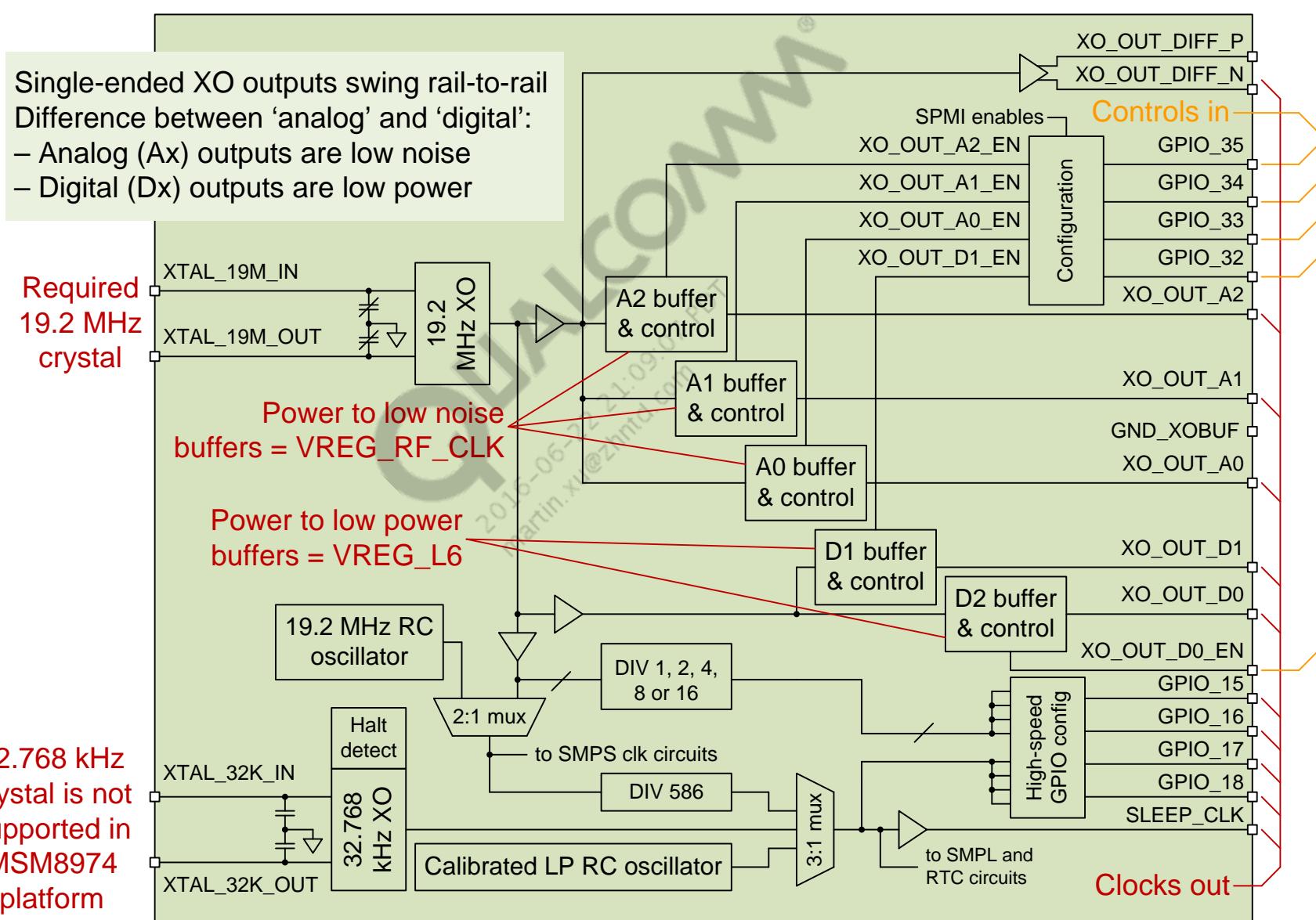


## System Clocks (1 of 2)

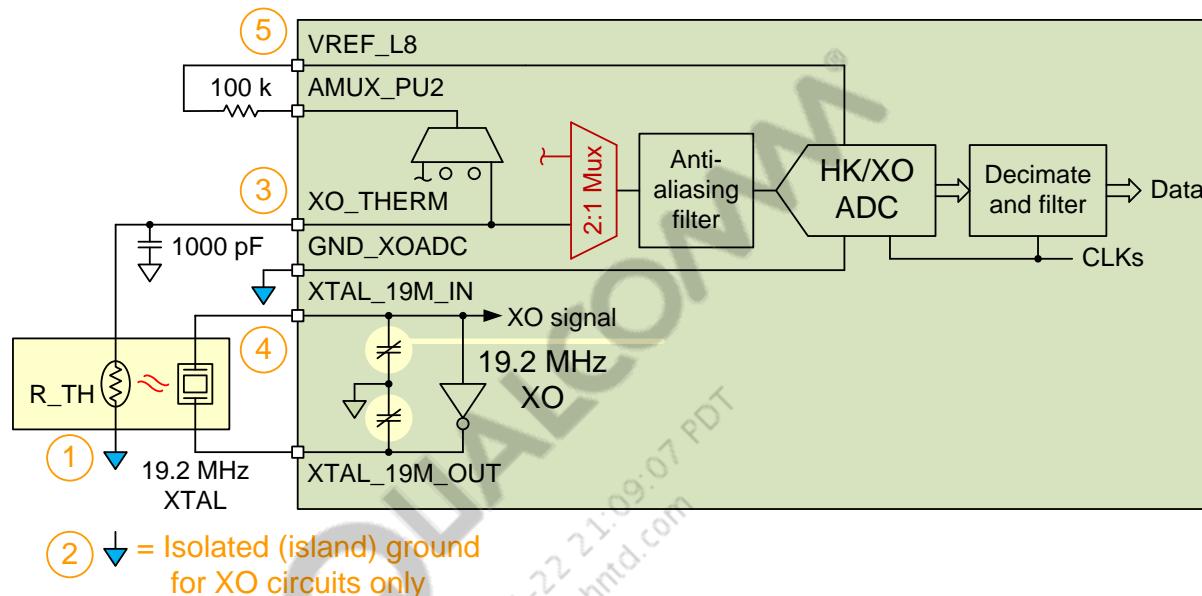
Several clocks and clock outputs are used for general housekeeping functions and elsewhere throughout the system:

- 19.2 MHz crystal oscillator (XO) circuit: the system's master clock
- Five sets of XO controller and buffer circuits
- Differential XO output
- 19.2 MHz RC oscillator for powerup and emergency backup
- Divided and buffered clock for MP3 support
- 32.768 kHz XO – or calibrated low-frequency RC oscillator – for sleep and for the realtime clock (RTC)
- Multiple buffered SLEEP clock outputs
- SMPS clocks

## System Clocks (2 of 2)



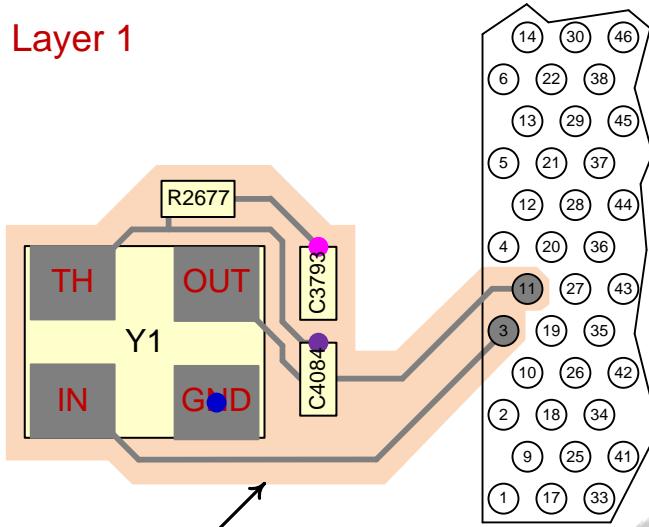
## 19.2 MHz XO Source – Schematic



- The thermistor is normally integrated into the same package as the crystal.
- Ground connections are critical to thermal management (more on the next slide).
- The XO ground is a surface-layer island that must be isolated from other ground fill areas. This island is also thermally isolated from the PMIC to prevent heating.
- Associated XO components are connected to this ground island: thermistor, GND\_XOADC.
- The output of the thermistor network is XO\_THERM – the node between the resistor and the thermistor; this analog voltage is routed directly to the XO/HK ADC.
- The XTAL\_19M\_IN and XTAL\_19M\_OUT nodes must not be loaded by external circuits. The PMIC provides other outputs for driving external loads (details later).
- The thermistor network and ADC circuits use the same voltage (VREG\_L8).

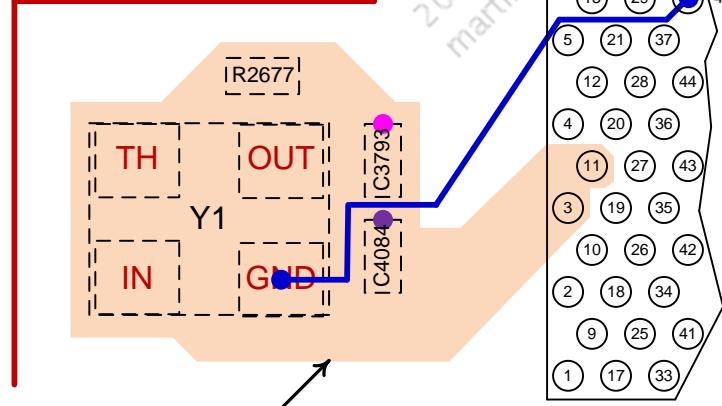
# 19.2 MHz XO Source – Layout Guidelines (1 of 3)

Layer 1



Orange is a 'moat' cleared of metal that isolates XO ground from other grounds

- = VREF\_XO
- = GND\_XOADC
- = XO\_THERM

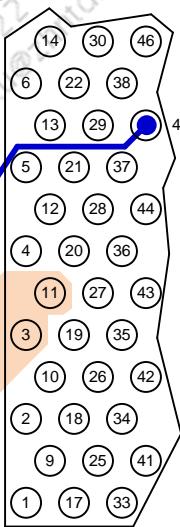


Maintain moat on layer 2 except for thin traces connecting ground points (blue)

See 19.2 MHz XO Source – Layout Guidelines (3 of 3)

Layer 2

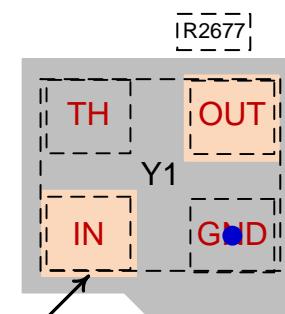
XO ground points connect to GND\_XOADC pin using thin traces



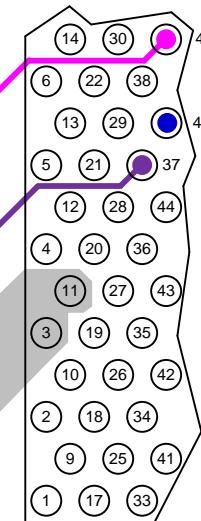
Deeper layers

Connect GND\_XOADC to main ground plane below pin 45

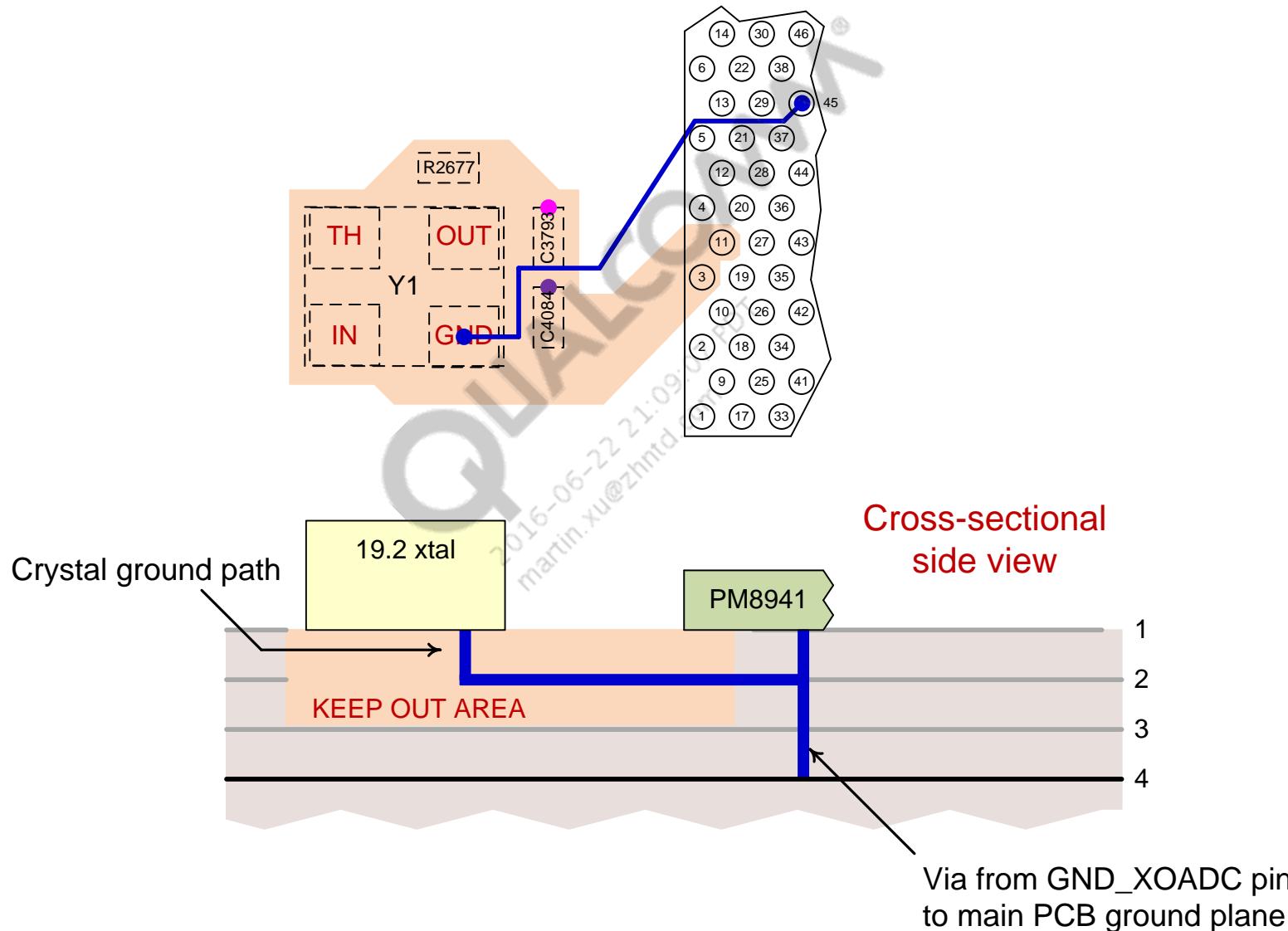
GND below in/out lines for improved isolation



Maintain clearance below in/out pads for reduced parasitic capacitance



## 19.2 MHz XO Source – Layout Guidelines (2 of 3)



See 19.2 MHz XO Source – Layout Guidelines (3 of 3) for more information.

## 19.2 MHz XO Source – Layout Guidelines (3 of 3)

Crystal location and connections (thermal concerns)

- Locate the crystal 1 to 3 cm from the PMIC.
- Provide keep out area as illustrated (no metal).
- Use thin traces for high thermal resistance.

Signal connections

- XTAL\_19M\_IN and XTAL\_19M\_OUT should not be routed as a differential pair – isolate them.
- Isolate from other signals (no parallel routing).
- Thermistor is integrated into the crystal package.

R & C close to crystal

- Ground connections.
- Connect crystal GND to PMIC GND\_XOADC pin using a thin trace.
- Connect GND\_XOADC pin to main GND using a dedicated via.

# Sleep/RTC Clock Generation and Outputs (1 of 3)

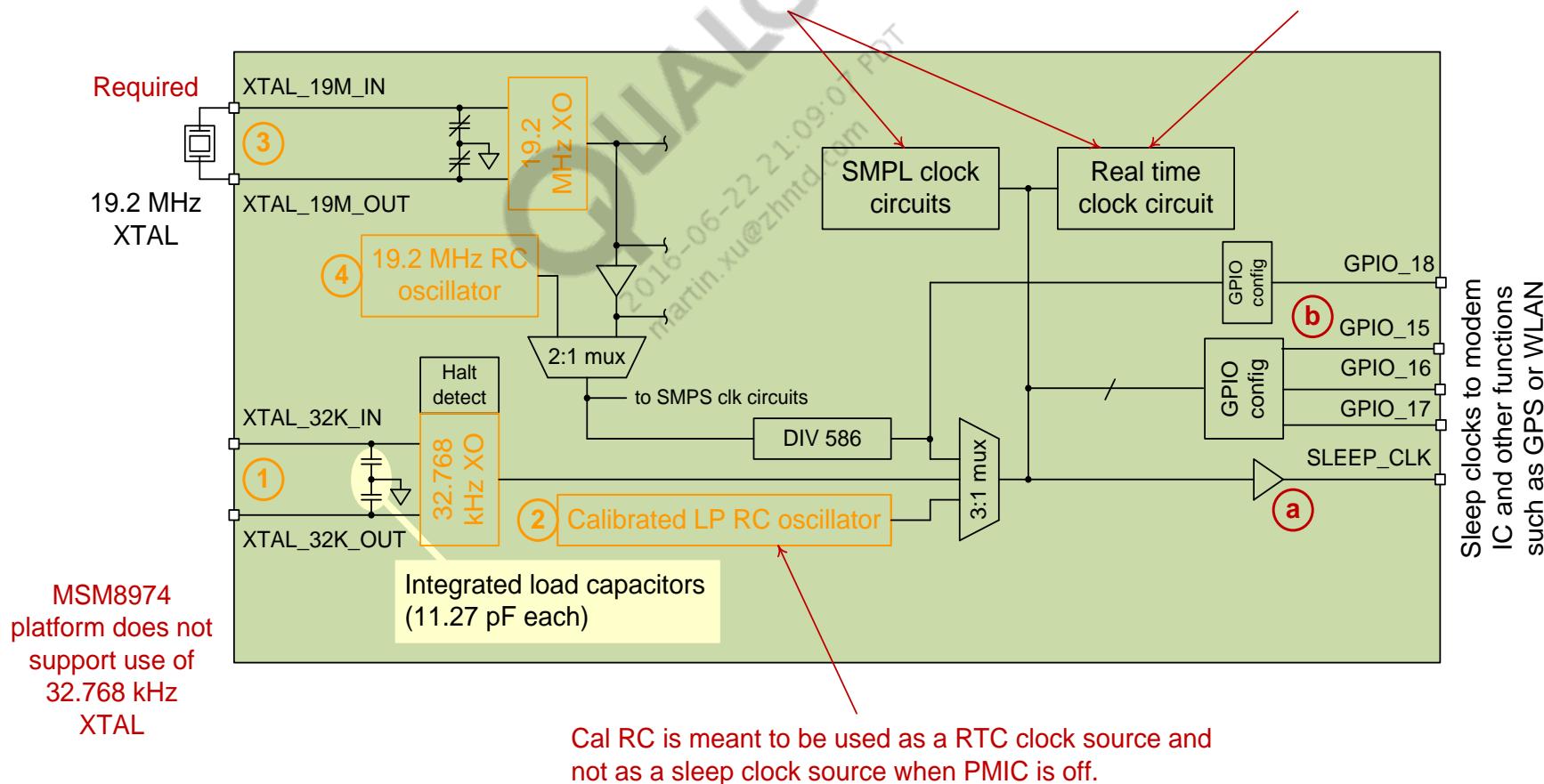
Further discussion on the next slide:

- Source options (orange)
- Switchover
- Output options (red)

- SMPL is supported even if the only power source is a keep-alive capacitor at VCOIN.
- RTC is not supported by keep-alive capacitor; requires qualified coin cell/super capacitor when the main battery is missing.

RTC input clock source

- Uses XO/586 when the device is in active and sleep mode
- Uses calibrated low-frequency RC oscillator when the device is off



## Sleep/RTC Clock Generation and Outputs (2 of 3)

### Source options

1. A 32.768 kHz crystal source: This low-power source can have high accuracy and stability, depending upon the external crystal; the 32.768 kHz oscillator circuit is disabled by default in hardware and is not supported in MSM8974 platform.
2. Calibrated low-frequency RC oscillator
  - Used as a source of RTC clock when PMIC is off; requires a qualified coin cell or super capacitor to support RTC when the battery is removed.
  - Periodically uses the XO signal for calibration, achieving accuracy suitable for RTC without an external crystal.
  - Eliminates the external 32.768 kHz crystal, but increases the sleep mode current consumption; the 32.768 kHz oscillator consumes about 1  $\mu$ A average current, while this solution consumes about 5.5  $\mu$ A average current.
3. The 19.2 MHz XO divided by 586 (32.7645 kHz nominal): This is the source of sleep clock and RTC clock when the device is in active and sleep mode.
4. The 19.2 MHz RC oscillator divided by 586 (32.7645 kHz nominal): 19.2 MHz RC oscillator is an on-chip circuit with coarse frequency accuracy:
  - Used during PMIC powerup until software switches over to XO/586.
  - Used in active or sleep mode only if other sources are unavailable.

**Note:** For Cal RC operation details, refer to the *Use of Super Capacitor for Cal-RC Application Note* (80-N4420-11).

## Sleep/RTC Clock Generation and Outputs (3 of 3)

### Switchover

- The 32.768 kHz signal is monitored to ensure continuous oscillation. If the 19.2 MHz XO oscillator source stops oscillating, a multiplexer automatically switches to the 19.2 MHz RC signal, and an interrupt is generated. Narrow pulses at the SLEEP\_CLK output may occur during this switchover.

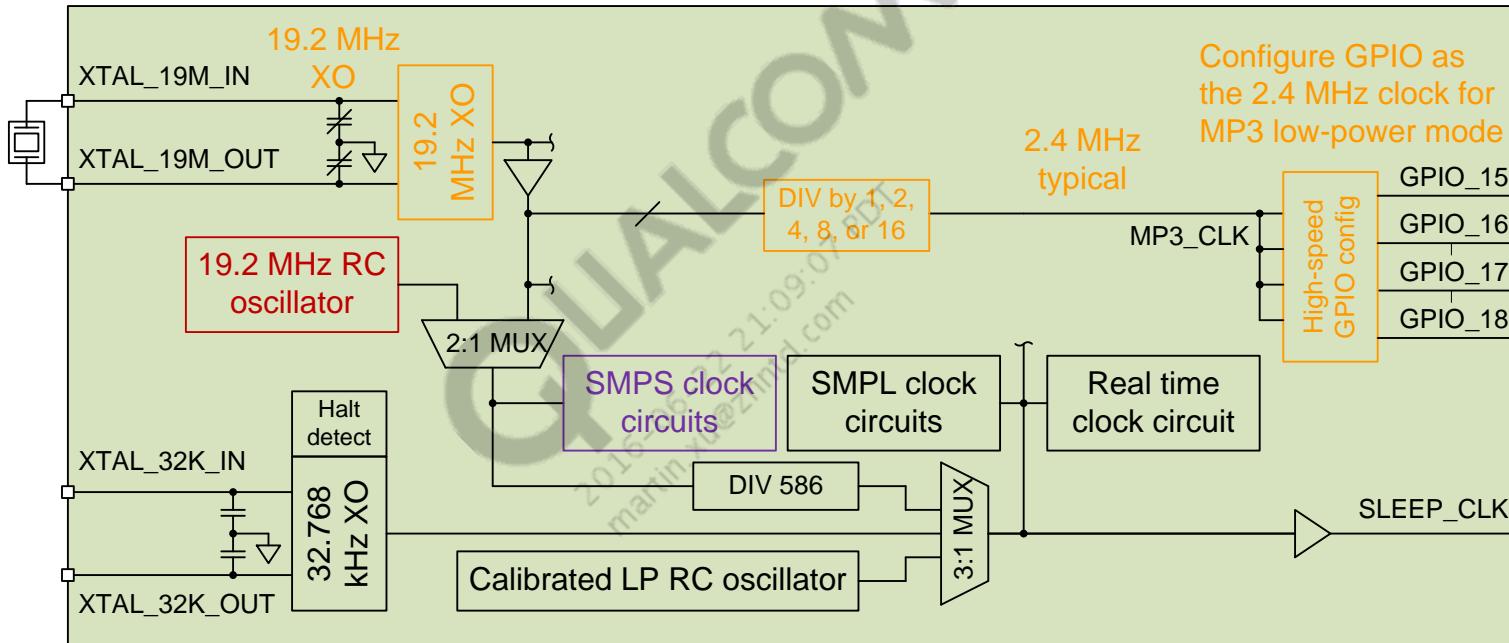
### Output options

1. A dedicated output pin (SLEEP\_CLK) for the modem IC and others; toggles only when the PMIC is on and stays low when the device is off, even though the crystal oscillator continues to run.
2. GPIO\_15, GPIO\_16, GPIO\_17, GPIO\_18 can be configured as sleep clock outputs to support other functions.

# Other Clock Topics (1 of 2)

## 1) MP3 clock

- 19.2 MHz XO source
- Divide by 8 for 2.4 MHz
- Configure high-speed GPIO for external routing



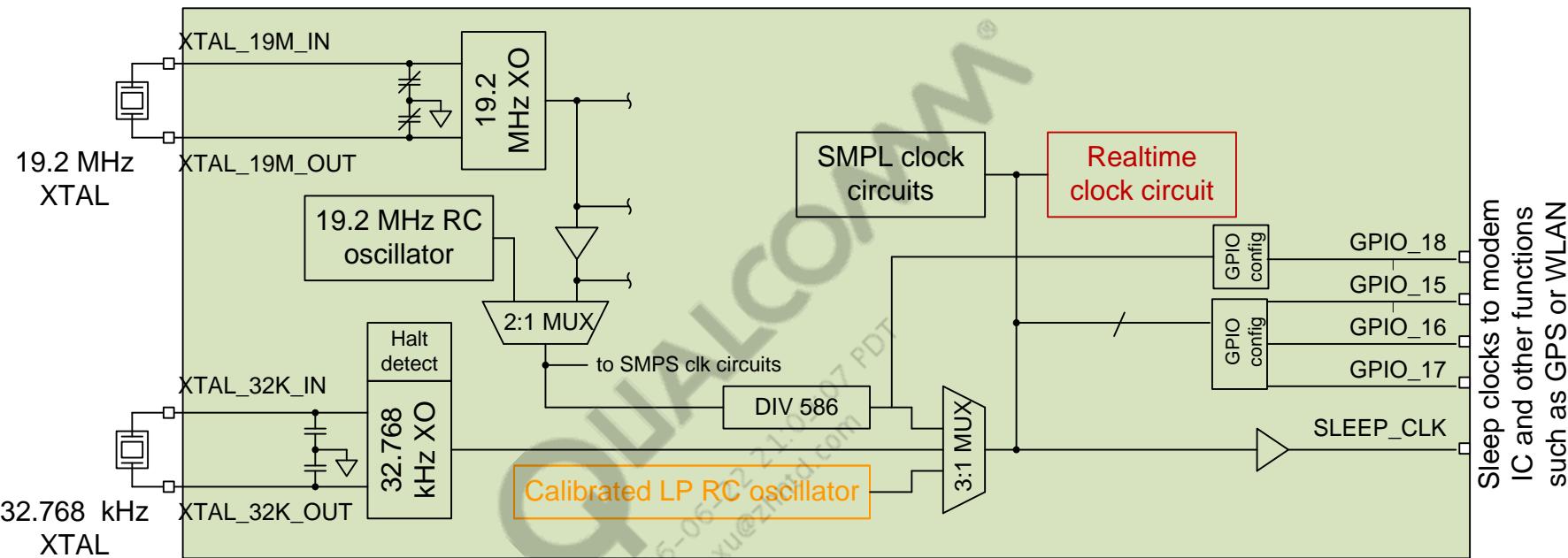
## 2) 19.2 MHz RC oscillator

- Default clock source during powerup
- Modem IC clears interrupts that allow switchovers to 32.768 kHz XTAL and 19.2 MHz XO sources
- Transitions synchronized, glitch-free
- RC oscillator powered down when not used to reduce power consumption; draws too much current for keep-alive battery – PMIC must be on
- Restarts if XTAL or XO halts

## 3) SMPS clocks

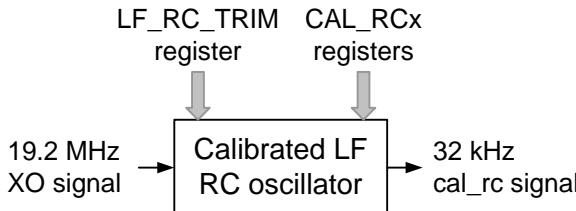
- The switched-mode power supplies are driven by one of two clock sources: 1) RC oscillator or 2) XO source (both 19.2 MHz nominal).
- Programmable and variable divide-by-3 creates 6.4 MHz
- Capable of skipping pulses; allows adjustments so that spectra due to transients can be shifted to minimize RFI

## Other Clock Topics (2 of 2)



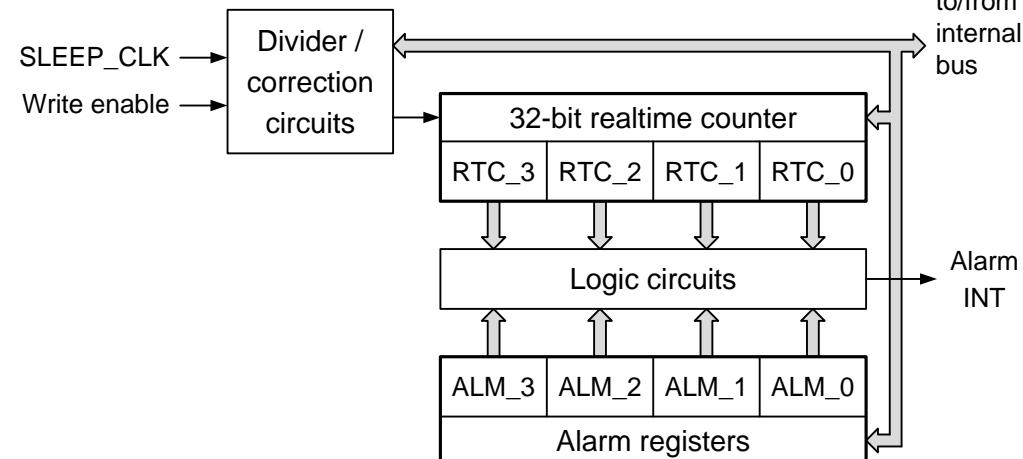
### 4) Calibrated low-frequency RC oscillator

- Periodically uses XO signal for calibration, achieving accuracy suitable for RTC without external crystal
- Eliminates the external 32.768 kHz crystal, but increases the sleep mode current consumption; the 32.768 kHz oscillator consumes about  $1 \mu\text{A}$  average current, while this solution consumes about  $5.5 \mu\text{A}$  average current



### 5) Realtime clock (RTC)

- For calendar and alarm functions



## RTC Accuracy

The PM8941 supports RTC function without the requirement of a 32 kHz sleep crystal. When the phone is on, a low-power 19.2 MHz XO provides the RTC clock. When the phone is off, the Cal RC is used to maintain the RTC clock.

RTC source	Battery current ( $\mu$ A)	Typical use case accuracy	Coin cap RTC run time, without battery	Notes
19.2 M XO divided (phone on)	80	2 ppm	NA	XO frequency divided by 586 is used as the RTC source.
Cal RC (phone off)	5.0	46 ppm (4 seconds per day)	1 hour	With default calibration frequency.
32K XO	2.5	30 ppm (2.6 seconds per day, error is determined by crystal tolerance)	2 hour	32 kHz XO is the traditional RTC source. Its performance is listed for comparison purpose only.

A typical case is defined as room temperature and typical battery voltage, 3.7 V or 3.2 V coin cell voltage.

**Note:** Assumes a 33 mF super capacitor.

## External Clock Components

The reference designs use the Kyocera CT2016DB19200C0FLHA1 as the 19.2 MHz crystal with integrated thermistor.

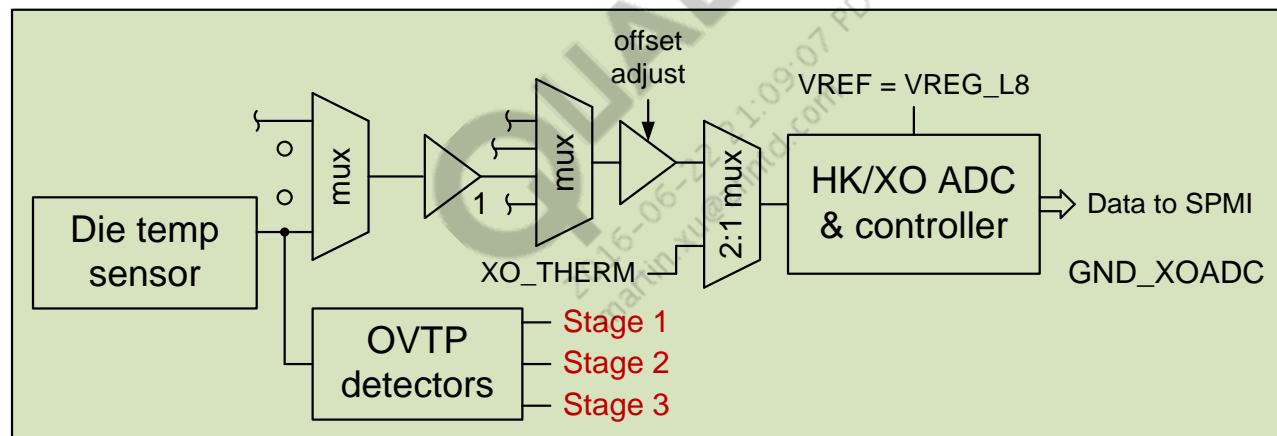
Refer to *19.2 MHz Modem Crystal Qualification Requirements and Approved Suppliers* (80-V9690-19) for the following information:

- Data needed from crystal suppliers to demonstrate compliance
- Approved suppliers for different crystal configurations
  - 2.0 mm × 1.6 mm package with integrated thermistor
  - 2.5 mm × 2.0 mm package with integrated thermistor
  - 2.5 mm × 2.0 mm package with pin 2 GND, pin 4 floating
  - 2.5 mm × 2.0 mm package with pins 2 and 4 GND
  - 3.2 mm × 2.5 mm package
- Discussion of various schematic options

## Over-temperature Protection

The PMIC provides over-temperature protection in stages, depending upon the level of urgency as the die temperature rises.

- Stage 0 – Normal operating conditions (less than 110°C); no interrupt is generated.
- Stage 1 – 110°C to 130°C; interrupt sent to modem IC without shutting down any PM circuits.
- Stage 2 – 130°C to 150°C; an interrupt is sent to the modem IC, and high-current drivers (LED drivers, backlight drivers, etc.) are shut down.
- Stage 3 – Greater than 150°C; an interrupt is sent to the modem IC, and PM functions are completely shut down.



Temperature hysteresis is incorporated such that the die temperature must cool significantly before the device can be powered on again.

- If any start signals are present while at stage 3, they are ignored until stage 0 is reached.
- When the device cools enough to reach stage 0 and a start signal is present, the PM circuits will power up immediately.

## Automatic Fault Protection (AFP)

The AFP feature of PM8941 is useful to protect the system from damage in the event of a catastrophe.

Example catastrophic events include:

- Water damage caused to handset
- Overheating of the handset due to component failure

The PMIC can be put in AFP mode by software or hardware.

- Upon detection of a fault, software can force the PMIC to enter AFP mode.
- If software is non-operational, the PMIC can still enter AFP mode via a dedicated watchdog timer.

## APP Mode – Entry and Exit

- Upon entry in APP mode, the PMIC executes a poweroff sequence:
  - High-current circuits, such as backlight drivers, are disabled.
  - The FET controls the turn-off system DC distribution paths (battery FET, USB OVP FET, etc.).
  - Clocks are turned off.
  - Regulators are turned off.
- A latch is set that blocks all the poweron triggers except KYPD\_PWR\_N.
- Once the APP poweroff sequence is completed and the latch is set, the off state is maintained until:
  - KYPD\_PWR\_N goes low, regardless of the VBAT level or charger presence.
  - All power sources except VCOIN – including VBAT and chargers – are off.
- When one of these events occurs, the latch is cleared and the APP watchdog timer is reset.
- Once the latch is cleared, the poweron triggers are no longer blocked and a normal powerup is executed at the next triggering event. If CBL\_PWRx\_N is tied to ground, an immediate poweron sequence is started when a valid battery is inserted.
- The pull-down on VBAT ensures its voltage changes fast enough to detect battery insertions/removals.

# AFP Watchdog Timer and VREG\_FAULT

## AFP watchdog timer

- The PMIC also has an AFP watchdog timer that can put the device in AFP mode.
- Watchdog timer has programmable timeout settings of 30, 60, 90, and 120 seconds (default).
- If the watchdog timer is enabled, it barks upon expiry.
- Software has to pet the watchdog timer before it bites (within 6 seconds after the bark) for normal operation to continue.
- If the watchdog bites, the PMIC enters AFP mode.

## VREG\_FAULT

- When the PMIC is in AFP mode, LDO VREG\_FAULT is available to power fault-related circuits.
- 1.2 or 1.8 V; 200 mA rating
- The AFP LDO is always off when the PMIC is in off mode.

## Other AFP comments

- During AFP poweroff, the PMIC registers are not accessible, but the AFP trigger information is preserved for debugging purposes if a valid coin cell is connected to VCOIN. In this case, the RTC continues to run.
- The PMIC can be configured to perform a warm reset after an AFP event.



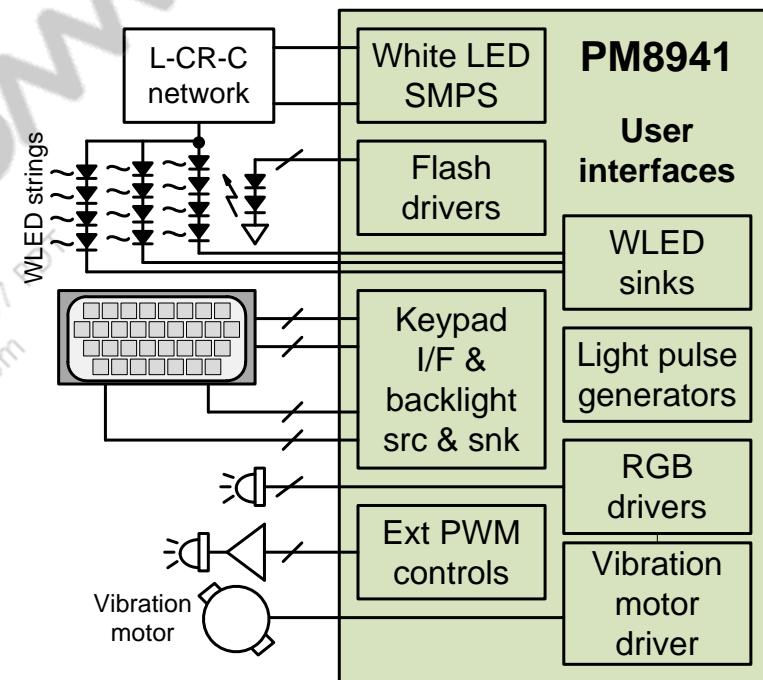
## Section 6

# User Interfaces

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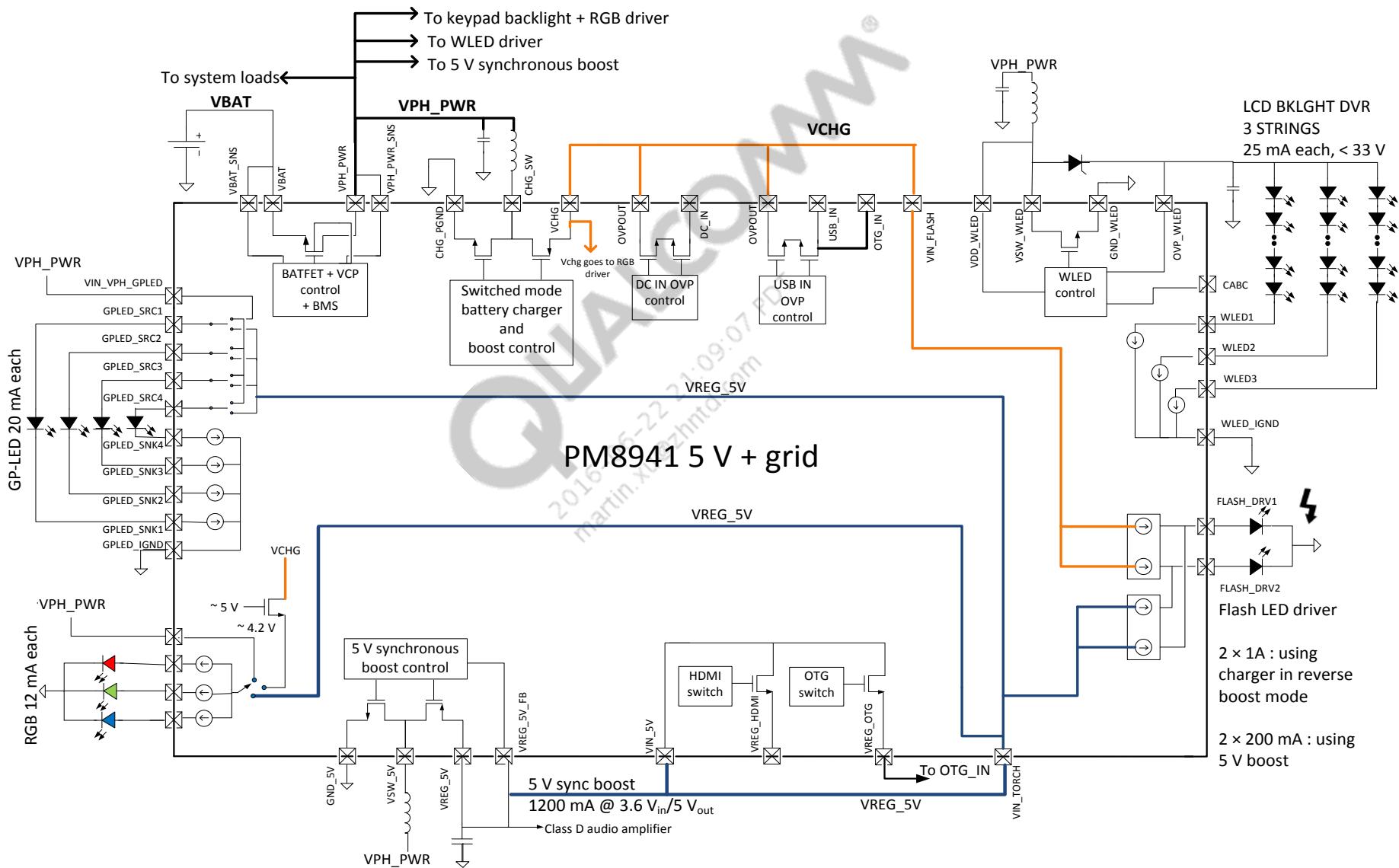
# User Interfaces Content

- Lighting architecture
- Light pulse generators
  - Architecture
  - Waveforms
  - Programmable parameters and controls
- RGB LED driver
- 2x 1 A flash driver
  - Feature summary
  - VPH\_PWR dip monitoring
  - Mask behavior
- White LED support
  - High-voltage SMPS
  - Schematic and layout guidelines
  - WLED string drivers
- Home row lighting/key illumination
- Keypad interface
- Vibration motor driver



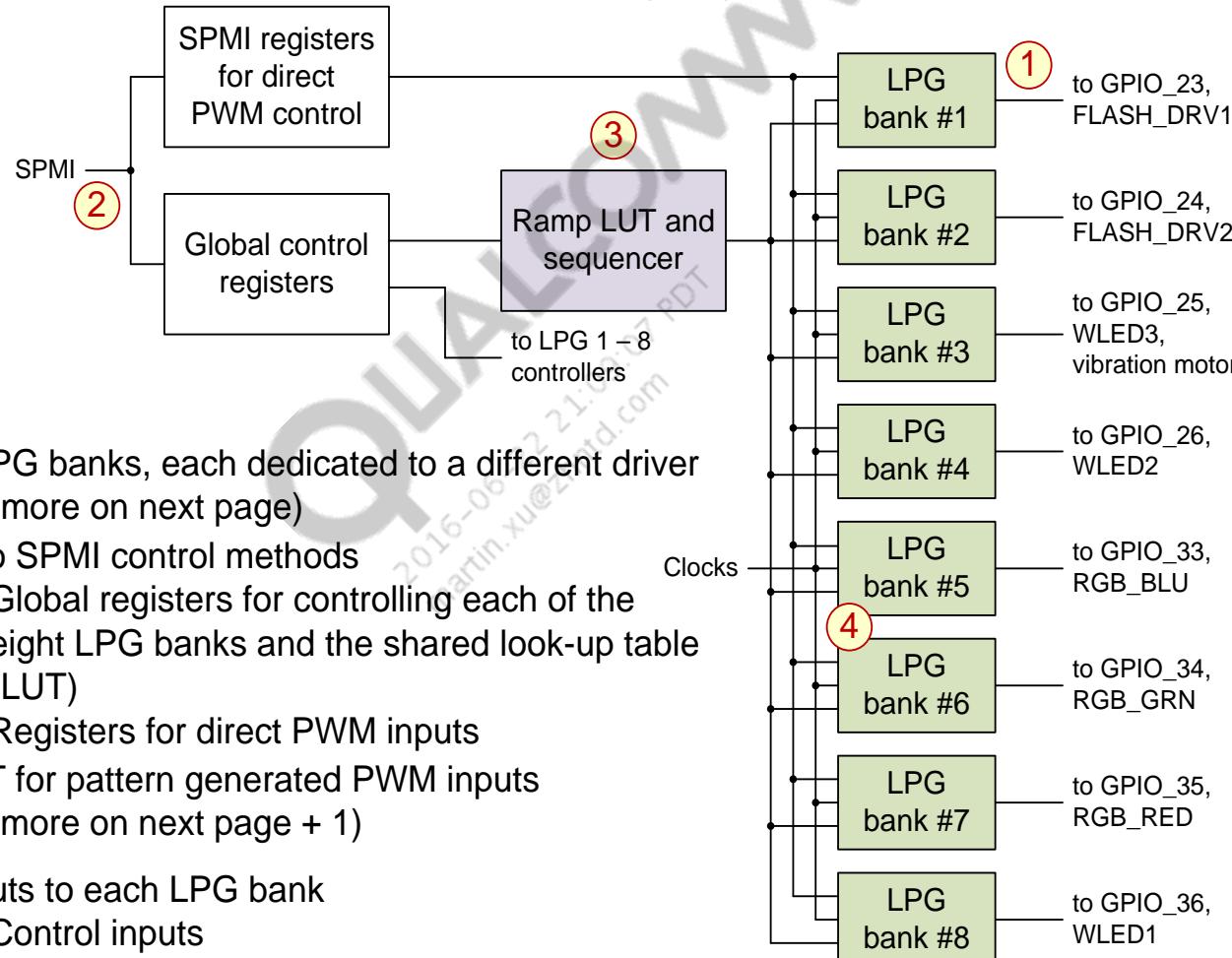
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# Lighting Architecture



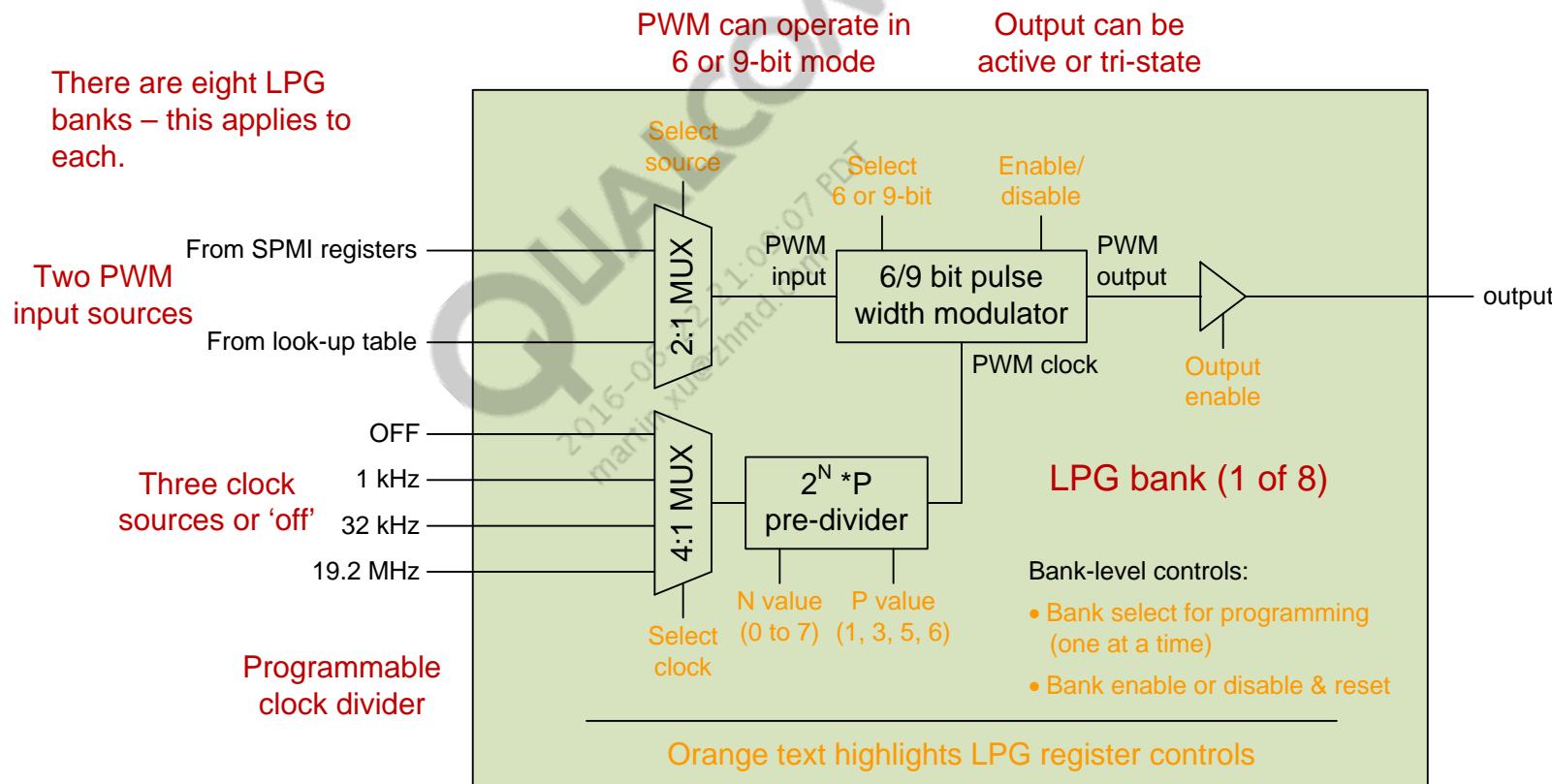
# Light Pulse Generators

Two light pulse generator (LPG) circuits – one eight-channel (shown below) and one four-channel that controls the keypad backlighting (GPLED sources and drivers)

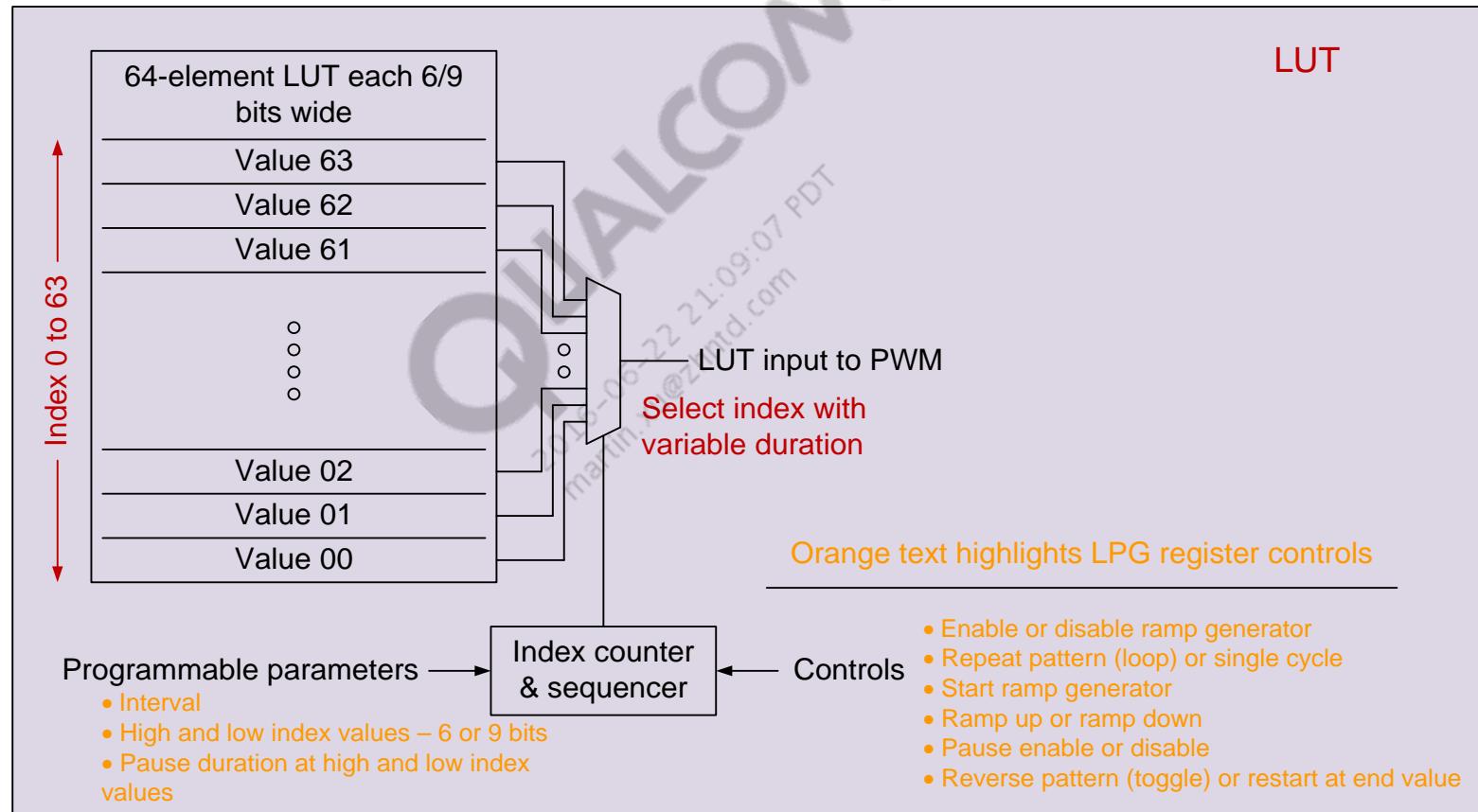


# LPG Banks

Item 1 from the previous Light Pulse Generators slide – eight LPG banks, each dedicated to a different driver

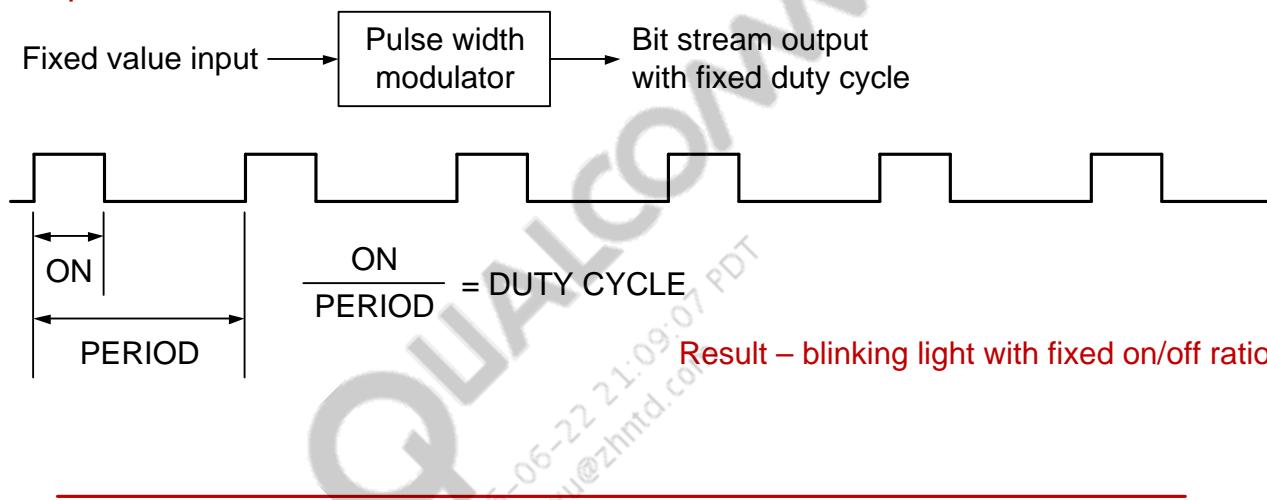


Item 3 from the Light Pulse Generators slide – look-up table for pattern generated PWM inputs

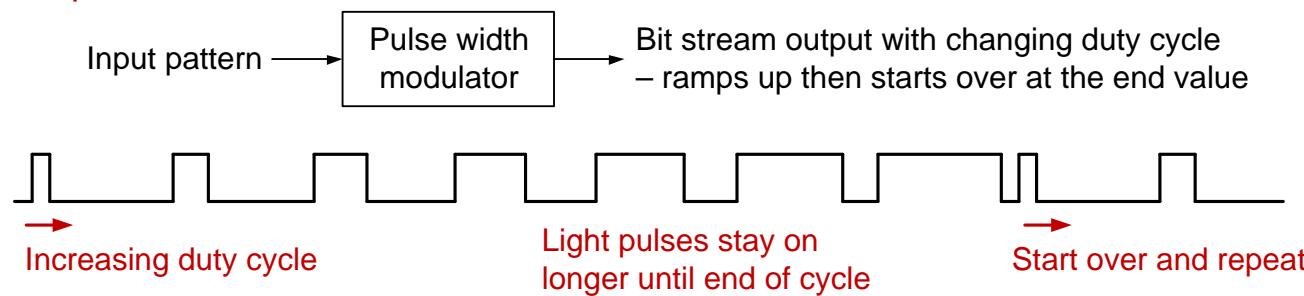


# Example PWM Output Waveforms

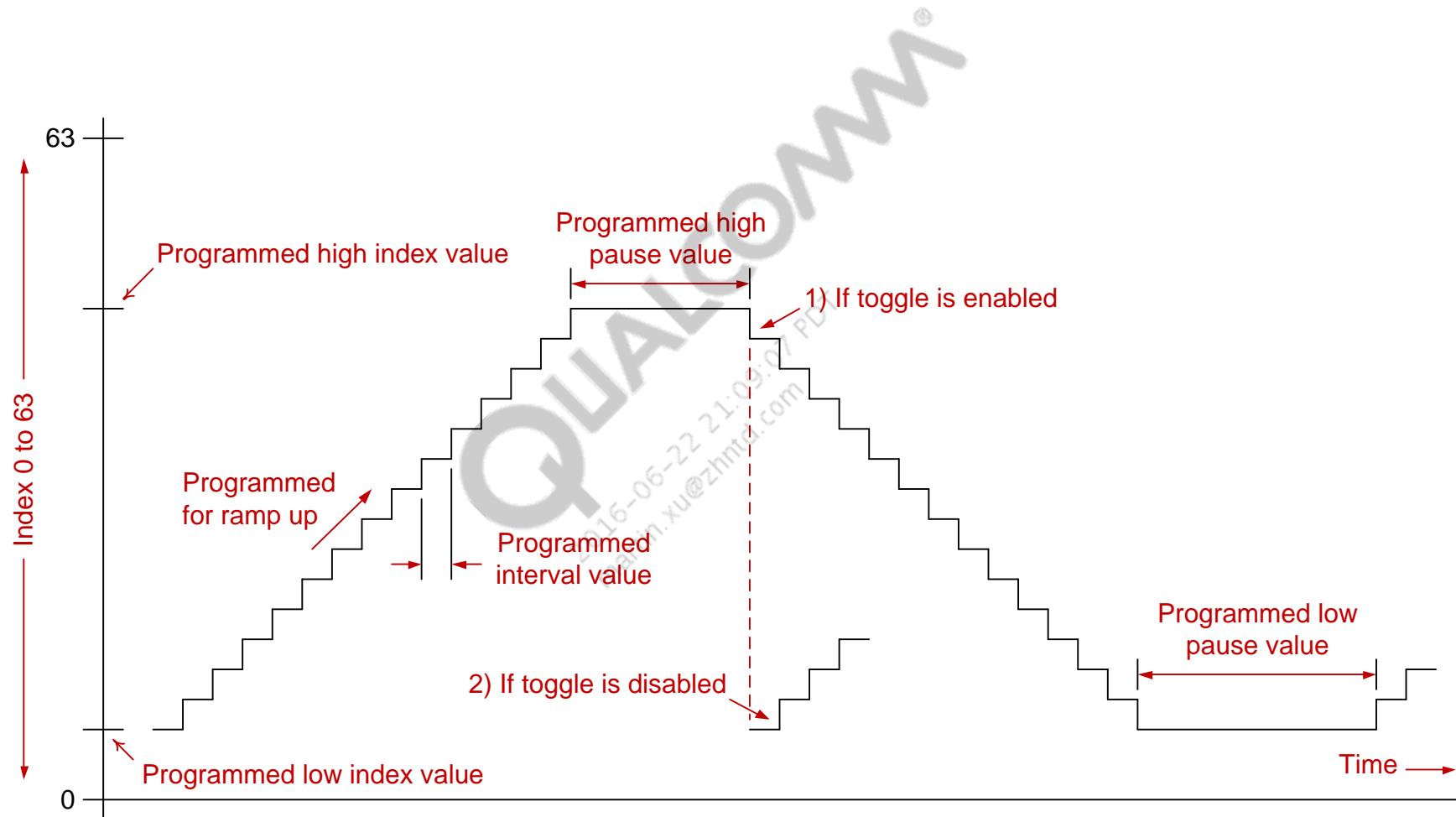
## Example 1



## Example 2



## Example PWM Input Patterns Via LUT

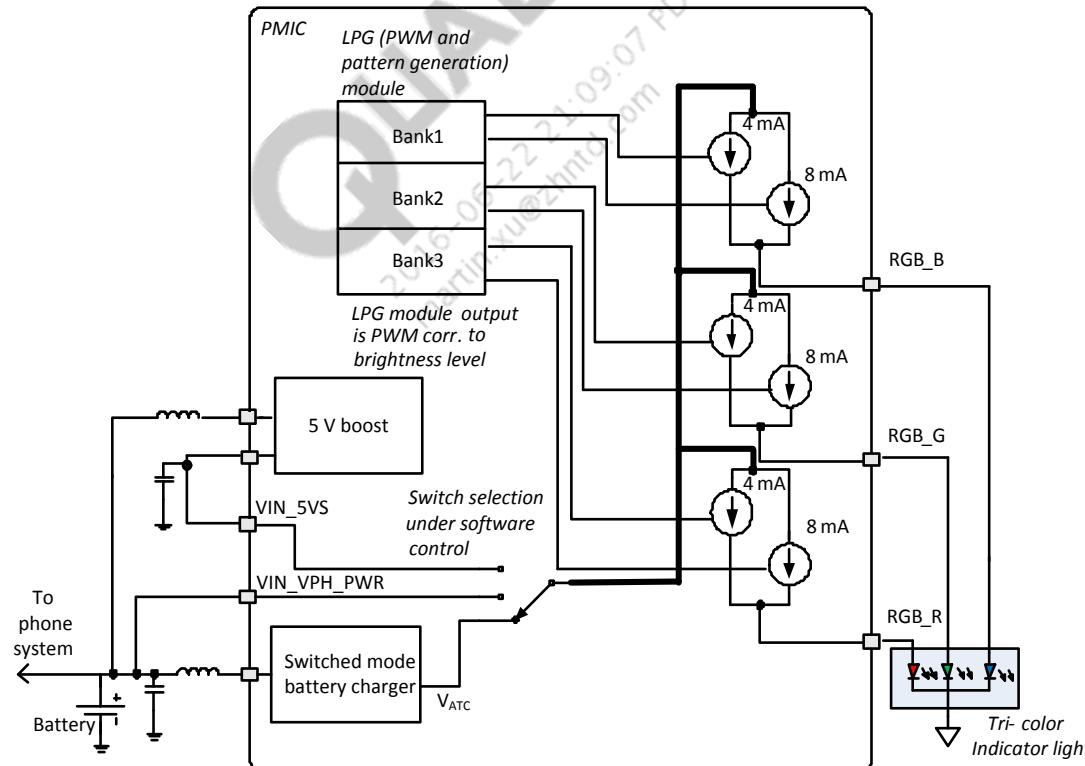


# LPG Programmable Parameters and Controls

Parameter or control	Description
Interval	Time spent at each LUT value 1 ms to ~ 1/2 sec; divided down from 1 kHz
Loop	Repeat the pattern or a single cycle
Ramp direction	Up – start low index value, end high value Down – start high value, end low value
Enable ramp generator	Enable or disable
Start LPG ramp	Ramp starts when set; cleared at ramp starts
End value toggle or restart	Toggle – reverse direction at end value Restart – return to start when end reached
High index values	6-bit or 9-bit
Low index values	6-bit or 9-bit
Enable PWM	Enable or disable
PWM input source	Directly from SPMI registers or from LUT
PWM clock source	OFF (no clock), 1 kHz, 32 kHz, or 19.2 MHz
Clock pre-divide value (P)	2, 3, 5, or 6
Clock pre-divide exponent (N)	0 to 7
Pause at low index value duration	1 to 16 (all) then 23 to 7000 (select values) – 1 kHz clock
Pause at high index value duration	1 to 16 (all) then 23 to 7000 (select values) – 1 kHz clock
Enable pause at low index value	Enable or disable
Enable pause at high index value	Enable or disable
PWM output enable	Active or tri-state mode
PWM size	6-bit or 9-bit
LPG bank select	Only one can be programmed at a time.
LPG bank enable	Each can be enabled or disabled individually; when disabled, the LUT is set to its low index value and the interval is set to 0.

## RGB LED Driver

- Independent brightness control of R, G, and B channels.
- Independently programmable duty cycle and period via three LPG channels.
- 8-bit resolution, digital dimming.
- Software control of power source switch from VPH\_PWR to VIN\_5VS when operating headroom is not met in mission mode.
- Constant current (4 mA/channel) during auto-trickle charging. By default, the R and G LEDs are lit.



# 2x 1 A Flash Driver

Flash power source:

- The charger module runs in reverse as boost in closed loop with the flash module to minimize internal power dissipation.

Concurrency:

- With external DC\_IN, charging is paused while the flash module and charger in reverse boost is used.

Video power sources

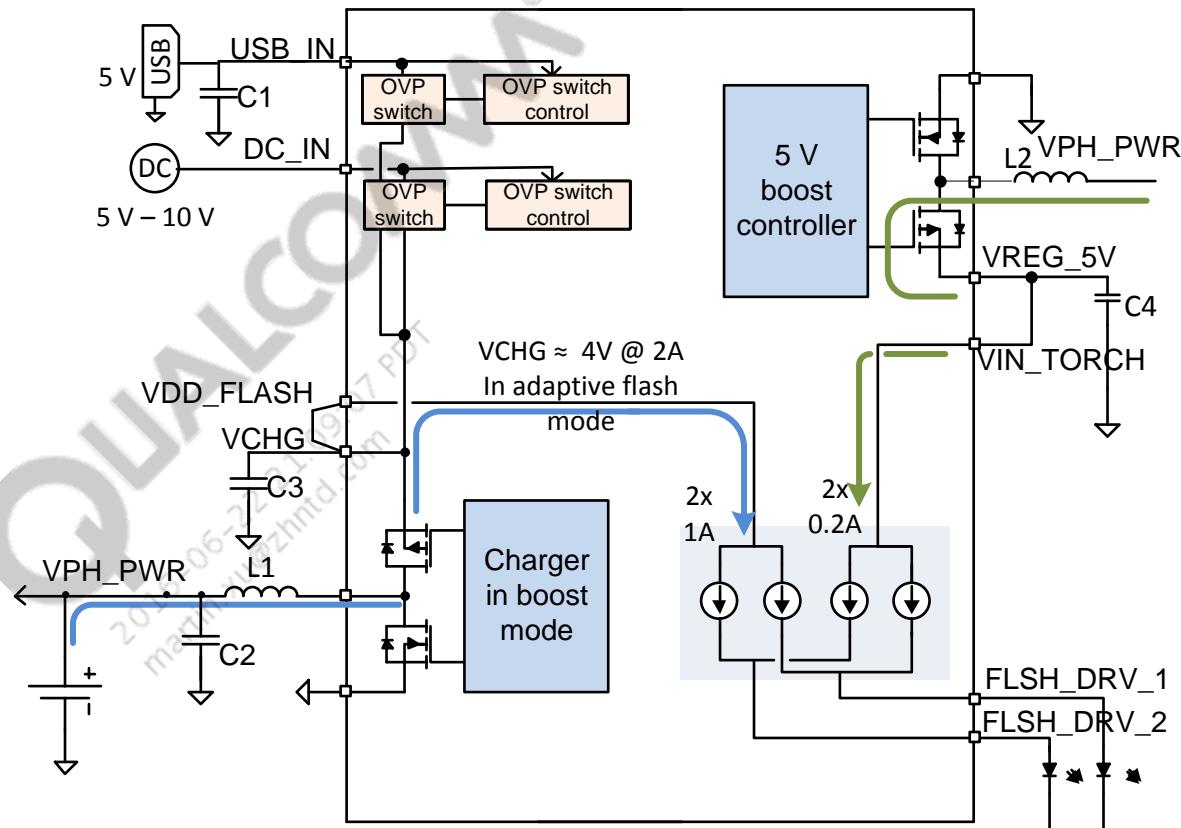
- Uses an internal 5 V boost regulator

Concurrency:

- With class D audio and USB OTG, video current is managed by SW.

Flash	Video
2 x 1 A	2 x 0.2 A

L1	Charger inductor	Toko DFE32251C, 1 $\mu$ H, $I_{sat} = 3.1$ A
C3	VCHG cap	2 x Murata 4.7 $\mu$ F/0603/16 V



Current path for flash mode : from Vph\_pwr to charger in boost mode and then using the 2 x 1 A current driver

Current path for video : from Vph\_pwr to internal boost (5 V, typ) and then using the 2 x 200 mA current driver

Keep FLSH\_DRV loop inductance below 100 nH

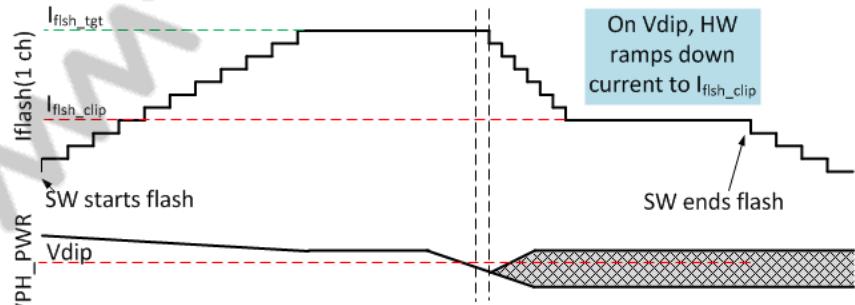
## 2x 1 A Flash Driver Feature Summary

- Two LED channels, independent current control, 12.5 mA step size
- 2x 1 A high side current driver for flash
  - Flash driver uses internal switched mode battery charger as a boost regulator.
  - Boost adaptively regulates supply rail (VCHG) to minimum headroom of 300 mV across the two current sources.
- 2x 200 mA high side current driver for video
  - Torch driver uses internal 5 V boost regulator.
- Supports hardware-controlled (GPIO) or software-controlled flash triggering
- Three mask inputs for current clipping during flash event
  - GSM\_PA\_ON, direct video to flash support, spare
- Low battery voltage monitoring
  - Monitors VPH\_PWR at PMIC pin and clips and/or freezes LED current if Vdip threshold is crossed.
- During flash pulse, the actual current set by software and hardware derating can be read out
- Safety features
  - Flash timeout, video watchdog timer, Open LED/Short LED fault detection, thermal derating during flash, hot LED detection.

# Flash LED VPH\_PWR Voltage Dip ( $V_{dip}$ ) Monitoring and Response

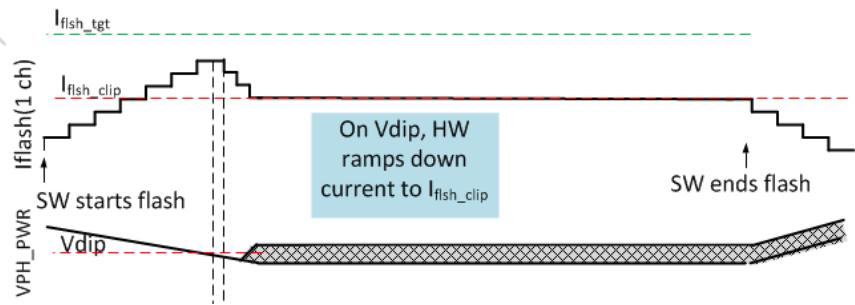
## Use case 1

- Flash is at target current, when an additional load causes  $V_{dip}$
- Hardware quickly ramps flash current down to  $I_{flash\_clip}$  until flash ends



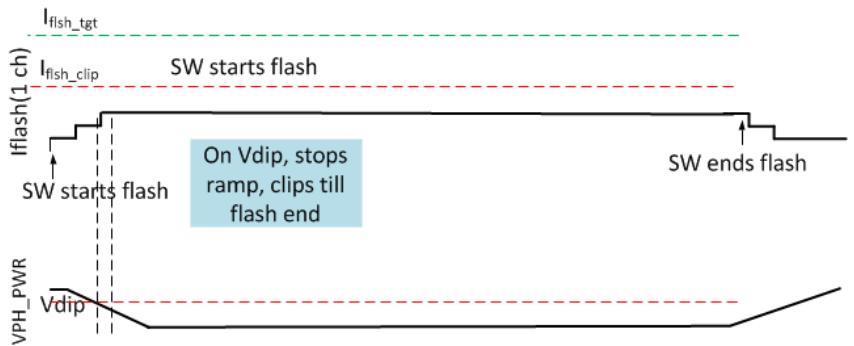
## Use case 2

- Flash current is ramping up, when Battery  $V_{dip}$  threshold occurs
- Hardware will quickly ramp flash current down to  $I_{flash\_clip}$  and keep it there until the flash ends



## Use case 3

- Weak battery, start of flash current causes  $V_{dip}$
- Hardware stops ramp and clips immediately, never reaching  $I_{flash\_clip}$
- Software reads out  $I_{actual}$  current



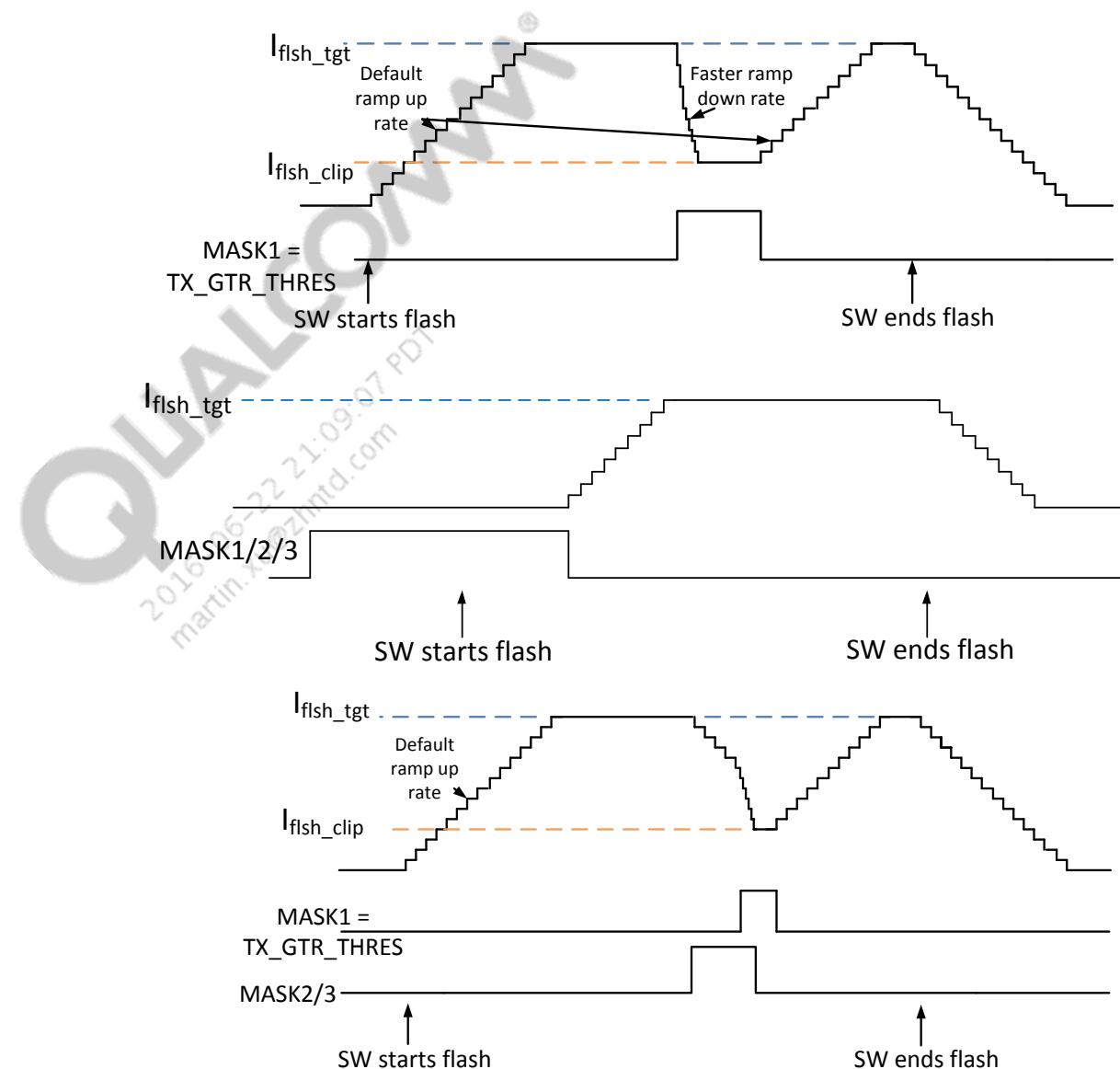
# Flash LED Mask Behavior

Mask 1 is used current reduction from Iflsh\_tgt to Iflsh\_clip during high-power GSM Tx. The MSM device sends Tx\_GTR\_THRES 130  $\mu$ s before PA on ramp.

Mask before software trigger disables Iflsh\_clip ramp until the mask is removed.

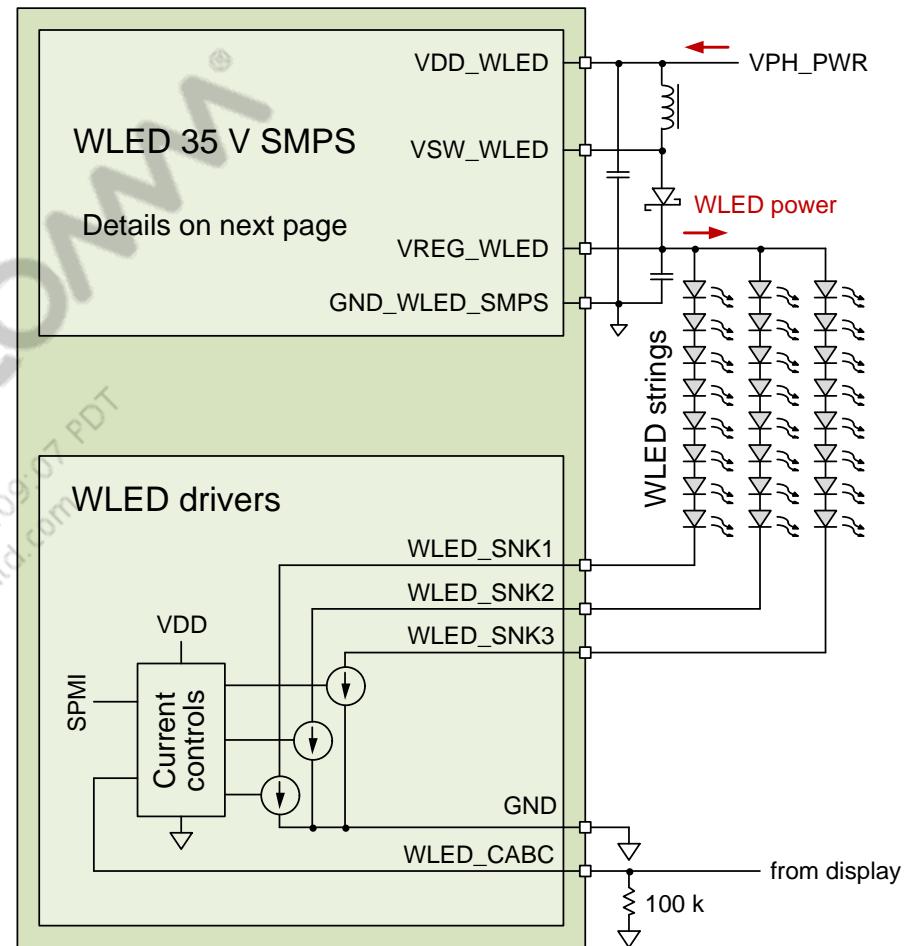
Mask 1 takes priority in ramp down rate over Mask 2/3.

All masks share setting (programmable) for Iflsh\_clip.



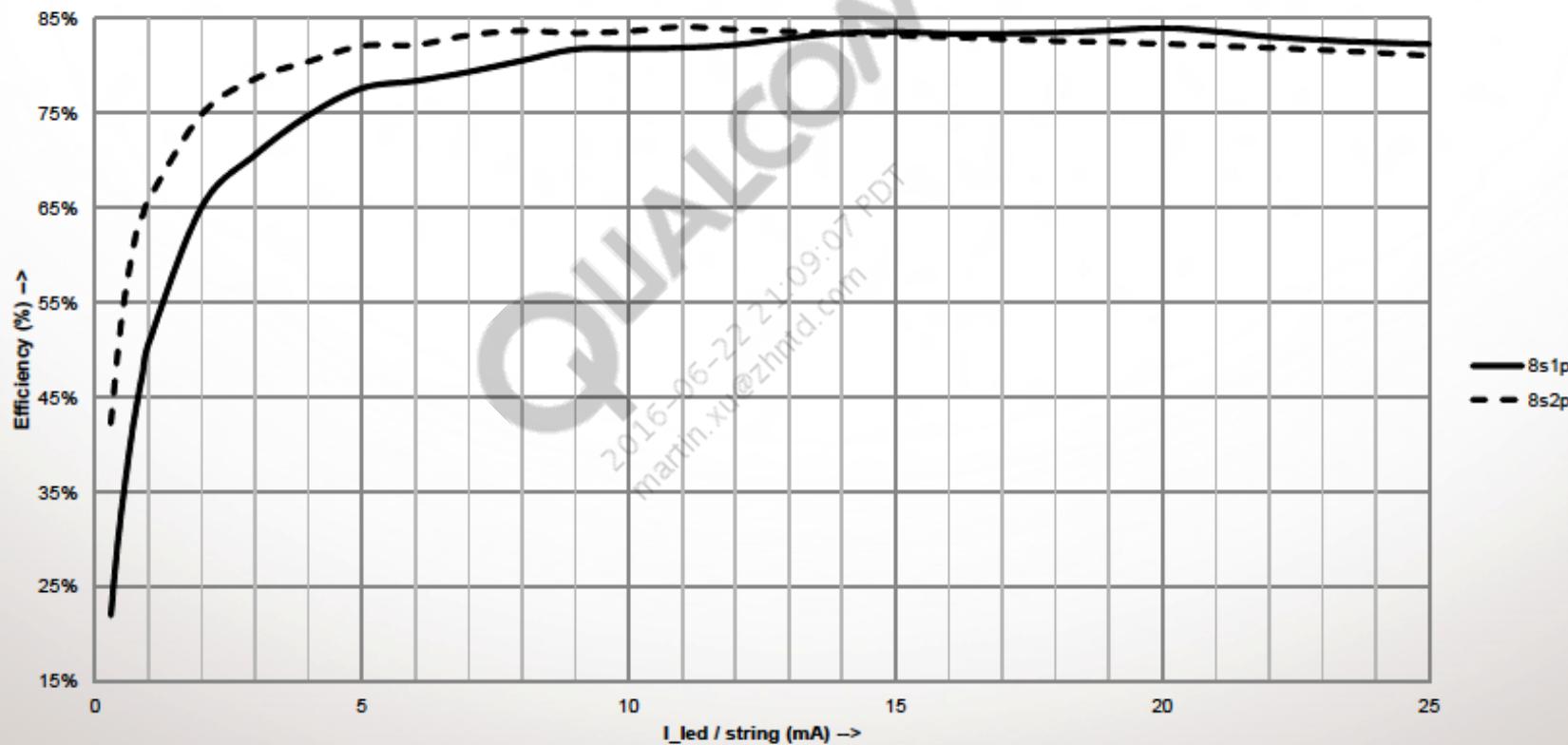
## White LED Support

- Integrated boost SMPS generates the high voltage needed for white LEDs.
  - SMPS details on next page
- Three ground-referenced current sinks.
  - Each support a string of up to eight LEDs
  - 25 mA each
  - Dedicated ground pin
- White LED content adaptive backlight control (CABC) is supported.
  - Connect the WLED\_CABC pin to ground through a 10 k resistor if this feature is not used.
  - Recommended switching frequency for the WLED boost is 800 kHz.

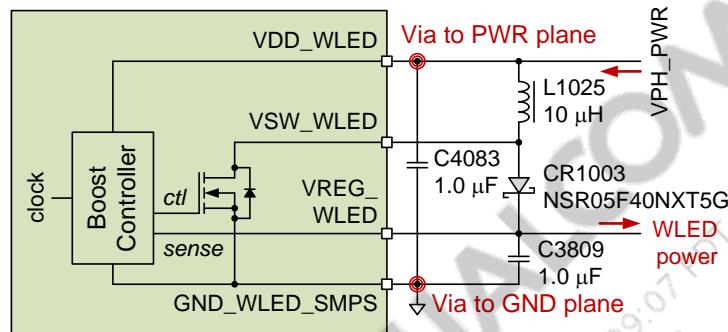


# WLED Boost Efficiency Plot

**VPH\_PWR = 3.6V, fsw = 0.8 MHz, 10  $\mu$ H, 4.7  $\mu$ F**  
**LED = NSSW206AT (~26V@25mA), I\_led / string = 0.3mA-25mA**



# WLED SMPS Schematic and Layout Guidelines



Same placement and layout guidelines apply to the WLED boost SMPS as HF SMPS. Example placement and layout can be seen in the top-level design topics section later in the slides.

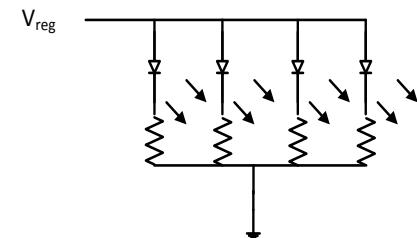
# Home Row Lighting/Key Illumination



2 to 4 WLEDs

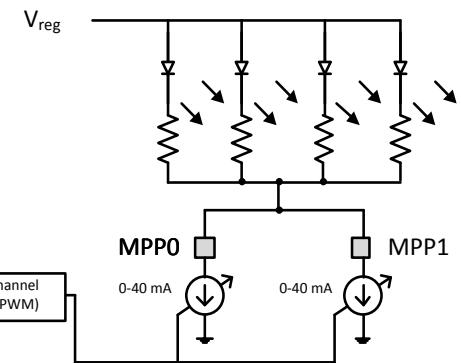
## Option #1

- Four ballast resistors for matching and current limiting
- Power source can be Vsys or regulated supply rail (see the diagram at the right)
- Available in most PMICs



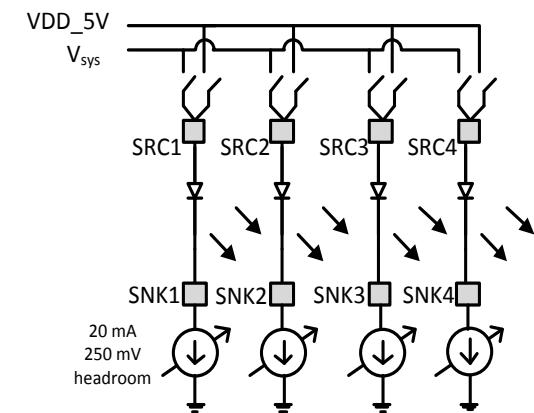
## Option #2

- Use one to two MPPs as current sinks (80 mA total, 500 mV headroom)
- Uses Vsys or regulated rail as power source
- LED brightness is controlled via PWM (6-bit/9-bit LPG output)
- Available in most PMICs



## Option #3

- Four individually programmable current sinks at 20 mA each
- Each current sink controlled via PWM (8-bit resolution)
- 250 mV headroom
- Software switch to Vbst (5 V) when Vsyst drops below threshold
- 2% matching, 2% accuracy



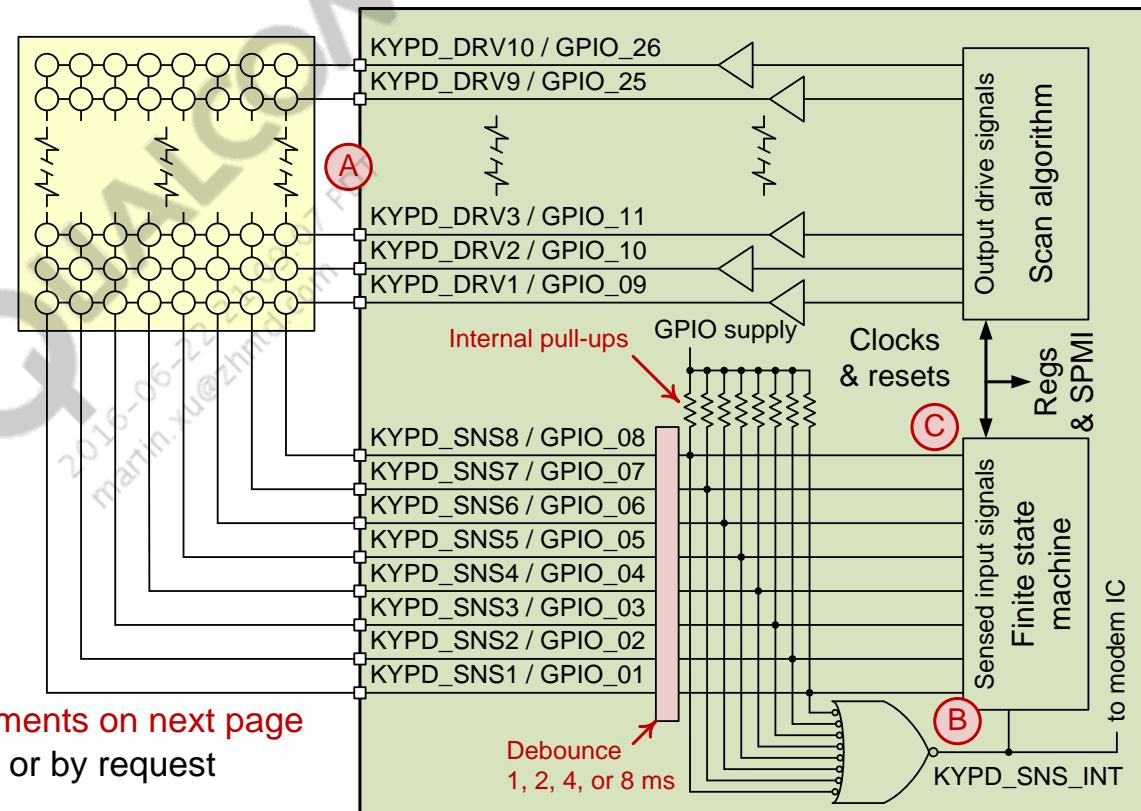
# Keypad Interface

A keypad button press is detected by ORing all column signals (KYPD\_SNSx) together

- Before a keypad button is pressed, all rows are driven low. **(A)**
- When a button is pressed, its corresponding column is pulled low (since all rows are low).
- The interrupt is asserted when any keypad button, from any column, is pressed. **(B)**

When the interrupt signal is received, the FSM requests the next scan.

- During a scan, each row is sequentially driven low, one at a time. **(A)**
- As each row is driven low, the columns are sensed. **(C)**
- The pressed button is identified when that button's column reads low while its row is driven low.



Other operational details – plus **enhancements on next page**

- A scan can be initiated by a key press or by request from FSM to get next keypad entry.
- After a scan, the FSM compares current and last data; an interrupt is generated if there was a change.
- The modem IC must read the stored key presses via SPMI.
- The delay between scans is programmable (4, 8, 16, 32, 64, or 128 ms).

## Keypad Scan Enhancements

Up to 16 keys can be programmed to wakeup the processor, while all others are masked out; masking is bypassed when the full keypad is enabled, ensuring that all keys can generate an interrupt for normal operation.

The wakeup can be executed in response to any of the following conditions:

- A software-defined single key is pressed, and no other keys are pressed.
- A software-defined two-key combination is pressed and no other keys are pressed.
- A software-defined three-key combination is pressed and not other keys are pressed.

The software-defined combinations are mutually exclusive – any key used for the one-key wakeup cannot be used in any other combination.

The one key/two-key/three-key press can be configured to generate a reset.

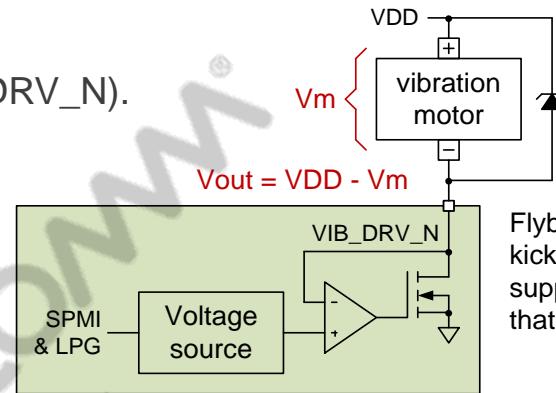
During debounce, the keypad continues to be scanned and sampled.

The entire key combination must be pressed during the reset debounce time to generate the intended warm or hard reset.

# Vibration Motor Driver

The vibration motor driver supports silent incoming-call alarms with a dedicated output pin (VIB\_DRV\_N).

- Programmable voltage output referenced to VDD
- When off, the output voltage is VDD
- Motor connected between VDD and VIB\_DRV\_N
- Voltage across motor is  $V_m = VDD - V_{out}$
- $V_{out}$  is the voltage at the PMIC pin.



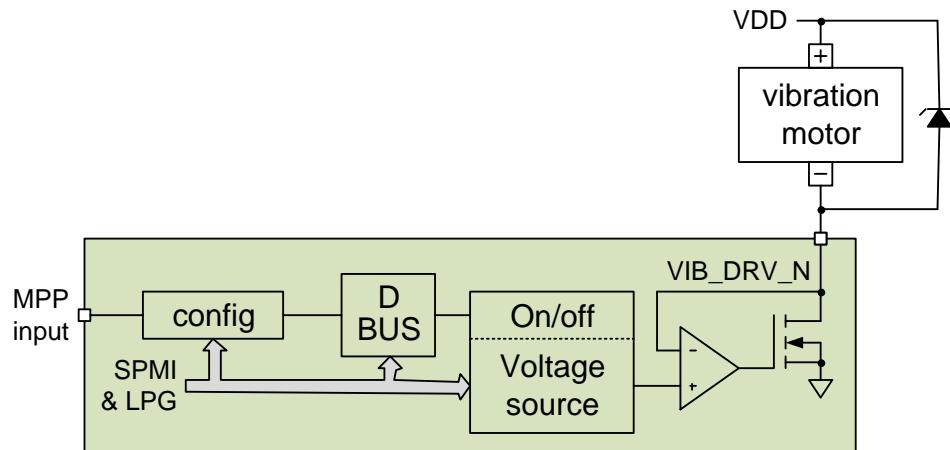
Flyback diode prevents inductive kickback during turn-off, thereby suppressing voltage transients that could damage the IC.

The driver is programmable for motor voltages from 1.2 to 3.1 V in 100-mV increments.

Short circuit current limiting protects the IC when the motor is stalled or shorted.

The PMIC provides the option to control the motor driver through an MPP, thereby providing greater flexibility in defining on and off vibration intervals. The following API software steps are required:

- Configure the MPP as a digital input.
- Define that MPP to be one of three DBUS signals.
- Define the polarity of the control signal.
- Define the vibration motor driver on/off control to the same DBUS signal.



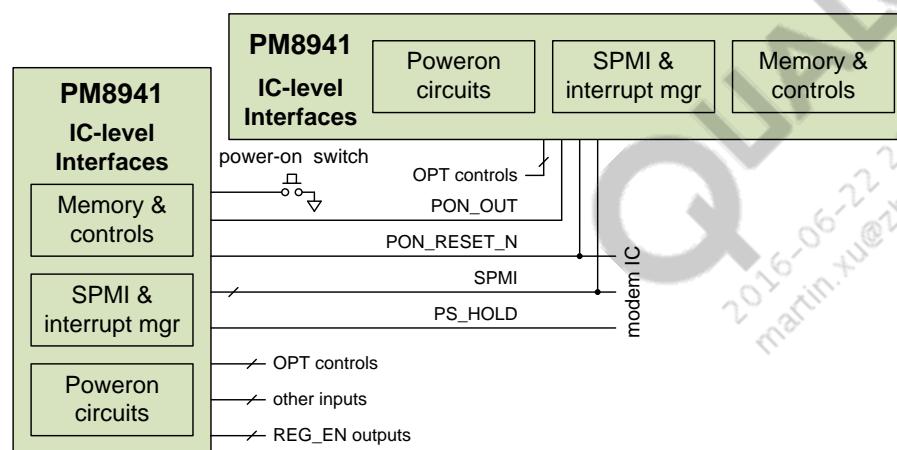


## Section 7

# IC-level Interfaces

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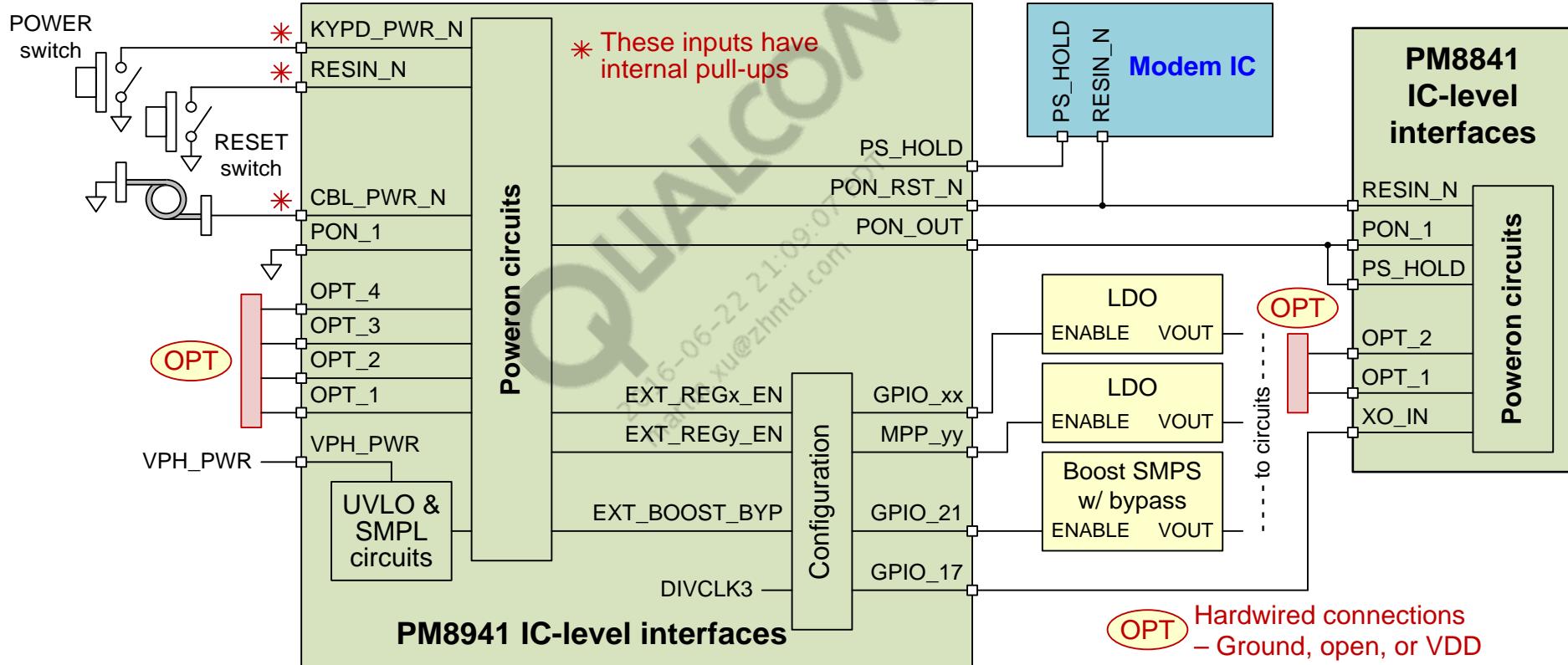
# IC-level Interfaces Content



- Poweron circuits and coordination between PMICs
- OPT hardware configuration controls
- Programmable boot sequence (PBS)
  - Use cases
  - Triggers
  - Programming
- Poweron/poweroff sequence
- Resets
  - Nomenclature
  - Reset sources
  - 3-stage reset
  - Reset timers
- Under-voltage lockout
- Sudden momentary power loss (SMPL)
- SPMI and interrupt managers
- Modem power management support
- Battery UICC alarm (BUA) interface
  - Introduction
  - Overview
  - Operation
- Other IC-level interface uses for MPPs and GPIOs

# Poweron Circuits

- Dedicated PM8941 circuits continuously monitor events that might trigger a poweron sequence.
- If an event occurs, these circuits power on the IC, determine the handset's available power sources, enable the correct source, enable the PM8841, and take the modem IC out of reset.



- To power up immediately upon battery insertion, tie KYPD\_PWR\_N or CBL\_PWR\_N to ground
- In this case, the PMIC is always on and the modem IC should clear the xxxPWR\_PU bit to turn-off the internal pull-up resistor, thereby reducing the PMIC quiescent current.

## PM8941 OPT Hardware Configuration Controls (1 of 2)

Four PM8941 pins – OPT\_[4:1] – must be hardwired to ground or VDD, or be left open (in a high-impedance state or Hi-Z); the settings of these four pins define or influence the following PM8941 parameters.

Each chipset that uses the PM8941 must set the OPT pins correctly for their particular application; the MSM8x74-based reference designs use these settings: OPT\_[4:1] = GND, GND, GND, GND.

OPT_1	External reset configuration
GND	KYPD_PWR_N + RESIN_N
Hi-Z	RESIN_N
VDD	KYPD_PWR_N

OPT_2	Chipset support
GND	MSM8974
Hi-Z	Reserved
VDD	Reserved

## PM8941 OPT Hardware Configuration Controls (2 of 2)

OPT_3	PMIC watchdog
GND	Disabled
Hi-Z	Enabled
VDD	Reserved

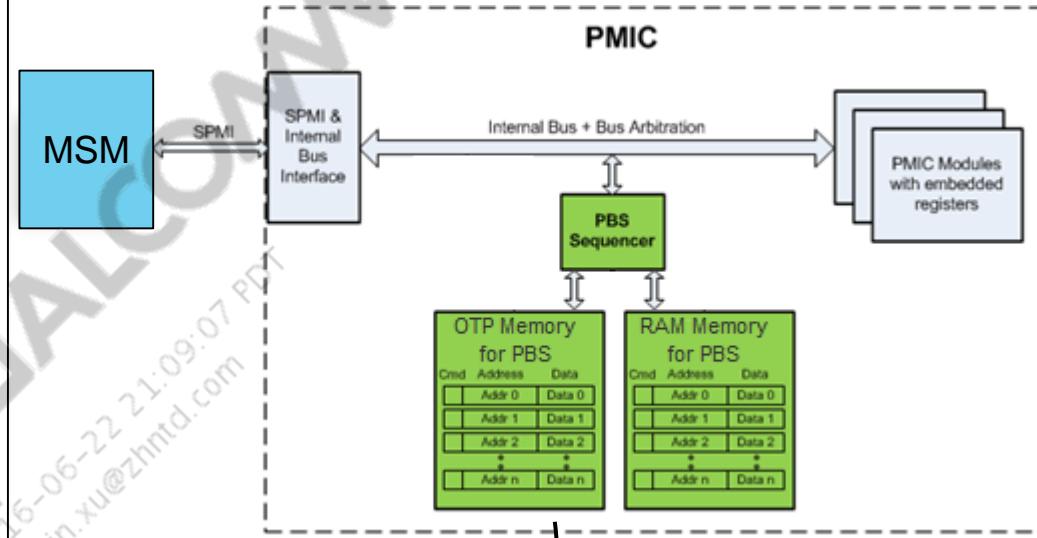
OPT_4	Chipset support
GND	MSM8974
Hi-Z	Reserved
VDD	Reserved

# Programmable Boot Sequence (PBS)

## Key features:

- Custom **programmable boot sequences** configured with OTP and RAM.
- Implemented as a series of address + data transactions which mimic normal software control.
- Programmable control of any PMIC resource in any order with any available programmable configuration.
- Support for **API-like routines** are implemented with OTP-defined sequences. Initiate via SPMI write to address pointer or via hardware trigger.
- Support for a **limited command set** of executable functions.

PBS illustrative concept drawing



### PBS command set

- Write/read
- Delay
- Compare
- End-of-sequence
- Up to 256 commands supported in RAM
- Up to ~232 commands supported in ROM (OTP) with some space reserved for PTE, version control

## PBS Use Cases

### Poweron sequence (OTP)

- Make decisions based on the state of option pins or other registers.
- Enable regulators, change GPIO/MPP states.
- Wait for event to occur (register to change state, timer to expire).
- Change register defaults (e.g., charger limits) prior to enabling module.

### Poweroff sequence (OTP)

### Custom poweroff sequence (RAM)

- Blink LED, toggle vibrator motor, etc., as handset shuts down.

### Battery UICC alarm (RAM)

- Disables LDOs based on hardware triggers (battery removal, UICC card removal).

### Sleep/wake batch sequence

- Several writes can be done quickly when entering/exiting sleep to reduce software workload.
- Can vibrate the VIB motor before initiating shutdown operation.

## PBS Triggers

- There are 16 different PBS clients in PM8941 and 8 in PM8841.
- Each client can be programmed to point to any address within OTP or RAM.
- Each client can trigger a sequence via software (e.g., register write) or a hardware trigger (see the list below).

### PM8941

- Trigger 1 – Secondary poweron
- Trigger 2 – Primary poweron
- Trigger 3 – Warm reset
- Trigger 4 – Shutdown
- Trigger 5 – XO\_OUT\_D0\_EN
- Trigger 6 – XO\_OUT\_D1\_EN
- Trigger 7 – Battery UICC alarm
- Trigger 8 – Reserved
- Trigger 9 – Pre-poweron
- Trigger 10 – Sleep
- Trigger 11 – RTC alarm
- Trigger 12 – RTC timer
- Trigger 13 – DTEST1
- Trigger 14 – DTEST2
- Trigger 15 – DTEST3
- Trigger 16 – DTEST4

### PM8841

- Trigger 1 –Secondary poweron
- Trigger 2 – Primary poweron
- Trigger 3 – Warm reset
- Trigger 4 – Shutdown
- Trigger 5 – DTEST1
- Trigger 6 – DTEST2
- Trigger 7 – DTEST3
- Trigger 8 – DTEST4

# Poweron/Poweroff/Warm Reset Sequence

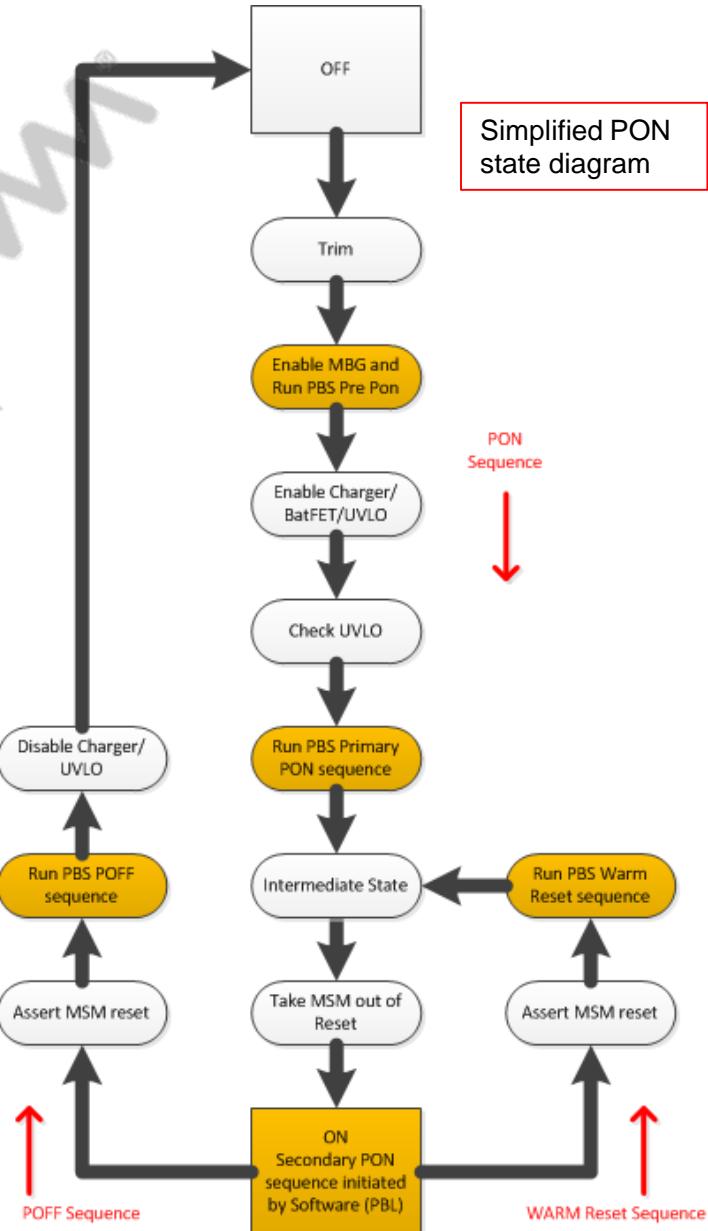
PBS is run three times during poweron.

- Configure features (e.g. charging) prior to enabling anything in the system.
- Enable the minimum infrastructure required to boot MSM and start fast low current boot image (FLCB).
- Enable Krait, eMMC, etc., once it is established that the battery is sufficient, or a charger is available.

PBS runs once during shutdown for regulator sequencing.

- Can also support shutdown indication (e.g., flash LED).

PBS runs once during warm reset.



2016-06-22 21:09:07 PDT  
martin.xu@zhntd.com

# PBS Programming

## PBS OTP

- Programmed during ATE by QTI; customers cannot modify it.
- Option pins allow for adjustment of the sequences or to set certain features within the PMIC.
- Some area needs to be reserved for future enhancement or workarounds.

## PBS RAM

- For bringup, programmed during SBL.
- Can be reprogrammed at anytime by software.
- PBS programming must be handled by trusted software.
- Some space will be reserved by QTI during development, but these sequences can potentially be moved into OTP prior to CS.
  - RAM sequences can prepend some ROM sequence (e.g., during POFF sequence, customer-specific POFF sequence is run and then it calls the OTP POFF sequence).

## Dual Poweron Sequence (1 of 2)

1. PM8941 receives a poweron trigger (e.g., KPD\_PWR\_N press).
2. PM8941 poweron sequence begins (PBS sequence runs). The following events take place:
  - BMS OCV measurement occurs.
  - EXT\_REG\_EN1 is asserted (VPH\_PWR) to enable external supplies.
  - PON\_OUT is asserted (1.8 V) to enable PM8841.
  - A timer starts to allow PM8841 to complete his sequence.
3. PM8841 receives poweron trigger (PON\_1 and PS\_HOLD are asserted).
4. PM8841 poweron sequence begins (PBS sequence runs). The following events take place:
  - S1 is turned ON (memory supply).
  - S2 is turned ON (core supply).
5. PM8841 PBS primary poweron sequence completes. Since PM8841 PS\_HOLD is already high, the PM8841 enters ON state.
6. PBS sequence on PM8941 continues.
  - The timer on PM8841 expires.
  - The regulators in primary poweron sequence are enabled in several steps.
7. The PM8941 PBS primary poweron sequence completes. PM8941 PON module deasserts PON\_RESET\_N and sets PS\_HOLD timer.
8. Once PON\_RESET\_N is deasserted, MSM comes out of reset. and PBL asserts PS\_HOLD. PM8941 enters ON state.
9. MSM SPON (Secondary PON) message to PM8941 and PM8841
10. PBS in PM8941 and PM8841 run the secondary poweron sequence.

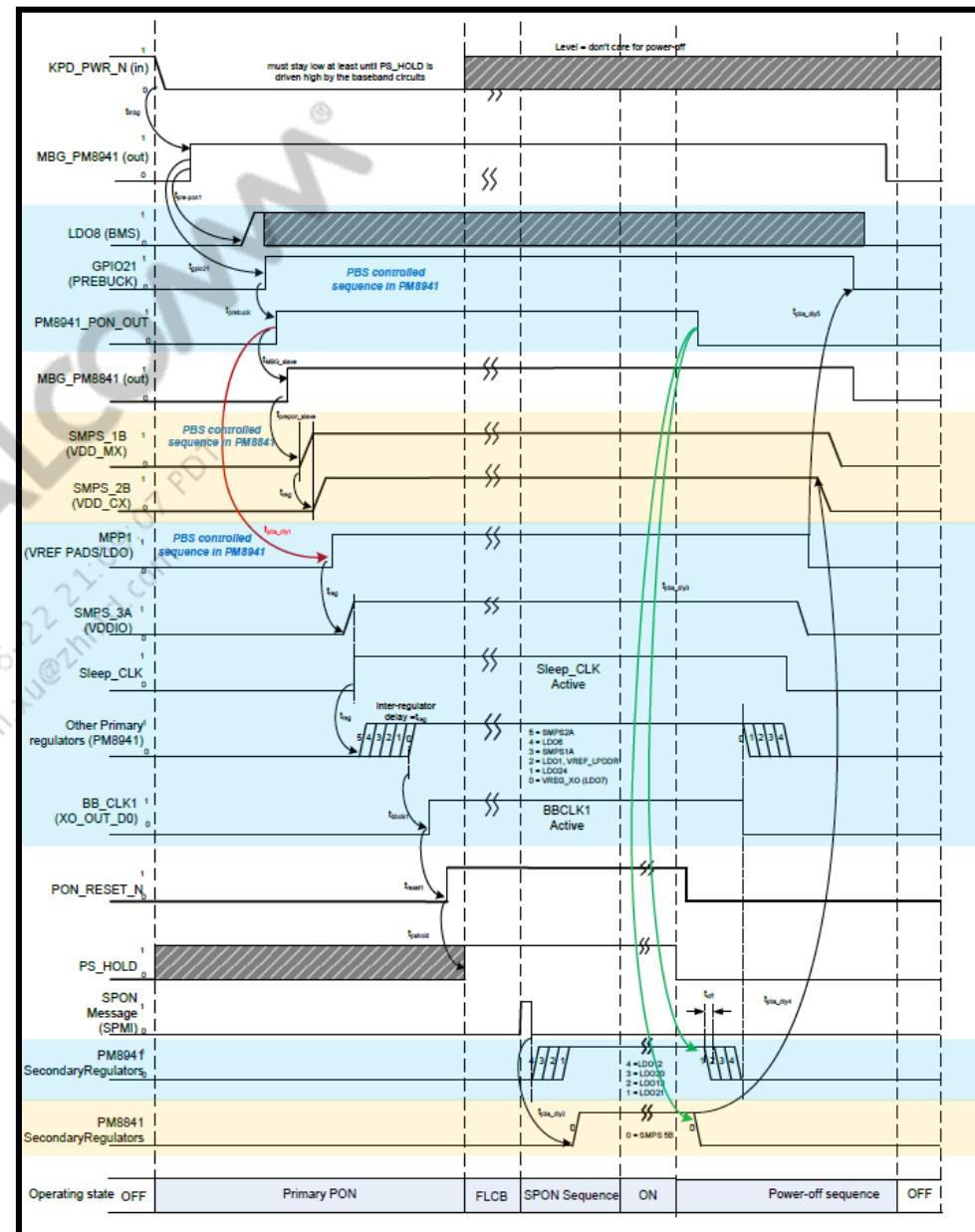
## Dual Poweron Sequence (2 of 2)

Poweron sequence spans PM8941 and PM8841

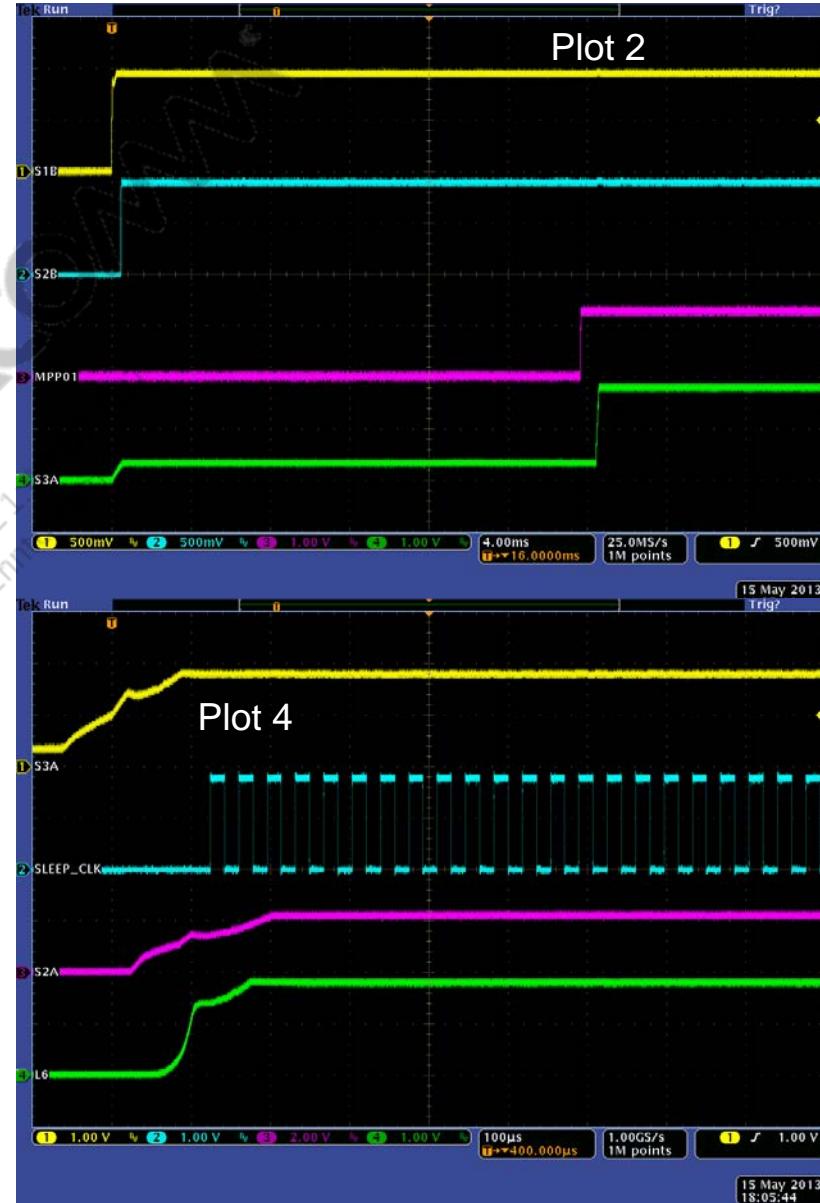
Split into two parts (both in OTP)

- Primary poweron sequence
- Secondary poweron sequence

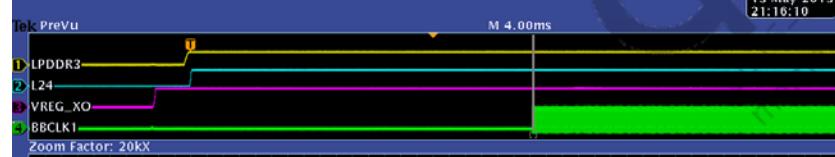
**Note:** See the example plots of power on and power off sequences measured on MSM8974 CDP in the next few slides.



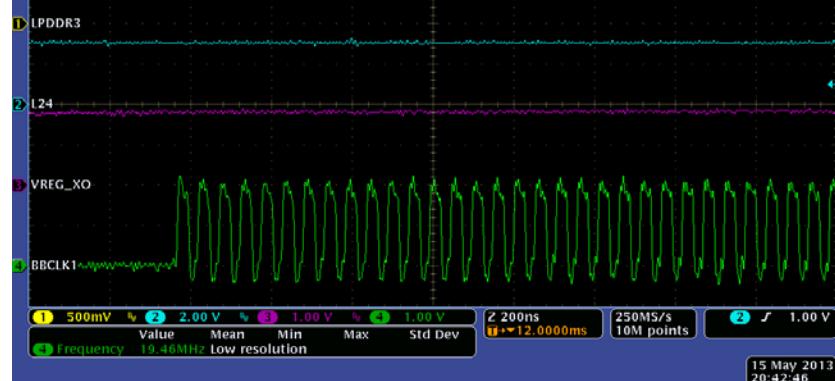
# Poweron Sequence Captured on MSM8974 CDP (1 of 3)



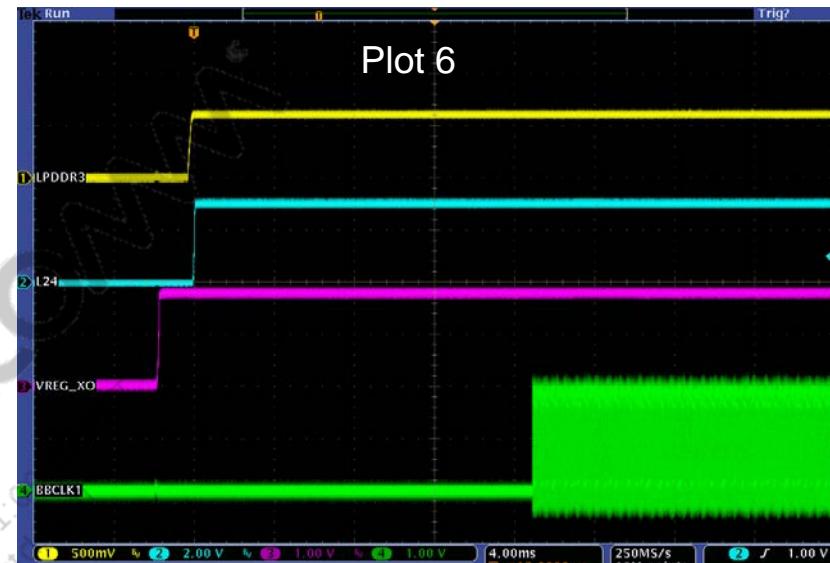
# Poweron Sequence Captured on MSM8974 CDP (2 of 3)



Plot 7



Plot 6



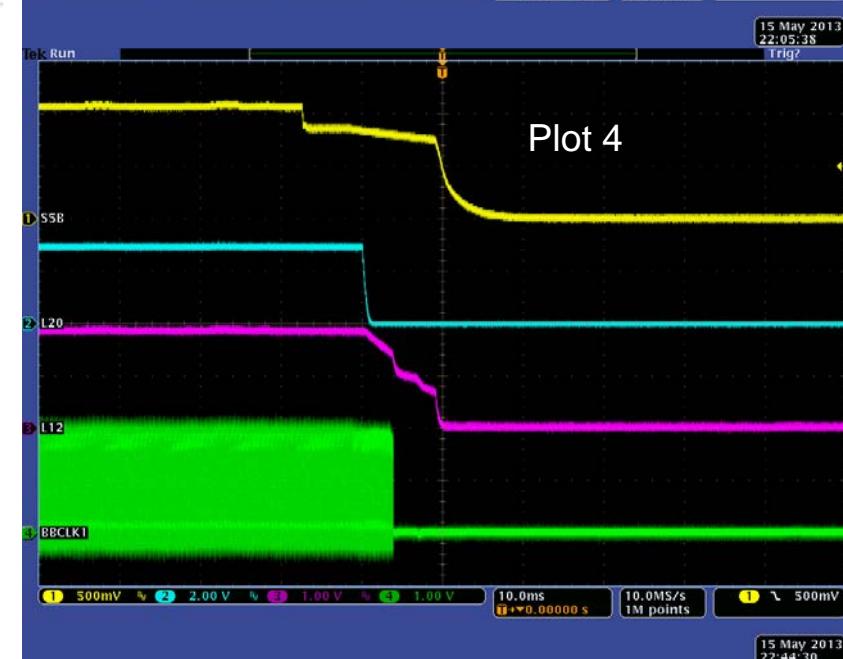
Plot 8



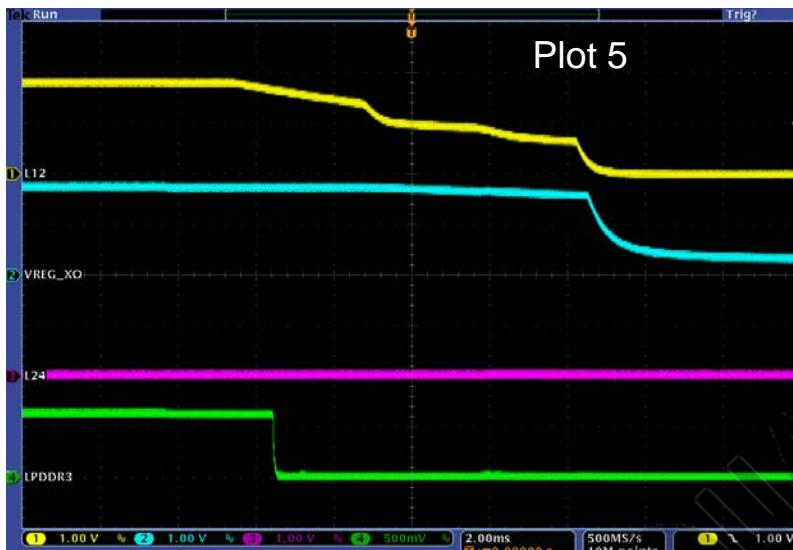
# Poweron Sequence Captured on MSM8974 CDP (3 of 3)



# Poweroff Sequence Captured on MSM8974 CDP (1 of 3)



# Poweroff Sequence Captured on MSM8974 CDP (2 of 3)



# Poweroff Sequence Captured on MSM8974 CDP (3 of 3)



## Resets – Nomenclature

### Reset triggers

- Internal and external triggers that are routed to the PMIC's poweron module. The poweron module decides what action should be taken, based on these triggers (e.g., over-temperature stage 3, KYPD\_PWR\_N, and RESIN\_N, PS\_HOLD).

### Reset types

- Describes the behavior of the PMIC during a reset or shutdown event (e.g., warm reset or hard reset event).
- The type of reset event is determined by configuration registers in the poweron module and broadcast throughout the PMIC using reset signals.

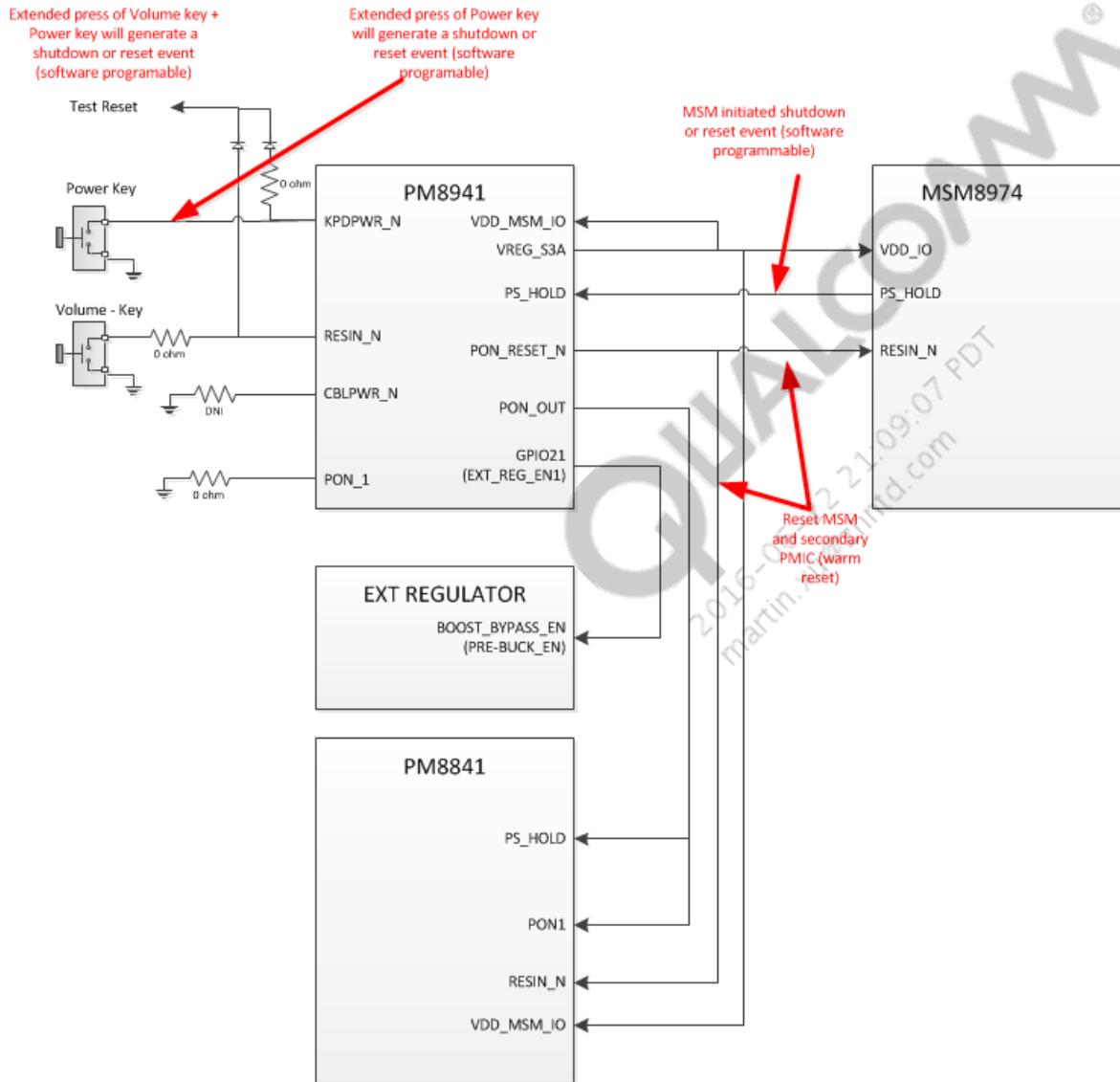
### Reset signals

- Signals that are generated in the poweron module and broadcast throughout the PMIC (e.g., xVdd\_rb, dVdd\_rb, global\_soft\_rb, and shutdown1\_rb).
- (Register) reset domains.
- Several reset domains exist to allow some PMIC registers to maintain state throughout certain reset events.

### Reset stages

- Three stages of resets: software configurable bark, software configurable reset, and failsafe reset.

# External Reset Block Diagram



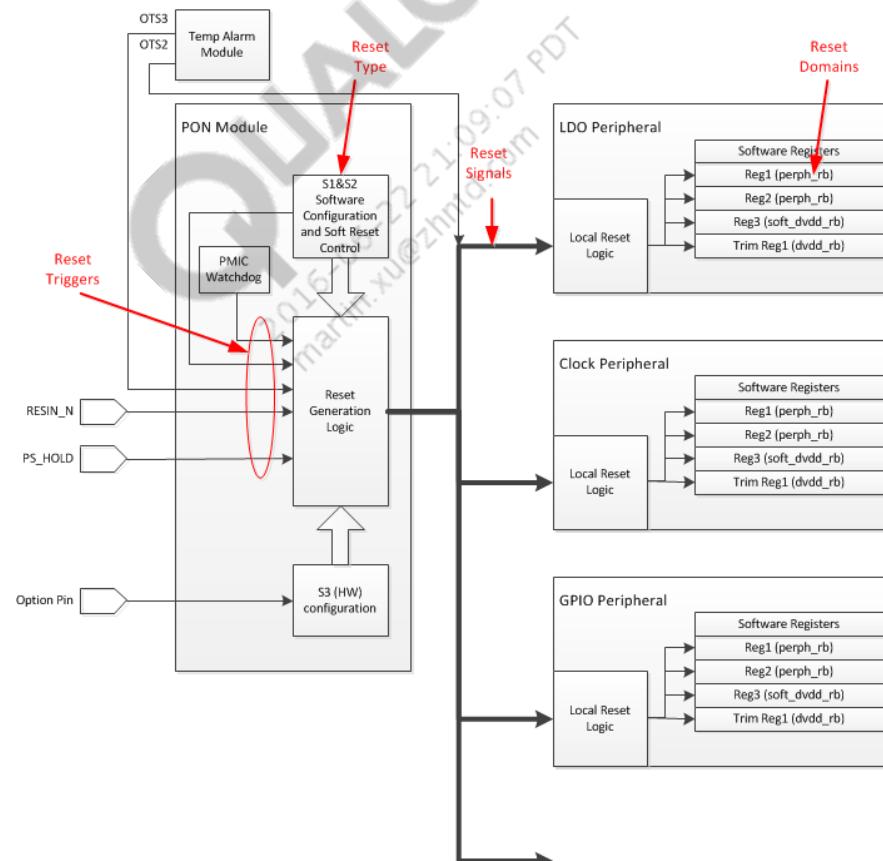
## Sources of reset (programmable)

- Power button (KYPD\_PWR\_N)
- Reset button (RESIN\_N)
- Power button + reset button
- Apps processor (PS\_HOLD)
- Keypad combination (up to three keys)
- Software write
- PMIC watchdog
- PMIC over-temperature sensor
- UVLO (mandatory immediate shutdown)

# Peripheral/Module Resets and Internal Reset Block Diagram

PMIC supports multiple triggers for reset

- (e.g., poweron button, overtemp, PS\_HOLD (apps processor), and dedicated reset button)
- By default, all peripherals will follow all resets.
- Software can individually configure each peripheral to ignore each reset trigger individually according to mask.
  - Maintain core rails during watchdog reset (for debug)
  - Maintain LCD backlight during reset (maintain LCD content through reset)



## 3-Stage Reset

### Stage 1 (software-configurable bark)

- PMIC generates interrupt, giving the MSM device the opportunity to fix the problem or gracefully reset the system. Example events that can cause a bark:
  - ▣ Overtemperature indicates system is getting too hot.
  - ▣ PMIC watchdog indicates that it has not kicked.

### Stage 2 (software-configurable bite)

- If reset is ignored, PMIC will force a reset event (selectable by software).

### Stage 3 (hardware-mandatory bite)

- User can generate a mandatory reset by long key press of RESIN\_N, KYPD\_PWR\_N or RESIN\_N and KYPD\_PWR\_N in combination (selectable via OPT\_1 pin setting as shown below).
  - ▣ Cannot be disabled by software
  - ▣ Resets PMIC back to factory default
  - ▣ Only intended as a backup option if stage 1 and stage 2 fail

#### OPT\_1 pin connection

VDD → KYPD\_PWR\_N  
Hi-Z → RESIN\_N  
GND → RESIN\_N + KYPD\_PWR\_N

## Reset Timers

#	Reset trigger	Stage 1 reset (debounce) timer	Stage 2 reset (delay) timer	Stage 3 reset timer
1	KYPD_PWR_N <sup>a, c</sup>	0–10.256 sec	0–2 sec	0 sec 2–128 sec
2	RESIN_N <sup>a, c</sup>	0–10.256 sec	0–2 sec	
3	KYPD_PWR_N + RESIN_N <sup>a, c</sup>	0–10.256 sec	0–2 sec	
4	Keypad press <sup>a</sup>	0–10.256 sec	0–2 sec	
5	PMIC watchdog <sup>b</sup>	0–127 sec	0 -127 sec	N/A
6	PS_HOLD	N/A	N/A	N/A
7	Global reset	N/A	N/A	N/A
8	Over-temperature reset	N/A	N/A	N/A

- a. Each reset trigger has individual debounce and delay timers. The default value of the debounce and delay timers are 10.256 sec and 2 sec, respectively. The reset triggers share the same stage 3 reset timer.
- b. The default value of the debounce and the delay timers for the PMIC watchdog reset is 31 sec and 1 sec.
- c. The default value of S3 timer is 64 sec or 100 sec depending on whether internal low frequency RC oscillator is in 32 kHz mode or 50 kHz mode.

# Under-Voltage Lockout (UVLO)

The UVLO circuit automatically turns off the PM8941 at severely low VDD conditions.

Although UVLO is a hardware feature, it allows for software interaction to realize additional features, such as SMPL recovery, poweron sequence abort, and watchdog timeout soft reset.

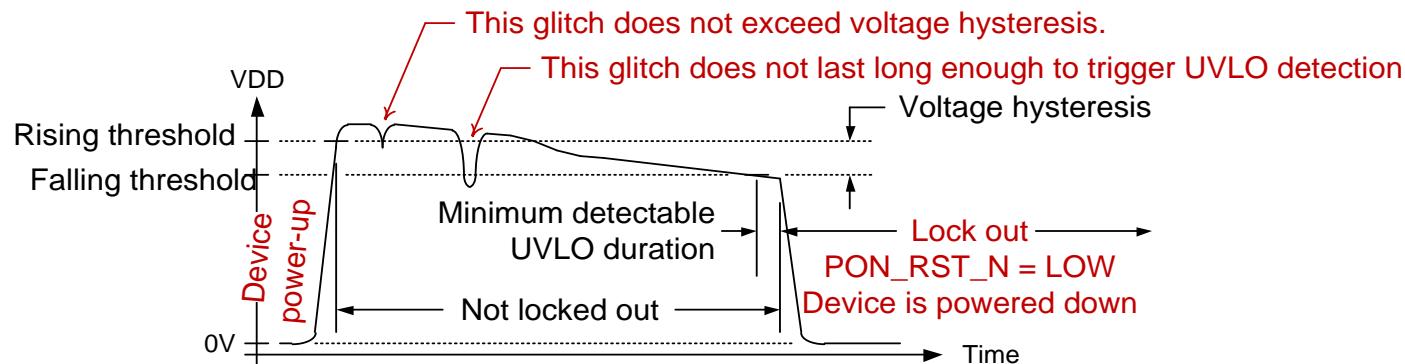
## Operation

- As the IC powers up, VDD must exceed a rising threshold (2.725 V, default) to initiate the poweron sequence.
- Voltage hysteresis (175 mV, default) and delays prevent minor glitches from being detected as UVLO events.
- If VDD drops below the falling threshold (UVLO rising threshold minus voltage hysteresis) for sufficient duration, a valid UVLO event is detected.
  - PON\_RST\_N is cleared (LOW) and the device is powered down.

## The UVLO rising threshold voltage is programmable.

- 1.675 V to 3.225 V in 50 mV increments (2.725 V, default)
- Other than this programmable threshold, software is not involved in UVLO detection.
- Hysteresis and time delays are not programmable, and UVLO events do not generate interrupts; they are reported to the modem IC via PON\_RST\_N as part of powerdown.

PMIC SBL settings	UVLO rising threshold		UVLO falling threshold	
	Default setting	SBL setting	Default setting	SBL setting
PM8941	2.725 V	2.775 V	2.550 V	2.475 V
PM8841	2.725 V	1.675 V	2.550 V	1.500 V



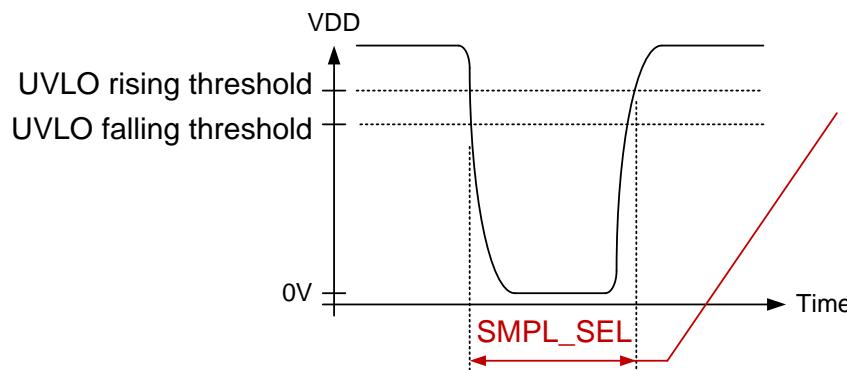
# Sudden Momentary Power Loss (SMPL)

When enabled by software → immediate and automatic recovery from a momentary PM8941 power loss.

- If VDD drops out of range (< 2.475 V nominal), then it returns in-range within a programmable interval of between 0.5 and 2.0 seconds, and the recovery is executed.

## Some operational details:

- UVLO event clears PON\_RST\_N; PMIC is powered down.
- Super capacitor or coin cell takes over as SMPL power source.
- If VDD returns to its valid range before timeout, a poweron sequence is initiated without software intervention, and an interrupt is sent to the modem IC indicating: 1) Power was momentarily lost, 2) RTC is corrupted due to insufficient voltage, and 3) Current PMIC actions are not a user initiated power-on sequence.
- If SMPL times out without VDD returning to its valid range – the handset must undergo normal poweron sequence whenever the next initializing event occurs.
- SMPL operation must be enabled by software and requires a coin cell or keep-alive capacitor (values listed below) at VCOIN.
- For a normal powerdown, SMPL must be disabled via software before de-asserting PS\_HOLD to avoid an inadvertent SMPL override.

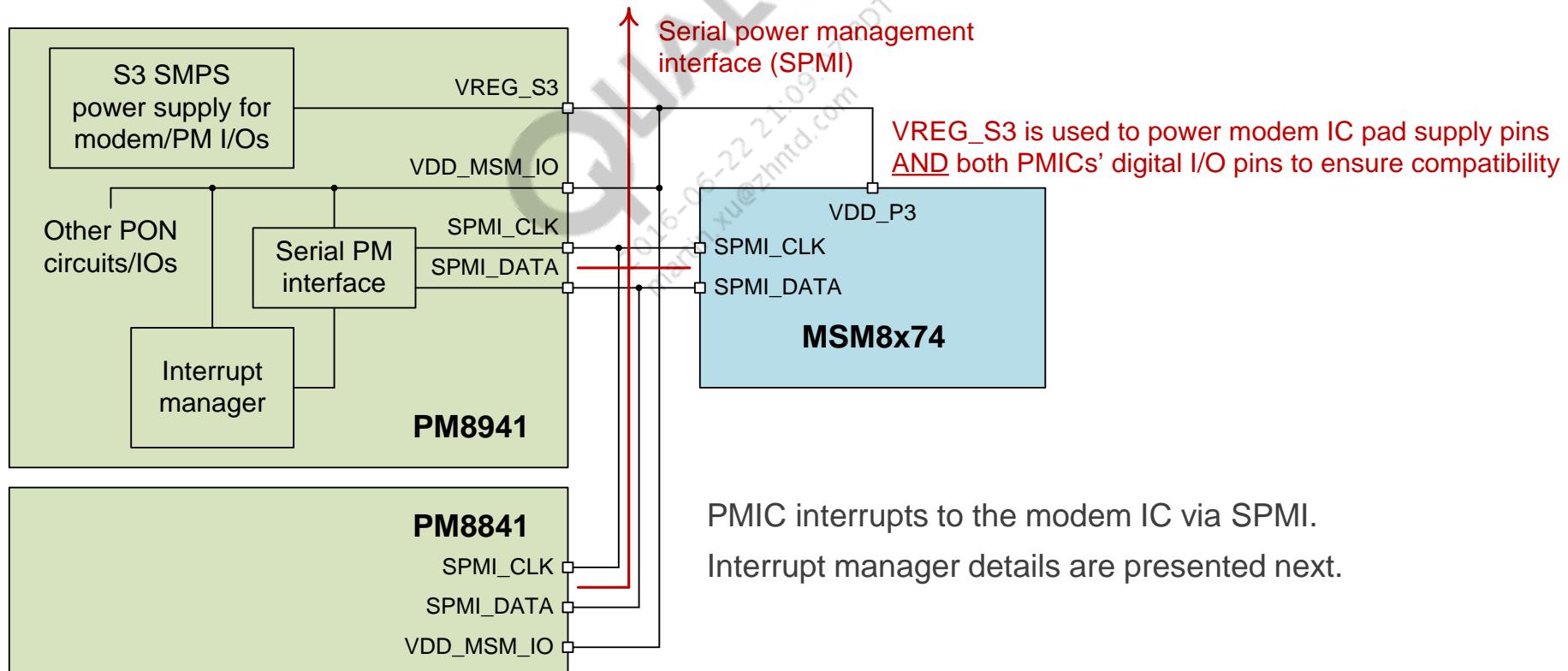


If VDD recovers within this programmed interval a poweron sequence is immediately and automatically initiated by power management circuits without software intervention.

If RTC support is not needed when battery is removed, a backup capacitor can be used on VCOIN pin. A ceramic capacitor with an effective capacitance of 10  $\mu$ F can support SMPL for up to 2 seconds.

## SPMI and Interrupt Manager

- SPMI – primary IC-level interface for efficient initialization, status, and control communications.
- Application programming interface (API) is used to program PMICs, indirectly exercising SPMI.
- The coin cell backs up several SPMI registers; at powerup, SPMI defaults are restored, except bits backed up by the coin cell – they are only restored to default values if the coin cell expired.



# Interrupt Manager Details

An interrupt manager receives internal reports on numerous functions and conveys status signals to the modem device, supporting its interrupt processing.

Each interrupt event has the following associated SPMI bits:

- Interrupt mask (read/write) – allows modem IC to ignore event; latched status hidden and interrupt are not asserted.
- Interrupt real-time status (read only) – follows realtime interrupt status (active or inactive) for standard configuration interrupts; special configuration interrupts are highlighted in red and defined further below.
- Interrupt latched status (read only) – set when event is active and interrupt mask bit is cleared; stays set until clear bit is set.
- Interrupt clear (read/write) – clears latched status automatically after latched status is read.

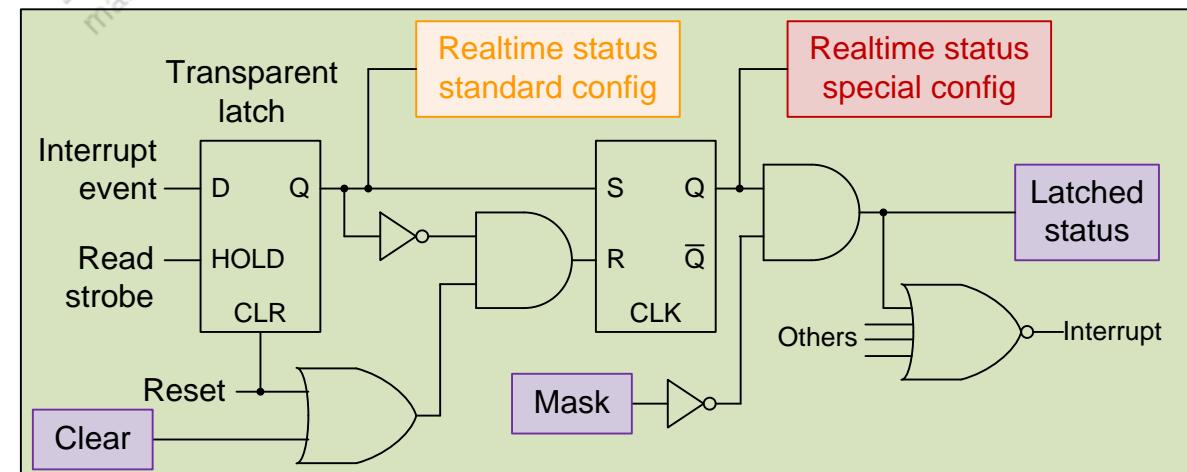
Unmasked interrupts notify the modem device that at least one interrupt has occurred.

Upon powerup, software should check the RTCRST interrupt – if set, the coin cell voltage is too low, and the RTC and SRAM contents and the SMPL and WDOG interrupts are unreliable.

Most interrupts are standard (orange), but four are special (red) interrupts:

- Real-time clock reset (RTCRST)
- Sudden momentary power loss (SMPL)
- MDM watchdog timeout (WDOG)
- Die over-temperature (OVERTEMP)

These are not realtime readable – they occur only when the PMIC is reset or when they cause a PMIC reset. They are latched and backed up via coin cell. Upon a PMIC restart, latched interrupts inform the modem device why they were triggered.

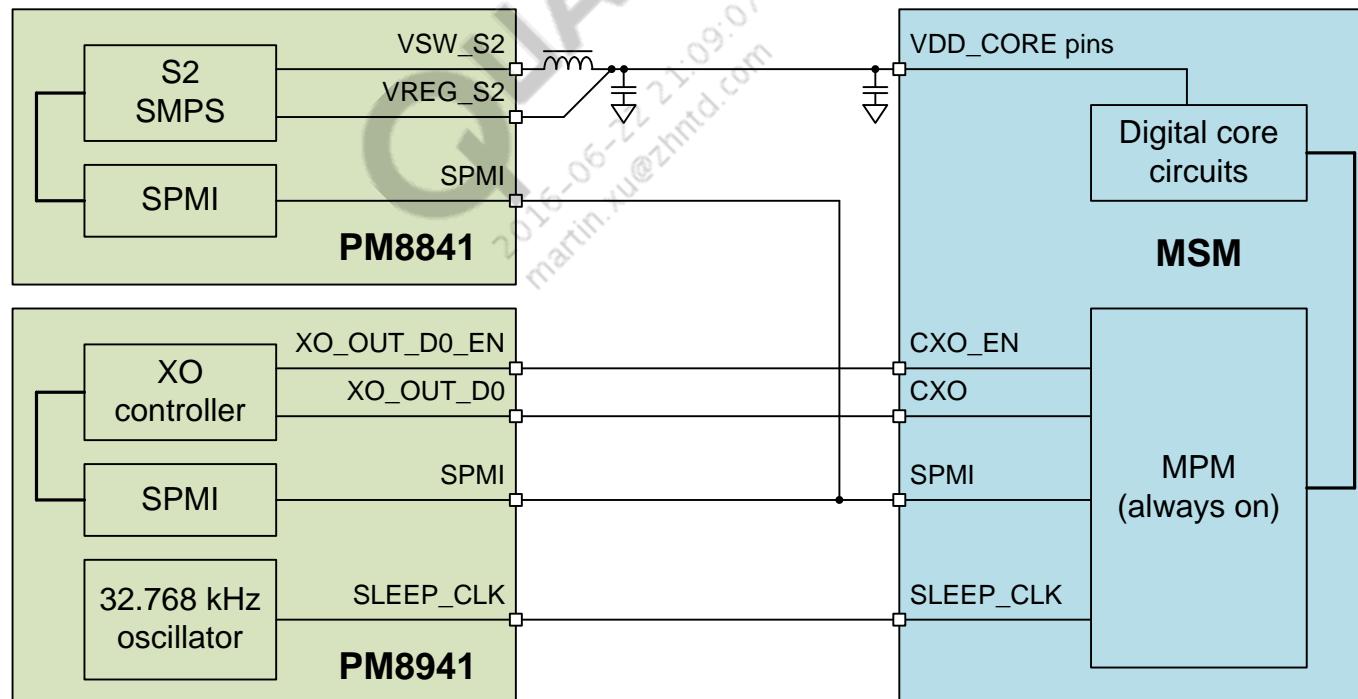


## Modem Power Management Support (1 of 2)

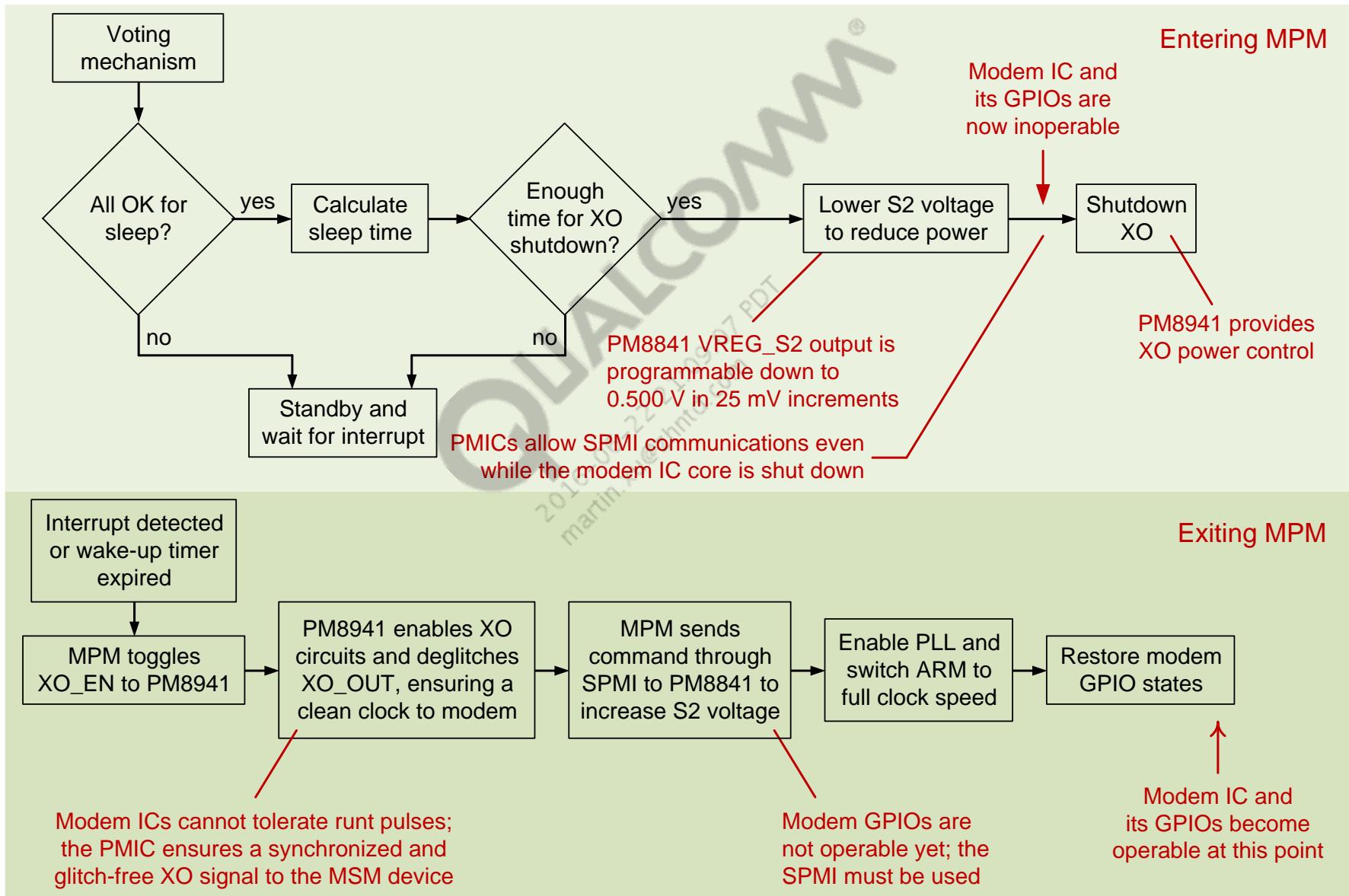
SPMI is able to communicate with the modem IC, even while its core circuits are powered down. PMIC features necessary to support MPM:

- Key regulator outputs programmable to 750 mV.
- SPMI continues modem communications, even while the modem IC core is powered down.
- The PMIC controls the XO power supply.
- The PMIC ensures a synchronized and glitch-free XO signal for the modem device.

Connections required for MPM support are illustrated below.



## Modem Power Management Support (2 of 2)



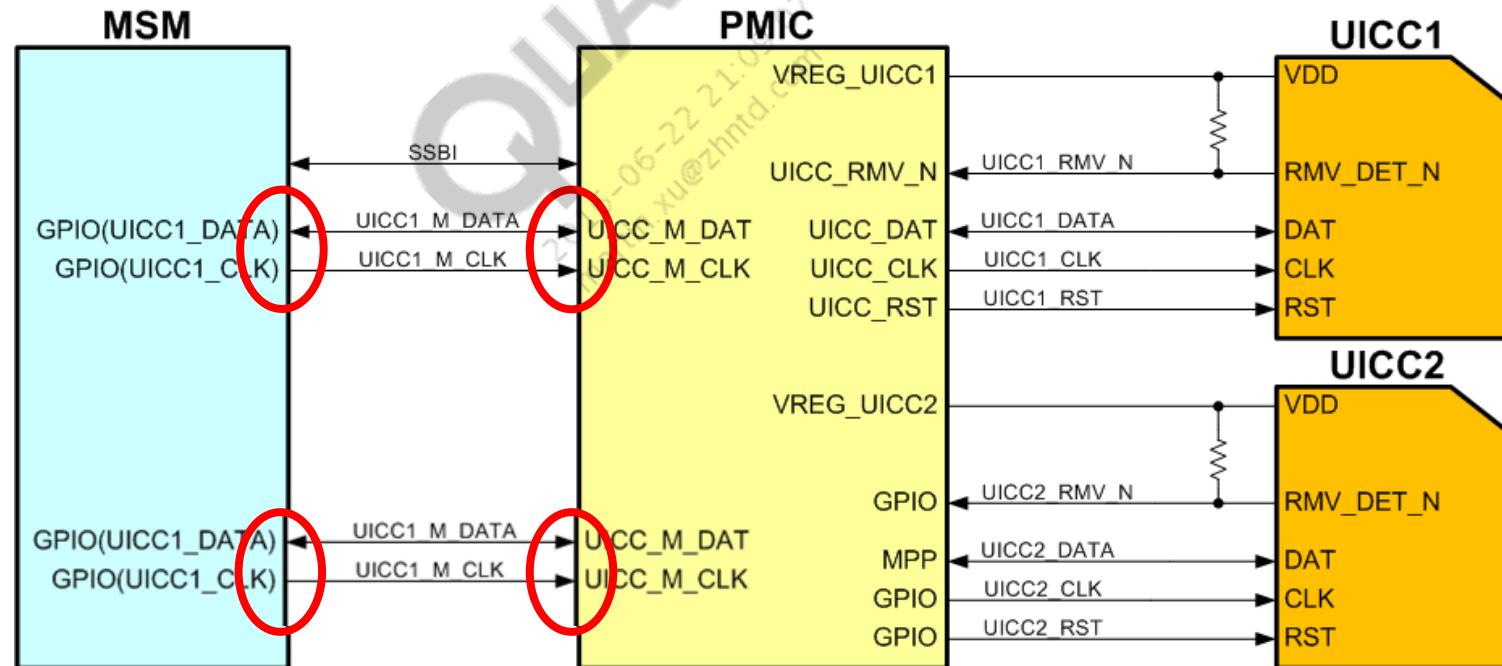
# Battery UICC Alarm (BUA) Interface – Introduction

MSM8960 required PM8921 to level shift every UIM interface

- This costs an additional eight pins in the system (for two UIM interfaces).
- Reducing the number of pins on the PMIC allows the PMIC to fit into smaller WLP packages.

To support UIM card removal detection/battery removal detection, a new, low latency, bidirectional interface was created.

- Battery UICC alarm (BUA) interface



# BUA Overview

ISO-7816-3 specifies that a smartcard (UICC/UIM) shall be powered down in a controlled and predefined manner.

Battery UICC alarm (BUA) is a bidirectional interface between the PMIC and the MSM that allows for a controlled power down of UICC when either the battery or the UICC is removed.

## System interconnect

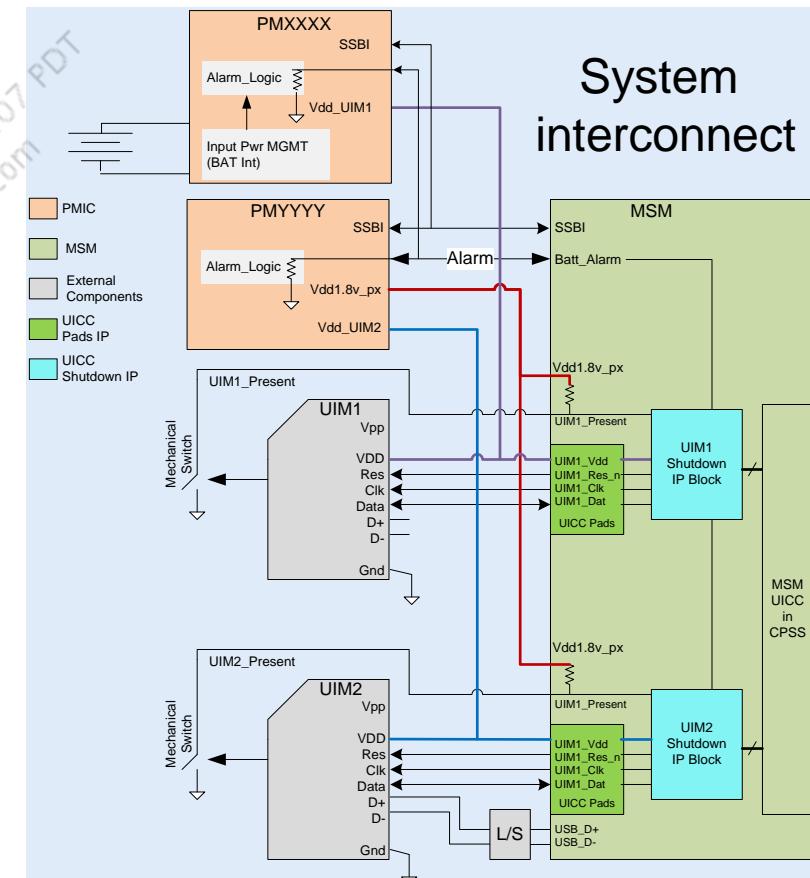
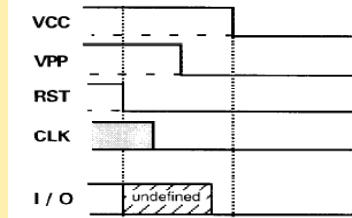
- UICC DATA/CLK/RST pins are connected directly to the MSM
- UICC supply is supplied from the PMIC

The PMIC alerts the MSM device over the bidirectional interface when a battery is removed so that the UICC can be deactivated while the system is still powered by capacitors.

The MSM device alerts the PMIC over the bidirectional interface when a UICC removal is initiated so that the UICC can be deactivated before it is completely removed.

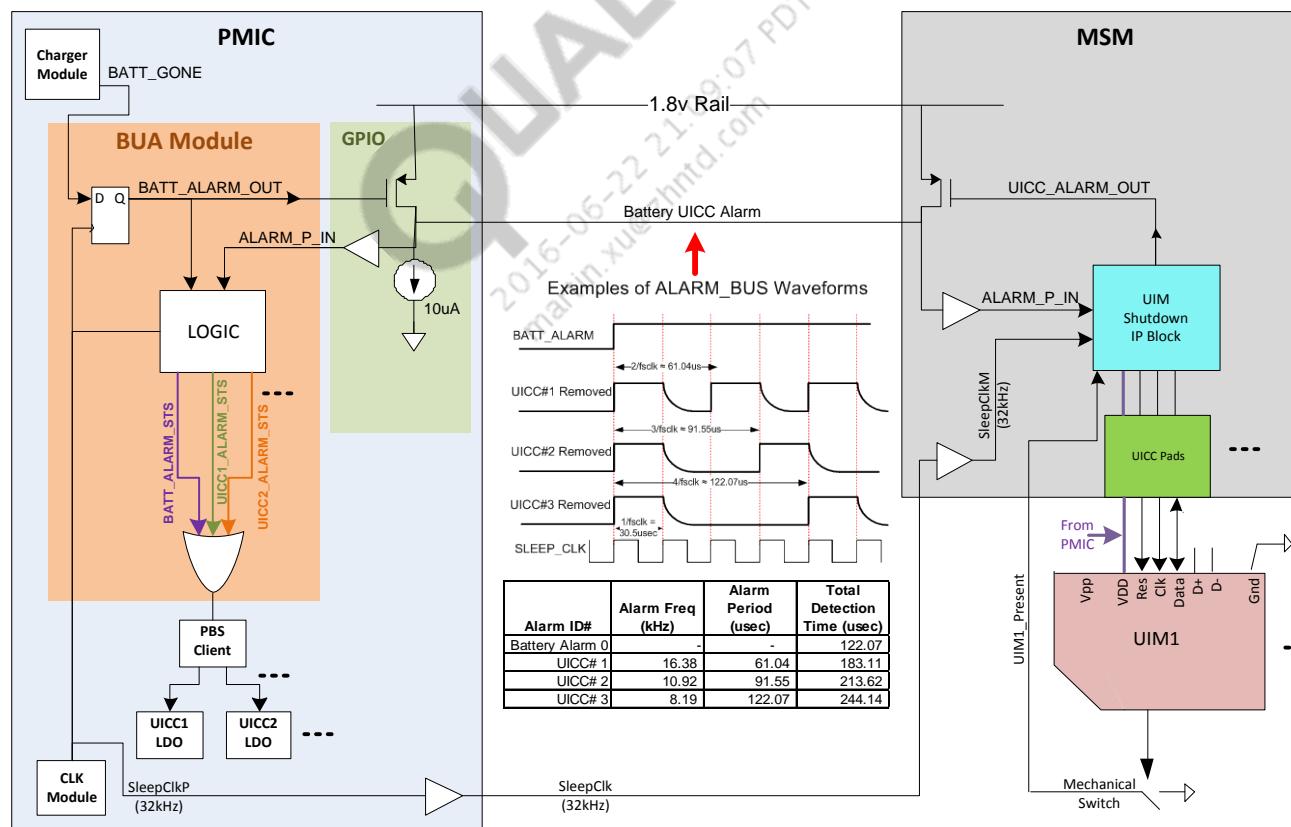
Alarm and deactivation are based in hardware; no software intervention is required.

## UICC deactivation



# BUA Operation

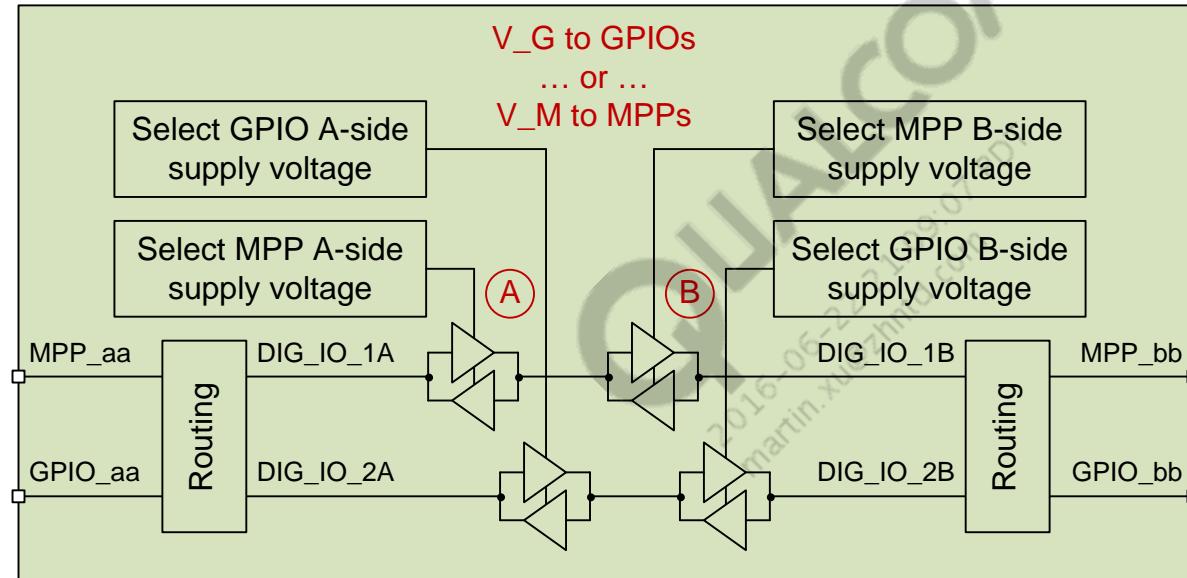
- Battery removal: PMIC detects battery removal and triggers the alarm by pulling it high. PMIC waits for a predetermined time while MSM shuts down DATA/CLK/RST and then powers down all UICC LDOs.
  - Battery removal to deactivation complete: ~884  $\mu$ s (nominal)
- UICC<sub>x</sub> removal: MSM detects UICC<sub>x</sub> removal via a mechanical switch. MSM shuts down DATA/CLK/RST and then triggers the alarm by pulsing a fSCLK/(x+1) signal. PMIC decodes the alarm and powers down UICC<sub>x</sub> LDO.
  - UICC removal to deactivation complete: ~1565  $\mu$ s (nominal)



# Other IC-level Interface Uses for MPPs or GPIOs (1 of 2)

## Level translators

Since the two sides (A and B) can run off different voltages, a level-translation is achieved.



### V\_M options for MPP\_01 to \_04

VDD\_L8\_16\_18\_19 = VPH\_PWR

VREG\_L1 = 1.225 V

VDD\_L2\_LVS1\_2\_3 = 1.8 V (VREG\_S3)

VREG\_L6 = 1.8 V

### V\_M options for MPP\_05 to \_08

VDD\_GPLED = VPH\_PWR

VREG\_L1 = 1.225 V

VDD\_L2\_LVS1\_2\_3 = 1.8 V (VREG\_S3)

VREG\_L6 = 1.8 V

### V\_G options for GPIO\_1 to \_14

VDD\_L8\_16\_18\_19 = VPH\_PWR

VREG\_L1 = 1.225 V

VDD\_L2\_LVS1\_2\_3 = 1.8 V (VREG\_S3)

VREG\_L6 = 1.8 V

### V\_G options for GPIO\_15 to \_18

VDD\_L2\_LVS1\_2\_3 = 1.8 V (VREG\_S3)

VREG\_L6 = 1.8 V

### V\_G options for GPIO\_19 to \_36

VDD\_RGB = VPH\_PWR

VDD\_TORCH = TBD

VDD\_MSM\_IO = 1.8 V (VREG\_S3)

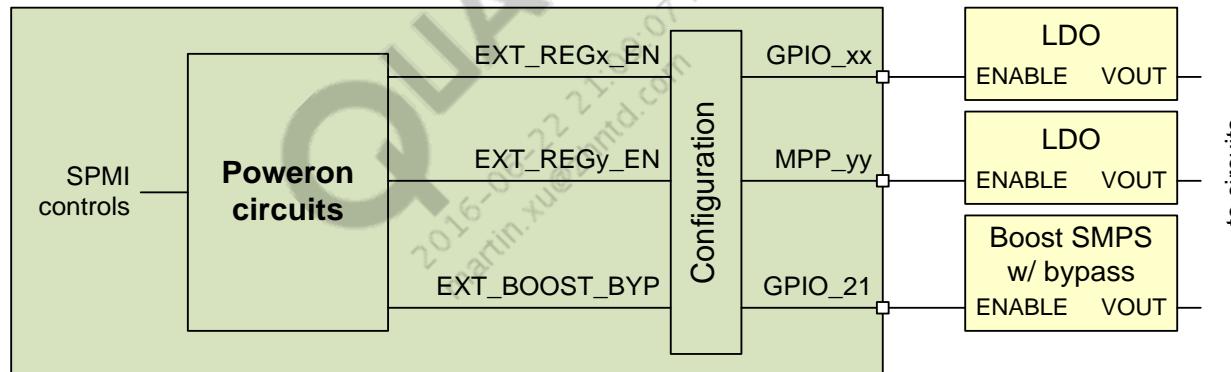
VREG\_L4 = 1.8 V

VREG\_L6 = 1.8 V

## Other IC-level Interface Uses for MPPs or GPIOs (2 of 2)

### External LDO or SMPS controls

GPIO and MPP outputs can control external LDOs, SMPS circuits, or power gating



Some GPIOs and MPPs can be included in the default-on poweron sequence, as discussed earlier.



## Section 8

# PMIC Configurable I/Os

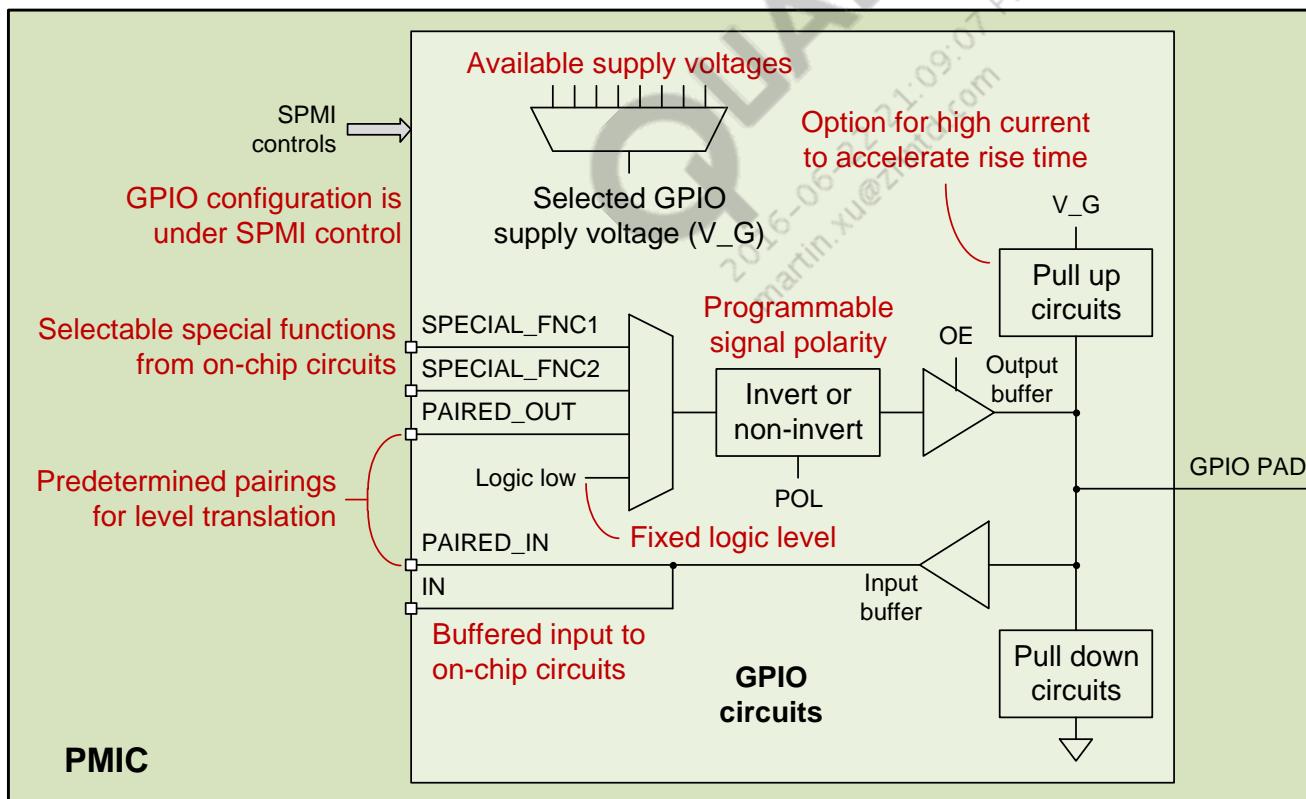
# PMIC GPIO Pins

36 GPIOs are available, all on the PM8941 (none on PM8841).

Some likely GPIO applications, which are discussed elsewhere: clock outputs; external current driver control; external LDO, SMPS, or power gate controls; status bit; XO controller input; and level translator.

GPIO pairs

- Each GPIO pin is assigned as a member of a pair.
- Each pair is a combination of sequential odd and even GPIO pins (GPIO\_1 is paired with GPIO\_2, etc.).
- Each member can be assigned a different supply, so each pair can be used as a digital level translator.



Note:

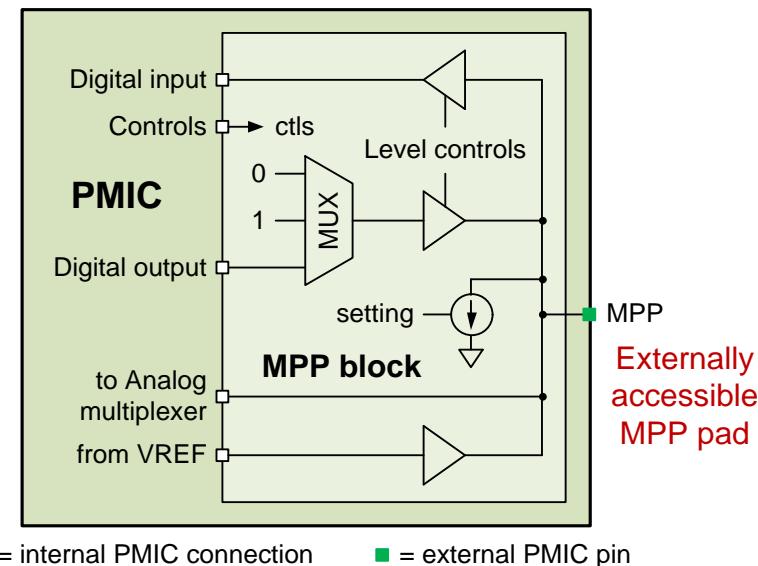
All GPIOs hardware default to digital input with 10  $\mu$ A pull-down. GPIO\_21 is driven high at VPH\_PWR level by PBS during PMIC poweron.

# PMIC Multipurpose Pins

- 12 MPPs are available: Eight on the PM8941 and four on the PM8841. All can be programmed to any of the following configurations.
  - Digital input – Digital inputs applied to the pin can be read via software, can trigger an interrupt, or can be routed to another MPP (making this pin the input side of a level translator or current sink controller). The logic level is programmable, providing compliance between I/Os running off different power supplies.
  - Digital output – The output signal can be set via software to logic LOW or HIGH, can come from this pin's complementary MPP (making this pin the output side of a level translator), or can be tri-stated for use as a switch. The logic level is programmable, providing compliance between I/Os running off different supplies.
  - Bidirectional I/O – The two MPPs making up a complementary pair can be jointly configured as a bidirectional, level-translating pair.
  - Analog input – Inputs are routed to the analog multiplexer switch network; if selected, that analog voltage is routed to the HK/XO ADC for digitization.
  - Analog output – Buffered version of on-chip voltage reference (VREF).
  - Programmable current sink – for driving LEDs.

## Notes:

1. PM8841 MPPs can be configured as analog inputs but with no AMUX present in the PMIC, the voltage cannot be read
2. Only odd PM8941 MPPs (MPP\_01, MPP\_03, MPP\_05, MPP\_07) can be configured as analog outputs.
3. Only even MPPs (MPP\_02, MPP\_04, MPP\_06, MPP\_08) have current sink capability.

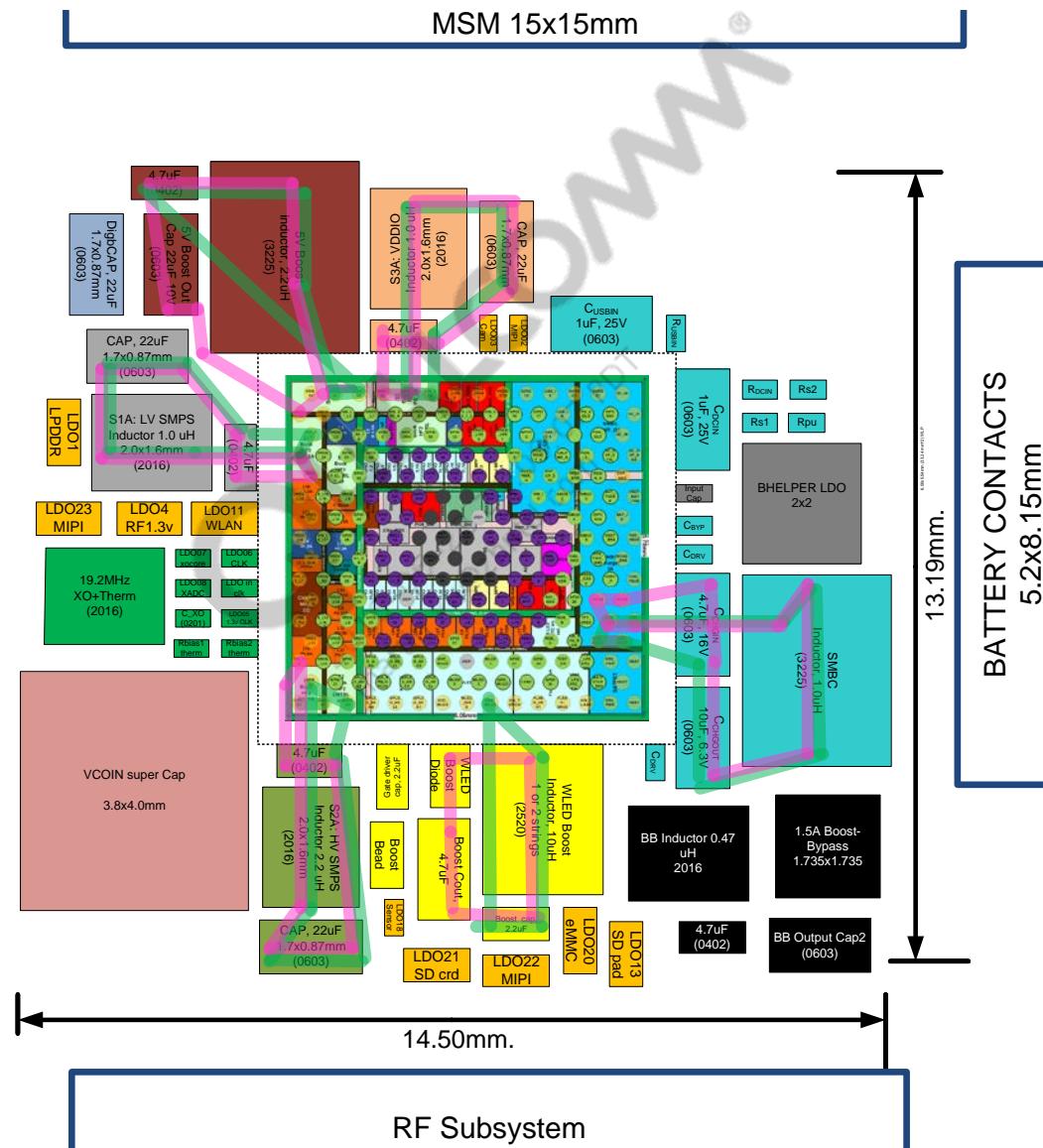




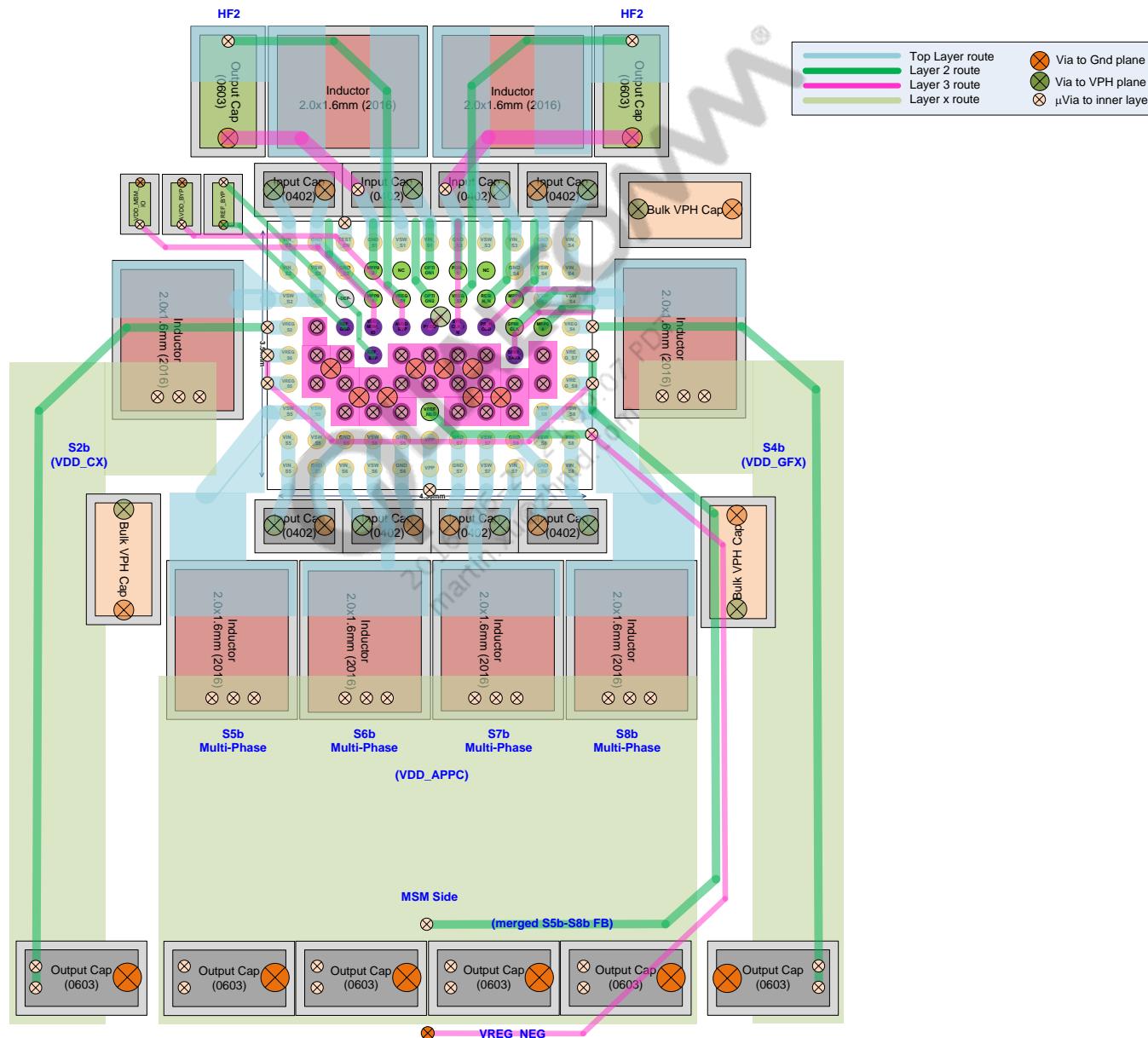
## Section 9

# PMIC Top-level Design Topics

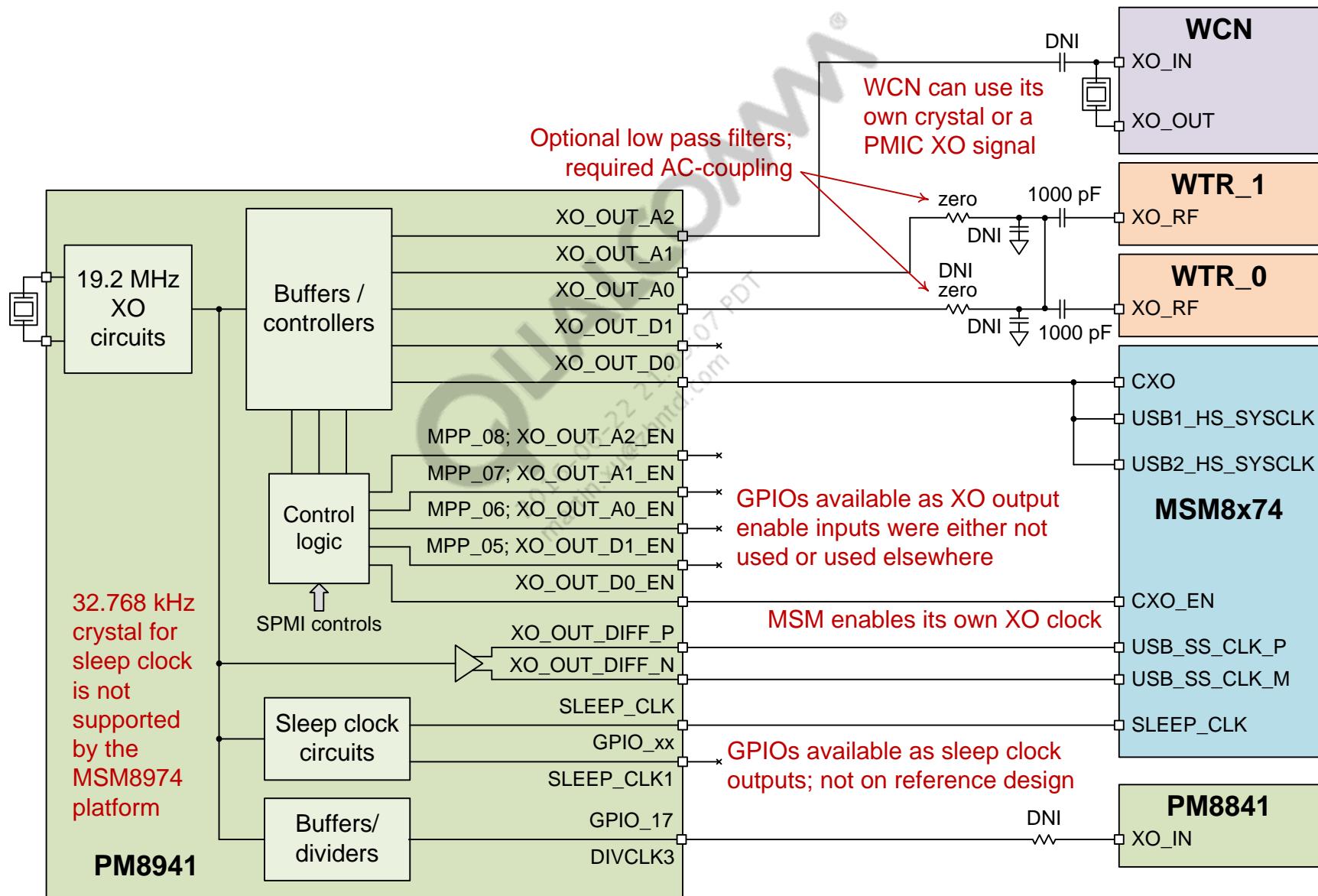
# Example PM8941 Top-level Parts Placement



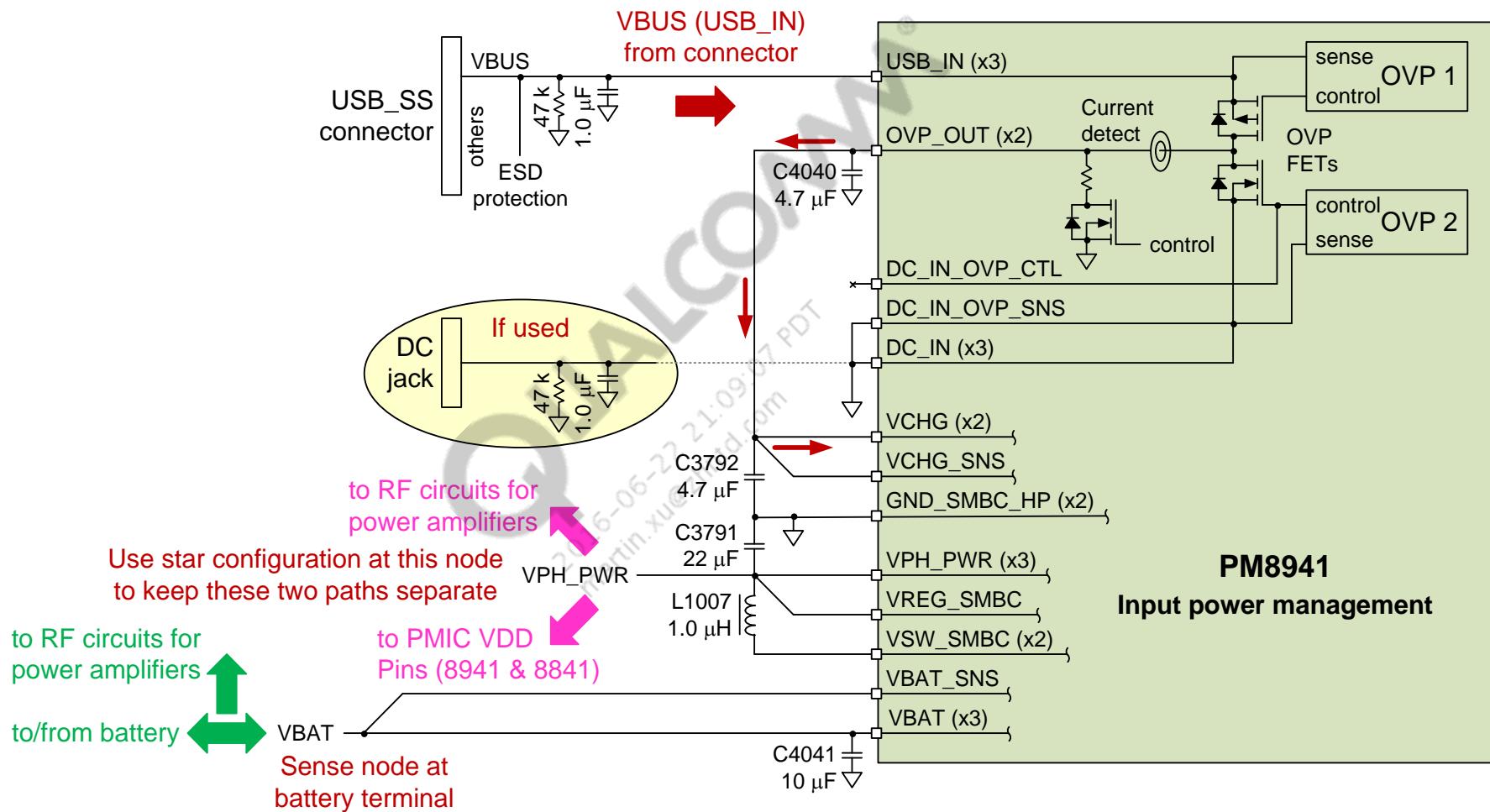
# Example PM8841 Top-level Parts Placement



# Example XO and Sleep Clock Distributions



# Example PM8941 Input DC Power – Schematic



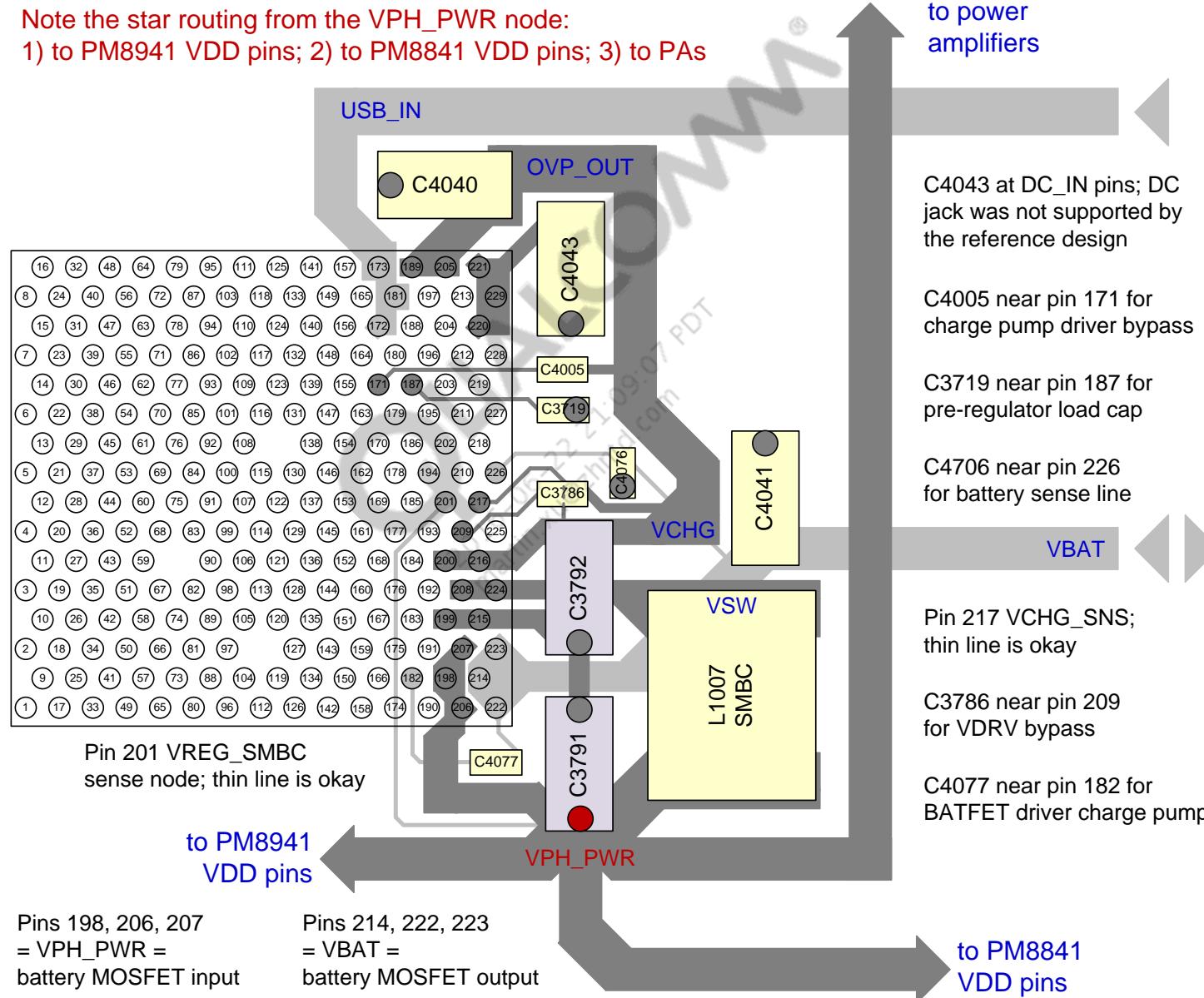
## Note:

Refer to the latest revision of the *MSM8274/MSM8274AB, MSM8674/MSM8674AB, and MSM8974/MSM8974AB Baseband Reference Schematic* (80-NA437-41) for the input DC power schematic.

# PMIC High-level Input DC Power – Layout Guidelines

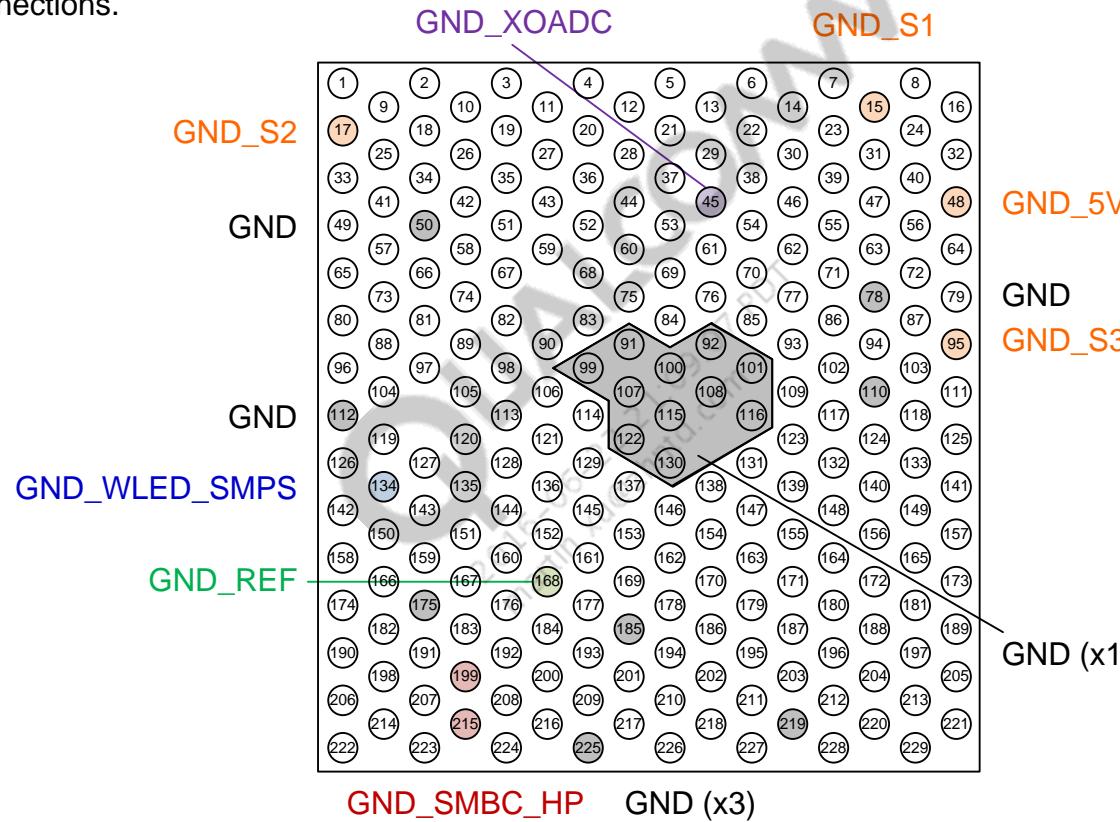
Note the star routing from the VPH\_PWR node:

- 1) to PM8941 VDD pins; 2) to PM8841 VDD pins; 3) to PAs



# PM8941 Ground Connections

Common ground pins near the IC center improve electrical ground, mechanical strength, and thermal continuity. These pins are tied together internally and should be connected to PCB ground. Several other pins provide special-purpose ground connections.

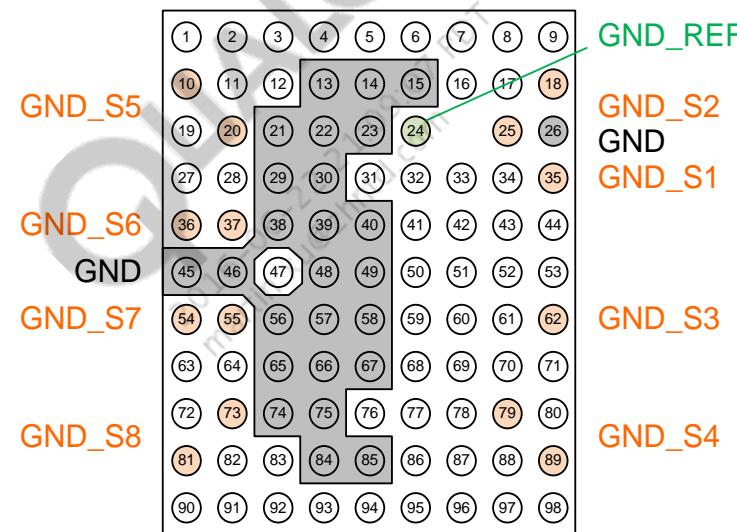


Common ground pins must be soldered to PCB pads located directly below the device, with many ground vias conducting PMIC heat directly to several inner layers. The inner layers should provide very large areas of ground fill and additional vias connected to outer layer ground fill areas. All these large ground surfaces minimize thermal resistance to the handset's ambient environment.

All others – shown in different colors – are special-purpose grounds that were discussed in the context of their assigned functionality within other sections of this document.

# PM8841 Ground Connections

Notes from the PM8941 ground connection page apply for the PM8841 as well.



# PM8941 Unused Pin Terminations (1 of 7)

Input power management				
Pin name/function	Pin termination if unused			Comments
	Internal charger + external BMS	External charger + internal or external BMS <sup>1</sup>	External charger + Bharger™ boost + internal or external BMS	
OTG_IN	GND	GND	GND	If an external OTG switch is used to power the OTG device, then OTG_IN should be left NC or connected to VOUT_5VS_OTG.
PHY_VBUS	USB1_PHY_VBUS	USB1_PHY_VBUS	USB1_PHY_VBUS	If an external charger can drive USB1_PHY_VBUS directly, then PHY_VBUS can be left floating.
USB_IN	VBUS	GND	GND	
DC_IN	DC_IN / GND	GND	GND	
DC_IN_OVP_CTRL	NC/Ext. OVPFET	GND	GND	Connect to the gate of the external OVP FET if used. Connect to GND if an external charger is used to indicate to SMBB use of an internal charger.
DC_IN_OVP_SNS	DC_IN	DC_IN	DC_IN	
OVP_CP_DRV	10 nF to VCHG	NC	NC	
OVP_OUT	VCHG	NC	NC	
VCHG	VDD_FLASH	NC	VDD_FLASH	
VCHG_SNS	VCHG	NC	VCHG	

<sup>1</sup>: Certain platforms such as APQ8074 do not use PM8941's charger/BMS. The battery is usually not directly connected to PM8941. PMIC is powered via VPH\_PWR. For such use cases, these are recommended unused pin terminations.

# PM8941 Unused Pin Terminations (2 of 7)

Pin name/function	Input power management			Comments
	Internal charger + External BMS	External charger + internal or external BMS <sup>1</sup>	External charger + Bcharger boost + internal or external BMS	
VREG_SMBC	VPH_PWR	VPH_PWR	VPH_PWR	
VSW_SMBC	1 µH inductor	NC	1 µH inductor	
VDRV_P	100 nF to VCHG	NC	100 nF to VCHG	
GND_CHG_HP	GND	GND	GND	
VPH_PWR	VPH_PWR	VPH_PWR	VPH_PWR	If an external charger is used, VPH_PWR should be tied to the system output of the external charger.
VBAT	VBATT	VPH_PWR	VPH_PWR	VBATT is the battery terminal; VBAT is the PMIC pin.
BATFET_CP_DRV	NC	NC	NC	
VBAT_SNS	VBATT	VBATT	VBATT	
VCOIN	>10 µF	>10 µF	>10 µF	A qualified coin-cell or super capacitor is required on VCOIN to support RTC via calibration RC when PMIC is OFF. A capacitor with effective capacitance of 10 µF is required on the VCOIN pin to support SMPL up to 2 sec.
VPRE_CAP	0.1 µF	NC	NC	

<sup>1</sup>: Certain platforms such as APQ8074 do not use PM8941's charger/BMS. The battery is usually not directly connected to PM8941. PMIC is powered via VPH\_PWR. For such use cases, these are recommended unused pin terminations.

## PM8941 Unused Pin Terminations (3 of 7)

Pin name/function	Input power management			Comments
	Internal charger + external BMS	External charger + internal or external BMS <sup>1</sup>	External charger + Bharger boost + internal or external BMS	
VREG_BMS	NC	0.47 µF to VPH_PWR (internal BMS)  NC (external BMS)	0.47 µF to VPH_PWR (internal BMS)  NC (external BMS)	
BMS_CSP	VBAT	VBATT_SENSE_P (internal BMS)  VBAT (external BMS)	VBATT_SENSE_P (internal BMS)  VBAT (external BMS)	
BMS_CSM	VBAT	VBATT_SENSE_M (internal BMS)  VBAT (external BMS)	VBATT_SENSE_M (internal BMS)  VBAT (external BMS)	
VREF_BAT	Bias or NC	NC	NC	
BAT_THERM	Bias or GND	NC	NC	
BAT_ID	GND	NC	NC	

1: Certain platforms such as APQ8074 do not use PM8941's charger/BMS. The battery is usually not directly connected to PM8941. PMIC is powered via VPH\_PWR. For such use cases, these are recommended unused pin terminations.

## PM8941 Unused Pin Terminations (4 of 7)

Output power management		
Pin name/function	Pin termination if unused	Comments
VIN_5VS	VREG_5V	
VOUT_5VS_OTG	NC	
VOUT_5VS_HDMI	NC	
VREG_LVS1	NC	
VREG_LVS2	NC	
VREG_LVS3	NC	
Any unused LDO output pin	Tie to LDO input pin (default ON LDO) NC (default OFF LDO)	SW should not enable the LDO
VSW_5V	NC	
VREG_5V	NC	
GND_5V	GND	
VREG_5V_SNS	NC	

# PM8941 Unused Pin Terminations (5 of 7)

General housekeeping		
Pin name/function	Pin termination if unused	Comments
XO_THERM	GND	
VREF_XO	NC	
GND_XOADC	GND	
AMUX_x	NC or GND	
AMUX_HW_ID	NC or GND	
AMUX_USB_ID	GND	
AMUX_PU1	VREG_L8	
AMUX_PU2	VREG_L8	
User interface		
Pin name/function	Pin termination if unused	Comments
RGB_R	NC	
RGB_G	NC	
RGB_B	NC	
VDD_RGB	VPH_PWR	

# PM8941 Unused Pin Terminations (6 of 7)

User interface		
Pin name/function	Pin termination if unused	Comments
GPLED_SRCx	NC	
GPLED_SNKx	NC	
VDD_GPLED	VPH_PWR	
VDD_WLED	VPH_PWR	
WLED_CABC	100 kΩ pull-down	It can also be directly grounded
VREG_WLED	NC	
VSW_WLED	NC	
GND_WLED_SMPS	GND	
WLED_SNKx	NC	
VIB_DRV_N	NC	
FLASH_DRVx	NC	
VDD_FLASH	NC	
VDD_TORCH	VREG_5V	

# PM8941 Unused Pin Terminations (7 of 7)

IC-level interface		
Pin name/function	Pin termination if unused	Comments
CBL_PWR_N	NC	
PON_1	GND	
KPD_PWR_N	NC	
RESIN_N	NC	

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martin.xu@zhntd.com

# Power Management Troubleshooting Techniques

The recommended troubleshooting sequence for an initial dual-PMIC powerup is as follows:

1. Check the PM8941 charger input power supply voltage (USB\_IN, OVP\_OUT, DC\_IN, and/or VCHG).
2. Check the PM8941 charger output voltage (VPH\_PWR).
3. Check the other input power pins (VDD\_xxx) at both PMICs.
4. Verify the logic levels at the external control pins:
  - PM8941 CBL\_PWR\_N
  - PM8941 KYPD\_PWR\_N
  - PM8941 OPT\_[4:1] and PM8841 OPT\_[2:1]
  - RESIN\_N at both PMICs
5. Check the internal reference voltages by probing the REF\_BYP pin on both PMICs.
6. Check the regulated voltages that default to their on state. Note that the sequence depends upon the hardwired connections at PM8941 OPT\_[4:1] and PM8841 OPT\_[2:1].
7. Each of these should settle to within 5 to 10% of their target voltage before the PMIC continues its poweron sequence by initiating the next regulator. The devices shut down if any of these default regulators do not turn on and settle properly.
8. If a device shuts down due to a failed regulator output, the start signal will have to be removed and reapplied to attempt another powerup.
9. Monitor PM8941 PON\_RST\_N; verify that it goes to logic high after all the default regulators power up correctly.
10. Monitor PM8941 PS\_HOLD; verify that it is at logic high. It can transition between logic states throughout the poweron sequence but must be stable at logic high within hundreds of milliseconds after the PON\_RST\_N signal went high. Confirm that this signal is applied to the PM8841 PS\_HOLD and PON\_1 pins.

If any of the first nine steps are not completed successfully, one of the installed PMICs has failed. If step 10 fails, there may be a problem with the modem device, one of the PMICs, or their interconnections.

# Questions?

You may also submit questions to: <https://support.cdmatech.com>

