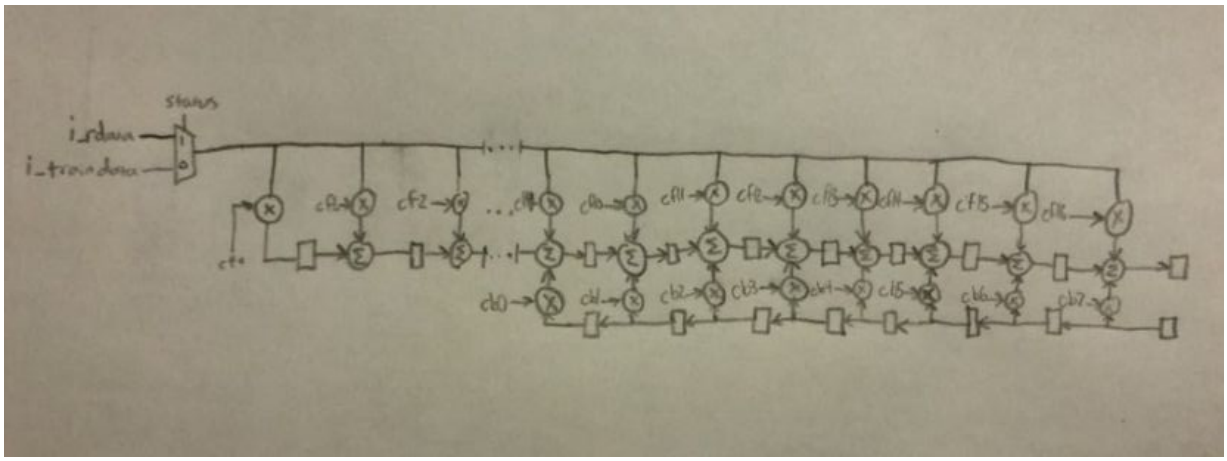
ECE 350
Final Project
Dan Browne & Logan Cooper

Design:



Code:

DFE:

```
`timescale 1ns / 1ns
/*
    Dan Browne & Logan Cooper
    ECE 350/450 - Computer Aided Design
    Final Project
    Design a self-adaptive Decision Feedback Equalizer (DFE) or (IIR filter)
*/

module mult(data, coef, product); //17 + 8 needed
    input signed [7:0] data;
    input signed [11:0] coef;
    output signed [7:0] product;

    assign product = data * coef;
endmodule

module sum(delay, multout, feedback, out);
    input [7:0] delay;
    input [7:0] multout;
    input [7:0] feedback;
    output [7:0] out;

    assign out =  delay + multout + feedback;
endmodule

module DFE(clock, reset, status, data_en, i_rdata, i_traindata, flag, o_ry);
    input clock, reset, status, data_en;
```

```
    input [7:0] i_rdata;                    // raw data: 1 sign bit + 2 integer
bits + 5 fraction bits
    input [7:0] i_traindata;                // training data to feed in; same
format as raw data

    output reg flag;                        // indicator for trianing/testing
    output [8:0] o_ry;                  // output data: 1 sign bit + 2 integer
bits + 6 fraction bits

    reg [11:0] weights;                     // weights for the system: carry
forward flag + carry back flag + 10 data bits
    reg [11:0] deltaf, deltab;              // delta weights for interface; we
can set this to be whatever we want

    // Temporary registers
    reg [7:0] R1 [16:0];    // feedforward delay
    reg [7:0] R2 [7:0];     // feedback delay
    reg [8:0] R3 [2:0];     // errors
    reg [7:0] R4 [16:0];    // input pipeline

    // Coefficiencs updated with delta weights
    reg [11:0] cb [7:0];            // Coefficients for the fbe
    reg [11:0] cf [16:0];           // Coefficients for ffe

    wire [7:0] R1_in [16:0];
    wire [7:0] add_in [15:0];
    wire [7:0] fb_out [7:0];

    integer i;

    wire [7:0] inselect;
    assign inselect = (status) ? i_rdata : i_traindata;

    assign o_ry = R1[16];

    //architecture pipeline
    //17 CF Multipliers
    mult mult0(inselect, cf[0], R1_in[0]);
    mult mult1(inselect, cf[1], add_in[0]);
    mult mult2(inselect, cf[2], add_in[1]);
    mult mult3(inselect, cf[3], add_in[2]);
    mult mult4(inselect, cf[4], add_in[3]);
    mult mult5(inselect, cf[5], add_in[4]);
    mult mult6(inselect, cf[6], add_in[5]);
    mult mult7(inselect, cf[7], add_in[6]);
    mult mult8(inselect, cf[8], add_in[7]);
    mult mult9(inselect, cf[9], add_in[8]);
    mult mult10(inselect, cf[10], add_in[9]);
    mult mult11(inselect, cf[11], add_in[10]);
    mult mult12(inselect, cf[12], add_in[11]);
    mult mult13(inselect, cf[13], add_in[12]);
    mult mult14(inselect, cf[14], add_in[13]);
    mult mult15(inselect, cf[15], add_in[14]);
    mult mult16(inselect, cf[16], add_in[15]);
```

```
    //8 CB Multipliers
    mult bmult0(R2[0], cb[0], fb_out[0]);
    mult bmult1(R2[1], cb[1], fb_out[1]);
    mult bmult2(R2[2], cb[2], fb_out[2]);
    mult bmult3(R2[3], cb[3], fb_out[3]);
    mult bmult4(R2[4], cb[4], fb_out[4]);
    mult bmult5(R2[5], cb[5], fb_out[5]);
    mult bmult6(R2[6], cb[6], fb_out[6]);
    mult bmult7(R2[7], cb[7], fb_out[7]);

    //16 Adders
    sum sum0(R1[0], add_in[0], 8'd0, R1_in[1]);
    sum sum1(R1[1], add_in[1], 8'd0, R1_in[2]);
    sum sum2(R1[2], add_in[2], 8'd0, R1_in[3]);
    sum sum3(R1[3], add_in[3], 8'd0, R1_in[4]);
    sum sum4(R1[4], add_in[4], 8'd0, R1_in[5]);
    sum sum5(R1[5], add_in[5], 8'd0, R1_in[6]);
    sum sum6(R1[6], add_in[6], 8'd0, R1_in[7]);
    sum sum7(R1[7], add_in[7], 8'd0, R1_in[8]);
    sum sum8(R1[8], add_in[8], fb_out[0], R1_in[9]);
    sum sum9(R1[9], add_in[9], fb_out[1], R1_in[10]);
    sum sum10(R1[10], add_in[10], fb_out[2], R1_in[11]);
    sum sum11(R1[11], add_in[11], fb_out[3], R1_in[12]);
    sum sum12(R1[12], add_in[12], fb_out[4], R1_in[13]);
    sum sum13(R1[13], add_in[13], fb_out[5], R1_in[14]);
    sum sum14(R1[14], add_in[14], fb_out[6], R1_in[15]);
    sum sum15(R1[15], add_in[15], fb_out[7], R1_in[16]);

    always @ (negedge clock or negedge reset) begin
        if (~reset) begin //reset the system
           weights <= 12'd0;
           deltaf <= 12'd0;
           deltab <= 12'd0;
           flag <= 1'd0;
           for (i=0; i < 17; i=i+1) begin //reset arrays
                if (i < 8)
                    R2[i] <= 8'd0;
                    cb[i] <= 8'd1;
                R1[i] <= 8'd0;
                cf[i] <= 8'd2;
           end
        end
        else begin
            for (i=0; i < 17; i=i+1)
                R1[i] <= R1_in[i]; //reset array
        end
    end
endmodule
```

Testbench:

```
`timescale 1ns / 1ns
/*
    Dan Browne & Logan Cooper
    ECE 350/450 - Computer Aided Design
    Final Project Testbench
    Design a self-adaptive Decision Feedback Equalizer (DFE) or (IIR filter)
*/
 module Final_Proj_Testbench;
      // Inputs
      reg clock, reset, status, data_en;
      reg [7:0] i_rdata, i_traindata;
      // Outputs
      wire flag;
      wire [8:0] o_ry;

      // Instantiate the Unit Under Test (UUT)
      DFE uut(
            .clock(clock),
            .reset(reset),
            .status(status),
            .data_en(data_en),
            .i_rdata(i_rdata),
            .i_traindata(i_traindata),
            .flag(flag),
            .o_ry(o_ry)
      );

      initial begin
            clock = 0;
            forever #10 clock = ~clock;
      end

      initial begin
        i_traindata = 8'd01;
        status = 1'd0;
        i_rdata = 8'd0;
        #90;
        forever #20 i_traindata = i_traindata + 8'd1;
      end
    //create a dumpfile
    initial begin
        $monitor($stime,,i_rdata,,i_traindata,,clock,,reset,,,o_ry);
        $dumpfile("Final_Project.dump");
        $dumpvars(0,uut);
    end
    initial begin
        reset=0;
        // Wait 100 ns for global reset to finish
        #100;
        reset=1;

        #500;
```

```
        $finish;
    end
endmodule
```

cmd.tcl:

```
read_verilog Final_Project.v

source Final_Project.con

set_operating_conditions -max slow -max_library NangateOpenCellLibrary_SS -min fast -min_library
NangateOpenCellLibrary_FF

uniquify
link
check_design
report_clock
report_wire_load
current_design DFE

compile

redirect -append ./report/constriant.rpt {report_constraint}
redirect -append ./constriant.rpt
report_constraint
report_timing -delay_type max
report_timing -delay_type min
report_area
report_power

current_design DFE
foreach_in_collection des [get_designs] {current_design $des
set verilogout_no_tri true
}

set hdlout_internal busses true
set bus_inference style "%s\[%d\]"
set verilogout_equation false
set verilogout_unconnected_prefix "SYNOPSYS_UNCONNECTED_"
define_name_rules my_rules -allowed {a-zA-Z0-9_} -equal_ports_nets -first_restricted "\\"
-replacement_char "_" -flatten_fulti_dimension_busses -add_dummy_nets_in_verilog_out
"SYNOPSYS_UNCONNECTED_%d" -map { {{"\\*cell\\*", "u"}, {"\*-return", "RET"}} }
change_name -rule my_rules -hierarchy
write -format verilog -hierarchy -output "./Final_Project_out.v"
write_sdc Final_Project.sdc -nosplit
history > cmd_test
```

fm_cmd.tcl:

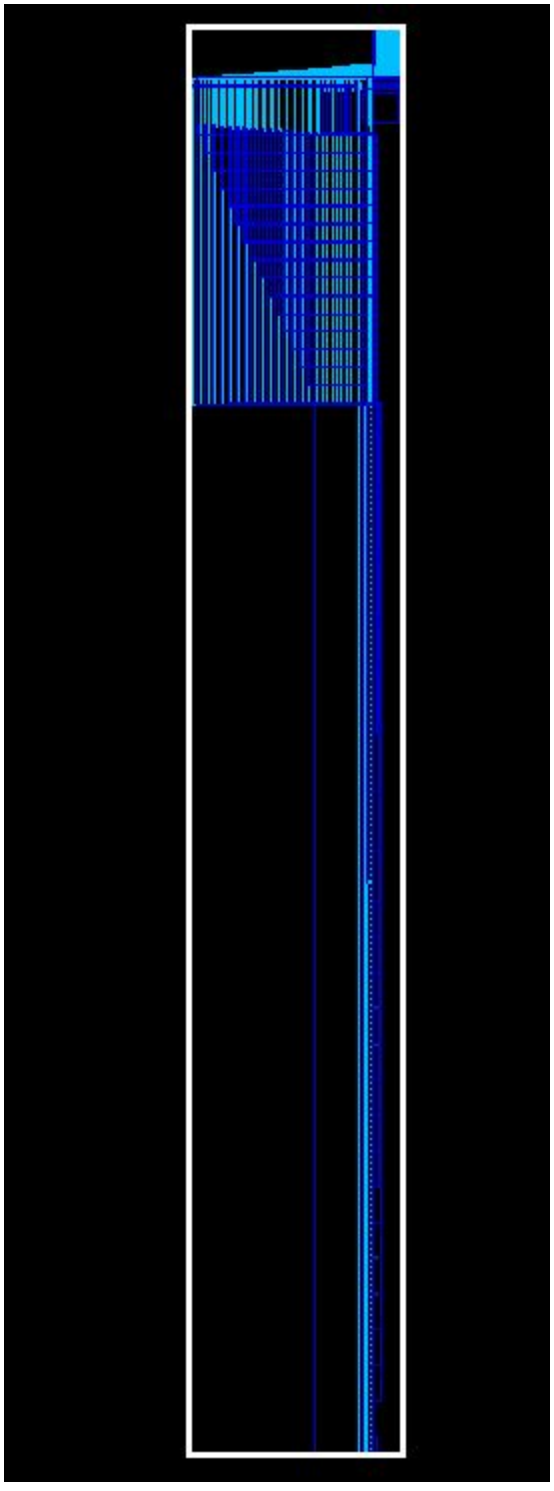
```
set_svf -append { ./default.svf }
read_verilog -container r -libname WORK -05 { ./rtl/Final_Proj.v }
set_top r:/WORK/TOP
read_verilog -container i -libname WORK -05 { ./vg/Final_Proj.vg }
read_db { /proj/ece350-014-
```

spring2020/ClassShare/45nm_libs_front_end/NLDM/NangateOpenCellLibrary_fast.db /proj/ece350-014-spring2020/ClassShare/45nm_libs_front_end/NLDM/NangateOpenCellLibrary_slow.db }
set_top i:/WORK/Final_Proj
set_implementation i:/WORK/Final_Proj
match
verify

Simulations:

Waveforms (Custom Test Case):

Schematic:



Constraints Report:

```
****************************************
Report : constraint
Design : DFE
Version: P-2019.03-SP5-1
Date   : Sun May 10 22:20:12 2020
****************************************


                                                  Weighted
    Group (max_delay/setup)       Cost     Weight     Cost
    ---------------------------------------------------------
    clock                         0.00       1.00     0.00
    default                       0.00       1.00     0.00
    ---------------------------------------------------------
    max_delay/setup                                    0.00

                             Total Neg  Critical
    Group (critical_range)     Slack    Endpoints    Cost
    ---------------------------------------------------------
    clock                         0.00         0     0.00
    default                       0.00         0     0.00
    ---------------------------------------------------------
    critical_range                                     0.00

                                                  Weighted
    Group (min_delay/hold)        Cost     Weight     Cost
    ---------------------------------------------------------
    clock (no fix_hold)           0.00       1.00     0.00
    default                       0.00       1.00     0.00
    ---------------------------------------------------------
    min_delay/hold                                     0.00


    Constraint                                         Cost
    ---------------------------------------------------------
    max_transition                                     0.00 (MET)
    max_capacitance                                    0.00 (MET)
    max_delay/setup                                    0.00 (MET)
    sequential_clock_pulse_width                       0.00 (MET)
    critical_range                                     0.00 (MET)
```

Power Report:

```
****************************************
Report : power
        -analysis_effort low
Design : DFE
Version: P-2019.03-SP5-1
Date   : Sun May 10 22:20:13 2020
****************************************


Library(s) Used:

    NangateOpenCellLibrary_SS (File: /proj/ece350-014-spring2020/ClassShare/45nm_libs_front_end/NLDM/NangateOpenCellLibrary_slow.db)


Operating Conditions: slow   Library: NangateOpenCellLibrary_SS
Wire Load Model Mode: top

Design        Wire Load Model            Library
------------------------------------------------
DFE                  5K_hvratio_1_1    NangateOpenCellLibrary_SS


Global Operating Voltage = 0.95
Power-specific unit information :
    Voltage Units = 1V
    Capacitance Units = 1.000000ff
    Time Units = 1ns
    Dynamic Power Units = 1uW    (derived from V,C,T units)
    Leakage Power Units = 1nW


  Cell Internal Power  = 128.6593 uW   (68%)
  Net Switching Power  =  59.7874 uW   (32%)
                         ---------
Total Dynamic Power    = 188.4466 uW  (100%)

Cell Leakage Power     =  56.6593 uW


                 Internal         Switching           Leakage            Total
Power Group      Power            Power               Power              Power   (   %    )  Attrs
--------------------------------------------------------------------------------------------------
io_pad             0.0000           0.0000              0.0000             0.0000  (   0.00%)
memory             0.0000           0.0000              0.0000             0.0000  (   0.00%)
black_box          0.0000           0.0000              0.0000             0.0000  (   0.00%)
clock_network      0.3007          21.9311             20.9385            22.2528  (   9.08%)
register          88.6271           4.8061        7.4826e+03           100.9158  (  41.17%)
sequential         0.0000           0.0000              0.0000             0.0000  (   0.00%)
combinational     39.7315          33.0501        4.9156e+04           121.9373  (  49.75%)
--------------------------------------------------------------------------------------------------
Total            128.6593 uW       59.7874 uW     5.6659e+04 nW        245.1059 uW
```

Area Report:

```
****************************************
Report : area
Design : DFE
Version: P-2019.03-SP5-1
Date   : Sun May 10 22:20:12 2020
****************************************

Library(s) Used:

    NangateOpenCellLibrary_SS (File: /proj/ece350-014-spring2020/ClassShare/45nm_libs_front_end/NLDM/NangateOpenCellLibrary_slow.db)

Number of ports:                         2874
Number of nets:                          6120
Number of cells:                         3002
Number of combinational cells:           2370
Number of sequential cells:               136
Number of macros/black boxes:               0
Number of buf/inv:                        324
Number of references:                      46

Combinational area:               4472.258006
Buf/Inv area:                      177.954001
Noncombinational area:             723.520023
Macro/Black Box area:                0.000000
Net Interconnect area:      undefined  (Wire load has zero net area)

Total cell area:                  5195.778029
Total area:                 undefined
Loading db file '/proj/ece350-014-spring2020/ClassShare/45nm_libs_front_end/NLDM/NangateOpenCellLibrary_slow.db'
Information: Propagating switching activity (low effort zero delay simulation). (PWR-6)
Warning: Design has unannotated primary inputs. (PWR-414)
Warning: Design has unannotated sequential cell outputs. (PWR-415)
```

Timing Report:

```
Report : timing
        -path full
        -delay max
        -max_paths 1
Design : DFE
Version: P-2019.03-SP5-1
Date   : Sun May 10 22:20:12 2020
****************************************

Operating Conditions: slow   Library: NangateOpenCellLibrary_SS
Wire Load Model Mode: top

  Startpoint: R1_reg[0][1]
              (rising edge-triggered flip-flop clocked by clock')
  Endpoint: R1_reg[1][7]
            (rising edge-triggered flip-flop clocked by clock')
  Path Group: clock
  Path Type: max

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  DFE                5K_hvratio_1_1        NangateOpenCellLibrary_SS

  Point                                                   Incr       Path
  --------------------------------------------------------------------------
  clock clock' (rise edge)                                5.00       5.00
  clock network delay (ideal)                             0.00       5.00
  R1_reg[0][1]/CK (DFFR_X1)                               0.00       5.00 r
  R1_reg[0][1]/Q (DFFR_X1)                                0.27       5.27 f
  sum0/delay[1] (sum_15)                                  0.00       5.27 f
  sum0/add_1_root_add_0_root_add_31_2/B[1] (sum_15_DW01_add_1_DW01_add_31)
                                                          0.00       5.27 f
  sum0/add_1_root_add_0_root_add_31_2/U1_1/S (FA_X1)      0.42       5.69 f
  sum0/add_1_root_add_0_root_add_31_2/SUM[1] (sum_15_DW01_add_1_DW01_add_31)
                                                          0.00       5.69 f
  sum0/add_0_root_add_0_root_add_31_2/A[1] (sum_15_DW01_add_0_DW01_add_30)
                                                          0.00       5.69 f
  sum0/add_0_root_add_0_root_add_31_2/U1_1/CO (FA_X1)     0.32       6.01 f
  sum0/add_0_root_add_0_root_add_31_2/U1_2/CO (FA_X1)     0.29       6.30 f
  sum0/add_0_root_add_0_root_add_31_2/U1_3/CO (FA_X1)     0.30       6.60 f
  sum0/add_0_root_add_0_root_add_31_2/U1_4/CO (FA_X1)     0.30       6.89 f
  sum0/add_0_root_add_0_root_add_31_2/U1_5/CO (FA_X1)     0.30       7.19 f
  sum0/add_0_root_add_0_root_add_31_2/U1_6/CO (FA_X1)     0.30       7.48 f
  sum0/add_0_root_add_0_root_add_31_2/U1_7/S (FA_X1)      0.36       7.84 f
  sum0/add_0_root_add_0_root_add_31_2/SUM[7] (sum_15_DW01_add_0_DW01_add_30)
                                                          0.00       7.84 f
  sum0/out[7] (sum_15)                                    0.00       7.84 f
  R1_reg[1][7]/D (DFFR_X1)                                0.01       7.85 f
  data arrival time                                                  7.85

  clock clock' (rise edge)                               15.00      15.00
  clock network delay (ideal)                             0.00      15.00
  R1_reg[1][7]/CK (DFFR_X1)                               0.00      15.00 r
  library setup time                                     -0.17      14.83
  data required time                                                14.83
  --------------------------------------------------------------------------
  data required time                                                14.83
  data arrival time                                                 -7.85
  --------------------------------------------------------------------------
  slack (MET)                                                        6.97
```

```
****************************************
Report : timing
        -path full
        -delay min
        -max_paths 1
Design : DFE
Version: P-2019.03-SP5-1
Date   : Sun May 10 22:20:12 2020
****************************************

Operating Conditions: fast   Library: NangateOpenCellLibrary_FF
Wire Load Model Mode: top

  Startpoint: R1_reg[0][1]
              (rising edge-triggered flip-flop clocked by clock')
  Endpoint: R1_reg[1][1]
            (rising edge-triggered flip-flop clocked by clock')
  Path Group: clock
  Path Type: min

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  DFE                5K_hvratio_1_1        NangateOpenCellLibrary_SS

  Point                                                   Incr       Path
  --------------------------------------------------------------------------
  clock clock' (rise edge)                                5.00       5.00
  clock network delay (ideal)                             0.00       5.00
  R1_reg[0][1]/CK (DFFR_X1)                               0.00       5.00 r
  R1_reg[0][1]/Q (DFFR_X1)                                0.36       5.36 r
  sum0/delay[1] (sum_15)                                  0.00       5.36 r
  sum0/add_1_root_add_0_root_add_31_2/B[1] (sum_15_DW01_add_1_DW01_add_31)
                                                          0.00       5.36 r
  sum0/add_1_root_add_0_root_add_31_2/U1_1/S (FA_X1)      0.16       5.52 r
  sum0/add_1_root_add_0_root_add_31_2/SUM[1] (sum_15_DW01_add_1_DW01_add_31)
                                                          0.00       5.52 r
  sum0/add_0_root_add_0_root_add_31_2/A[1] (sum_15_DW01_add_0_DW01_add_30)
                                                          0.00       5.52 r
  sum0/add_0_root_add_0_root_add_31_2/U1_1/S (FA_X1)      0.14       5.66 r
  sum0/add_0_root_add_0_root_add_31_2/SUM[1] (sum_15_DW01_add_0_DW01_add_30)
                                                          0.00       5.66 r
  sum0/out[1] (sum_15)                                    0.00       5.66 r
  R1_reg[1][1]/D (DFFR_X1)                                0.01       5.67 r
  data arrival time                                                  5.67

  clock clock' (rise edge)                                5.00       5.00
  clock network delay (ideal)                             0.00       5.00
  R1_reg[1][1]/CK (DFFR_X1)                               0.00       5.00 r
  library hold time                                       0.02       5.02
  data required time                                                 5.02
  --------------------------------------------------------------------------
  data required time                                                 5.02
  data arrival time                                                 -5.67
  --------------------------------------------------------------------------
  slack (MET)                                                        0.65
```

Analysis:

1. **Design Architecture:** For our design we ended up pipelining our inputs in order to accurately propagate everything. We also pipelined our architecture so that we can easily delay our output to begin on the 9th clock cycle as demonstrated in the MATLAB code. Along the pipeline, multiplication and modules from the feed forward and feedback components are fed into a summation module which propagates to locations further down the pipeline. In order to conserve power, we decided to hold all of the weights and deltas into single registers so that it minimized the amount of clocking needed in our design.
2. **Critical Path/Timing Report:** The critical path of the system starts at the input of either the training data or the distorted input signal and goes through all adders which involves 17 clock cycles to complete. The longest path taken between clock cycles is where the input needs to go through any of the multiplying modules and then the summation module to update the current data going through the summation path. The timing report includes multiple paths taken from the input to the output and vary in required time and arrival time depending on the path taken.
3. **Formal Verification:** We were unable to reach this portion of the project however this step would include comparing the output gained from running the designed module with a specific set of inputs and comparing that to the expected results. This is a more precise step than verifying the outputs through VCS not only because it uses the gate-level netlist received from Design Vision, but it is able to verify outputs better than manually doing so.
4. **Prime Time Timing**: We were also unable to reach this version of the project however this step would involve verifying timing checks throughout the entire system. This goes

more in depth than the timing report received from Design Vision through running the .tcl file and gives the user more accurate results regarding any timing problems or infractions.

Filepath:

~/proj/ece350-014-spring2020/llc220/Final