Quadrature Decoder Code Example

2.0

Features

- Project uses TCPWM component with Quadrature Decoder mode configuration
- Indicate capture interrupts on LED

General Description

This code example demonstrates the TCPWM component usage in the Quadrature Decoder mode.

Development kit configuration

This code example is designed to run on the CY8CKIT-042 kit from Cypress Semiconductor. A description of the kit, along with more example programs and ordering information, can be found at http://www.cypress.com/go/cy8ckit-042.

The project requires configuration settings changes to run on other kits from Cypress Semiconductor. Table 1 is the list of the supported kits. To switch from CY8CKIT-042 to any other kit, change the project's device with the help of Device Selector called from the project's context menu.

Table 1. Development Kits vs Parts

Development Kit	Device
CY8CKIT-042	CY8C4245AXI-483
CY8CKIT-040	CY8C4014LQI-422
CY8CKIT-042-BLE	CY8C4247LQI-BL483
CY8CKIT-044	CY8C4247AZI-M485
CY8CKIT-046	CY8C4248BZI-L489
CY8CKIT-041	CY8C4045AZI-S413 / CY8C4146AZI-S433
CY8CKIT-048	CY8C4A45LQI-483

The pin assignments for the supported kits are in Table 2.

Table 2. Pin Assignment

Pin Name	Development Kit						
	CY8CKIT-042	CY8CKIT-040	CY8CKIT-042 BLE	CY8CKIT-044	CY8CKIT-046	CY8CKIT-041	CY8CKIT-048
LED_GREEN	P0[2]	P1[1]	P3[6]	P2[6]	P5[3]	P2[6]	P2[6]
PhiA_Out	P2[0]	P2[0]	P2[0]	P2[0]	P2[0]	P2[0]	P2[0]
PhiA_In	P0[1]	P0[1]	P0[1]	P0[1]	P0[1]	P0[1]	P4[0]
PhiB_In	P0[0]	P0[0]	P0[0]	P0[0]	P0[0]	P0[0]	P4[1]

The following steps should be performed to observe the project operation:

1. Connect PhiA_Out to PhiA_In.
2. Connect the logic low (Gnd) or the logic high (3.3V) signal to PhiB_In.
3. Build the project and program the hex file on to the target device.
4. Power cycle the device and observe the results on the LEDs.

Project configuration

The code example consists of the following components: TCPWM, Clock, two digital output pins, two digital input pins, and Interrupt. The TCPWM is used as the Quadrature Decoder mode with the 1x Decoding mode. One of the output pins is used for PhiA signal generation. Another output pin is used to reflect a capture event when interrupts happen.

Project description

The counter is initialized with the mid-point counter value (0x8000) on an index event. A positive edge on phiA increments the counter when phiB is 0 and decrements the counter when phiB is 1. In the project, the TCPWM counts from 0x8000u down to 0u or from0x8000 to 0xFFFFu . If the counter reaches the 0xFFFFu value, the interrupt happens, the green color LED toggles, and the counter is initialized with the mid-point value (0x8000u).

The index event is generated by the API (QuadDec_TriggerCommand(QuadDec_MASK, QuadDec_CMD_RELOAD)).

The phiA signal is generated by the PhiAbGeneration function in the main.c file.

If the phiB signal connected to the logic low signal, a simulation is emulated, when the shaft is rotating in the clockwise direction (A leads B). If the phiB signal is connected to the logic high signal, a situation is emulated, when the shaft is rotating in the counter-clockwise direction (B leads A).

Expected results

The green color LED is toggling when the counter value is captured (0xFFFF).

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