1、(10p)

1-bit comparator – logic expression , draw the circuit and complete the time diagram

A	B		$F_{A<B}$	$F_{A=B}$	$F_{A>B}$
0	0		0	1	0
0	1		1	0	0
1	0		0	0	1
1	1		0	1	0

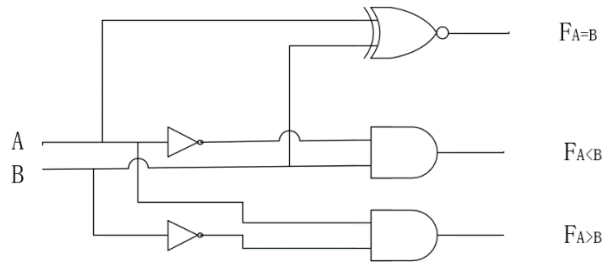
Expression:

$F_{A=B} = \overline{A \oplus B}$

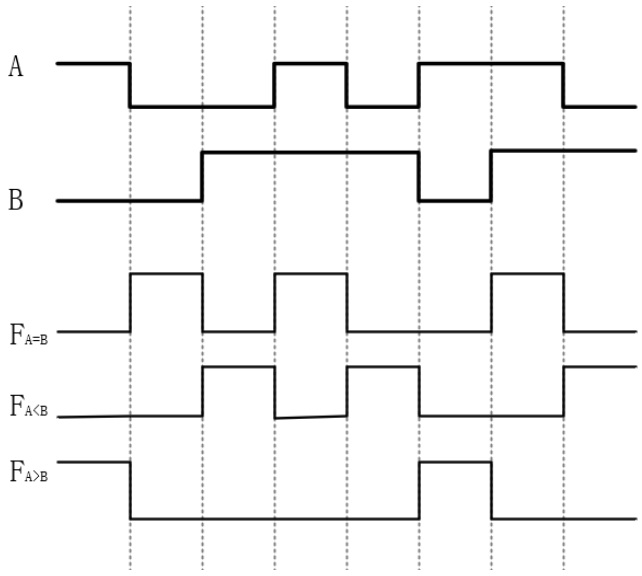
$F_{A<B} = \overline{A}\ B$

$F_{A>B} = A\ \overline{B}$

Circuit: (4p)



Time diagram: (6p)



2、(10p)

reduce the expression $F(x,y,z,w) = \sum m(2,4,6,8,13,14,15) + \sum d(0,7,9,10)$

Karnaugh map：(6p)

zw \ xy	00	01	11	10
00	d	1		1
01			1	d
11		d	1	
10	1	1	1	d

$$F = \bar{y}\bar{w} + \bar{x}\bar{w} + yz + x\bar{z}w \qquad (4p)$$

或将$x\bar{z}w$替换为xyw

即：$F = \bar{y}\bar{w} + \bar{x}\bar{w} + yz + xyw$

3、(15p)Give the truth table of 1-bit full adder, and implement it using 1-of-8 multiplexer.

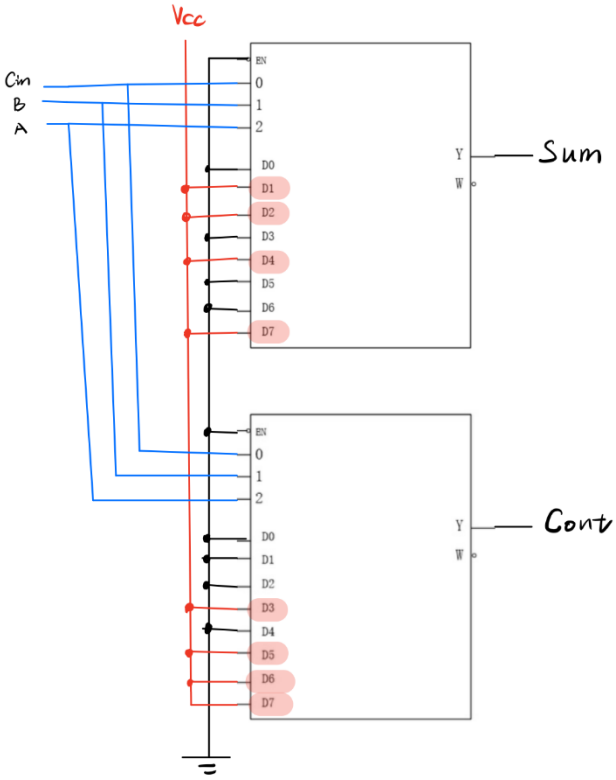
Truth Table：(8p)

A	B	Cin	Cout	Sum
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

1- of-8 multiplexer：(7p)

$$Cout = f(a,b,Cin) = \sum m(3,5,6,7)$$

$$Sum = f(a, b, Cin) = \sum m(1, 2, 4, 7)$$



4、$f(a, b, c) = b\bar{c} + a\bar{b} + abc$

1)(10p) SOP and POS

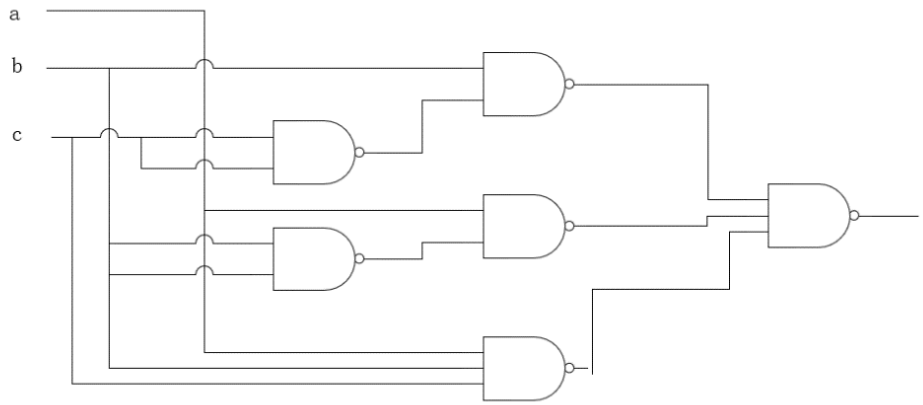
$f(a, b, c) = \sum m(2, 4, 5, 6, 7) = \bar{a}b\bar{c} + a\bar{b}\bar{c} + a\bar{b}c + ab\bar{c} + abc$ (5p)

$f(a, b, c) = \prod M(0, 1, 3) = (a + b + c)(a + b + \bar{c})(a + \bar{b} + \bar{c})$ (5p)

2) (10p)nand gates

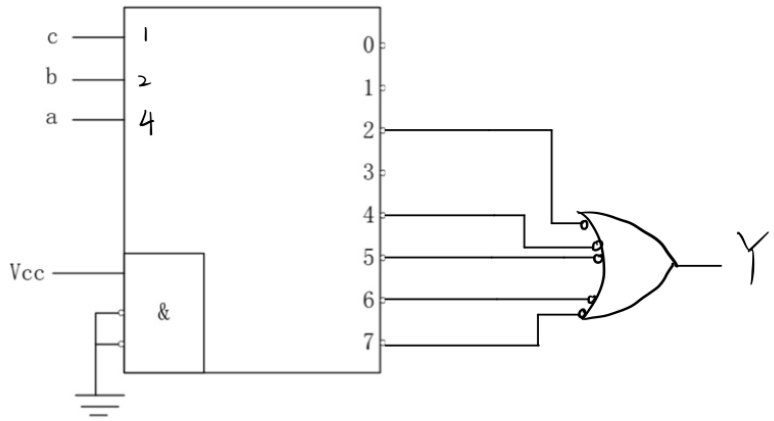
$f(a, b, c) = \overline{\overline{b\bar{c}} \cdot \overline{a\bar{b}} \cdot \overline{abc}}$ (5p)

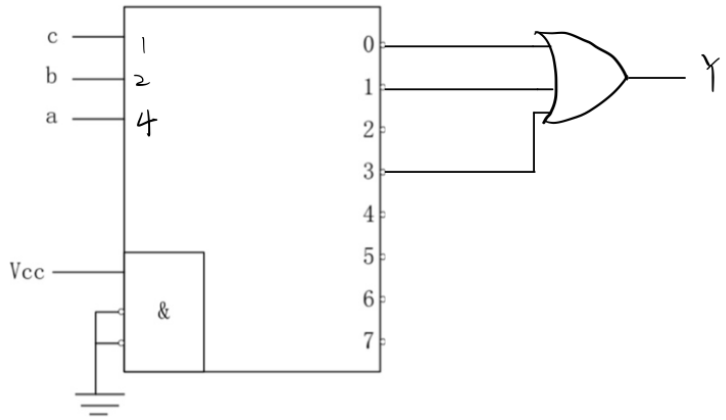
(或者是 $\overline{\bar{a} \cdot \overline{b\bar{c}}}$)



(5p)

3) (15p) 3-line-to-8-line decoder





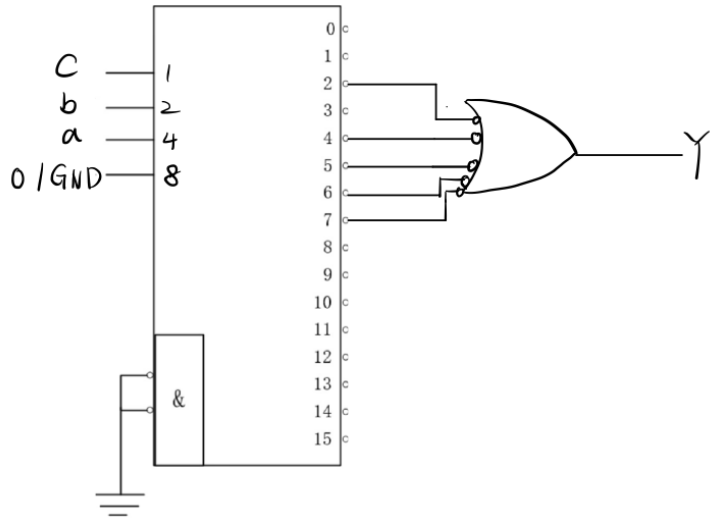
输出采用低有效输出，最小项使用与非门（非-或门）连接，或最大项使用或门连接。

4)(15p) 1-of-16 decoder　(4-to-16 decoder)

可以将最高位接 1，此时采用输出位 8-15，

或者将最高位接 0，此时采用输出位 0-7，

最小项采用与非（非-或）门，或利用最大项使用或门输出。



5)(15p)1-of-4 multiplexer

(4p)

ab / c	00	01	11	10
0	0	1	1	1
1	0	0	1	1

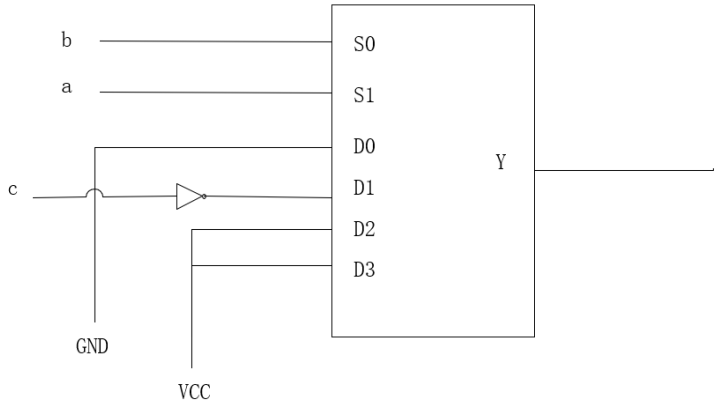
ab / c	00	01	11	10
0	0	1	1	1
1	0	0	1	1

$D_0=0$ $D_1=C'$ $D_3=1$ $D_2=1$

降维(4p)

a / b	0	1
0	0	1
1	C’	1

选择一个数据输入端作为信号输入，S1 连接 a,S0 连接 b,D0 接地，D1 接 c’,D2 和 D3 接 Vcc　(7p)


b
a
c
S0
S1
D0
D1
D2
D3
Y
GND
VCC