四川大学数字逻辑复习题（2019～2020 - 1）

课程号：304131030 课程名称：数字逻辑（双语） 任课教师：潘薇吴志红卢晓春陈虎吕泽均熊伟袁学东兰时勇

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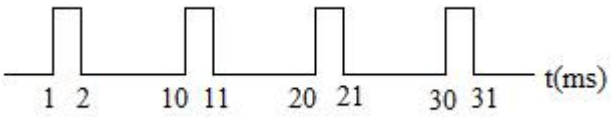
Chapter 1

Digital Analog logic levels Digital Waveforms ICs

P12 TRUE/FALSE QUIZ 1~9; SELF TEST 1~12

1. As the following waveform shows, it's period is ( ) and frequency is ( ).



Chapter 2

Decimal Binary Octal Hexadecimal Conversion Binary Arthmetics Signed Numbers

Complement Codes Error Detection Codes

P58 TRUE/FALSE QUIZ 1~11; SELF TEST 1~20

1. Covert the following numbers to the indicated radix numbers.

a). $(1101011.1)_2$ = ( )$_{10}$ = ( )$_{BCD}$

b). $(1011101.0101)_2$ = ( )$_{16}$ = ( )$_8$

c). $(01000101.011000100101)_{BCD}$ = ( )$_{10}$ = ( )$_2$ = ( )$_{16}$

d). $(52.625)_{10}$ = ( )$_2$ = ( )$_{16}$ = ( )$_{BCD}$.

2. Perform the following binary multiplications:

a) 111×101 b) 1110×1101

3. Convert each decimal number into its corresponding 2s complement code prior to performing the indicated operation.

a) (-101)+ (11) b) (63)- (-15)

4.The following is the operation of the complement, which is correct. ( )

	original code	complement code
A	01110001	01111111
B	10011001	11100111
C	10010010	11101101
D	00110010	11001110

Chapter 3

Gates: Inverter/AND/OR/NAND/NOR/E-OR/E-NOR…　　Truth Tables　　Logic Expressions

P100　TRUE/FALSE QUIZ 1~7, 9;　　SELF TEST 1~4, 9

1. An exclusive-NOR function *f*(*A*,*B*) is expressed as __________.

Chapter 4

Boolean Algebra　Logic Circuits　　Simplificaion　　Standard Forms　SOP　　POS　　K-Map

P153　TRUE/FALSE QUIZ 1~10;　　SELF TEST 1~18

1. Demonstrate by means of truth tables the validity of $AB' + A'B = (A+B)(A'+B')$。

2. Prove the identity of the following Bootlean equation, using algebraic manipulation: $AB+\overline{A}C + (\overline{B}+\overline{C})D = AB+\overline{A}C+D$。

3. Simplify the Boolean expressions to expessions containing a minimum number of literals: $F=A(C+BD)(\overline{A}+BD)+B(\overline{C}+DE)+BC$，and implement it using logic gates。

4. A Karnaugh map is a diagram made up of squares that is to simplify Boolean eqations. Each square represents a__________or__________from an equation.

5. ____________is a term in a Boolean equation that represents a condition where an output variable is a logical 0 in the output function truth table.

6. Simplify the following Boolean equations:

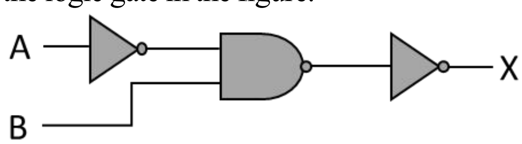
   1) R = f(w,x,y,z) = ∑m(1,3,4,5,6,9,11,12,13,14)

   2) T = a’ bc+ad’ +bcd’

   3)G = y’z+w’xy’+w’xy+xy’z

7. ApplyDeMorgan’s theorems to the following: $\overline{(A+\overline{B\overline{C}}+CD)}+\overline{\overline{BC}}$

8. Write the Boolean expression for the logic gate in the figure.



9. Convert the following expression to standard SOP forms and develop its truth table: $\overline{A}(B+\overline{C})+A(B\oplus C)$

10. Using Boolean algebra, simplify the following expression: $(B+BC)(B+\overline{B}C)(B+D)$

11. Use a Karnaugh map to reduce each expression.

   a) $F(a,b,c,d)=\sum m(2,4,6,8,9,12,13,14,15)$

   b) $F(x,y,z,w)=\sum m(2,4,6,8,13,14,15)+\sum d(0,7,9,10)$

Chapter 5

Combinatioonal Logic Circuits　Analysis /Design　Universal gates

P188　TRUE/FALSE QUIZ 1~10;　　SELF TEST 1~10

1. Implement F=AB+A(B+C)+B(B+C) using and only using 2 input AND and OR。

2. Design a truth table to indicate a majority of three inputs is true, write down the simplified Boolean equation.

3. A four-bit binary character is presented to a circuit that must detect whether the input is a legitimate BCD code. If a non-BCD code is entered, the output is to be true(logical 1). Please construct the truth table and write down the simplified Boolean equation.

4. Use AND gates, OR gate, and inverters as needed to implement the following logic expressions as stated.

a) $X = A(CD + B)$　　b) $X = \overline{ABC} + B(EF + \overline{G})$

5. The standard AND-OR is a logical expression consisting of (　　　　).

a) 与项相或　　b)最小项相或　　c)最大项相与　　d)或项相与

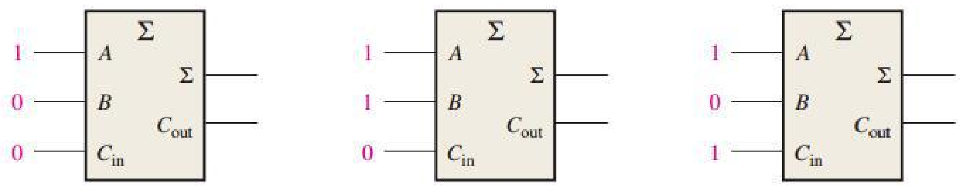
Chapter 6

Adders　Comparators　Decoders　Encoders　MUX　Parity Generators/Checkers

P246　TRUE/FALSE QUIZ 1~10;　　SELF TEST 1~12

1. If a 4-16 decoder with active-LOW outputs exhibits a LOW on the decimal 6 output, what are the inputs?

2. For each of the three full-adders in Figure, determine the outputs.

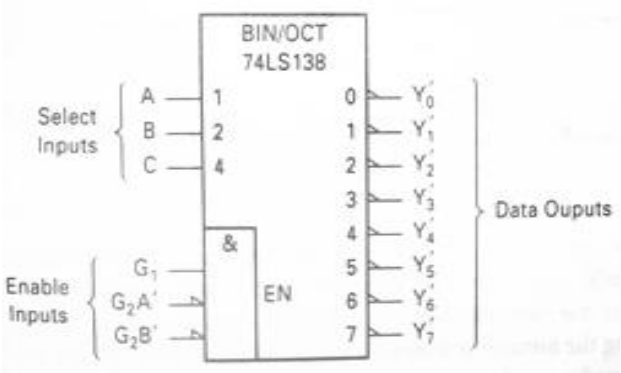


(a)　(b)　(c)

3. The following sequences of bits (right-most bit first) appear on the inputs to a 4-bit parallel adder. Determine the resulting sequence of bits on each sum output.

A_1	1010
A_2	1100
A_3	0101
A_4	1101
B_1	1001
B_2	1011
B_3	0000
B_4	0001

4. Use the decoder 74LS138 with active-LOW outputs to implement the function of a full-adder.



Chapter7

Latches/Flip Flops　　Edge-Triggered

P298　TRUE/FALSE QUIZ 1~7;　　SELF TEST 1~3, 5~9

Chapter 8

Counters　　Asynchronous/Synchronous

P353　TRUE/FALSE QUIZ 1~10;　　SELF TEST 1~7, 9~11, 13,14

1. Assume the clock for a 3-bit binary counter is 512MHz. The output frequency of the third stage is____MHz.
2. How many flip-flops does a modulus-8 ring counter require ？

Chapter 9

Registers　　Shift　　Serial/Parallel

P394　TRUE/FALSE QUIZ 1~10;　　SELF TEST 1~8

1. A register's function include (　　)

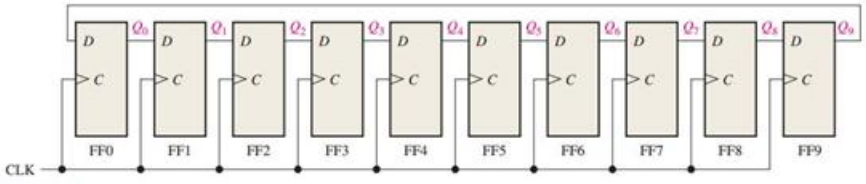
a) data storage　　b) data movement　　c) neither a) not b)　　d) both a) and b)

2. To parallel load a byte of data into a shift register with a synchronous load, there must be (　　)

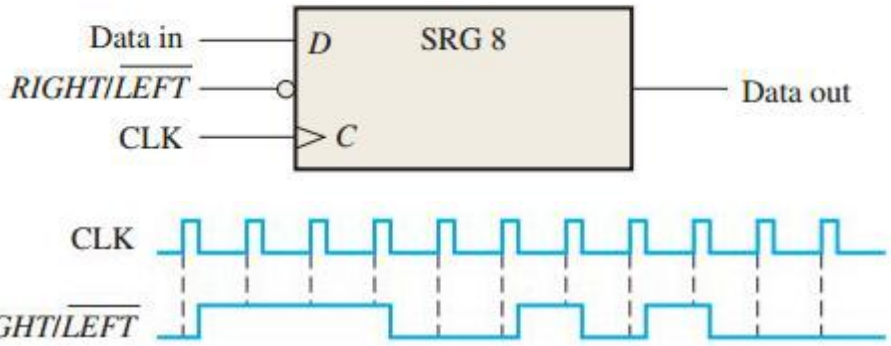
a) one clock pulse　　b) one clock pulse for each I in the data

c) eight clock pulses　　d) one clock pulse for each 0 in the data

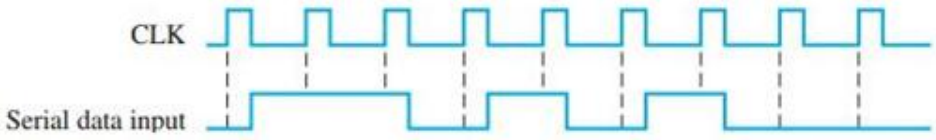
3. For the ring counter in Figure, show the waveforms for each flip-flop output with respect to the clock. Assume that FF0 is initially SET and that the rest are RESET. Show at least ten clock pulses.



4. For the 8-bit bidirectional register in Figure, determine the state of the register after each clock pulse for the RIGHT/LEFT control waveform given. A HIGH on this input enables a shift to the right, and a LOW enables a shift to the left. Assume that the register is initially storing the decimal number seventy-six in binary, with the right-most position being the LSB. There is a LOW on the data-input line.

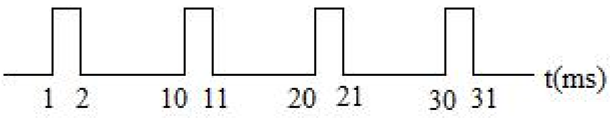


5. For the data input and clock in Figure, determine the states of each flip-flop in the shift register of Figure and show the Q waveforms. Assume that the register contains all 1s initially.



Chapter 1

1. As the following waveform shows, it's period is (10ms) and frequency is (100Hz).



Chapter 2

1. Covert the following numbers to the indicated radix numbers.

a). $(1101011.1)_2$ = (107.5)$_{10}$ = (100000111.0101)$_{BCD}$

b). $(1011101.0101)_2$ = (5C.5)$_{16}$ = (135.24)$_8$

c). $(01000101.011000100101)_{BCD}$ = (45.625)$_{10}$ = (101101.101)$_2$ = (2D.A)$_{16}$

d). $(52.625)_{10}$ = ( )$_2$ = ( )$_{16}$ = ( )$_{BCD}$.

2. Perform the following binary multiplications:

a). 111×101   b). 1110×1101

```
(a)      111
       × 101
    ---------
         111
     0   00
    11   1
    ---------
   100   011
```

```
(b)      1110
       × 1101
    ----------
         1110
     0   000
    11   10
   111   0
    ----------
  1011   0110
```

3. Convert each decimal number into its corresponding 2s complement code prior to performing the indicated operation.

a). (-101)+ (11)   b). (63)- (-15)

4. The following is the operation of the complement, which is correct. ( )

	original code	complement code
A	01110001	01111111
B	10011001	11100111
C	10010010	11101101
D	00110010	11001110

Chapter 3

1. An exclusive-NOR function *f(A,B)* is expressed as *A'B'+AB* .

Chapter 4

1. Demonstrate by means of truth tables the validity of $AB' + A'B = (A + B)(A' + B')$。

2. Prove the identity of the following Bootlean equation, using algebraic manipulation: $AB+\overline{A}C + (\overline{B} + \overline{C})D = AB + \overline{A}C + D$。

3. Simplify the Boolean expressions to expessions containing a minimum number of literals: F=$A(C+BD)(\overline{A} + BD)+B(\overline{C} + DE)+BC$， and implement it using logic gates。

4. A Karnaugh map is a diagram made up of squares that is to simplify Boolean eqations. Each square represents a __minterm__ or __maxterm__ from an equation.

5. __Maxterm__ is a term in a Boolean equation that represents a condition where an output variable is a logical 0 in the output function truth table.

6. Simplify the following Boolean equations:

(1) R = f(w,x,y,z) = ∑m(1,3,4,5,6,9,11,12,13,14)

(2) T = a'bc+ad'+bcd'

(3) G = y'z+w'xy'+w'xy+xy'z

Answers:

(1) R = XY'+X'Z+XZ'

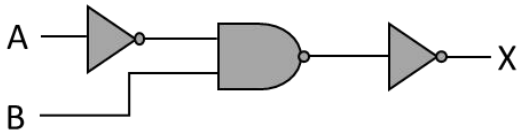
(2) T = a'bc+ad'

(3) G = w'x+y'z

7. ApplyDeMorgan's theorems to the following: $\overline{(A + \overline{B\overline{C}} + CD)} + \overline{\overline{B\overline{C}}}$

$= \overline{A}B\overline{C}(\overline{C} + \overline{D}) + BC = \overline{A}B\overline{C} + BC = \overline{A}B + BC$

8. Write the Boolean expression for the logic gate in the figure.



X=$\overline{\overline{A}B}$

9. Convert the following expression to standard SOP forms and develop its truth table: $\overline{A}(B + \overline{C}) + A(B \oplus C)$

$\overline{A}BC + \overline{A}B\overline{C} + AB\overline{C} + \overline{A}\overline{B}\overline{C} + A\overline{B}C$

A	B	C	X
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0

10. Using Boolean algebra, simplify the following expression: (B+BC)(B+$\overline{B}C$)(B+D) =B

11. Use a Karnaugh map to reduce each expression.

a) F(a,b,c,d)=∑ m(2,4,6,8,9,12,13,14,15)

b) F(x,y,z,w)=∑ m(2,4,6,8,13,14,15) + ∑ d(0,7,9,10)

(a)

cd / ab	00	01	11	10
00				1
01	1			1
11	1	1	1	1
10	1	1		

F=ab+ac’ +bd’ +a’ cd’

(b)

zw / xy	00	01	11	10
00	d			1
01	1		d	1
11		1	1	1
10	1	d		d

F=zw’+yz+x’w’+y’w’+xz’w

Chapter 5

1.Implement F=AB+A(B+C)+B(B+C) using and only using 2 input AND and OR。

2. Design a truth table to indicate a majority of three inputs is true, write down the simplified Boolean equation.

Answer:

A	B	C	Y
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

AB / C	00	01	11	10
0			1	
1		1	1	1

Y＝AB＋BC＋AC

3. A four-bit binary character is presented to a circuit that must detect whether the input is a legitimate BCD code. If a non-BCD code is entered, the output is to be true(logical 1). Please construct the truth table and write down the simplified Boolean equation.

Answer:

hex	A_3	A_2	A_1	A_0	Y
0	0	0	0	0	0
1	0	0	0	1	0
2	0	0	1	0	0
3	0	0	1	1	0
4	0	1	0	0	0
5	0	1	0	1	0
6	0	1	1	0	0
7	0	1	1	1	0
8	1	0	0	0	0
9	1	0	0	1	0
a	1	0	1	0	1
b	1	0	1	1	1
c	1	1	0	0	1
d	1	1	0	1	1
e	1	1	1	0	1
f	1	1	1	1	1

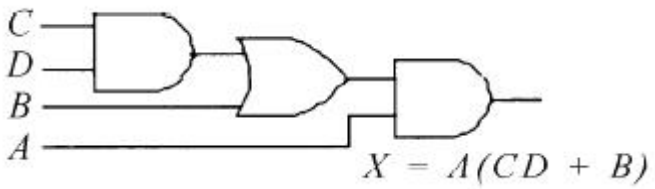
AB / CD	00	01	11	10
00			1	
01			1	
11			1	1
10			1	1

$Y = AB + AC$

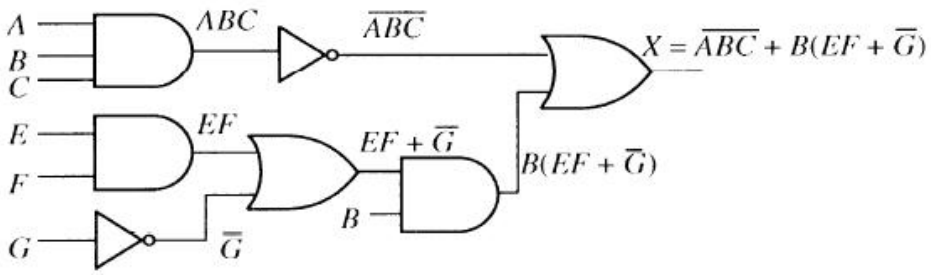
4. Use AND gates, OR gate, and inverters as needed to implement the following logic expressions as stated.

a) $X = A(CD + B)$ b) $X = \overline{ABC} + B(EF + \overline{G})$

(a)



(b)



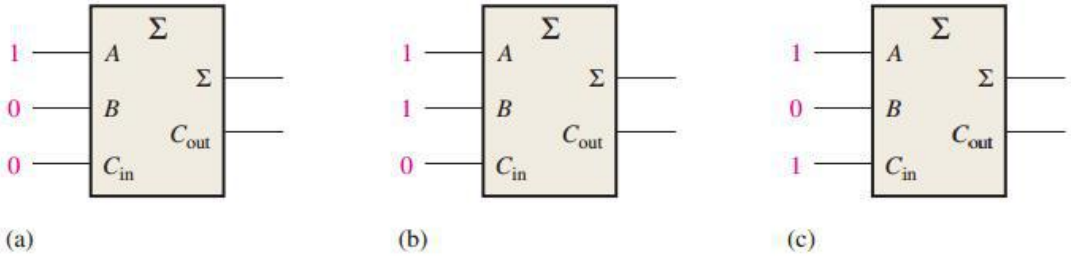
5. The standard AND-OR is a logical expression consisting of (B).

a) 与项相或　　b)最小项相或　　c)最大项相与　　d)或项相与

Chapter 6

1. If a 4-16 decoder with active-LOW outputs exhibits a LOW on the decimal 6 output, what are the inputs?

2. For each of the three full-adders in Figure, determine the outputs.



(a) The input bits are A = 1, B = 0, and Cin = 0. 1 + 0 + 0 = 1 with no carry, Therefore, ∑ = 1 and Cout = 0.

(b) The input bits are A = 1, B = 1, and Cin = 0. 1 + 1 + 0 = 0 with a carry of 1, Therefore, ∑ = 0 and Cout = 1.

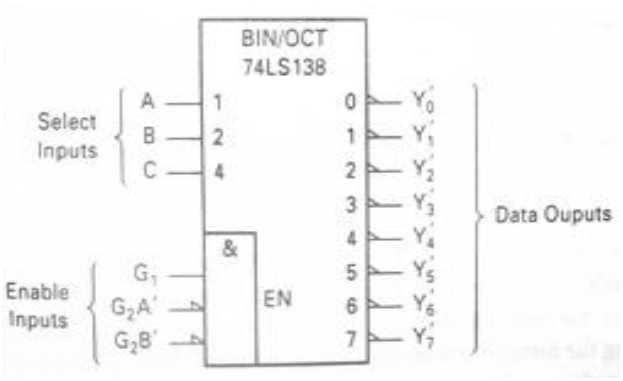
(c) The input bits are A = 1, B = 0, and Cin = 1. 1 + 0 + 1 = 0 with a carry of 1,, Therefore, ∑ = 0 and Cout = 1.

3. The following sequences of bits (right-most bit first) appear on the inputs to a 4-bit parallel adder. Determine the resulting sequence of bits on each sum output.

A_1	1010
A_2	1100
A_3	0101
A_4	1101
B_1	1001
B_2	1011
B_3	0000
B_4	0001

∑1 = 0111; ∑2 = 0011; ∑3 = 1110; ∑4 = 1110

4. Use the decoder 74LS138 with active-LOW outputs to implement the function of a full-adder.



解：（1）根据全加器的功能需求，列出真值表：

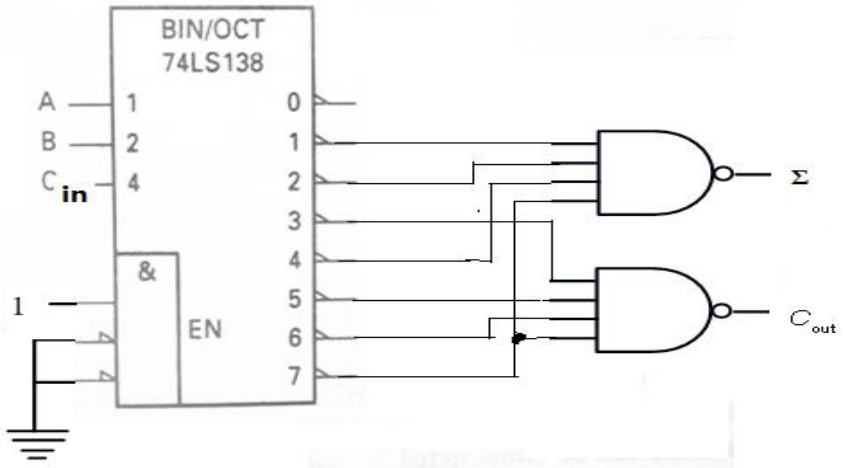
Inputs			Outputs	
A	B	C_{in}	C_{out}	Σ
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

（2）根据真值表写出输出的逻辑函数（最小项表达式）：

$$\Sigma = \Sigma m(1,2,4,7) = = \overline{m_1} \bullet \overline{m_2} \bullet \overline{m_4} \bullet \overline{m_7}$$

$$C_{out} = \Sigma m(3,5,6,7) = \overline{m_3} \bullet \overline{m_5} \bullet \overline{m_6} \bullet \overline{m_7}$$

根据 3 线-8 线译码器 74LS138 输入输出的有效电平，结合译码器的输出对应最小项 $\overline{Y_i} = \overline{m_i}$，i=0～7，再选用逻辑与非门实现电路设计如下：（5 分）



Chapter 9

1. A register's function include (d)

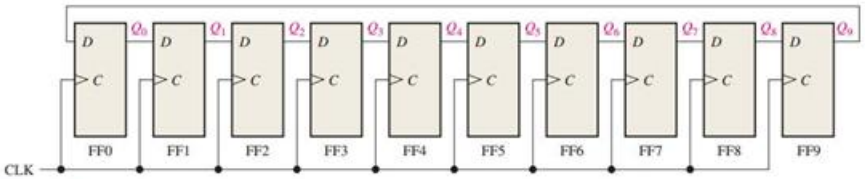
a) data storage b) data movement c) neither a) not b) d) both a) and b)

2. To parallel load a byte of data into a shift register with a synchronous load, there must be (a)

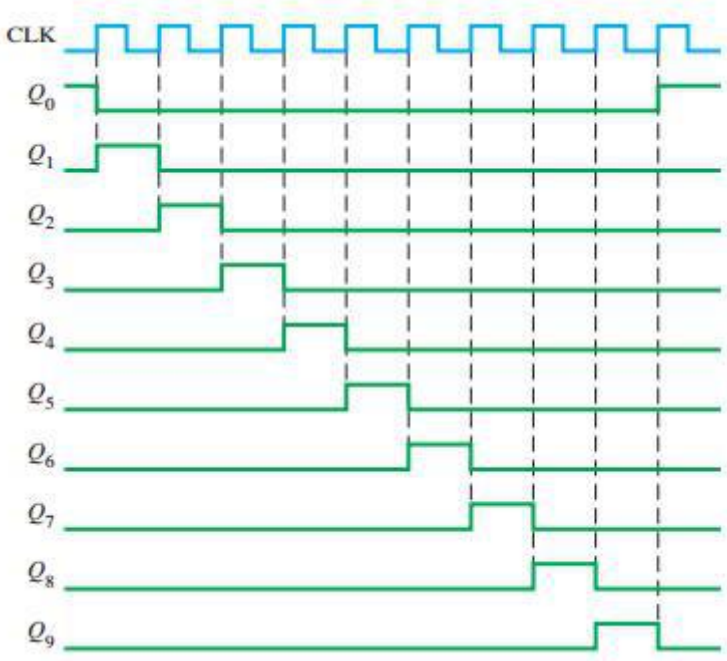
a) one clock pulse b) one clock pulse for each I in the data

c) eight clock pulses d) one clock pulse for each 0 in the data

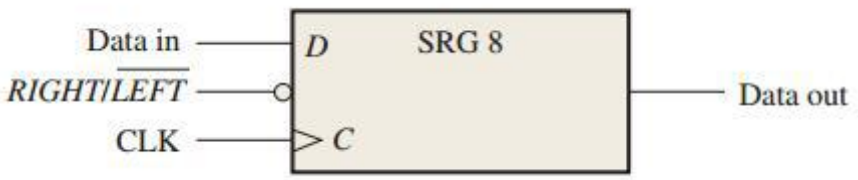
3. For the ring counter in Figure, show the waveforms for each flip-flop output with respect to the clock. Assume that FF0 is initially SET and that the rest are RESET. Show at least ten clock pulses.

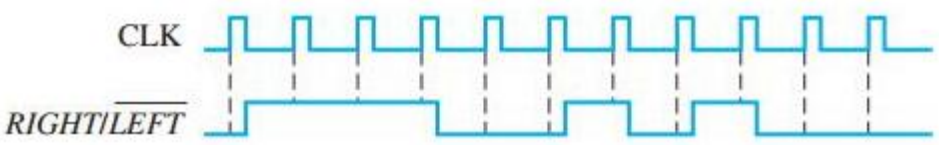


Answer:



4. For the 8-bit bidirectional register in Figure, determine the state of the register after each clock pulse for the RIGHT/LEFT control waveform given. A HIGH on this input enables a shift to the right, and a LOW enables a shift to the left. Assume that the register is initially storing the decimal number seventy-six in binary, with the right-most position being the LSB. There is a LOW on the data-input line.





Answer:

Initially (76): 01001100

CLK1: 10011000 left

CLK2: 01001100 right

CLK3: 00100110 right

CLK4: 00010011 right

CLK5: 00100110 left

CLK6: 01001100 left

CLK7: 00100110 right

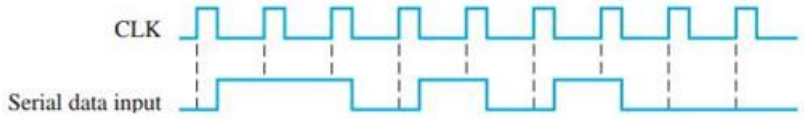
CLK8: 01001100 left

CLK9: 00100110 right

CLK10: 01001100 left

CLK11: 10011000 left

5. For the data input and clock in Figure, determine the states of each flip-flop in the shift register of Figure and show the Q waveforms. Assume that the register contains all 1s initially.



Answer: