1. Covert the following numbers to the indicated radix numbers. (12p)

　　a). $(27.4)_8 = ($　　$)_2 = ($　　$)_{16} = ($　　$)_{10} = ($　　$)_{8421BCD}$

　　b). $(01000110.01110101)_{BCD} = ($　　$)_{10} = ($　　$)_2 = ($　　$)_{16}$

2. Calculate the following: (8p)

　　a) $1110 + 1011$　　b) $11001 - 10011$　　c) 1011×101　　d) $10010 \div 110$

3. Complete the following table of equivalent values. Use binary numbers with a sign bit and 7 bits for the value. (12p)

Decimal	Sign-magnitude	1's complement	2's complement
123			
-98			

4. For the input waveforms below, determine the output for the NAND gate and draw the timing diagram. (8p)
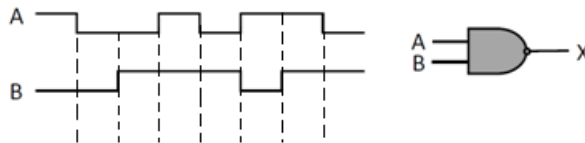
5. Write the Boolean expression for the logic gate: (6p)
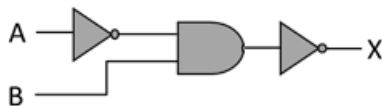
6. Apply DeMorgan's theorems to the following and simplify it: $\overline{(A + \overline{B\overline{C}} + \overline{C}D)} + \overline{BC}$ **(12p)**

7. Using Boolean algebra, simplify the following expression: $A(C+BD)(\overline{A} + BD) + B(\overline{C} + DE) + BC$ **(4p)**

8. Convert the following expression to standard SOP forms and develop its truth table: $\overline{A}(B + \overline{C}) + B \oplus C$ **(10p)**

9. Use a Karnaugh map to reduce each expression: (18p)

a) $f(a,b,c,d) = \Sigma(0,4,6,7,8,9,11,12,13,15)$　　　b) $f(a,b,c,d) = \Sigma m(0,2,4,8,10,14) + \Sigma d(5,6,7,12)$

10. Use AND gates, OR gate, and inverters as needed to implement the following logic expressions as stated. (10p)

　　a) $X = A(BD + C)$　　(3p)　　　(b) $X = \overline{A\overline{B}C} + B(A\overline{D} + \overline{C})$ (7p)