##### 数字逻辑（双语）2020年下学期第三次测试题

##### 一. Choose the best answer from the four choices. (30points)

1. 8 channel data selector, of which address input (select control) have（ ）

A.One B.Two C.Three D.Four

2.For synchronous RS flip-flops, if S= , the logic function of the（ ）flip-flop can be completed.

A.JK B. D C.T D.

3.A register’s function include （ ）.

A.Data storage B. data movement

C.Neither A not B D. Both A and B

4.To parallel load a byte of data into a shift register with a synchronous load, there must be（ ）.

A .One clock pulse B. One clock pulse for each I in the data

C.Eight clock pulses D. One clock pulse for each 0 in the data

5.A modulus-5 ring counter require （ ）.

A. Eight flip-flops B. Three flip-flops

C. Five flip-flops D. Twelve flip-flops

6. The group of bits 01110101 is serially shifted (left-most bit first) into an 8-bit parallel output shift register with an initial state of 11100100. After three clock pulses, the register contains （ ）.

A. 01110101 B. 11011100

C .10111100 D. 01111100

二．Fill in the blanks with the correct answer. (15 points)

1.A modulus-15 counter has 15 states requiring flip-flops.

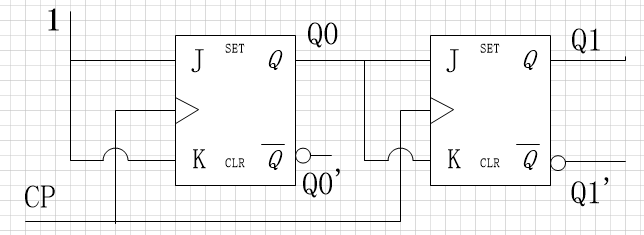
2. A 4-bit binary up/down counters is in the binary state of zero. The next state in the DOWN mode is .

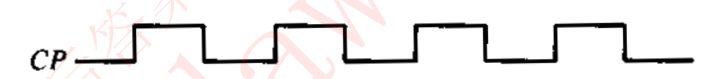
3.A J-K flip-flop with J=1 and K=1 has a 10KHz clock input,then the Q is a KHz square wave.

4.A circuit with 5 flip-flops can store bits binary numbers, that is,include states at most

**二.Calculation and Analysis.(55points)**

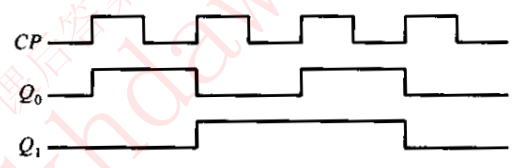
**1.Given the timing diagram for Q0 ,Q1.(10points)**



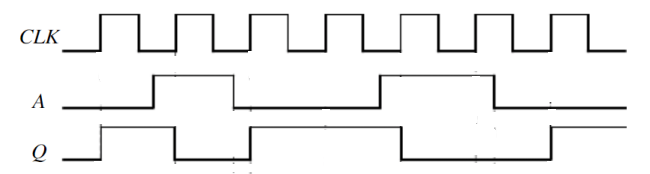
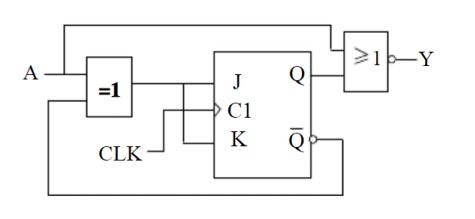


Q0

Q1



**2.draw the state table and state diagram, and complete the timing diagram by showing Y output according to the circuit in the following Figure. Assume the initial values are Q=0.(15 points)**



参考答案：(1)

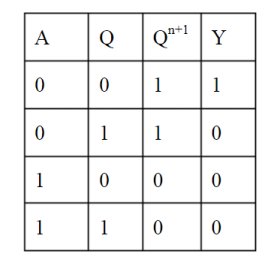
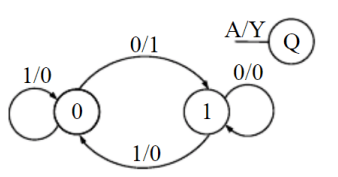
Write the characteristic equation 

Write the excitation equation

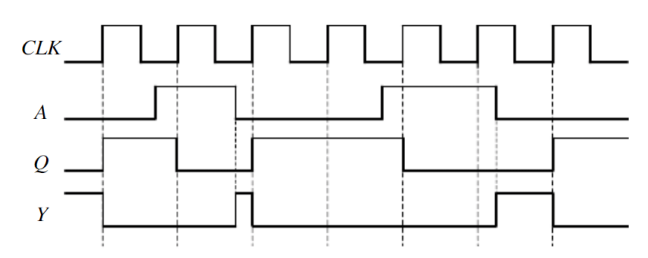
Write the next state equation.

Write the output variable equations.  （上面每个式子2分，共8分）

State table State diagram（2分）

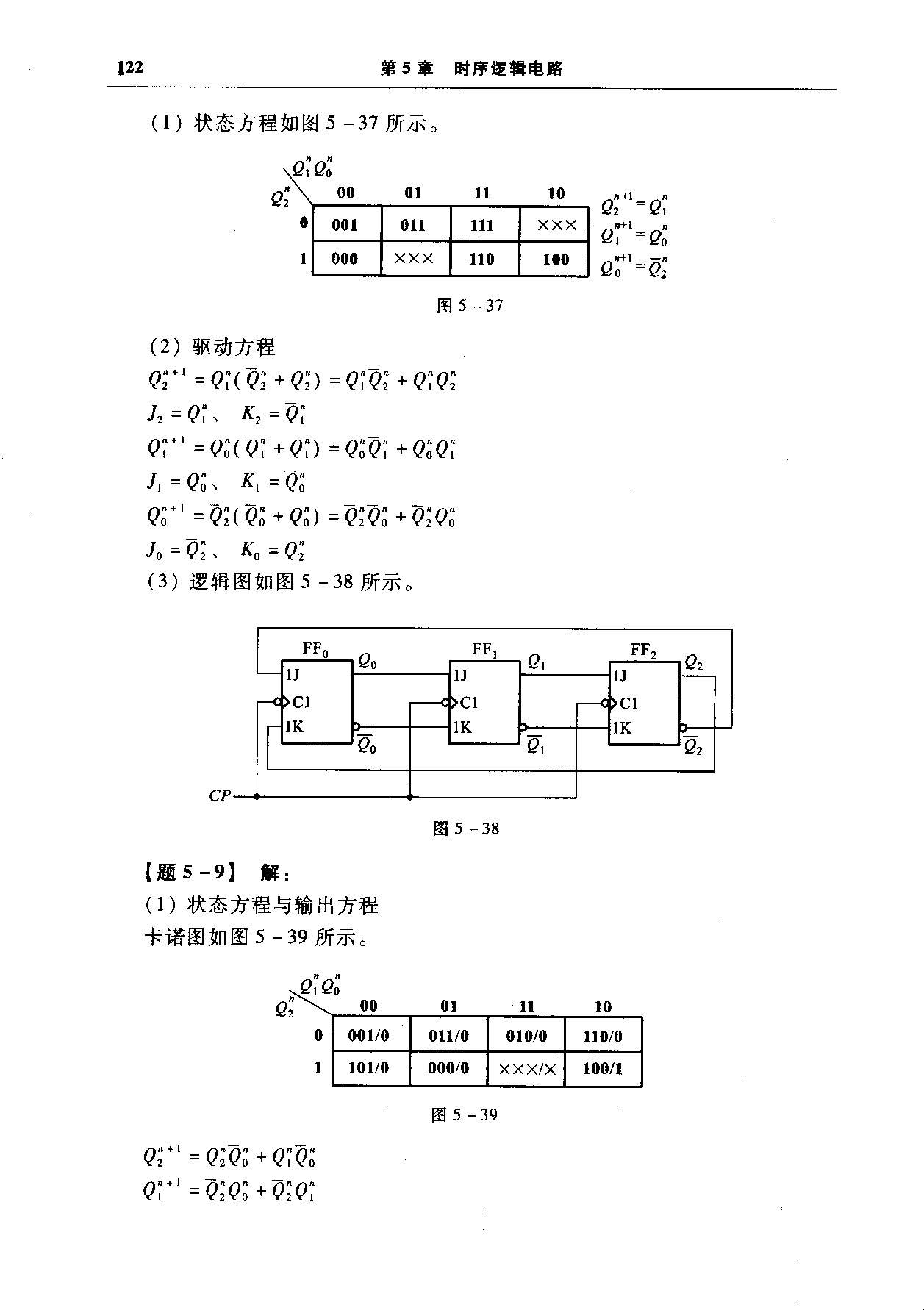
 

(2)Timing diagram（2分）

（3分）

**3.Please design a synchronous timing diagram with J,K flip-flop triggered by falling edge, the statechart diagram of which is shown as follows.(15points)**





（每项各5分）

**4.Design a counter to produce the following sequence: 1, 4, 5, 7, 1, …(open answer) (15points)**