# Fabiano Libano

## Bio

Birthday: March 8, 1996 | Birthplace: Madrid, Spain | Nationality: Brazil
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## Education

**Doctor's Degree | Computer Engineering**
Arizona State University, ASU, Tempe, United States.
2018 - 2021
Advisor: John Brunhaver
Topic: Novel low-overhead hardening methods and RHDB accelerator architectures for matrix multiplication and neural networks on FPGAs/ASICs.

**Master's Degree | Computer Engineering**
Universidade Federal do Rio Grande do Sul, UFRGS, Porto Alegre, Brazil
2017 - 2018
Advisor: Paolo Rech
Topic: Reliability analysis and hardening of neural networks on FPGAs.

**Bachelor's Degree | Computer Engineering**
Universidade Federal do Rio Grande do Sul, UFRGS, Porto Alegre, Brazil
2013 - 2017

## Languages

**Portuguese**
Understanding, Speaking, Writing, Reading: Mother Language

**English**
Understanding, Speaking, Writing, Reading: Fluent

**Spanish**
Understanding, Speaking, Writing, Reading: Fluent

## Main Fields of Interest

1. Fault-Tolerance, Reliability & Radiation Effects
2. Computer Architecture, Digital Systems & FPGAs
3. Artificial Intelligence & Machine Learning
4. Space Exploration
5. Bioinformatics

## Skills & Expertise

1. Radiation Testing: More than 1000 hours of hands on experience with neutron beam testing at RAL-ChipIR (UK) and at LANL-LANSCE (US). In addition to that, I have also had a brief experience with gamma cells for TID effects, and laser sources for evaluating potential architectural vulnerabilities (AVF) in integrated circuits.
2. RTL & FPGAs: Over 5 years of experience with FPGAs, writing application-specific, high-performance RTL descriptions, as well as fast prototyping with high-level synthesis (HLS). Particularly, I have a vast knowledge of the Xilinx environment, devices and development tools. Proficient in both Verilog and VHDL.
3. AI & Machine Learning: Experience with modeling, training and deploying artificial neural networks for image processing, linear regression and classification tasks. Furthermore, I have experience with reduced precision training and trimming techniques for neural networks. I have worked extensively with TensorFlow.
4. Languages (from most to least proficient): Python, C, Shell, Verilog, C++, VHDL, Java, Objective-C, Swift, Assembly, SQL, JavaScript.
5. Tools (from most to least proficient): Vivado, TensorFlow, Vitis, Xcode, Android Studio, Caffe, SPICE, Virtuoso, Wireshark, MATLAB, Photoshop.

## Awards

### IEEE NPSS Transactions on Nuclear Science Best Paper

2022

“Selective Hardening for Neural Networks in FPGAs” (#6 on my Publications list) was chosen by TNS editors to receive the 2022 best paper award. Eligible papers are those published in the 3rd year prior (2019), and the winner is the paper judged most useful to the Nuclear Science community according to the rate of downloads and citations in the 3 calendar years including the year of publication.

## Publications

1. F. Libano, P. Rech, “Reliability Analysis of Feed-Forward Artificial Neural Networks in System on Chips”, presented at Silicon Errors in Logic-Systems Effects (IEEE), 2017.
2. F. Libano, P. Rech, L. Tambara, J. Tonfat, F. Kastensmidt, “Evaluation of Feed-Forward Artificial Neural Networks Reliability in FPGAs”, presented at Nuclear and Space Radiation Effects Conference (IEEE), 2017.
3. F. Libano, P. Rech, L. Tambara, J. Tonfat, F. Kastensmidt, “On the Reliability of Feed-Forward Artificial Neural Networks in FPGAs”, at IEEE Transactions on Nuclear Science, 2017.
4. F. Libano, B. Wilson, M. Wirthlin, P. Rech, “Selective Hardening for Neural Networks in FPGAs”, at Nuclear and Space Radiation Effects Conference (IEEE), 2018.
5. F. Benevenuti, F. Libano, V. Pouget, F. Kastensmidt, P. Rech, “Comparative Analysis of Inference Errors in a Neural Network Implemented in SRAM-Based FPGA Induced by Neutron Irradiation and Fault Injection Methods”, presented at Symposium on Integrated Circuits and Systems Design (IEEE), 2018.
6. F. Libano, B. Wilson, J. Anderson, M. Wirthlin, C. Cazzaniga, C. Frost, P. Rech, “Selective Hardening for Neural Networks in FPGAs”, at IEEE Transactions on Nuclear Science, 2019.
7. F. Santos, C. Lunardi, D. Oliveira, F. Libano, P. Rech, “Reliability Evaluation of Mixed-Precision Architectures”, at International Symposium on High-Performance Computer Architecture (IEEE), 2019.
8. F. Libano, B. Wilson, M. Wirthlin, J. Brunhaver, “Understanding the Impact of Binary Quantization on the Reliability of Neural Networks on FPGAs” presented at Radiation and its Effects on Components and Systems (IEEE), 2019.
9. F. Libano, B. Wilson, M. Wirthlin, P. Rech, J. Brunhaver, “Understanding the Impact of Quantization, Accuracy, and Radiation on the Reliability of Convolutional Neural Networks on FPGAs”, at IEEE Transactions on Nuclear Science, 2020.
10. F. Libano, P. Rech, B. Neuman, J. Leavitt, M. Wirthlin, J. Brunhaver, “Evaluating the Impact of Reducing Data Precision on the Reliability of Neural Networks on FPGAs ”, presented at Nuclear and Space Radiation Effects Conference (IEEE), 2020.
11. F. Libano, P. Rech, J. Brunhaver, “On the Reliability of Xilinx’s Deep Processing Unit and Systolic Arrays for Matrix Multiplication”, presented at Radiation and its Effects on Components and Systems (IEEE), 2020.
12. F. Libano, P. Rech, B. Neuman, J. Leavitt, M. Wirthlin, J. Brunhaver, “How Reduced Data Precision and Degree of Parallelism Impact the Reliability of Convolutional Neural Networks on FPGAs”, at IEEE Transactions on Nuclear Science, 2021.
13. F. Libano, P. Rech, J. Brunhaver, “Efficient Error Detection for Matrix Multiplication with Systolic Arrays on FPGAs”, under review at IEEE Transactions on Computers, 2021.

## Work Experience

### Intel | Reliability Engineer

2022-Nowadays

I am currently working at Intel's Advanced Reliability Characterization (ARC) group. My NDA limits the extent to which I can share information regarding my day-to-day activities and the company's overarching goals. However, I can state that my line of work involves extensive architectural knowledge for tracking fault propagation and conceiving mitigation strategies. My work is also very experimental in nature, as I am in charge of designing/running experiments as well as parsing/interpreting experimental data. For experiment design, I often write sets of scripts that interact with real-world equipment (i.e. motors, sensors, lasers) and collect data. Afterwards, such data is parsed and often visualized using data-science libraries (i.e. pandas, scikit, plotly).

### ASU | PhD Student & Research Assistant

2018-2021

Worked on novel hardening techniques as well as on dedicated RHDB accelerator architectures for matrix multiplication and neural networks on FPGAs/ASICs. Particularly, thorough experimentation and a comprehensive analysis of multi-level fault models, my research aims to develop error detection/correction methods with minimum added costs (compared to traditional modular redundancy). Moreover, I have been involved in designing setups for beam experiments with FPGAs and with a fully custom chip, which integrates multiple different compute units and test structures. Additionally, I am currently involved in a project that focuses on efficient HW\SW co-design, in which accurate kernel identification enables optimal hardware acceleration decisions, for increased performance.

### Los Alamos National Laboratory | Intern/Student @ 2019 Radiation Effects Summer School

Summer 2019

The experience at LANL was very unique, in the sense that I was able to do a lot of hands-on work with different types of radiation experiments (neutron generators for evaluating SEEs, gamma cells for evaluating TID effects, and laser sources for evaluating architectural vulnerabilities). At the same time, I have learned a lot from the theoretical stand point, as I have attended more than 50 hours of classes and lectures, from world-renowned researchers on a number of very relevant topics, ranging from particle physics, radiation testing methodologies, high-performance computing, space applications and beyond. Particularly, I have evaluated the impact of reducing the floating-point precision on neural networks in FPGAs, both in terms of accuracy and radiation sensitivity.

**UFRGS | M.S. Student sponsored by CAPES-MEC (Coordination of Improvement of Graduate Level Personnel - Ministry of Education - Brazil)**

2017 - 2018

Researcher with specialization in reliability and fault tolerance of FPGA and SoC components under harsh conditions, such as radiation-rich environments. The main focus of my research has been to evaluate the behavior of Artificial Neural Networks, used in safety-critical applications such as autonomous driving and space missions, most often for real-time image processing. I've also been working on proposing out-of-the-box selective hardening techniques, based on AVF, in order to improve the overall system reliability with very low overhead in terms of resources and power. The results have been presented in relevant conferences as well as published in IEEE journals.

**UFRGS | Intern in the Scientific Initiation Program of CNPq (National Council of Scientific and Technological Development - Brazil)**

2015 - 2017

As an undergraduate student, the focus of my research was to evaluate the reliability of simple Artificial Neural Networks, used for Pattern Recognition and Linear Regression, implemented in FPGA. The obtained results were presented in IEEE conferences.

**Queen Mob | iOS Developer**

03/2012 - 10/2012

Worked on new apps, such as "Turismo Bento" and other mobile solutions for regional clients of southern Brazil.

**Independent | Apple iOS Licensed Developer**

2010 - 2013

Developer of personal projects, including an app called "iTaxi" with a high level of acceptance by the users, coverage by national magazines, newspapers and tv shows.

## Open Source Projects

**Libano's Systolic Array Generator**

https://github.com/lllibano/SystolicArray | https://github.com/lllibano/LABFT

Inspired by state-of-the-art neural network accelerators like Google's DPU and Xilinx's TPU, I proposed a high-performance integer matrix multiplication accelerator for Xilinx FPGAs. Through clever bit manipulation and time-multiplexed DSPs, my architecture achieves a parallelism factor of 4, outperforming comparable prior work, while utilizing less resources and being more energy efficient. In addition, I wrote a parametric Python script that allows anyone to generate custom-sized arrays that fit their needs and constraints, in a matter of minutes.

## References

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