Fabiano Pereira Libano

Bio

Birthday: March, 8, 1996 | Born in: Madrid, Spain | Nationality: Brazilian
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Education

Doctor's Degree | Computer Engineering
Arizona State University, ASU, Tempe, United States.
Ongoing

Master's Degree | Computer Engineering
Universidade Federal do Rio Grande do Sul, UFRGS, Porto Alegre, Brazil
2017 - 2018

Bachelor's Degree | Computer Engineering
Universidade Federal do Rio Grande do Sul, UFRGS, Porto Alegre, Brazil
2013 - 2017

High Education
Colégio Anchieta, ANCHIETA, Porto Alegre, Brazil
2011 - 2012

Secondary Education
Escola de Educação Básica Rainha do Brasil, EEB RB, Brazil
2008 - 2010

Primary Education
Colégio Marista Champagnat, CHAMPAGNAT, Brazil
2002 - 2007

Languages

Portuguese

Understanding, Speaking, Writing and Reading: Mother Language.

English

Understanding: Fluent, Speaking: Fluent, Writing: Fluent, Reading: Fluent

Spanish

Understanding: Functional, Speaking: Basic, Writing: Basic, Reading: Functional

Main Fields of Expertise/Interest

1. Radiation Reliability and Fault Tolerance of FPGAs/SoCs
2. Hardware Description Languages (VHDL) and Digital Systems Design
3. Artificial Intelligence / Machine Learning
4. Software Engineering / Mobile Applications
5. Bioinformatics

Publications

1. F. Libano *et al*, “Reliability Analysis of Feed-Forward Artificial Neural Networks in System on Chips”, presented at Silicon Errors in Logic-Systems Effects (IEEE), 2017.
2. F. Libano *et al*, “Evaluation of Feed-Forward Artificial Neural Networks Reliability in FPGAs”, presented at Nuclear and Space Radiation Effects Conference (IEEE), 2017.
3. F. Libano *et al*, “On the Reliability of Feed-Forward Artificial Neural Networks in FPGAs”, at IEEE Transactions on Nuclear Science, 2017.
4. F. Libano *et al*, “Selective Hardening for Neural Networks in FPGAs”, at Nuclear and Space Radiation Effects Conference (IEEE), 2018.
5. F. Benevenuti, F. Libano *et al*, “Comparative Analysis of Inference Errors in a Neural Network Implemented in SRAM-Based FPGA Induced by Neutron Irradiation and Fault Injection Methods”, presented at Symposium on Integrated Circuits and Systems Design (IEEE), 2018.
6. F. Libano *et al*, “Selective Hardening for Neural Networks in FPGAs”, at IEEE Transactions on Nuclear Science, 2018.
7. F. Santos, F. Libano *et al*, “Reliability Evaluation of Mixed-Precision Architectures”, at International Symposium on High-Performance Computer Architecture (IEEE), 2019.

Work Experience

ASU | PhD Student & Research Assistant

Ongoing

I am currently working on the development of a full custom chip, which integrates multiple different dedicated hardware accelerators, executing simultaneously. This is a large scale project, involving a lot of researchers, but I am particularly assigned to tasks like RTL generation and communication channels/protocols. In addition to that, I am also working on adding features to an existing rad-hard processor's Verilog, as well as verifying its functionality using different hierarchical granularities.

UFRGS | M.S. Student sponsored by CAPES-MEC (Coordination of Improvement of Graduate Level Personnel - Ministry of Education - Brazil)

2017 - 2018

Researcher with specialization in reliability and fault tolerance of FPGA and SoC components under harsh conditions, such as radiation-rich environments. The main focus of my research has been to evaluate the behavior of Artificial Neural Networks, used in safety-critical applications such as autonomous driving and space missions, most often for real-time image processing. I've also been working on proposing out-of-the-box selective hardening techniques in order to improve the overall system reliability with very low overhead in terms of resources and power. The obtained results have been presented in international conferences as well as published in IEEE journals.

UFRGS | Intern in the Scientific Initiation Program of CNPq (National Council of Scientific and Technological Development - Brazil)

2015 - 2017

As an undergraduate student, the focus of my research was to evaluate the reliability of simple Artificial Neural Networks, used for Pattern Recognition and Linear Regression, implemented in FPGA. The obtained results were presented in IEEE conferences.

Queen Mob | iOS Developer

03/2012 - 10/2012

Worked on new apps, such as "Turismo Bento" and other mobile solutions for regional clients of southern Brazil.

Apple | Licensed Developer

2010 - 2013

Developer of personal projects, including an application called "iTaxi" with a high level of acceptance by the users, and coverage by national magazines, local newspapers and television programs.

References

John Brunhaver
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ASU

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UFRGS | Los Alamos National Laboratory

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Université de Montpellier