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ES232(30000counts)

DMM Analog front end/Peak

Digital multi-meter

Features

- 30000 counts dual-slope SADC (**3 cnvs/s.**)
- Input signal full scale: 340mV (Max. 3399x count)
- Built-in 300 counts fast speed (x10) FADC
- Fast ADC conversion rate: 30 times/s
- 100L LQFP package
- 3V DC regulated power supply
- Support digital multi-meter function

  *Voltage measurement (AC/DC)

  *Current measurement (AC/DC)

  *Support AC+DC RMS mode

  *Dual mode for frequency with voltage or current

  ***Resistance measurement (300.00Ω – 300.00MΩ)**

  ***Capacitance measurement (30.000nF – 300.00mF)**
  (Taiwan patent no.: 323347, 453443)

  (China patent no.: 200710106702.8)

  *Diode or continuity mode measurement

  ***Frequency counter with duty cycle display:**

  30.000Hz – 300.00MHz

  5.0% – 95.0%
- **ADP mode with two terminals** (AC or DC mode is available)
- 3dB BW selectable for low pass filter at AC mode
  (**Taiwan patent no.: 362409**)
  (**China patent no.: 200920153001.X**)
- Band-gap reference voltage output
- Peak-hold measurement
  (**Taiwan patent no.:476418**)
- 3-wire serial bus for MPU I/O port
- MPU I/O power level selectable by external pins
- On-chip buzzer driver and frequency selectable by MPU command
- High-crest-factor signal detection
  (**Taiwan patent no.: 234661**)
- Multi-level battery voltage detection
- Support sleep mode by external chip select pin

Application

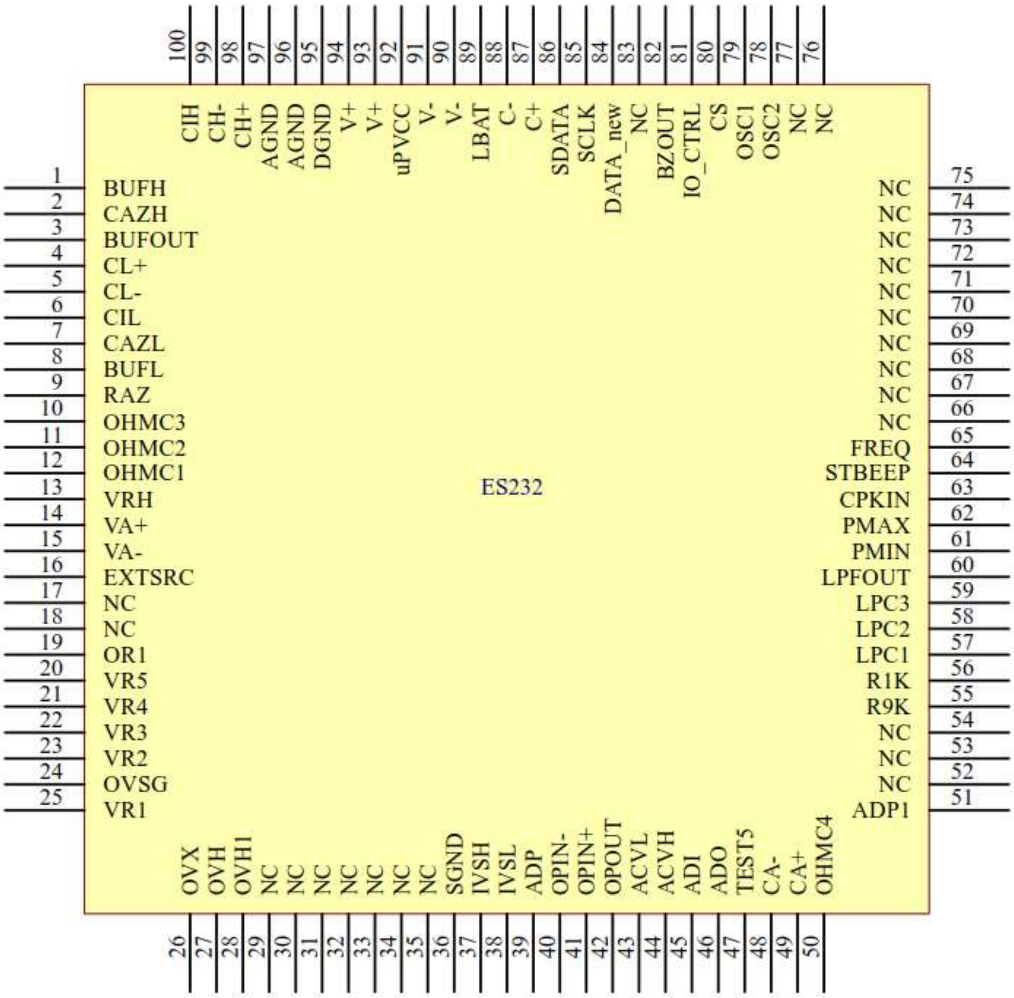
Clamp-on meter

Digital multi-meter

Description

ES232 is an analog frond end chip of DMM built-in 30000(SADC)/300(FADC) counts dual ADCs. The SADC is operated at slower speed for higher resolution. The FADC is operated at higher speed for lower resolution. ES232 provides voltage & current (AC/DC) measurement, resistance measurement, capacitance measurement, diode/continuity measurement, frequency measurement, duty cycle measurement and voltage peak-hold function. The ES232 also supports multi-level battery detection, low-pass-filter feature for AC mode and dual mode measurement for V+F & A+F. A 3-wire serial bus for MPU I/O port will be used easily for firmware design. Flexible function design is supported for different kinds of DMM or Clamp-on meter application.

Pin Assignment



Pin Description

Pin No	Symbol	Type	Description
1	BUFH	O	High-speed buffer output pin.
2	CAZH	O	High-speed auto-zero capacitor connection.
3	BUFOUT	O	Filter capacitor connection for AC+DC RMS mode.
4	CL+	IO	Positive connection for reference capacitor of high-resolution A/D.
5	CL-	IO	Negative connection for reference capacitor of high- resolution A/D.
6	CIL	O	High-resolution integrator output. Connect to integral capacitor.
7	CAZL	O	High-resolution auto-zero capacitor connection.
8	BUFL	O	High-resolution Buffer output pin.
9	RAZ	O	Buffer output pin in AZ and ZI phase.
10	OHMC3	O	Filter capacitor connection for resistance mode.
11	OHMC2	O	Filter capacitor connection for resistance mode.
12	OHMC1	O	Filter capacitor connection for resistance mode.
13	VRH	O	Output of band-gap voltage reference. Typically –1.23V
14	VA+	I	De-integrating voltage positive input. The input should be higher than VA-.
15	VA-	I	De-integrating voltage negative input. The input should be lower than VA+.
16	EXTSRC	I	External source input available for Res/Diode/ADP mode
17	NC	-	Not connected
18	NC	-	Not connected
19	OR1	O	Reference resistor connection for 300.00Ω range
20	VR5	O	Voltage measurement ÷10000 attenuator(1000.0V)
21	VR4	O	Voltage measurement ÷1000 attenuator(300.00V)
22	VR3	O	Voltage measurement ÷100 attenuator(30.000V)
23	VR2	O	Voltage measurement ÷10 attenuator(3.0000V)
24	OVSG	O	Sense low voltage for resistance/voltage measurement
25	VR1	I	Measurement Input. Connect to a precise 10MΩ resistor.
26	OVX	I	Sense input for resistance/capacitance measurement
27	OVH	O	Output connection for resistance measurement
28	OVH1	O	Output connection1 for resistance measurement (optional)
29	NC	-	Not connected
30	NC	-	Not connected
31	NC	-	Not connected
32	NC	-	Not connected
33	NC	-	Not connected
34	NC	-	Not connected
35	NC	-	Not connected
36	SGND	G	Signal Ground.
37	IVSH	I	Current measurement input for 3000.0µA, 300.00mA and 30.000A modes.
38	IVSL	I	Current measurement input for 300.00µA, 30.000mA.
39	ADP	I	Measurement input in ADP mode.
40	OPIN-	I	Independent operational amplifier negative input
41	OPIN+	I	Independent operational amplifier positive input
42	OPOUT	O	Independent operational amplifier output
43	ACVL	O	DC signal low input in ACV/ACA mode. Connect to negative output of external AC to DC converter.
44	ACVH	O	DC signal high input in ACV/ACA mode. Connect to positive output of external AC to DC converter.
45	ADI	I	Negative input of internal AC-to-DC OPAMP.
46	ADO	O	Output of internal AC-to-DC OPAMP.
47	TEST5	O	Buffer output of OVSG
48	CA-	IO	Negative auto-zero capacitor connection for capacitor measurement

49	CA+	IO	Positive auto-zero capacitor connection for capacitor measurement
50	OHMC4	O	Filter capacitor connection for resistance mode.
51	ADP1	I	Measurement input in ADP mode.
52	NC	-	Not connected
53	NC	-	Not connected
54	NC	-	Not connected
55	R9K	O	Connect to a precise 9KΩ resister for capacitor measurement.
56	R1K	O	Connect to a precise 1KΩ resister for capacitor measurement.
57	LPC1	O	Capacitor C1 connection for internal low-pass filter
58	LPC2	O	Capacitor C2 connection for internal low-pass filter
59	LPC3	O	Capacitor C3 connection for internal low-pass filter
60	LPFOUT	O	Capacitor C1 connection for internal low-pass filter
61	PMIN	O	Minimum peak hold output
62	PMAX	O	Maximum peak hold output.
63	CPKIN	I	Bypass capacitor for peak mode
64	STBEEP	O	Fast low-impedance sensed output for CONT./Diode mode Build-in a internal comparator for OVX pin.
65	FREQ	I	Frequency counter input, offset V-/2 internally by the chip.
66-77	NC	-	Not connected
78	OSC2	O	Crystal oscillator output connection
79	OSC1	I	Crystal oscillator input connection
80	CS	I	Set to high to enable ES232. Set to low to enter sleep mode
81	IO_CTRL	I	MPU I/O level LOW setting. Connect to DGND or V-.
82	BZOUT	I	Buzzer frequency output. Normal low state.
83	NC	-	Not connected
84	DATA_NEW	O	New ADC data ready
85	SCLK	I	Serial clock input
86	SDATA	IO	Serial data input/output
87	C+	O	Positive capacitor connection for on-chip DC-DC converter.
88	C-	O	Negative capacitor connection for on-chip DC-DC converter.
89	LBAT	I	Low battery configuration input.
90	V-	P	Negative supply voltage.
91	V-	P	Negative supply voltage.
92	uPVCC	P	MCU I/O power level connection.
93	V+	O	Output of on-chip DC-DC converter.
94	V+	O	Output of on-chip DC-DC converter.
95	DGND	G	Digital ground.
96	AGND	G	Analog ground.
97	AGND	G	Analog ground.
98	CH+	IO	Positive connection for reference capacitor of high-speed A/D.
99	CH-	IO	Negative connection for reference capacitor of high-speed A/D.
100	CIH	O	High-speed integrator output. Connect to integral capacitor.

Absolute Maximum Ratings

Characteristic	Rating
Supply Voltage (V- to AGND)	-4V
Analog Input Voltage & EXTSRC pin	V- -0.6 to V+ +0.6
V+	V+ ≥ (AGND/DGND+0.5V)
AGND/DGND	AGND/DGND ≥ (V- -0.5V)
Digital Input (IO_CTRL=V-)	V- -0.6 to uPVCC+0.6
Power Dissipation. Flat Package	500mW
Operating Temperature	-20℃ to 70℃
Storage Temperature	-55℃ to 125℃

Electrical Characteristics

TA=25℃, V- = -3.0V

Parameter	Symbol	Test Condition	Min.	Typ.	Max	Units
Power supply	V-		-2.8	-3.0	-3.2	V
Operating supply current In DCV mode	I_{DD}	Normal operation	—	2.8	3.2	mA
	I_{SS}	In sleep mode	—	1	3	μA
SADC[2] Voltage roll-over error		10MΩ input resistor	—	—	±0.02	%F.S[1]
FADC[3] Voltage roll-over error		10MΩ input resistor	—	—	±0.5	%F.S[1]
SADC[2] voltage nonlinearity	NLV1	Best case straight line	—	—	±0.02	%F.S[1]
FADC[3] voltage nonlinearity	NLV2	Best case straight line	—	—	±1.0	%F.S[1]
Voltage full scale range of SADC[2]		VA+-VA- = 200mV	—	300	339	mV
Voltage full scale range of FADC[3]		VA+-VA- = 200mV	—	300	—	mV
Input Leakage for VR1 input			-10	1	10	pA
Zero input reading		10MΩ input resistor	-000	000	+000	Count
Band-gap reference voltage	V_{RH}	100KΩ resistor between VRH and AGND	-1.30	-1.22	-1.14	V
Open circuit voltage for 300Ω range measurement			—	V-	—	V
Open circuit voltage for other Ω measurement			—	V_{RH}	—	V
Open circuit voltage for 30.00nS range measurement			—	-0.68	—	V
Internal pull-high to 0V current		Between V- pin and CS	—	1.2	—	μA
AC frequency response at 3.000V range		±1%	—	40-400	—	HZ
		±5%	—	400-2000	—	
OP unity gain bandwidth	GB	C_L=10pF R_L=10MΩ	—	200	—	kHz
OP slew rate at unity gain	SR		—	3.5	—	V/us
OP input offset voltage	V_{IO}		—	0.1	—	mV
OP input bias current	I_B		—	10	—	pA
OP input common mode voltage range	V_{ICR}		—	± 2	—	V

3dB frequency for LPF[4] active	f_{3dB}	3dB=Full (ADP)	100	—	—	kHz
		3dB=10k (ADP)	—	10	—	kHz
		3dB=1k (ADP)	—	1	—	kHz
Multi-level low battery detector	V_{t1}	LBAT vs. V-	—	2.15	—	V
	V_{t2}		—	2.03	—	V
	V_{t3}		—	1.83	—	V
Peak-hold mode pulse width		ACIN =40 ~ 400Hz	100[6]	1000	—	us
STBEEP comparator in Diode mode		OVX to SGND	—	+9	—	mV
STBEEP comparator in Cont. mode		OVX to SGND	—	-7	—	mV
HCF detection voltage		VR2-VR5	—	1100	—	mV
Frequency input sensitivity (*FREQ*)	Fin	Square wave with Duty cycle 40-60%	500	—	—	mVp
Frequency input sensitivity (*FREQ*)	Fin	Sine wave	400	—	—	mVrms
Reference voltage temperature coefficient	TC_{RF}	100KΩ resister Between VRH -20℃<TA<70℃	—	—	50	ppm/℃
Capacitance measurement Accuracy		30nF – 300mF	-2.5	—	2.5	%F.S
			-30	—	30	counts

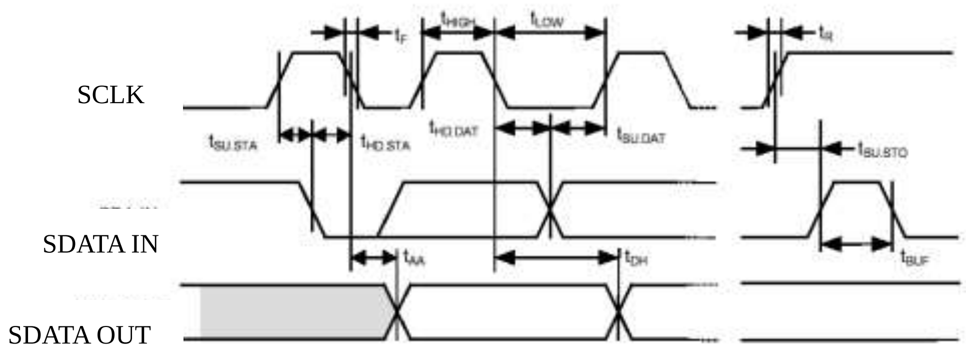
Note:

1. Full Scale (30000 counts for SADC and 300 counts for FADC)
2. SADC = High resolution ADC (slow speed)
3. FADC = High speed ADC (lower resolution)
4. ES232 built-in 3rd order low pass filter available for AC mode
5. Gain calibration is necessary for higher accuracy
6. Available for ADP input terminal.

AC electrical characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit
SCLK clock frequency	f_{SCLK}	-	-	100	kHz
SCLK clock time “L”	t_{LOW}	4.7	-	-	us
SLCK clock time “H”	t_{HIGH}	4.0	-	-	
SDATA output delay time	t_{AA}	0.1	-	3.5	
SDATA output hold time	t_{DH}	100	-	-	ns
Start condition setup time	$t_{SU.STA}$	4.7	-	-	us
Start condition hold time	$t_{HD.STA}$	4.0	-	-	
Data input setup time	$t_{SU.DAT}$	200	-	-	ns
Data input hold time	$t_{HD.DAT}$	0	-	-	
Stop condition setup time	$t_{SU.STO}$	4.7	-	-	us
SCLK/SDATA rising time	t_R	-	-	1.0	
SCLK/SDATA falling time	t_F	-	-	0.3	
Bus release time	t_{BUF}	4.7	-	-	

MPU I/O timing diagram



Function Description

1. MPU serial I/O function overview

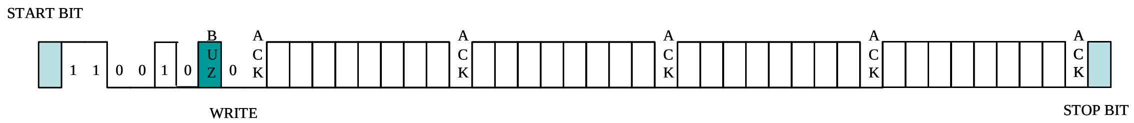
1.1 Introduction

ES232 configures a 3-wire serial I/O interface to external microprocessor unit (MPU). The SDATA pin is bi-directional and SCLK & DATA_NEW are unilateral. The SDATA pin is configured by open-drain circuit design. The DATA_NEW is used to check the data buffer of ADC ready or not. When the ADC conversion cycle is finished, the DATA_NEW pin will be pulled high until MPU send a valid read command to ES232. After the first ID byte is confirmed, the DATA_NEW will be driven to low until the next ADC conversion finished again.

The data communication protocol is shown below. The write protocol is configured by an ID byte with four command bytes. The read protocol is configured by an ID byte with ten data bytes.

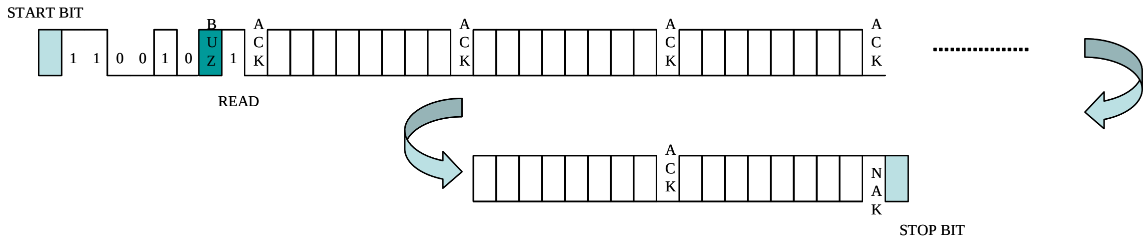
Write command:

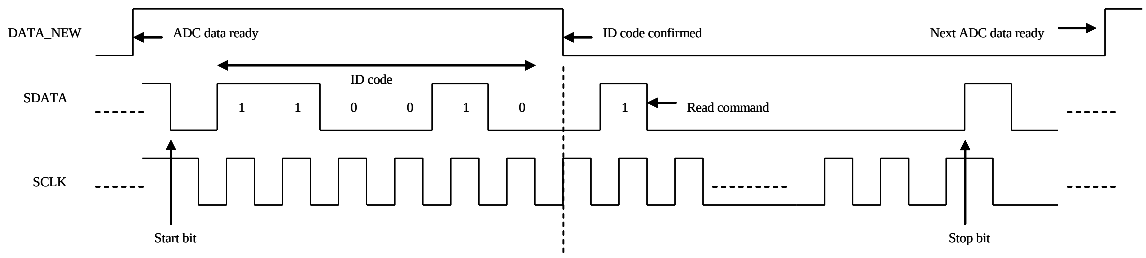
ID byte, Write control byte1, Write control byte2, Write control byte3, Write control byte4



Read command:

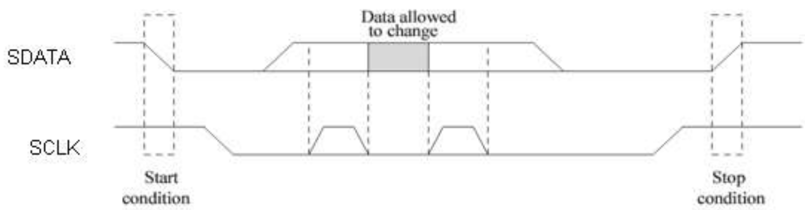
ID byte, Read data byte1, Read data byte2 ~ Read data byte9, Read data byte10





The ID byte of ES232 is header of "110010" followed by a buzzer on/off control bit and R/W bit. The start/stop bit definition is shown on the diagram below.

Start and Stop bit



1.2 Read/Write command description

The write command includes one ID byte with four command bytes. If the valid write ID code is received by ES232 at any time, the write command operation will be enabled.
The next table shows the content of write command:

Byte	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
ID	1	1	0	0	1	0	**BUZ**	R/W=0
W1	**SHBP/DCSEL**	**F3**	**F2**	**F1**	**F0**	**Q2**	**Q1**	**Q0**
W2	**B0**	**B1**	**B2**	**0**	**0**	**FQ2**	**FQ1**	**FQ0**
W3	**AC**	**BUFCAL**	**BUF_ACDC**	**EXT**	**FD**	**LPF1**	**LPF0**	**RP**
W4	**PEAK**	**PCAL**	**0**	**0**	**0**	**OP0**	**OP1**	**EXT_ADP**

Auxiliary low-resistance detection control bit for Continuity and Diode modes: **SHBP**

AC+DC mode selection control bit for AC+DC mode: **DCSEL**

Measurement function control bit: **F3/F2/F1/F0**

Range control bit for V/A/R/C modes: **Q2/Q1/Q0**

Range control bit for Freq mode: **FQ2/FQ1/FQ0**

Buzzer frequency selection: **B2/B1/B0**

Buzzer driver ON/OFF control bit: **BUZ**

AC mode control enable bit: **AC**

PEAK/Calibration mode enable bit: **PEAK/PCAL**

3dB BW for low-pass-filter selection: **LPF1/LPF0**

External source for Diode mode control bit: **EXT**

OP configuration control bit: **OP1/OP0**

Frequency mode input resistance control bit or output resistance control bit for AC+DC mode: **RP**

Buffer control bits for AC+DC mode: **BUFCAL/BUF_ACDC**

ADP mode control bit: **EXT_ADP**

F+ duty mode at 30kHz range auxiliary control bit: **FD**

The read command includes one ID byte with ten data bytes. When DATA_NEW is ready[1], MPU could send the read data command to get the result of ADC conversion

(D0/D1/D2/D3)[2] or status flag from ES232.

The next table shows the content of read command.

Byte	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
ID	1	1	0	0	1	0	**BUZ**	R/W=1
R1	**ASIGN**	**BSIGN**	**PMAX**	**PMIN**	**BTS0**	**BTS1**	**STA0**	**ALARM**
R2	**HF**	**LF**	**LDUTY**	**STA1**	**F_FIN**	**D0:0**	**D0:1**	**D0:2**
R3	**D0:3**	**D0:4**	**D0:5**	**D0:6**	**D0:7**	**D0:8**	**D0:9**	**D0:10**
R4	**D0:11**	**D0:12**	**D0:13**	**D0:14**	**D0:15**	**D0:16**	**D0:17**	**D0:18**
R5	**D1:0**	**D1:1**	**D1:2**	**D1:3**	**D1:4**	**D1:5**	**D1:6**	**D1:7**
R6	**D1:8**	**D1:9**	**D2:0**	**D2:1**	**D2:2**	**D2:3**	**D2:4**	**D2:5**
R7	**D2:6**	**D2:7**	**D2:8**	**D2:9**	**D2:10**	**D2:11**	**D2:12**	**D2:13**
R8	**D2:14**	**D2:15**	**D2:16**	**D2:17**	**D2:18**	**D3:0**	**D3:1**	**D3:2**
R9	**D3:3**	**D3:4**	**D3:5**	**D3:6**	**D3:7**	**D3:8**	**D3:9**	**D3:10**
R10	**D3:11**	**D3:12**	**D3:13**	**D3:14**	**D3:15**	**D3:16**	**D3:17**	**D3:18**

[1]Note: DATA_NEW will be active with D1 data updated when one fast ADC (FADC) conversion finished. If MCU access slow ADC output only, ten FADC conversion cycle delay is necessary. DATA_NEW for frequency or capacitance mode will be active when D0 or D3 data ready.

[2]Note: D0/D1/D2/D3 all are binary code format. D0 is SADC output and D1 is FADC output. The maximum data is 339xx counts for SADC and 33x counts for FADC. The maximum counts for PEAK mode is ~54000, so D0 bit 17-18 could be ignored..

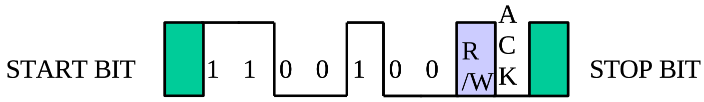
The ADC data output for measurement mode: **F3/F2/F1/F0**

F3	F2	F1	F0	Measurement mode	Read data bytes
0	0	0	0	V mode	D0(0:18), D1(0:9)
0	0	0	1	ACV + Hz(%) mode	D0(0:18), D1(0:9), D2(0:18), D3(0:18)
0	0	1	0	A mode	D0(0:18), D1(0:9)
0	0	1	1	ACA + Hz(%) mode	D0(0:18), D1(0:9), D2(0:18), D3(0:18)
0	1	0	0	Resistance mode	D0(0:18), D1(0:9)
0	1	0	1	Continuity mode	D0(0:18), D1(0:9)
0	1	1	0	Diode mode	D0(0:18), D1(0:9)
0	1	1	1	F + duty mode	D0(0:18), D2(0:18), D3(0:18)
1	0	0	0	Capacitance Mode	D0(0:18)
1	0	0	1	ADP mode	D0(0:18), D1(0:9)
1	0	1	0	ADP + Hz(%) mode	D0(0:18), D1(0:9), D2(0:18), D3(0:18)

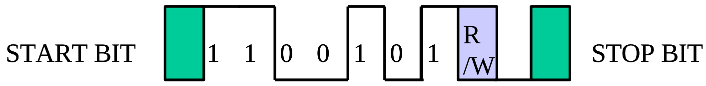
Buzzer frequency selection: **B2/B1/B0**

B2	B1	B0	Buzzer frequency
0	0	0	1.00kHz
0	0	1	1.33kHz
0	1	0	2.00kHz
0	1	1	2.22kHz
1	0	0	2.67kHz
1	0	1	3.08kHz
1	1	0	3.33kHz
1	1	1	4.00kHz

Set B2-B0 properly to get the target frequency. Use **BUZ** control bit to enable/disable the *BUZOUT* (pin82) driver output. If MPU control BUZ only, it is available to set ID byte with ending of stop bit.



Buzzer OFF



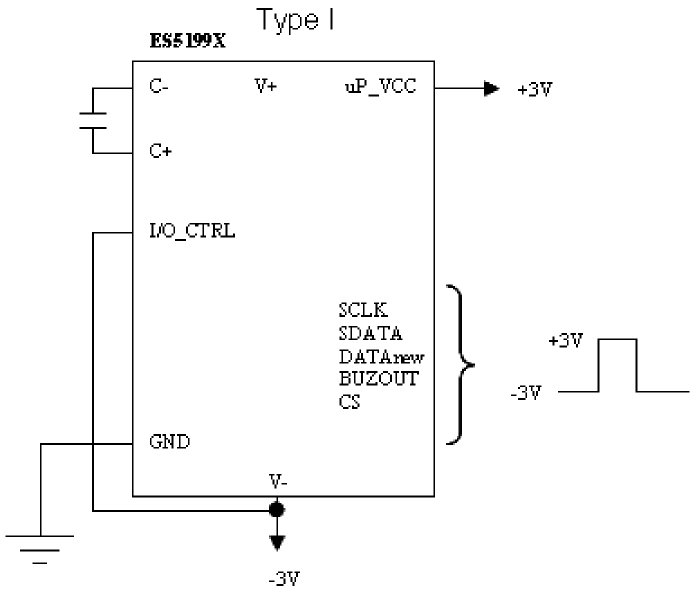
Buzzer ON

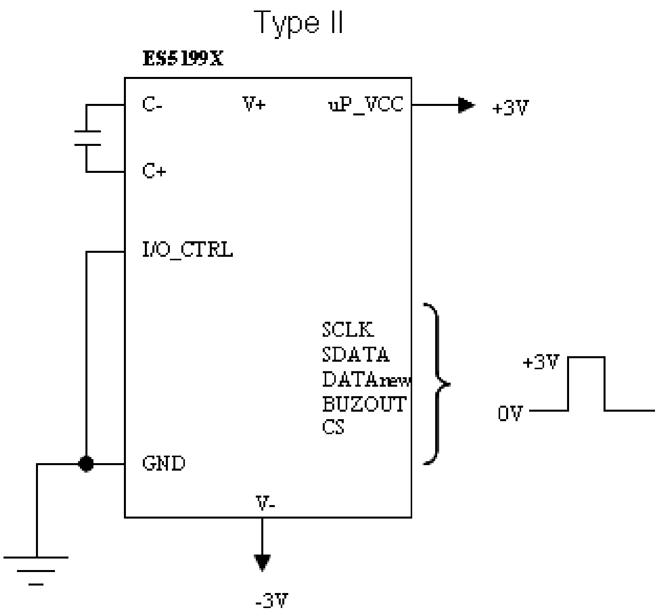
Measurement mode	ASIGN	BSIGN	PMAX	PMIN	BTS0	BTS1	ALARM
V mode	●	●	●	●	●	●	●
ACV + Hz mode			●	●	●	●	●
A mode	●	●	●	●	●	●	●
ACA + Hz mode			●	●	●	●	●
Res. mode					●	●	
Cont. mode					●	●	
Diode mode	●	●			●	●	
F + duty mode					●	●	
Cap. Mode					●	●	●
ADP mode	●	●	●	●	●	●	
ADP + Hz mode			●	●	●	●	
Measurement mode	HF	LF	LDUTY	STA0	STA1	F_FIN	
V mode							
V + Hz mode	●	●		●	●	●	
A mode							
A + Hz mode	●	●		●	●	●	
Res. mode							
Cont. mode							
Diode mode							
F + duty mode	●	●	●	●	●	●	
Cap. Mode				●			
ADP mode							
ADP + Hz mode	●	●		●	●	●	

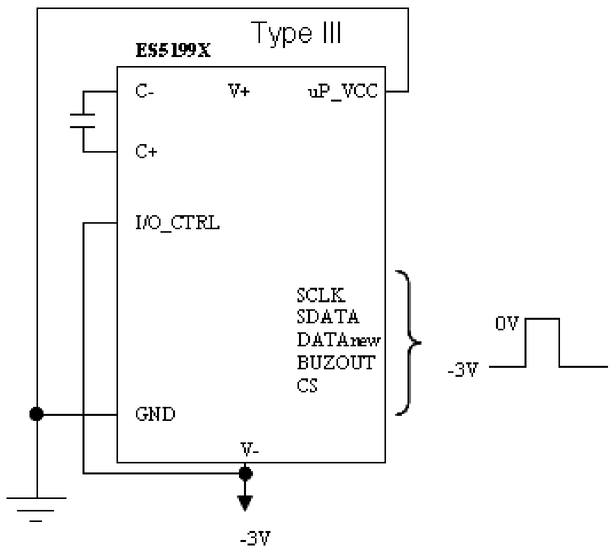
Description of status flags:
ASIGN: Sign bit of SADC output (-1 * D0 if ASIGN=1)
BSIGN: Sign bit of FADC output (-1 * D1 if BSIGN=1)
PMAX: Indicates D0 output is the voltage of the peak maximum capacitor (pin62)
PMIN: Indicates D0 output is the voltage of the peak minimum capacitor (pin61)
BTS0/BTS1: Multi-level battery voltage indication
ALARM: Large capacitor indication/High crest factor signal detection in ACV mode
HF: Higher frequency indication for Hz mode
LF: Lower frequency indication for Hz mode
LDUTY: Low duty indication for Hz + duty mode
STA0/STA1: divider indication for Hz mode
STA0: Status flag for capacitor discharging mode
F_FIN: Measurement cycle finished for Hz mode

1.3 Power & I/O level selection

The ES232 provide a flexible I/O level setting for different MPU system configuration. The uP_VCC should be connected to the same potential of external Vcc of MCU. The uP_VCC is allowed to be set between DGND ~ V+. The IO_CTRL pin selects the Vss level of MCU. If IO_CTRL is set to DGND, the Vss level of MCU is the same as DGND. If IO_CTRL is set to V-, the Vss level of MCU is the same as V-.







2. Operating Modes

2.1. Voltage Measurement

MPU send write command to select the voltage measurement function. The Hz mode measurement is available to be enabled with the ACV function (set **AC** bit to 1) simultaneously. The measured signal is applied to *VR1* terminal (pin25) through 10MΩ.

See the next table of function command:

F3	F2	F1	F0	AC	Measurement mode	Read data bytes
0	0	0	0	0	DCV mode	D0(0:18), D1(0:9)
0	0	0	0	1	ACV mode	D0(0:18), D1(0:9)
0	0	0	1	1	ACV + Hz(%) mode	D0(0:18), D1(0:9), D2(0:18), D3(0:18)

Note1: D0/D1/D2/D3 all are binary format. ASIGN/BSIGN are the sign bit of D0/D1, respectively.

Note2: See PEAK mode (section 2.10) also.

Range control for voltage mode (ACV/DCV)

Q2	Q1	Q0	Full Scale Range	Divider Ratio	Resister Connection
0	0	0	300.00mV	1	VR1 (10MΩ)
0	0	1	3.0000V	1/10	VR2 (1.111MΩ)
0	1	0	30.000V	1/100	VR3 (101kΩ)
0	1	1	300.00V	1/1000	VR4 (10.01kΩ)
1	0	0	1000.0V	1/10000	VR5 (1kΩ)

Frequency range control for ACV+Hz(%) mode

FQ2	FQ1	FQ0	Full Scale Range
0	0	0	30.00Hz
0	0	1	300.0Hz
0	1	0	3.000kHz
0	1	1	30.00kHz
Duty Cycle			20% ~ 80%

Note: See frequency/duty mode (section 2.9) also

ALARM bit at voltage mode is used for high crest factor (HCF) signal detection. If MPU check the ALARM status flag active when data and range are stable, it should consider the making the existing range up to avoid the signal clamping saturation caused by HCF signal. There is higher peak voltage with lower RMS value for HCF signal. So if the range is up according to the ALARM bit, MCU should set the lower under-limit counts temporarily to avoid the ranging unstable for this case.

2.2 Current measurement

MPU send write command to select the current measurement function. The Hz mode measurement is available to be enabled with the ACA function (set **AC** bit to 1) simultaneously. The measured signal is applied to *IVSL/IVSH* terminals (pin37-38).

See the next table of function command:

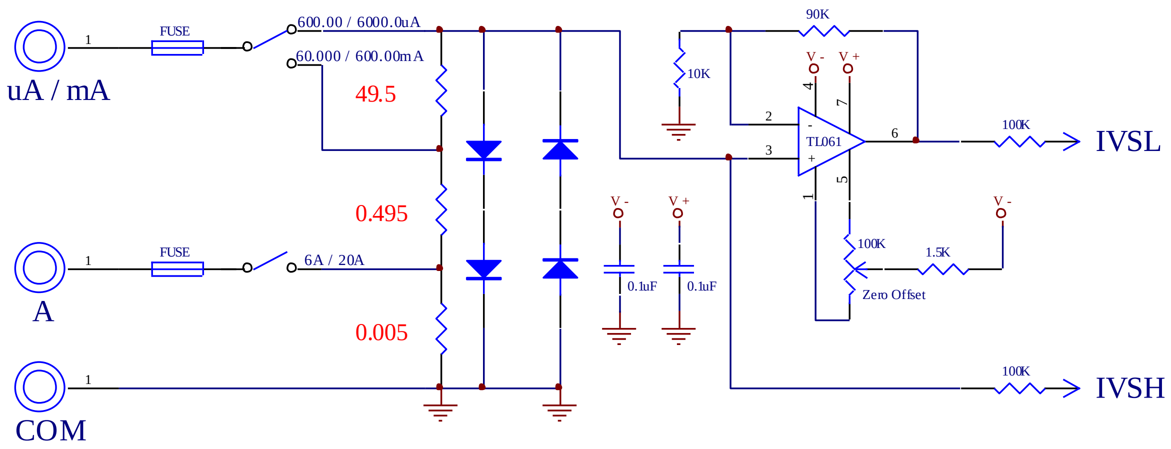
F3	F2	F1	F0	AC	Measurement mode	Read data bytes
0	0	1	0	0	DCA mode	D0(0:18), D1(0:9)
0	0	1	0	1	ACA mode	D0(0:18), D1(0:9)
0	0	1	1	1	ACA + Hz(%) mode	D0(0:18), D1(0:9), D2(0:18), D3(0:18)

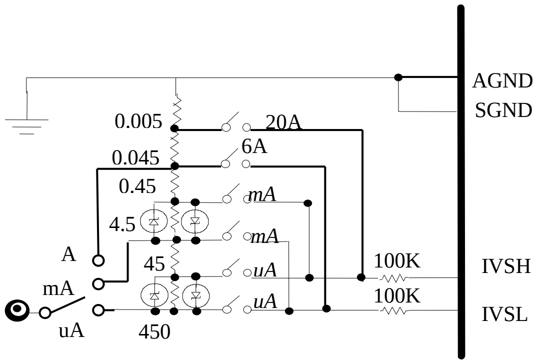
Note1: D0/D1/D3 all are binary format. ASIGN/BSIGN are the sign bit of D0/D1, respectively.
Note2: See PEAK mode (section 2.10) also.

Range control for current mode (ACA/DCA)

Q2	Q1	Q0	Full Scale Range	Input terminal
0	0	0	300mV→ 30000counts	IVSL
0	0	1	300mV→ 30000counts	IVSH

Current measurement mode configuration examples: (max. voltage drop 300mV)





(max voltage drop = ~ 1V)

Frequency range control for ACA+Hz(%) mode

FQ2	FQ1	FQ0	Full Scale Range
0	0	0	30.00Hz
0	0	1	300.0Hz
0	1	0	3.000kHz
0	1	1	30.00kHz
Duty Cycle			20% ~ 80%

Note: See frequency mode (section 2.9) also.

2.3 Low pass filter (LPF) mode for ACA/ACV mode

A 3rd order low pass filter with is built in ES232. The 3dB bandwidth of the low pass filter could be selectable by MPU. The LPF mode is active when the LPF control bit is set to be active. When PEAK mode is active, the LPF mode will be disabled temporarily until the PEAK mode is cancelled.

The LPF mode is allowed to be enabled in F + duty mode to reject high-frequency noise for sine wave input, but the 3dB will be fixed at 10kHz only.

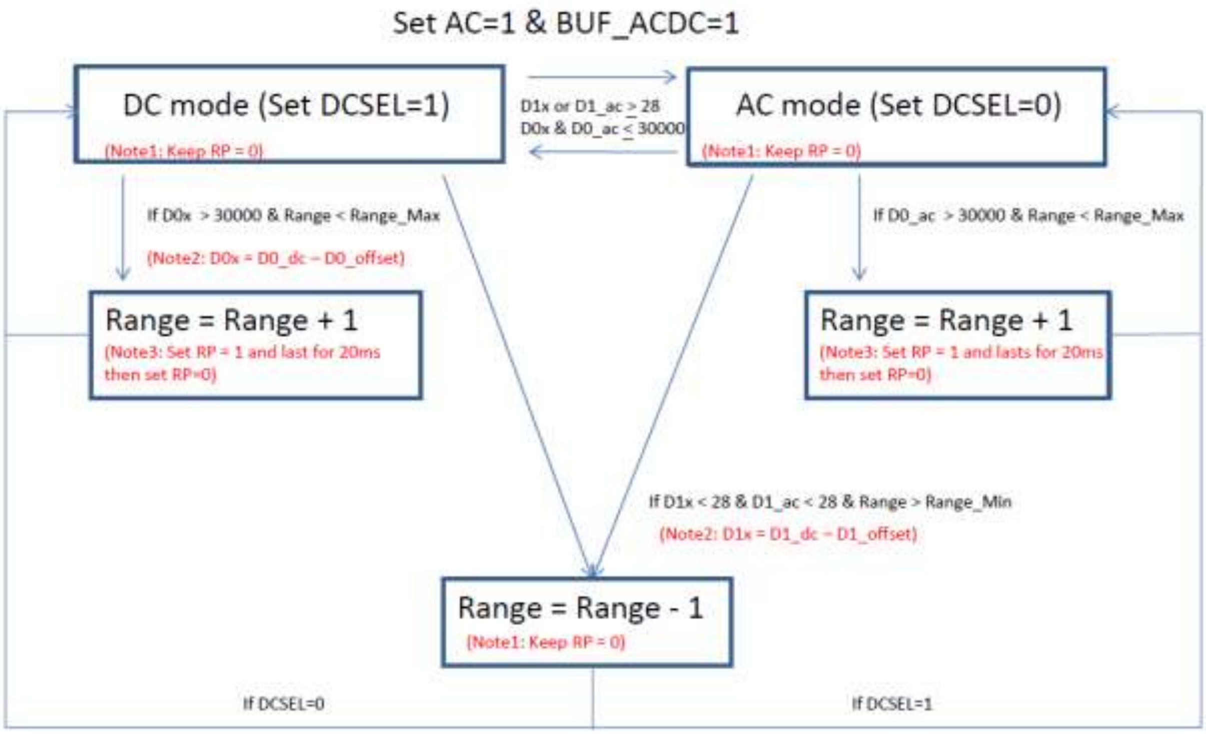
LPF1	LPF0	Low pass filter effect
0	0	Disable
0	1	3dB = 1kHz
1	0	3dB = 10kHz
1	1	3dB > 100kHz

2.4 AC+DC mode measurement

Set control bit **BUF_ACDC**=1 to enter AC+DC RMS measurement mode. The additional DC low-pass filter buffer will be enabled. The DC phase output of AC+DC mode will be sent to ADC when **DCSEL**=1. The AC phase output of AC+DC mode will be sent to ADC when **DCSEL**=0. The zero offset of DC low pass filter buffer should be calibrated by setting **BUFCAL**=1. The AC+DC RMS mode is supported as follow:

F3	F2	F1	F0	AC	BUF_ACDC	Measurement mode	Read data bytes
0	0	0	0	1	1	DCV+ACV mode	D0(0:18), D1(0:9)
0	0	1	0	1	1	DCA+ACA mode	D0(0:18), D1(0:9)
1	0	0	1	1	1	ADP DC+AC mode	D0(0:18)

The auto range scheme for AC+DC RMS mode is recommended as below:



- Note1: When data is not overflow (larger than 30000 counts), always keep to set **RP**=0.
- Note2: Set **BUF_CAL** = 1 to enter CAL mode to read D0_offset & D1_offset
- Note3: If Range is increasing, set **RP**=1 to reduce settling time for BUFOUT (D0_dc) when range is modified. If **RP**=1, wait 20ms then set **RP**=0 again.

The D0_dc & D0_ac is the original data from SADC of ES232. The D1_dc & D1_ac is the original data from FADC of ES232. D0x & D1x is real dc value deducted by dc buffer offset. The final AC+DC RMS result is square root of sum of $D0x^2$ and $D0\_ac^2$.

2.5 Resistance Measurement

MPU send write command to select the resistance measurement function.

F3	F2	F1	F0	Measurement mode	Read data bytes
0	1	0	0	Resistance mode	D0(0:18), D1(0:9)

Note1: D0/D1 both are binary format. ASIGN/BSIGN bits are ignored. When RP=1, the D1 data should be ignored.

Range control for resistance mode

Q2	Q1	Q0	Full Scale Range	Relative Resistor	Equivalent value
0	0	0	300.00Ω	OR1	[1]100Ω
0	0	1	3.0000KΩ	VR5	1KΩ
0	1	0	30.000KΩ	VR4 || VR1	10KΩ
0	1	1	300.00KΩ	VR3 || VR1	100KΩ
1	0	0	3.0000MΩ	VR2 || VR1	1MΩ
1	0	1	30.000MΩ	VR1	10MΩ
1	1	0	300.00MΩ	VR1	10MΩ

[1]Note: OR1 resistor is 200Ω .

2.6 Capacitance Measurement

MPU send write command to select the capacitance measurement function.

F3	F2	F1	F0	Measurement mode	Read data bytes
1	0	0	0	Capacitance mode	D0(0:18)

Note1: D0 is binary format. ASIGN bit is ignored.

Range control for capacitance mode

Q2	Q1	Q0	Full Scale Range	Relative Resistor	Measurement Period
0	0	0	30.000nF*	-	0.3 sec
0	0	1	300.00nF*	OVX pin VR	0.75 sec
0	1	0	3.0000uF*	-	0.75 sec
0	1	1	30.000uF*	R9K / R1K	2.4 sec max.
1	0	0	300.00uF*	R9K / R1K	3.0 sec max.
1	0	1	3.0000mF*	R9K / R1K	6.0 sec max.
1	1	0	30.000mF*	R9K / R1K	6.0 sec max.
1	1	1	300.00mF*	R9K / R1K	30 sec max.

- The displayed counts in ES232 capacitance mode is recommended to be divided by 10. (3000 counts displayed is recommended)
- ALARM bit at capacitance mode is used for increasing the ranging speed. If MPU check the ALARM=1, it can directly set range to the next range, as shown in the following table, and the ADC output should be ignored.

ALARM bit = 1	Current Range	Next Range
	<30.000uF	30.000uF
	30.000uF	3.0000mF
	3.0000mF(1)	300.00mF

Note 1: ALARM bit is not guaranteed work in range of 3.0000mF.

- STA0 status bit is used for detection of DUT capacitor voltage. If STA0=1, the internal capacitor discharging mode is active and the capacitance measurement is inhibited. It is recommended to discharge the DUT capacitor externally.

2.7 Continuity Check measurement

MPU send write command to select the continuity measurement function.

F3	F2	F1	F0	Measurement mode	Read data bytes
0	1	0	1	Continuity mode	D0(0:18), D1(0:9)

Note1: D0/D1 both are binary format. ASIGN/BSIGN bits both are ignored.

Continuity mode shares the same configuration with 300.00Ω resistance measurement circuit and support the low-resistance detection. If the *STBEEP* output (pin64) is low, it means the low-resistance status is detected (It means the *OVX* terminal voltage less than -7mV). It could be faster than the FADC result, so MPU could monitor the *STBEEP* output and FADC (D1) data output make the high-speed detection for short circuit detection. Set

SHBP=1 to enable the built-in buzzer driving automatically when *STBEEP* is active.

2.8 Diode Measurement

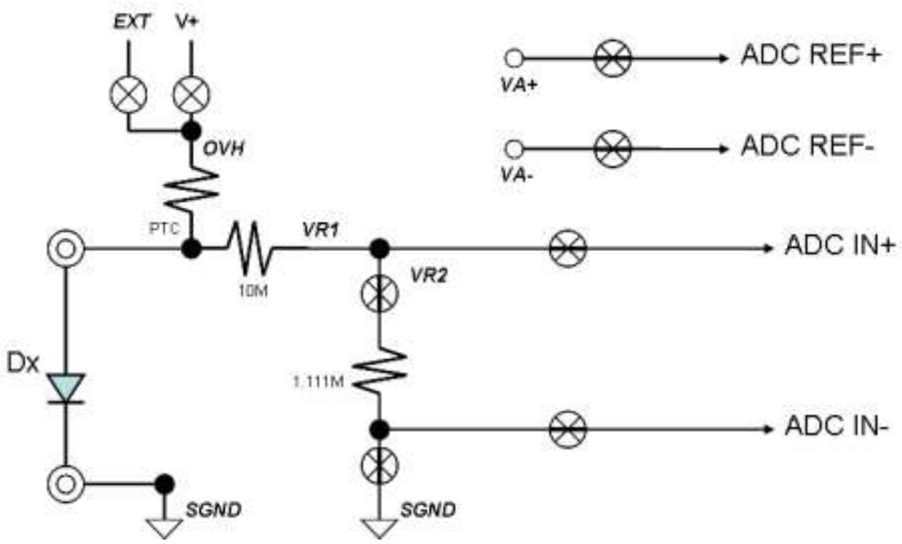
MPU send write command to select the diode measurement function.

F3	F2	F1	F0	Measurement mode	Read data bytes
0	1	1	0	Diode mode	D0(0:18), D1(0:9)

Note1: D0/D1 both are binary format. ASIGN/BSIGN are the sign bit of D0/D1, respectively.

Diode measurement mode shares the same configuration with 3.0000V voltage measurement circuit and support the low-resistance detection. If the *STBEEP* output (pin64) is low, it means the low-resistance status is detected (It means the *OVX* terminal voltage less than 9mV). It could be faster than the FADC result, so MPU could monitor the *STBEEP* output and FADC (D1) data output make the high speed detection for short circuit detection. Set **SHBP**=1 to enable the built-in buzzer driving automatically when *STBEEP* is active.
The default source voltage at diode mode is the same as V+ potential. MPU could set the control bit **EXT**=1 to change the source voltage to external source. The external voltage source (positive or negative) input applied from *EXTSRC* (pin16). The available external source range should be from V+ to V-.

DIODE mode configuration



2.9 Frequency/duty cycle mode measurement

The default typical input impedance of frequency with duty cycle mode is 1MΩ. The MPU could set control bit **RP**=1 to change the input impedance down to 100kΩ. MPU send write command to select the frequency/duty cycle measurement function.

F3	F2	F1	F0	Measurement mode	Read data bytes
0	1	1	1	Hz + Duty mode	D0(0:18), D2(0:18), D3(0:18)

Note1: D0/D2/D3 all are binary format. ASIGN bit is ignored.

Note2: Set LPF1 = 1 to enable the smooth function for sine wave input automatically

Range control for frequency mode

FQ2	FQ1	FQ0	Full Scale	Conversion period
0	0	0	30.000Hz	700ms (fixed)
0	0	1	300.00Hz	700ms (fixed)
0	1	0	3.0000KHz	700ms (fixed)
0	1	1	30.000KHz	700ms (fixed)
1	0	0	300.00KHz	700ms (fixed)
1	0	1	3.0000MHz	700ms (fixed)
1	1	0	30.000MHz	700ms (fixed)
1	1	1	300.00MHz	700ms (fixed)

Available minimum frequency input F_{MIN} = 4.000Hz

Frequency & duty cycle mode computed by D0/D2/D3 (If F_FIN=1)

Flag	STA0=1	STA0=0	
Range*		STA1=1	STA1=0
30.000Hz	FREQ=1000000000/D3	FREQ=4000000000/D3	FREQ=8000000000/D3
300.00Hz	FREQ=100000000/D3	FREQ=400000000/D3	FREQ=1600000000/D3**
3.0000KHz	FREQ=20000000/D3	FREQ=320000000/D3	FREQ=2560000000/D3***
[1]30.000KHz	FREQ=2000000/D3	FREQ=256000000/D3	FREQ=2048000000/D3
300.00KHz	FREQ = D0-1		
3.0000MHz			
30.000MHz			
300.00MHz			

*Note: The Hz measurement of AC+Hz mode is recommended to support 3000 counts displayed

**Note: If D3 < 40000, simple arithmetic mean is necessary to get the 0.01Hz resolution

***Note: If D3 < 50000, simple arithmetic mean is necessary to get the 0.0001 KHz resolution

[1]Note: Set FD=1 to change the frequency calculation at 30kHz range to FREQ = D0 – 1.

Status Flag	**LDUTY=1**	**LDUTY=0**
Duty cycle (<30kHz)	10000-D2*10000/D3	D2*10000/D3

The status flag F_FIN indicate the frequency input signal available (> F_{MIN}) or not. If the computed result less than F_{MIN}, the frequency/duty cycle readings should be set to zero.

The status flags HF & LF are used for fast judgment of proper range. If frequency input is larger than 7 kHz, HF will be active. If frequency input is floating or frequency detected too low, LF will be active.

Auto range consideration for MPU by using Status Flags of frequency mode

<table>
<tr><th rowspan="2">Flag
Range</th><th>F_FIN=0</th><th>F_FIN=1</th><th colspan="2">F_FIN=1</th></tr>
<tr><th>LF=0</th><th>LF=1*</th><th>HF=LF=0</th><th>HF=1**</th></tr>
<tr><td rowspan="2">30.000Hz
300.00Hz
3.0000KHz</td><td rowspan="3">Data and Range is not necessary to be updated</td><td>Hz/Duty=0</td><td rowspan="3">Change range depends on data computed</td><td rowspan="2">Set range to 30.000kHz range</td></tr>
<tr><td rowspan="2">Set range to 30.000Hz range</td></tr>
<tr><td>30.000KHz
300.00KHz
3.0000MHz
30.000MHz
300.00MHz</td><td>Change range depends on data computed</td></tr>
</table>

*Note: LF=1 @ 30Hz range implies the frequency is not available to be measured. The Hz/Duty readings should be set to zero.

**Note: When ACV+Hz/ACA+Hz/ADP+Hz mode is selected, the HF status should be ignored. Change range depends on data calculation result.

Duty cycle mode range (Input sensitivity > 2Vpp @ duty cycle = 5.0% & 95.0%)

Freq. range	**Duty range***
30.000Hz 300.00Hz	5.0% - 95.0%
3.0000KHz	10.0 % - 90.0%
**30.000KHz	20.0% – 80.0%

***Note: Duty range for AC+Hz(%) is 20% ~ 80%.**

****Note: Set FD=1 to improve the duty cycle resolution at 30kHz range.**

2.10 ADP mode

MPU send write command to select the ADP mode measurement function. The Hz mode measurement is available to be enabled with the ADP AC function (set AC bit to 1) simultaneously. The measured signal is applied to *ADP* terminal (pin39 and pin51). The signal full scale is 300mV for DC mode and 300mVrms for AC mode.

See the next table of function command:

F3	F2	F1	F0	AC	Measurement mode	Read data bytes
1	0	0	1	0	ADP DC mode	D0(0:18), D1(0:9)
1	0	0	1	1	ADP AC mode	D0(0:18), D1(0:9)
1	0	1	0	1	ADP + Hz(%) mode	D0(0:18), D1(0:9), D2(0:18), D3(0:18)

Note1: D0/D1/D3 all are binary format. ASIGN/BSIGN are the sign bit of D0/D1, respectively.
Note2: See PEAK mode (section 2.10) also.

Range control for ADP mode (AC/DC)

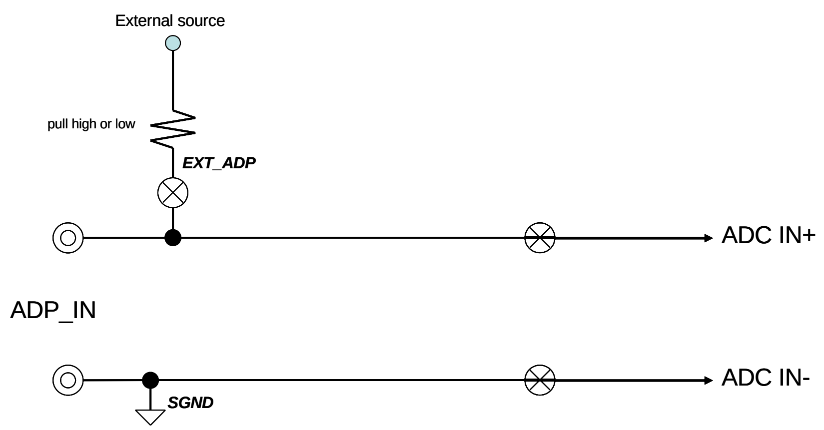
Q2	Q1	Q0	Full Scale Range	Input terminal
0	0	0	300mV→ 30000counts	ADP
1	1	1	300mV→ 30000counts	ADP1

Frequency range control for ADP+Hz(%) mode

FQ2	FQ1	FQ0	Full Scale Range
0	0	0	30.00Hz
0	0	1	300.0Hz
0	1	0	3.000kHz
0	1	1	30.00kHz
Duty Cycle			20% ~ 80%

Note: See frequency mode (section 2.9) also

If MPU set the control bit **EXT_ADP**=1, the voltage on *EXTSRC* pin could be switched to *ADP* terminal internally. It is helpful for a voltage pulled application of ADP mode.



2.11 Peak-hold measurement mode

ES232 provides a peak hold function to capture the real peak value for voltage or current measurement mode. In a case of a 1V sine wave input voltage, the peak hold function gets a maximum peak value of 1.414V and minimum peak value of –1.414V ideally. Set the control bit **PEAK**=1 to force the ES232 entering PEAK measurement mode. Peak Hold function is divided into two parts of peak maximum and peak minimum conversion. High resolution SADC performs peak maximum and peak minimum conversion in turn, not at the same time. The status flag PMAX or PMIN shows which type the peak value is. If PMAX=1(PMIN=1), the SADC output D0 is the conversion data on *PMAX (PMIN)* terminals (pin 61/62). The MPU should make the comparison procedure to get the maximum value of *PMAX* data and minimum value of *PMIN* data. The max counts for D0 is 54000.

Peak calibration mode

At PEAK-Hold measurement mode, the offset voltage of internal operation amplifier will cause an error. To obtain a more accurate value, the offset error must be canceled. ES232 provides the peak calibration feature to remove the influence on accuracy by internal offset voltage. Set the control bit **PCAL**=1 to enter peak calibration mode. When PCAL mode is active, the SADC of ES232 will output the calibration value of peak maximum and minimum conversion in turn. The offset values should be memorized respectively and deducted from the data of *PMAX/PMIN* at the normal peak measurement mode.

Set PCAL=1 or PEAK=1		
Status indication	**PMAX=1, PMIN=0**	**PMAX=0, PMIN=1**
ADC data	$V_{PMAX.C}$	$V_{PMIN.C}$

$V_{PMAX.C}$ and $V_{PMIN.C}$ are not the real-time value of peak-hold voltage. They are the voltage stored on terminal capacitor (pin61-62). Because the capacitor will be self-discharging, so MCU need to compare the $V_{PMAX.C}$ & $V_{PMIN.C}$ respectively and memorize the maximum and minimum peak values in turn.

2.12 Sleep

Set *CS* pin (pin 80) to logic low to make the ES232 entering the sleep mode. The current consumption will be less than 3uA typically. Set *CS* pin to logic high or kept floating, the ES232 will return to normal operation.

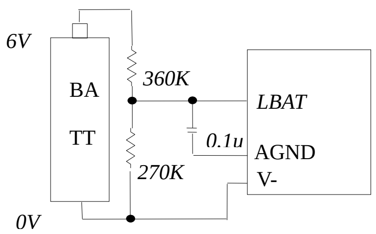
2.13 Multi-level battery voltage indication

The ES232 is built-in a comparator for batter voltage indication. The voltage is applied to *LBAT* pin (pin 89) vs. *V*- terminal. MPU could check the status bit BTS1/BTS0 and monitor the *LBAT* voltage status.

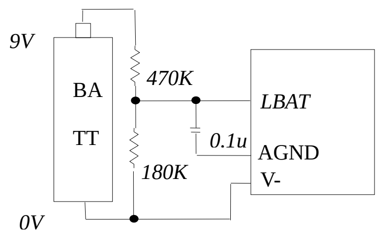
Battery voltage	BTS1	BST0
$V_{LBT} > V_{t1}$	1	1
$V_{t2} < V_{LBT} < V_{t1}$	1	0
$V_{t3} < V_{LBT} < V_{t2}$	0	1
$V_{LBT} < V_{t3}$	0	0

Low battery configuration for 9V/1.5V*4/1.5V*3 battery

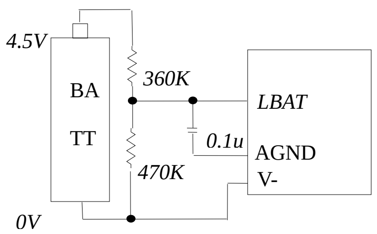
Low battery test circuit (a)



Low battery test circuit (b)



Low battery test circuit (c)



2.14 Independent OPAMP

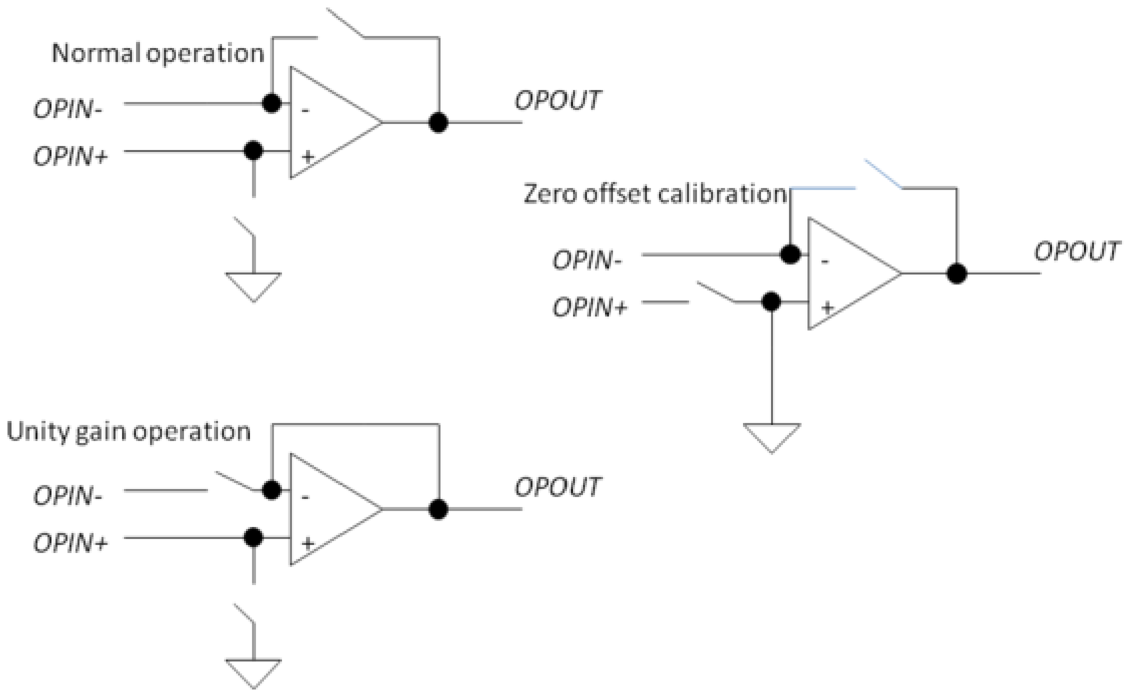
ES232 is built-in an independent OPAMP with low drift offset using for general purpose.

MPU could control the OP1/OP0 to change the OPAMP configuration:

OP1	OP0	OPAMP configuration
0	0	Normal
0	1	OP disable
1	0	Unity gain buffer
1	1	Zero calibration

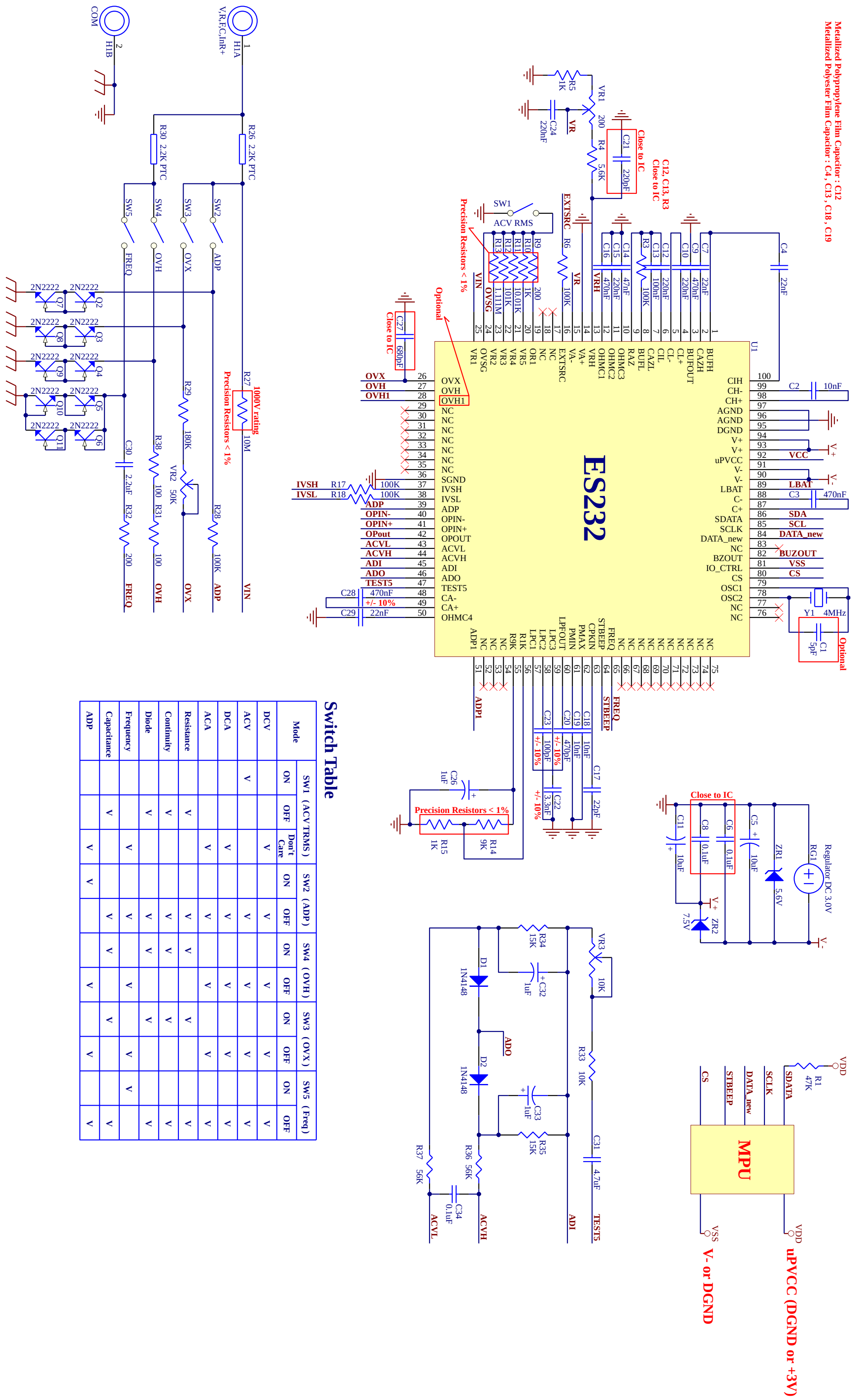
Note: If AC=1, it is recommended to set FD=1 simultaneously.

Independent OPAMP configuration



3. Application Circuit

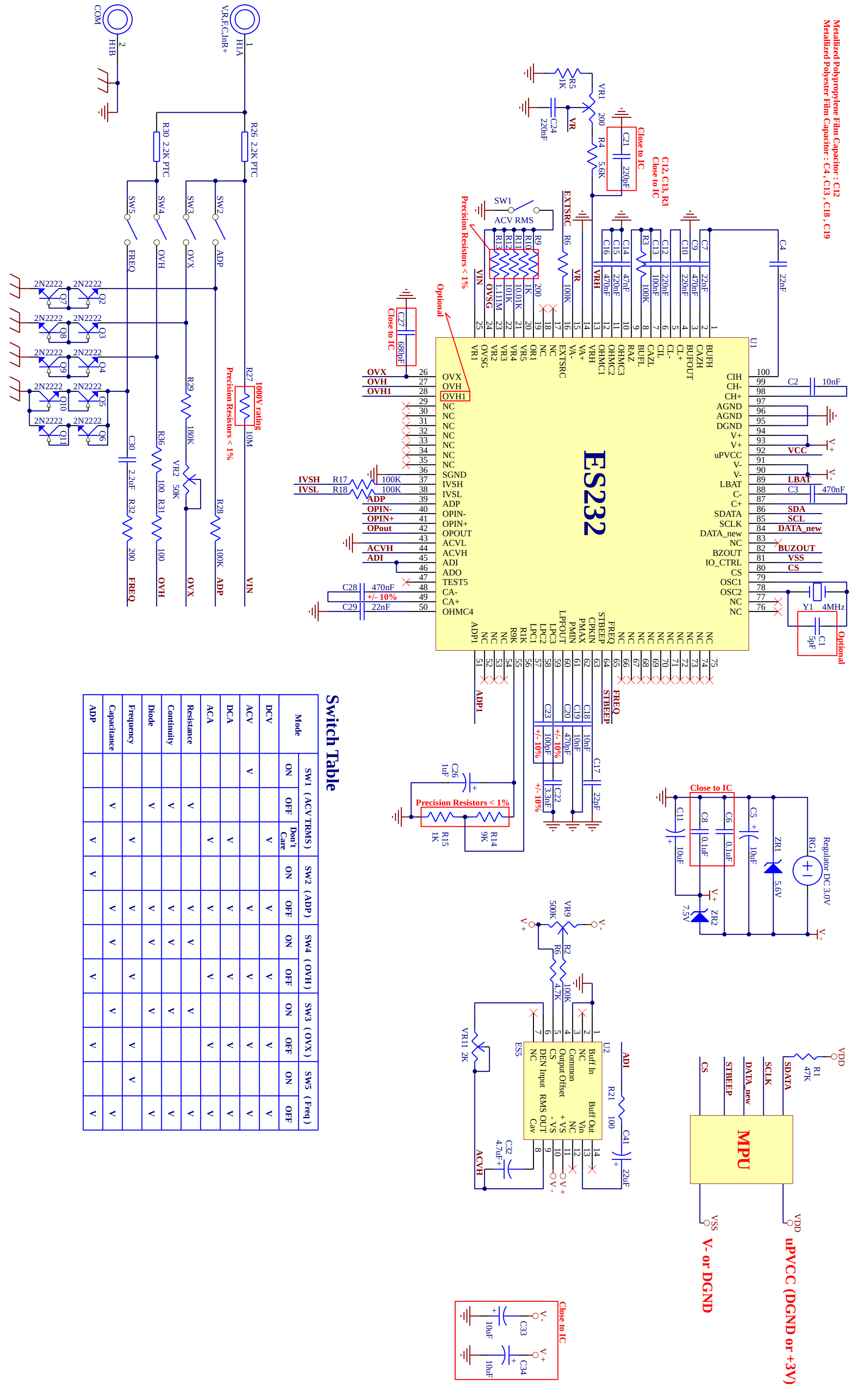
3.1 AVG circuit



Switch Table

Mode	SW1 (ACV TRMS) ON	SW1 (ACV TRMS) OFF	SW1 (ACV TRMS) Don't Care	SW2 (ADP) ON	SW2 (ADP) OFF	SW4 (OVH) ON	SW4 (OVH) OFF	SW3 (OVX) ON	SW3 (OVX) OFF	SW5 (Freq) ON	SW5 (Freq) OFF
DCV			V		V		V		V		V
ACV	V				V		V		V		V
DCA			V		V		V		V		V
ACA			V		V		V		V		V
Resistance		V			V	V		V			V
Continuity		V			V	V		V			V
Diode		V			V	V		V			V
Frequency			V		V		V		V	V	
Capacitance		V			V	V		V			V
ADP			V	V			V		V		V

3.2 RMS circuit (ES5)

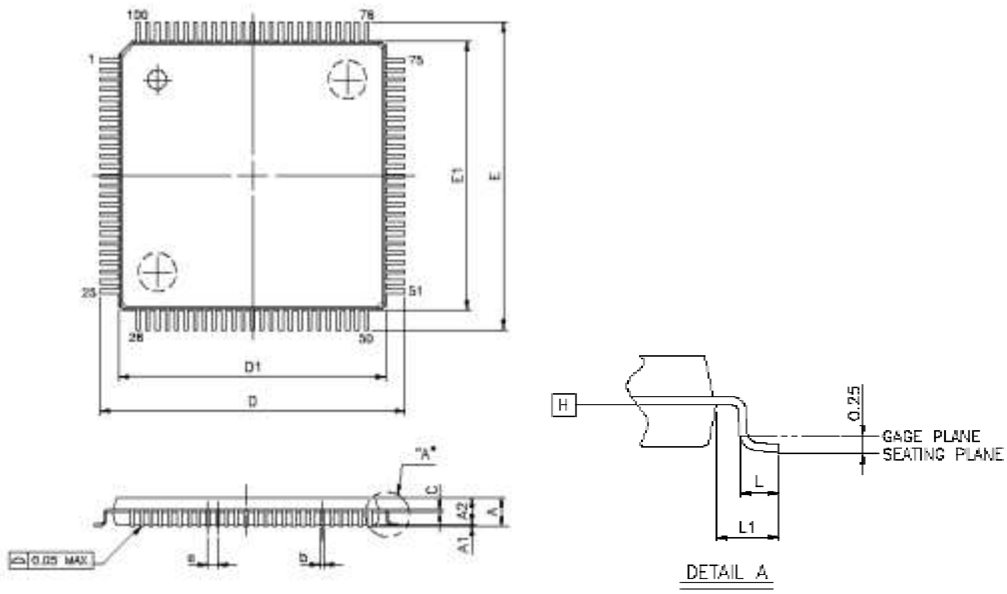


Switch Table

Mode	SW1 (ACV TRMS) ON	SW1 (ACV TRMS) OFF	SW1 (ACV TRMS) Don't Care	SW2 (ADP) ON	SW2 (ADP) OFF	SW4 (OVH) ON	SW4 (OVH) OFF	SW3 (OVX) ON	SW3 (OVX) OFF	SW5 (Freq) ON	SW5 (Freq) OFF
DCV			V		V		V		V		V
ACV	V				V		V		V		V
DCA			V		V		V		V		V
ACA			V		V		V		V		V
Resistance		V			V	V		V			V
Continuity		V			V	V		V			V
Diode		V			V	V		V			V
Frequency			V		V		V		V	V	
Capacitance		V			V	V		V			V
ADP			V	V			V		V		V

4. Package Information

4.1 100L LQFP Outline drawing



4.2 Dimension parameters

VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	MIN.	NOM.	MAX.
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
b	0.17	0.20	0.27
c	0.09	0.127	0.20
D	16.00 BSC		
D1	14.00 BSC		
E	16.00 BSC		
E1	14.00 BSC		
e	0.50 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		