

Delta-Sigma Analog-to-Digital Converters

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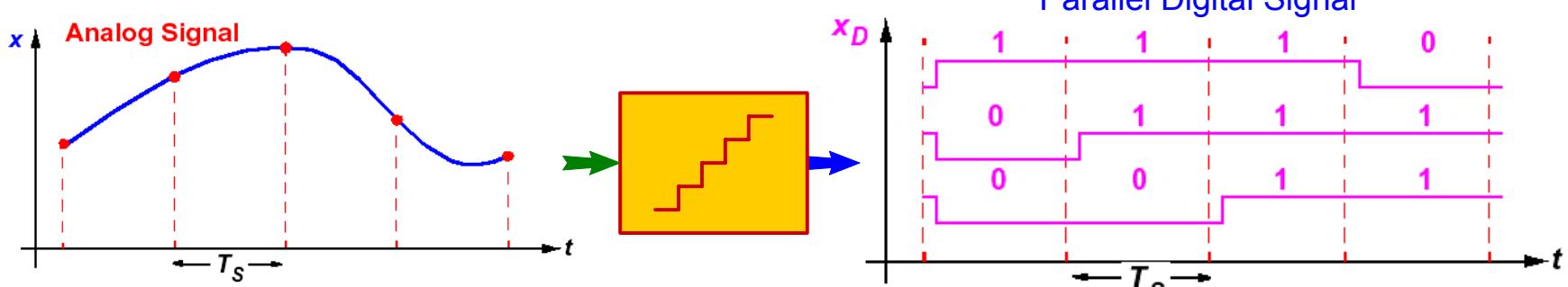
Introduction

● Data Converters

- Although digital circuits are robust and can be realized extremely small, the physical world nevertheless remains stubbornly analog
 - Data converters are needed to interface with the digital signal processing (DSP) core

● Analog-to-Digital Converters (ADC) & Digital-to-Analog Converters (DAC)

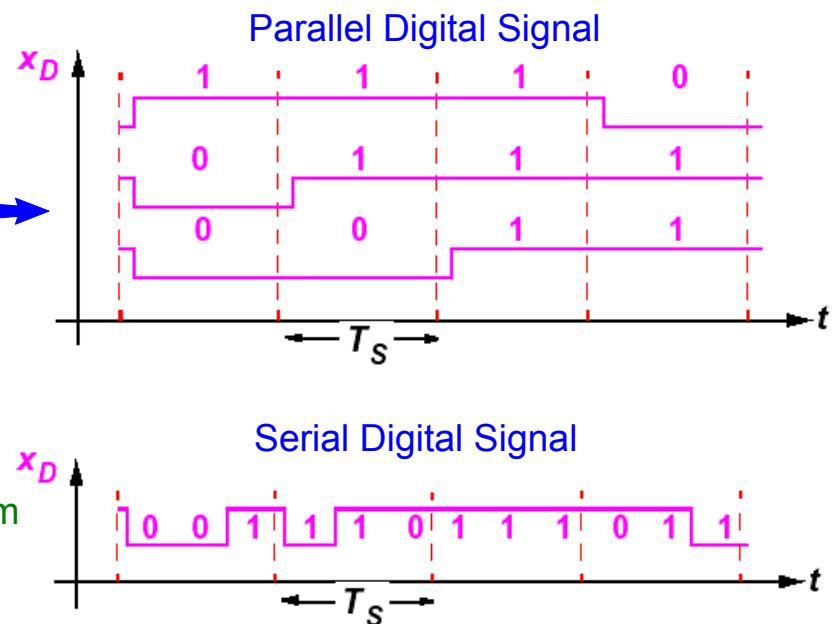
■ Sample & Quantization



► Sampling frequency : $f_s = 1/T_s$

► Aliasing or folding

- The signal overlaps with its replicas in spectrum
- Nonlinear distortion



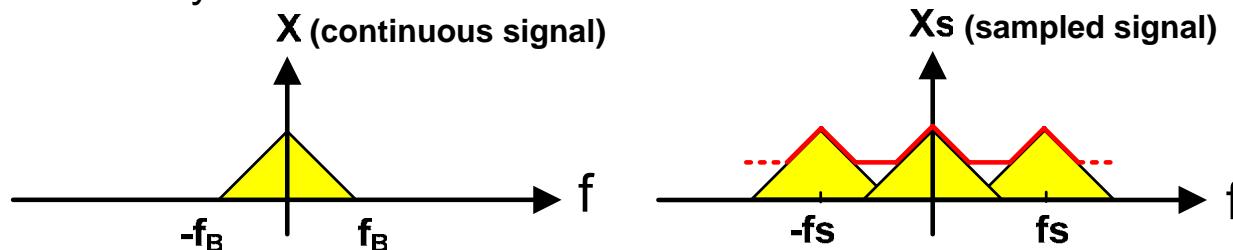
Data Converters

● Nyquist-Rate Converters

- One-to-one correspondence between the input and output samples

- ▶ Regardless of the earlier input samples

- ▶ No memory



- Nyquist rate ($f_N = 2f_B$)

- ▶ The sampling rate = twice the bandwidth of the input signal **to avoid aliasing**

- ▶ Brick-wall anti-aliasing filter (AAF)

- ▶ Nonlinear phase distortion

- ▶ Nyquist-rate converters operate at 1.5~10×Nyquist rate

- The converter is too slow for most high-resolution signal-processing applications

- ▶ Dual slope integrating converters – 2^N clock cycles

- Anti-aliasing filter ($f_{3dB} = fs/2$) is required for Nyquist-rate data converter

- ▶ To prevent the out-of-band noise coupling into the interest band

Data Converters

- Oversampling Data Converters

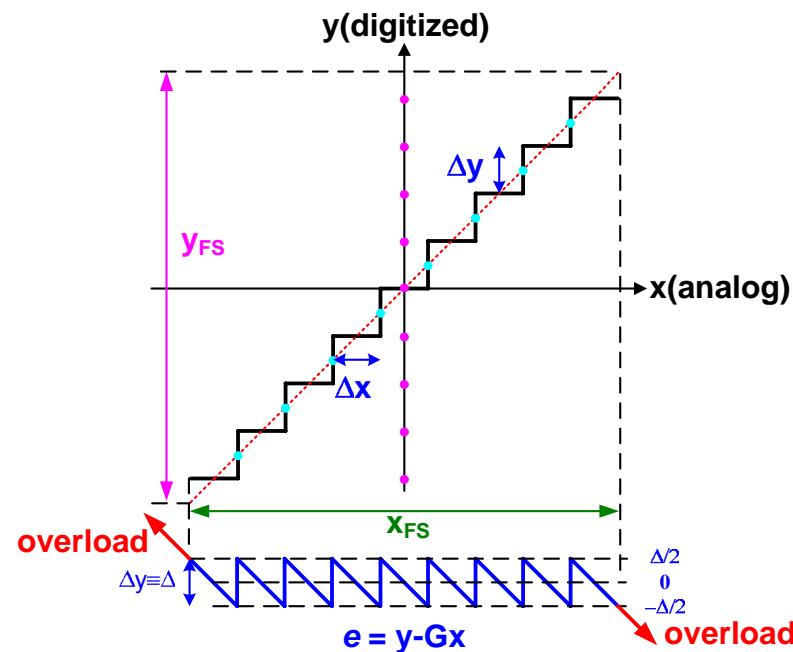
- The sampling rate is much higher than Nyquist rate
 - ➡ Between 8 and 512
- Utilize all preceding input values
- Only a comparison of complete input and output waveforms in the time or frequency domain can be used to evaluate the converter's accuracy
- Relaxed requirements of analog components compared to those associated with Nyquist-rate converters
 - ➡ Analog anti-aliasing filters for ADCs, smoothing filters for DACs
- At the cost of faster operation and complicated digital circuits
 - ➡ Both are getting cheaper as digital IC technology advances
- Oversampling data converters are gradually taking over in many applications previously dominated by Nyquist-rate ones
 - Delta-Sigma ($\Delta\Sigma$) Modulators



Quantization

- Quantization Type

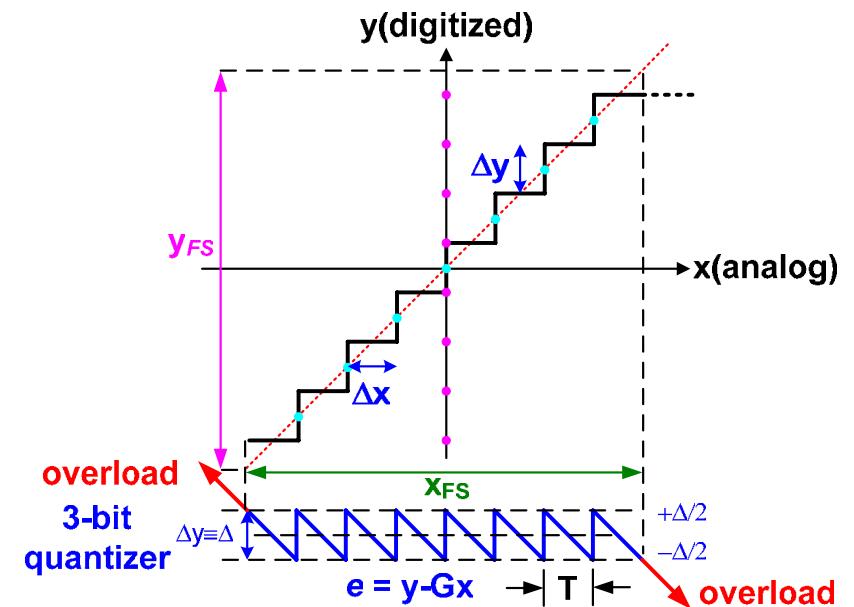
 - Mid-Tread



Output constant at the middle
of the input range

- The number of levels = $2^N + 1$
- Maximum amplitude of input signal = $\frac{\Delta \cdot 2^N}{2}$

 - Mid-Rise



Output transition at the middle
of the input range

- The number of levels = 2^N
- Gain of quantizer
 $G = y_{FS} / x_{FS}$

Signal-to-Noise Ratio (SNR)

- The Max rms Value of Sinusoidal Signal

$$V_{in(rms)_max} = \frac{2^N \cdot \Delta}{2\sqrt{2}}$$

- Quantization Error ($e = V_Q = y - G \cdot x$)

- The mean square power of quantization error (noise) P_Q

$$e = V_{Q(rms)} = \sqrt{\frac{1}{T} \int_{-T/2}^{T/2} \Delta^2 \left(\frac{-t}{T}\right)^2 dt} = \frac{\Delta}{\sqrt{12}} \Rightarrow P_{Q(rms)} = \frac{\Delta^2}{12}$$

- Peak Signal-to-Noise Ratio (SNR_{peak})

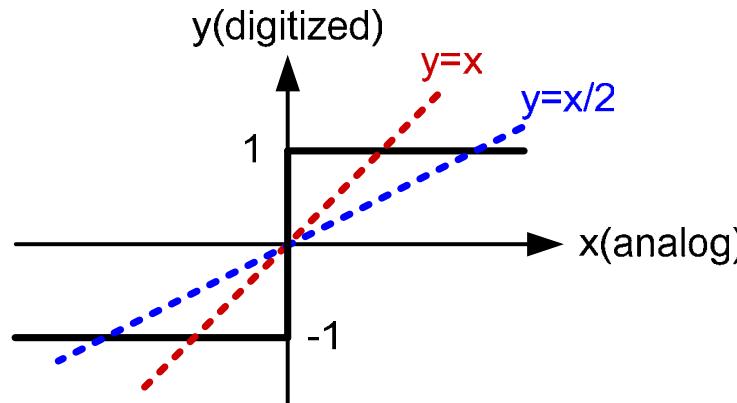
$$SNR_{peak} = 10 \log\left(\frac{P_{in}}{P_Q}\right) = 20 \log\left(\frac{V_{in(rms)}}{V_{Q(rms)}}\right)$$

$$SNR_{peak}(dB) = 10 \times \log(2^{2N}) + 10 \times \log\left(\frac{3}{2}\right) = \underline{6.02 \times N + 1.76}$$



Quantization

- Binary Quantization (Single-bit)



$$e = y - Gx$$

The gain G (k) of the quantizer is not defined easily

- Minimize the mean square value (average power) of the error sequence e

$$\sigma_e^2 = \lim_{N \rightarrow \infty} \frac{1}{N} \sum_{n=0}^N e(n)^2 = \lim_{N \rightarrow \infty} \frac{1}{N} \sum_{n=0}^N [y(n)^2 - 2Gy(n)x(n) + G^2x(n)^2]$$

- The minimized average error occurs when

$$G = \frac{\lim_{N \rightarrow \infty} \frac{1}{N} \sum_{n=0}^N [y(n)x(n)]}{\lim_{N \rightarrow \infty} \frac{1}{N} \sum_{n=0}^N [x(n)^2]} = \lim_{N \rightarrow \infty} \frac{\frac{1}{N} \sum_{n=0}^N |x(n)|}{\frac{1}{N} \sum_{n=0}^N [x(n)^2]} = \frac{E[|x|]}{E[x^2]}$$

Inner (scalar) product

- The optimal value of G (k) is dependent on the statistics of its input x
- The value of k is dependent on the statistics of its input x
- $\Rightarrow x \uparrow \Rightarrow k \downarrow$



Quantization

- Random Signal Assumption

- Quantization error  Quantization noise

- The error is independent of the input signal
- The error is uncorrelated from sample to sample
- The error has equal probability of lying anywhere in the range of $\pm\Delta/2$

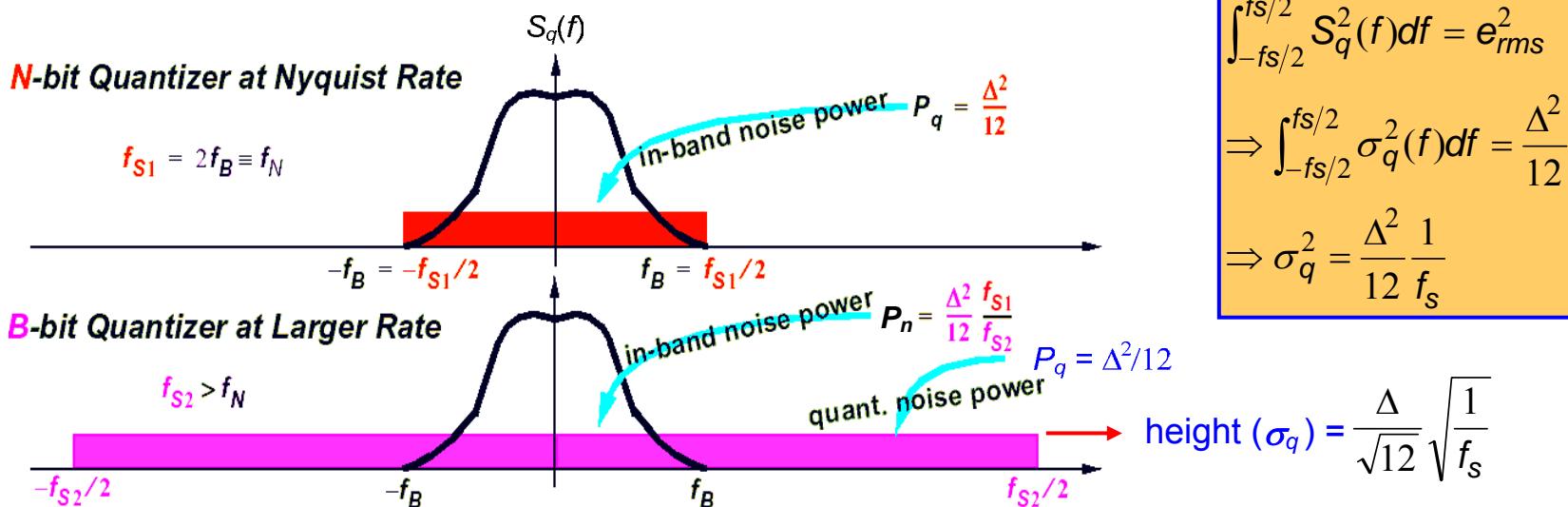
uniform noise
power spectral density



- White noise signal
 - The power spectral density is constant

Oversampling

- A signal is sampled at frequency $f_s = 1/T \gg$ Nyquist rate f_N
 - All the quantization noise power folds into the frequency band $-f_s/2 \leq f \leq f_s/2$
 - The spectral density of quantization noise $S_q(f)$



- The noise power falls into the signal bandwidth f_B

$$\Rightarrow P_n = \int_{-f_B}^{f_B} S_q^2(f) df = \frac{\Delta^2}{12} \left(\frac{2f_B}{f_s} \right) = \frac{\Delta^2}{12} \frac{1}{OSR}$$

$$\text{Over Sampling Ratio OSR} = \frac{f_s}{2f_B} = \frac{f_s}{f_N}$$

- The maximum SNR $\text{SNR}_{max} = 10 \log(\frac{P_{in}}{P_n}) = 1.76 + 6.02N + 10 \log(\text{OSR})$

→ Oversampling reduces the in-band rms noise 3dB/octave or 0.5bits/octave

Performance Metrics

■ SNDR

- ▶ Ratio of signal power to the power of noise plus distortion

$$\text{SNDR} = 20 \log \left(\frac{\text{signal power}}{\text{noise + harmonics}} \right)$$

■ Dynamic range (DR)

- ▶ Denotes the range of input signal amplitudes for which useful output can be obtained from a system

■ Effective number of bits (EOB)

$$\text{Resolution EOB} = \frac{\text{SNR}_{\text{peak}} - 1.76}{6.02}$$

- ▶ How small analog signal can be digitized

■ Spurious-Free Dynamic Range (SFDR)

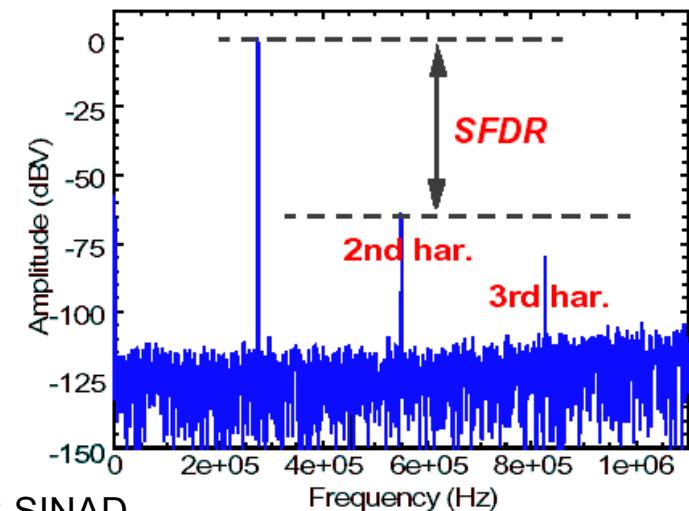
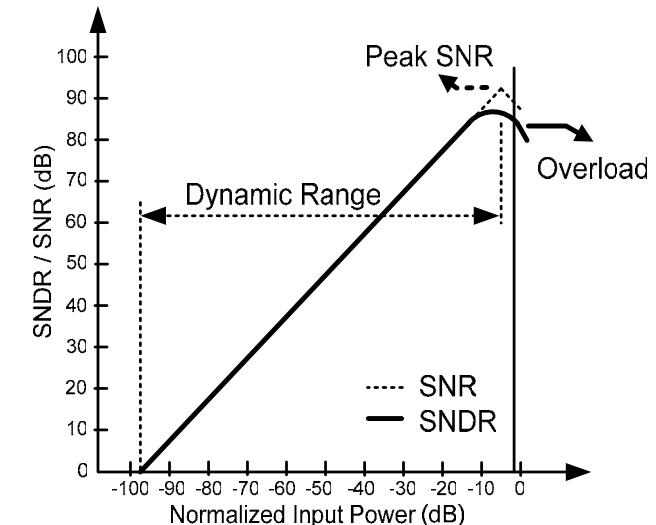
- ▶ Ratio between the signal and the maximum distortion power

■ Signal to noise-plus-distortion ratio (SINAD)

- ▶ The reciprocal of THD plus noise

$$20 \log \left| \frac{1}{\text{THD} + \text{Noise}} \right|$$

- ▶ Ex. 0.0015% THD+N \Rightarrow 15ppm \Rightarrow -96.5dBc \Rightarrow 96.5dB SINAD



Nonideal Quantization

● Imperfections

■ Offset

► Deviation of the first transition

■ Gain error

► Different slope of the transfer curve

■ Differential NonLinearity (DNL)

► the difference between the maximum of deviations of the practical step sizes and the nominal value of one least significant bit (LSB)

► $DNL \geq 1\text{LSB} \rightarrow \text{Missing code}$

■ Integral NonLinearity (INL)

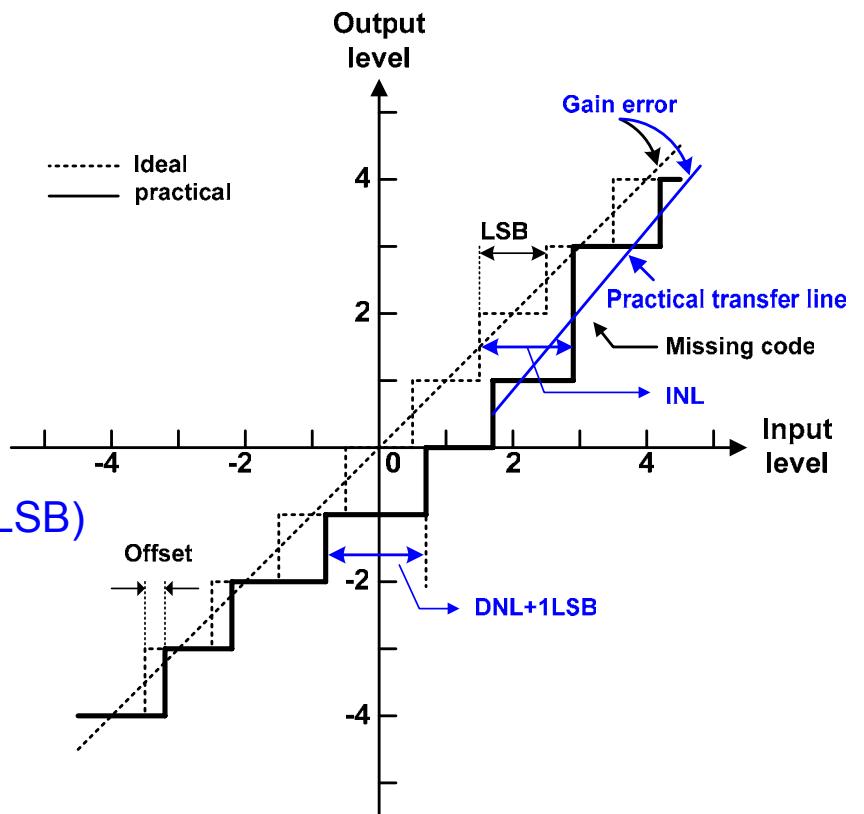
► the deviation of the practical transfer characteristic from the ideal straight line characteristic of the quantizer

● Two-Level Quantization

■ The threshold need not be accurately positioned

► Linearity inherently

► Suffer from spurious tones in delta sigma oversampling ADC



The Fundamentals of Lowpass Delta Sigma Modulators

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Delta-Sigma ($\Delta\Sigma$) Modulators

- Basic Performance

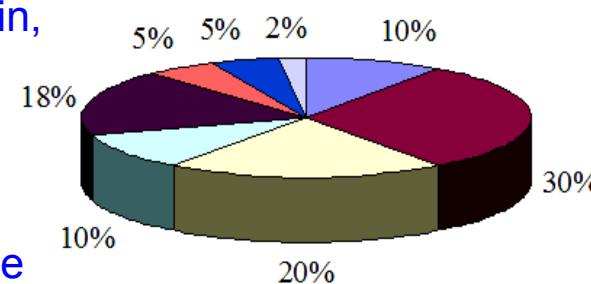
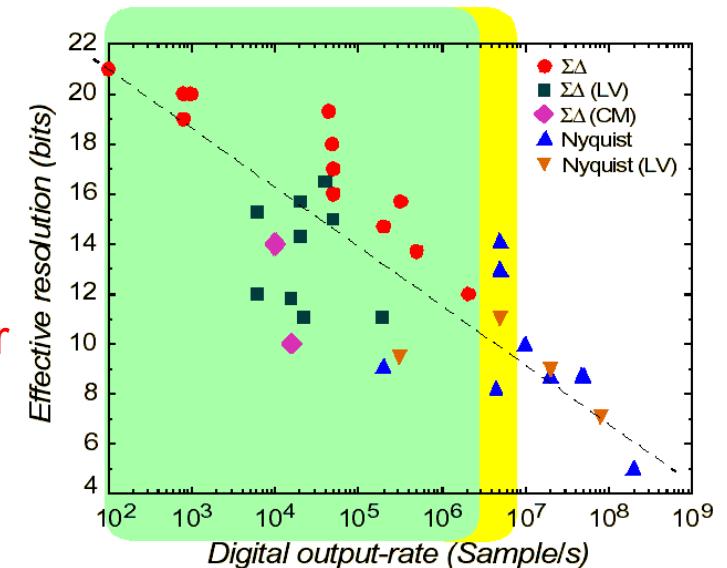
- Resolution - bits
- Speed - Hz
 - There is a trade-off between resolution and speed

- Delta-Sigma ($\Delta\Sigma$) Modulator or Sigma-Delta Modulator

- Oversampling ADC
 - Developed four decades ago
 - Wide region of resolution-frequency plane
 - High-resolution medium-to-low speed applications

- Good tolerance to matching, opamp gain, and other second-order phenomena

- Relax the requirement for analog anti-aliasing filters in oversampling technique

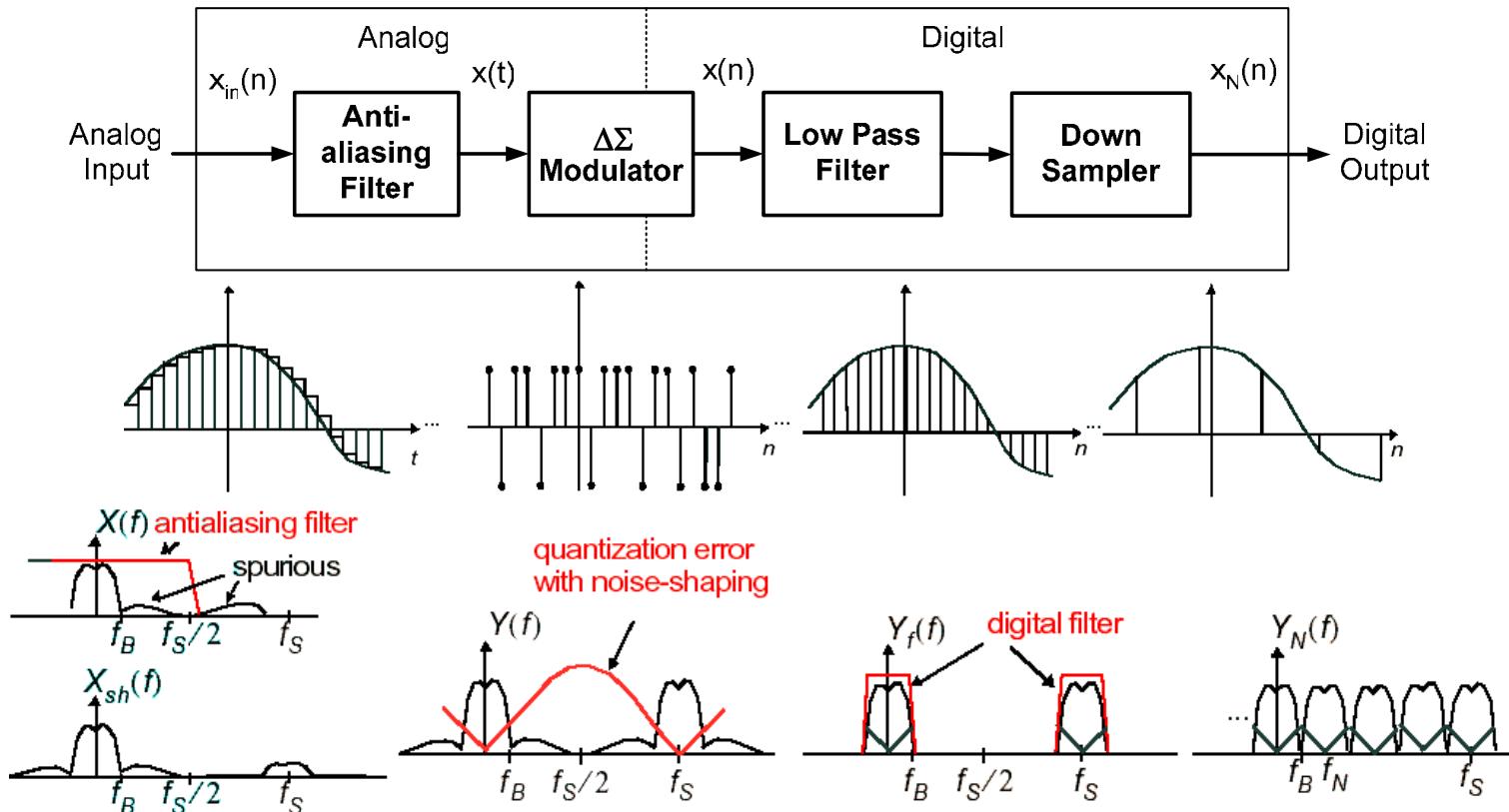


Power Management
Wireless Communication
High Resolution Measurement
Digital Recording Studio
DVD application
MIDI and Audio Instrument
CMOS Image Sensor
Magnetic Sensor

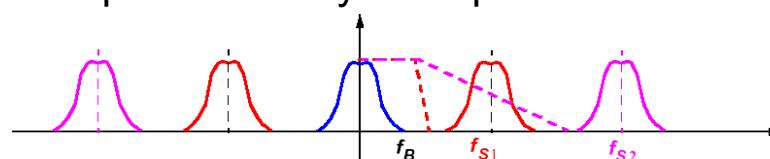


Delta-Sigma Oversampling ADCs

● Oversampling with Noise Shaping

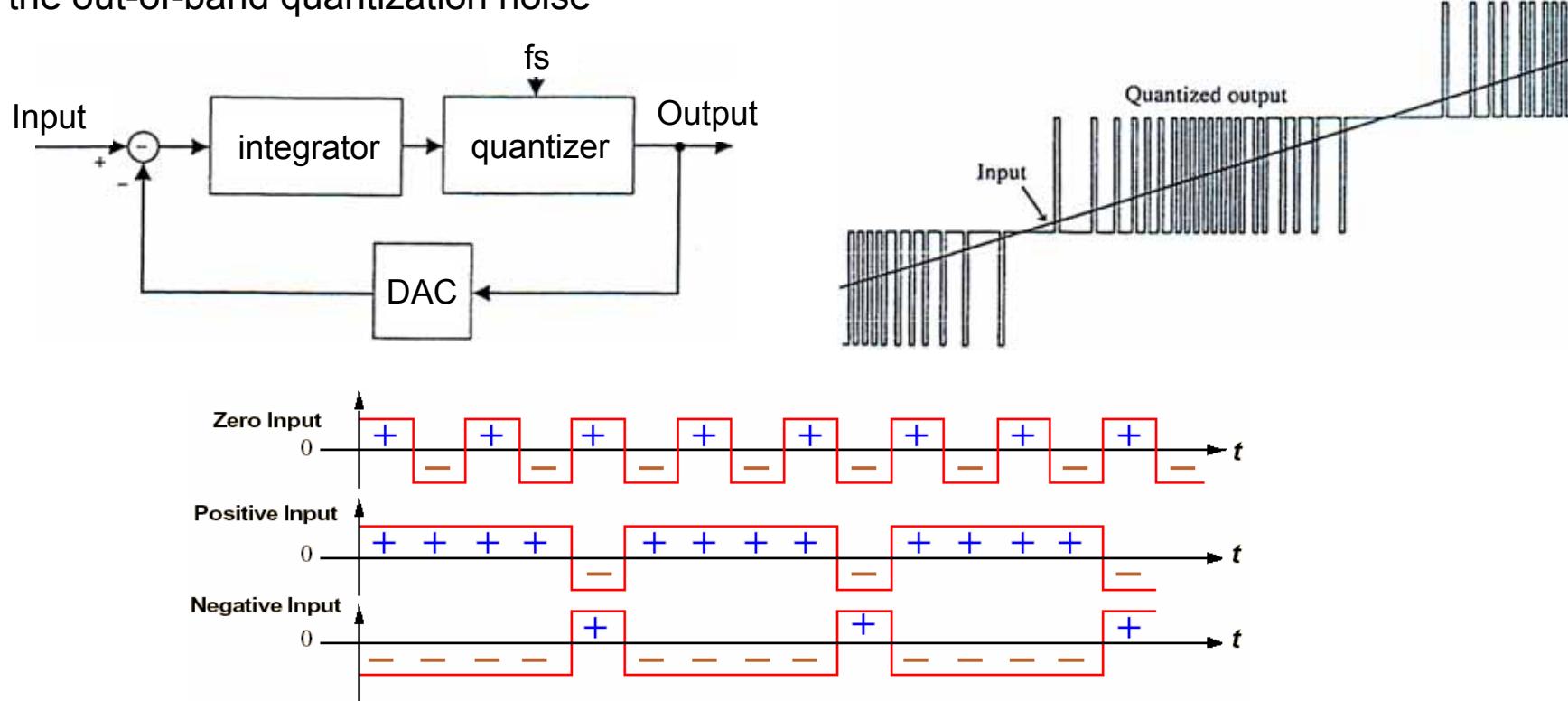


- Improve the SNR by moving the quantization noise outside the signal band
- Anti-aliasing filter can be implemented by a simple RC filter for the reason of large oversampling ratio



Delta-Sigma Oversampling ADCs

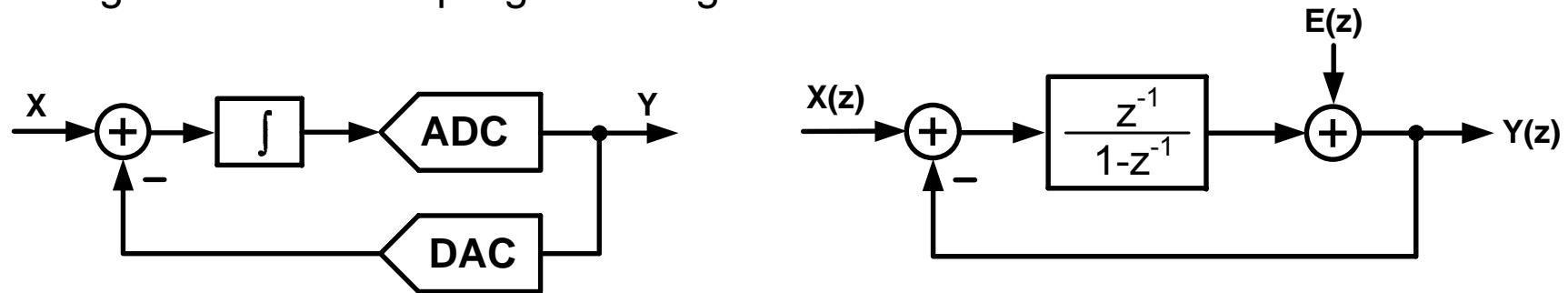
- **$\Delta\Sigma$ modulator** converts the analog signal into a noise-shaped low-resolution digital signal
- **Decimator** converts a high-resolution digital signal at a lower sampling rate ($2f_0$) and removes the out-of-band quantization noise



- The feedback forces the average value of the local quantized signal to track the average input in low frequency band
 - ▶ Due to the high gain of the integrator

Delta-Sigma ($\Delta\Sigma$) Modulators

- Block Diagram of Oversampling Delta-Sigma Modulators



- Integrator — the order of noise-shaping
 - ➡ Continuous-time — Gm-C circuit
 - ➡ Discrete-time — Switched-capacitor circuit
- An internal low-resolution ADC and DAC
- A loop filter is in the forward path of the loop
 - ➡ High gain in the signal band
 - ➡ The in-band “noise” is strongly attenuated
- Nonlinear distortion in the DAC is a major limitation on the performance
 - ➡ Single-bit quantization – inherently linear
 - ➡ Multi-bit quantization with digital correction or dynamic matching techniques

Delta-Sigma Modulators

- Interpolative Structure

- Two independent input – input signal $X(z)$ and quantization noise $E(z)$
 - The maximum level of $X(z)$ must remain within the maximum level of feedback signal for stability consideration

- Signal transfer function $STF(z)$

- Noise transfer function $NTF(z)$

$$STF(z) = \frac{Y(z)}{X(z)} = \frac{H(z)}{1 + H(z)} \quad NTF(z) = \frac{Y(z)}{E(z)} = \frac{1}{1 + H(z)}$$

- The output of the modulator

$$Y(z) = STF(z)X(z) + NTF(z)E(z)$$

- $H(z)$: Discrete-time integrator

$$H(z) = A_0 \frac{z^{-1}}{1 - z^{-1}} \text{ (delaying)}$$

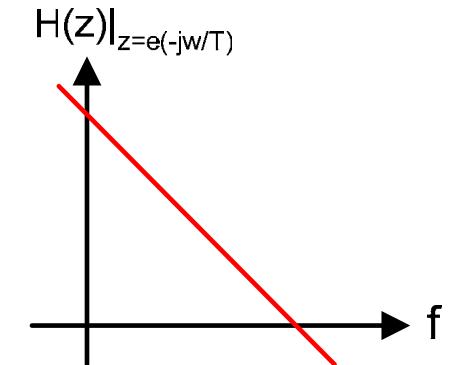
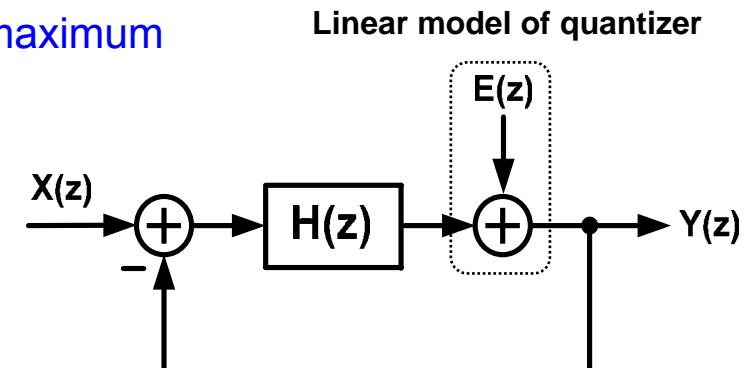
$$H(z) = A_0 \frac{1}{1 - z^{-1}} \text{ (delay-free)}$$

- A large magnitude of $H(z)$ must be chosen over the interest band

- $STF(z)=1$ (lowpass function)

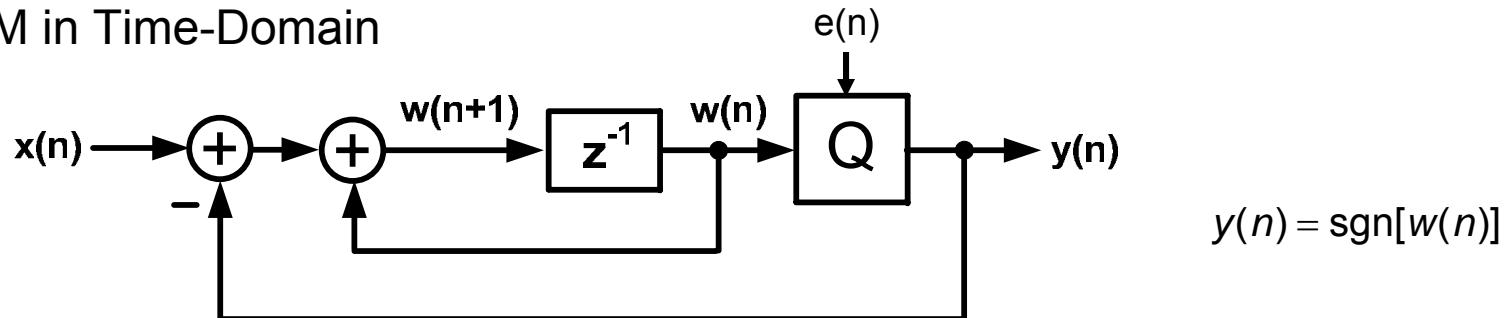
- $NTF(z)=0$ (highpass function)

- The zeros of the $NTF(z)$ equals to the poles of $H(z)$



First-Order Delta-Sigma Modulators

- 1-Bit DSM in Time-Domain



$$w(n+1) = w(n) + x(n) - y(n) \quad \text{for } n = 1, 2, \dots, N$$

$$w(N+1) - w(1) = \sum_{n=1}^N [x(n) - y(n)]$$

$$\lim_{N \rightarrow \infty} \frac{w(N+1) - w(1)}{N} = \lim_{N \rightarrow \infty} \frac{1}{N} \sum_{n=1}^N x(n) - \lim_{N \rightarrow \infty} \frac{1}{N} \sum_{n=1}^N y(n)$$

- Assume the loop is stable, so that $w(n)$ is bounded (finite)

- $\Rightarrow 0 = \bar{x} - \bar{y}$

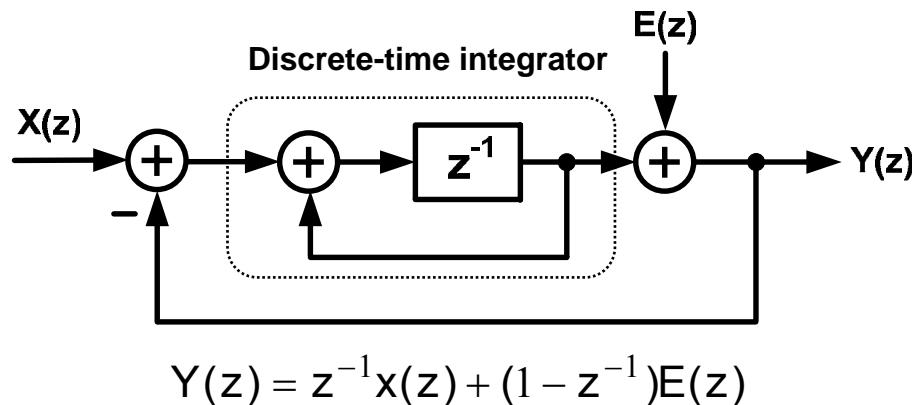
- \Rightarrow The average value of the digital output y becomes a good approximation of the input
 - The average value of discrete-time integrator's input equals to zero

- Make the first difference of the quantization error while leaving the signal unchanged except for a delay

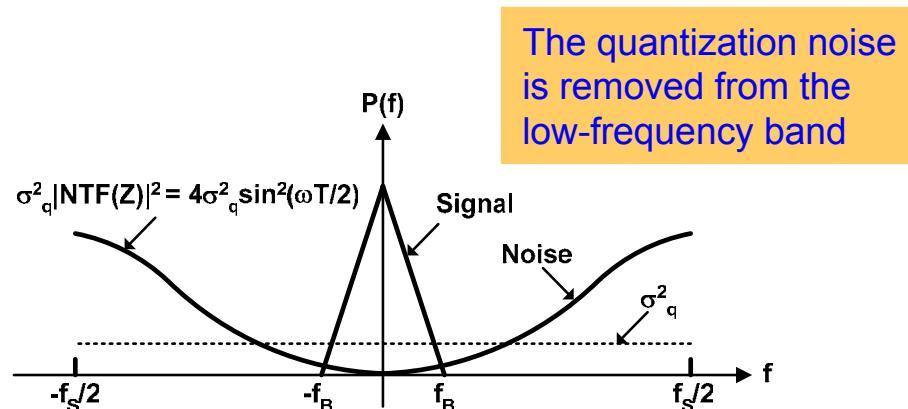
$$y(n) = x(n-1) + e(n) - e(n-1)$$

First-Order Delta-Sigma Modulators

- 1-Bit DSM in z-Domain



- Noise-Shaping in Frequency-Domain (for $f \ll f_s$)



- The maximum SNR

$$SNR_{max} = 1.76 - 5.17 + 6.02N + 30\log(OSR)$$

- Discrete-time integrator $H(z) = \frac{z^{-1}}{1 - z^{-1}}$

→ A pole at dc ($z=1$)

$$z = e^{j\omega T} = 1 \Rightarrow \omega T = 2\pi f/f_s = 0$$

- The quantization noise

→ high-pass filtered

→ A zero at dc

$$|NTF(z)| = |1 - e^{-j\omega T}| = |1 - e^{-j2\pi f/f_s}| = 2 \sin\left(\frac{\pi f}{f_s}\right)$$

→ The quantization noise power

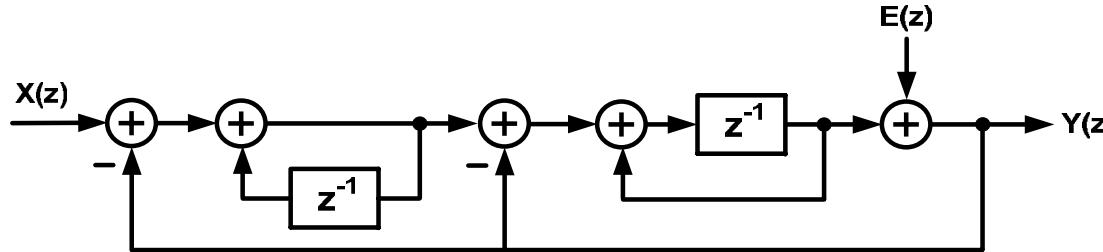
$$P_n = \int_{-f_B}^{f_B} S_q^2(f) |NTF(z)|^2 df \approx \left(\frac{\Delta}{12}\right)^2 \frac{\pi^2}{3} \frac{1}{OSR^3}$$

Doubling the OSR gives an SNR improvement by 9dB or 1.5bits/octave

Second-Order Delta-Sigma Modulators

- Boser-Wooley Modulator

- The noise power decreased as the noise-shaping order increased



$$Y(z) = X(z)z^{-1} + (1 - z^{-1})^2 E(z)$$

$$STF(z) = z^{-1} \quad NTF(z) = (1 - z^{-1})^2$$

$$|NTF(z)| = [2 \sin(\frac{\pi f}{f_s})]^2$$

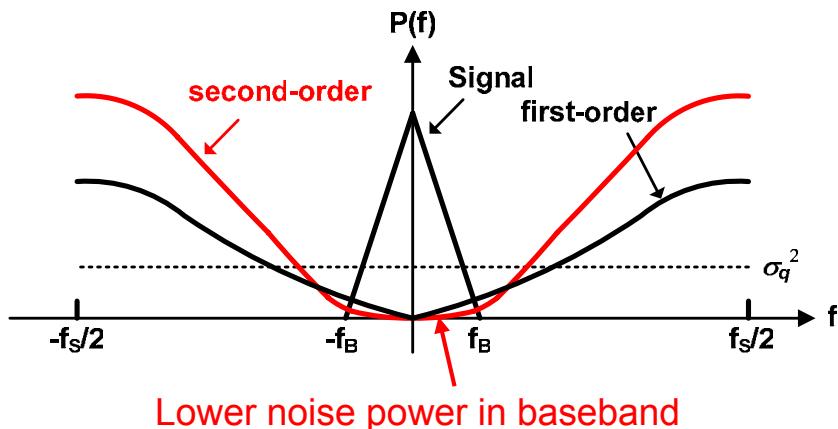
► The quantization noise power

$$\triangleright P_n = \int_{-f_B}^{f_B} S_q^2(f) |NTF(z)|^2 df \approx (\frac{\Delta^2}{12}) \frac{\pi^4}{5} \frac{1}{OSR^5}$$

► The maximum SNR

$$\triangleright SNR_{max} = 1.76 - 12.9 + 6.02N + 50\log(OSR)$$

Doubling the OSR gives an SNR improvement by 15dB or 2.5bits/octave

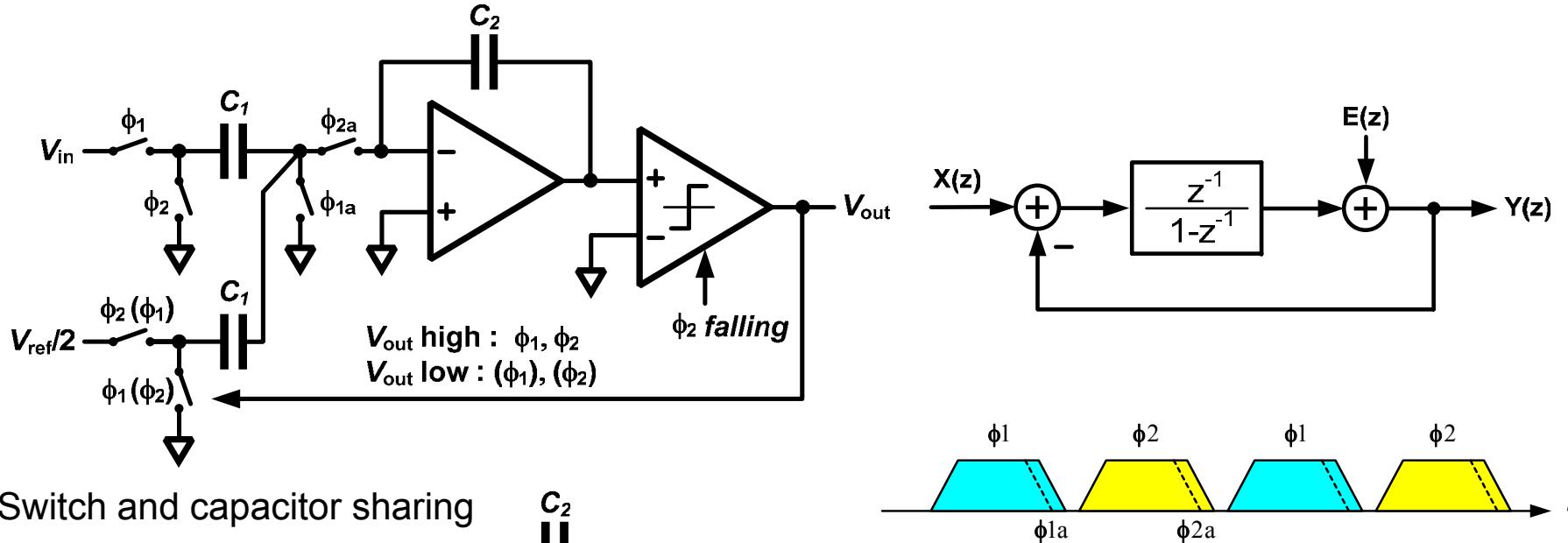


- Given that a 1-bit A/D converter has a 6-dB SNR what sample rate is required to obtain a 96-dB SNR (or 16-bit) if $f_B = 25\text{kHz}$ for straight oversampling as well as first- and second-order noise shaping?

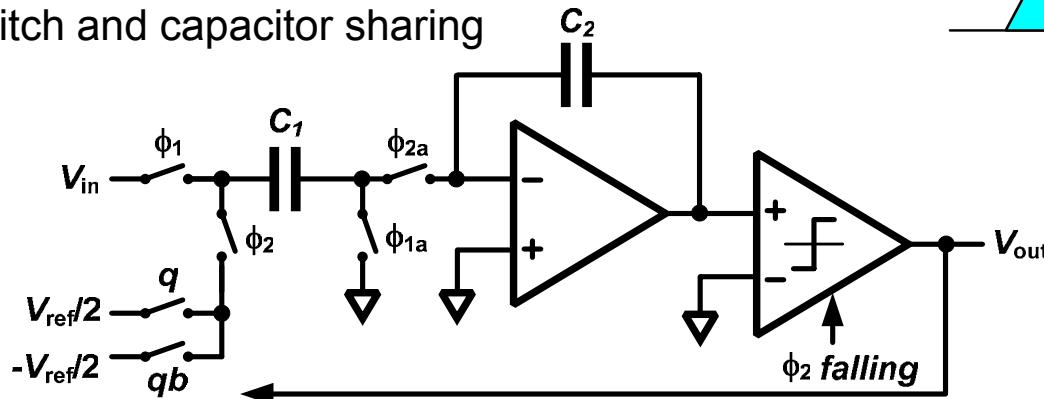
- Without noise shaping $\rightarrow \approx 50,000\text{GHz}$ (!)
- First-order noise shaping $\rightarrow \approx 73\text{MHz}$
- Second-order noise shaping $\rightarrow \approx 5.7\text{MHz}$

Implementation

- Switched-Capacitor Circuits for First-order $\Delta\Sigma$ ADC



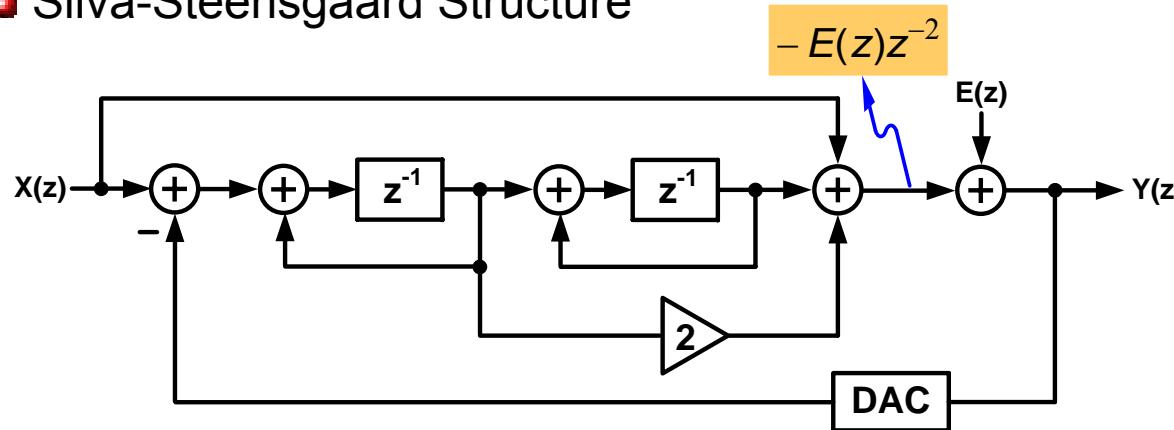
- Switch and capacitor sharing



► Scaling of feedback relative to input is not allowed

Alternative Second-Order Delta-Sigma Modulators

- Silva-Steensgaard Structure



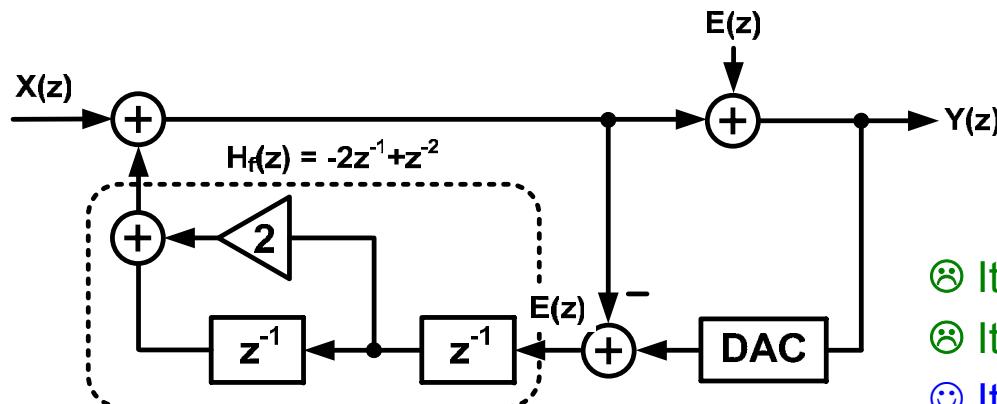
It is advantage if the modulator is the input stage of MASH structure

- Direct feedforward path
- Single feedback path

$$Y(z) = X(z) + (1 - z^{-1})^2 E(z)$$

😊 The loop filter do not need to process signal, the requirements on its linearity may be reduced

- Error-Feedback Structure



😦 ENOB < 10-bit for single-bit ADC

$$Y(z) = X(z) + E(z)[1 + H_f(z)]$$

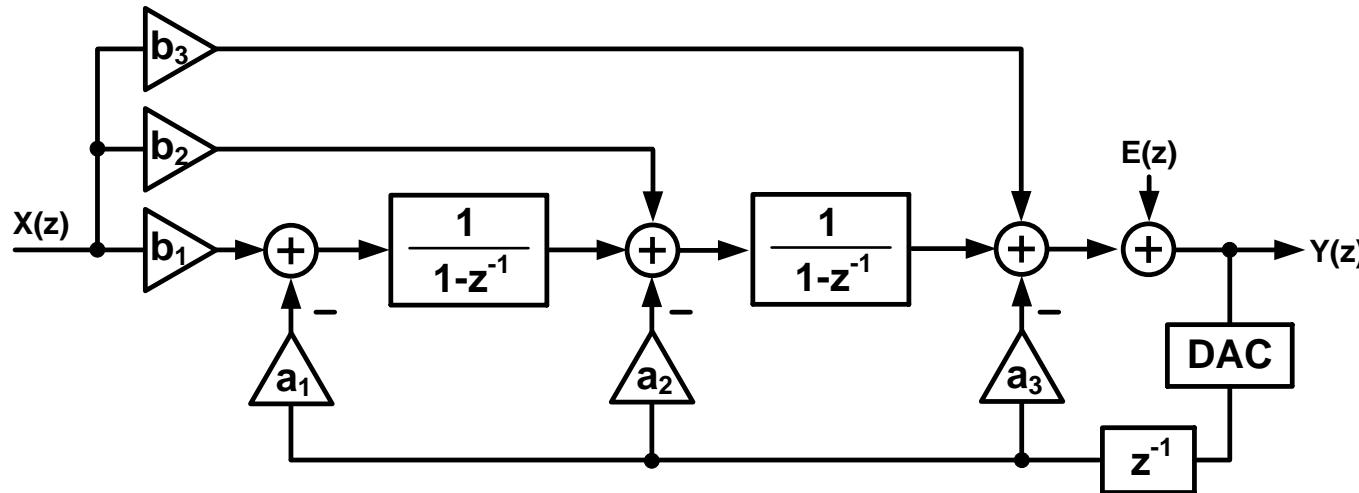
$$NTF(z) = (1 - z^{-1})^2 = [1 + H_f(z)]$$

$$\Rightarrow H_f(z) = -2z^{-1} + z^{-2}$$

- 😦 It is impractical for analog $\Delta\Sigma$ loops
- 😦 It is very sensitive to variations of its parameters
- 😊 It is very useful in the digital loops required in $\Delta\Sigma$ DACs

Alternative Second-Order Delta-Sigma Modulators

- Generalized Second-Order Structures



$$STF(z) = \frac{B(z)}{A(z)} \quad NTF(z) = \frac{(1 - z^{-1})^2}{A(z)}$$

STF has two zeros and single pole at $z=0$ and two nonzero poles

$$B(z) = b_1 + b_2(1 - z^{-1}) + b_3(1 - z^{-1})^2$$

$$A(z) = 1 + (a_1 + a_2 + a_3 - 2)z^{-1} + (1 - a_2 - 2a_3)z^{-2} + a_3z^{-3}$$

☺ A “free” second-order FIR pre-filter incorporated into ADC ($a_1=a_2=1, a_3=0$)

☺ More flexibility for enhancing stability and improving dynamic range

Design Methodology for Stability

Integrator Output Swing

- Too large output swing makes the internal state unfeasible

► Coefficients scaling (Signal scaling)

Root Locus

$$STF(z) = \frac{k}{z^2 + (-2 + \beta + k\gamma)z + (1 + k + \alpha - \beta - k\gamma)}$$

$$NTF(z) = \frac{z^2 + (\beta - 2)z + (1 + \alpha - \beta)}{z^2 + (-2 + \beta + k\gamma)z + (1 + k + \alpha - \beta - k\gamma)}$$

► α moves the **zeros** of the NTF along the unit circle for optimum noise shaping

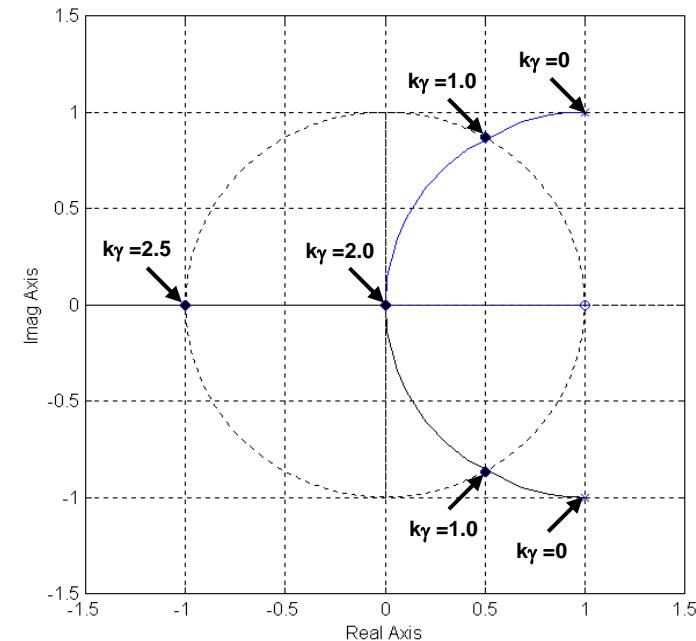
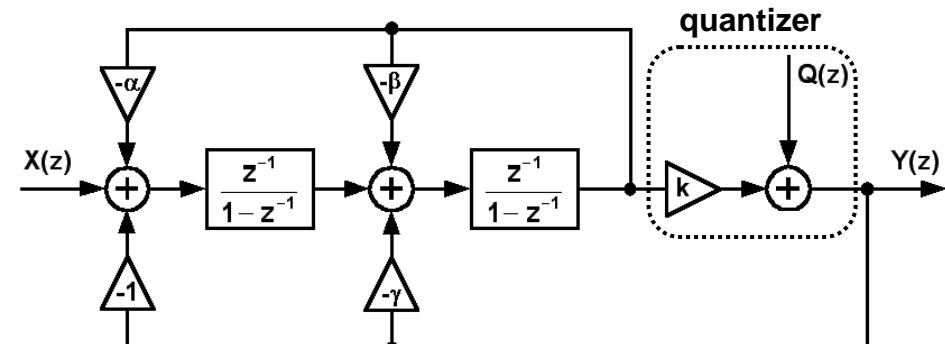
► γ adjusts the **poles** of the NTF to obtain a more stable modulator

► β models the effects of the finite opamp gain

► For $\alpha = 0, \beta = 0$

$$NTF(z) = \frac{(z-1)^2}{z^2 + (k\gamma - 2)z + (2 - k\gamma)}$$

► Utilize the root locus to determine the feedback gain γ



Optimal Second-Order Modulators

- Optimal Topology
- Optimize NTF

- In the passband for high values of OSR

$$|NTF(z)| = \left| \frac{(1-z^{-1})^2}{A(z)} \right| \approx \frac{1}{|A(1)|} \omega^2$$

- Shifting the NTF zeros from $z = 1$ to $z = e^{\pm j\alpha}$

$$|NTF(z)| \approx \frac{1}{|A(z)|} (\omega - \alpha)(\omega + \alpha) = \frac{1}{|A(z)|} (\omega^2 - \alpha^2)$$

$A(z) \approx A(1)$ is assumed

- A measurement of the in-band noise

$$I(\alpha) = \int_0^{\omega_B} (\omega^2 - \alpha^2)^2 d\omega$$

$$\Rightarrow \frac{dI(\alpha)}{d\alpha} = 0$$



$$\alpha_{opt} = \frac{\omega_B}{\sqrt{3}}$$

SNR is improved by $10\log_{10}(9/4)=3.5\text{dB}$

- $I(0)/I(\alpha_{opt})=9/4$

→ SNR improve 3.5 dB

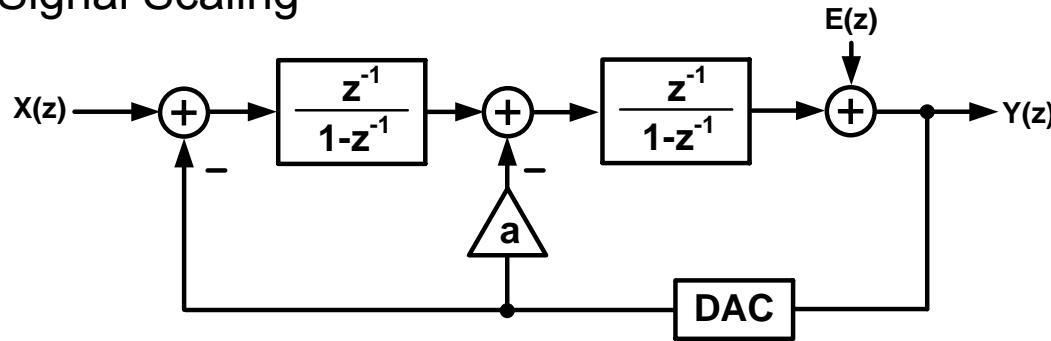
- The highest SNDR

- The pole-zero plot & its SNDR curve – exhaustive research
 - Find the optimal denominator of NTF



Signal Scaling

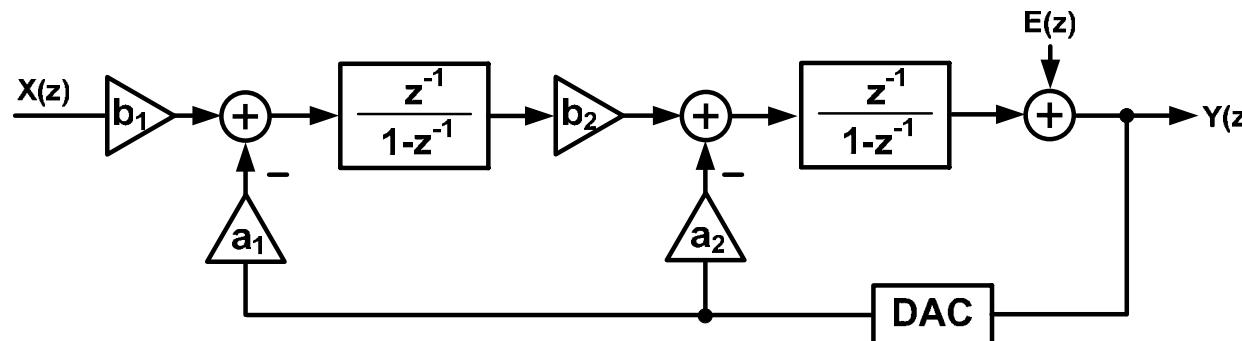
- Signal Scaling



choose $a = 2$

■ Output swing of integrator1 = $\pm \zeta_1$

■ Output swing of integrator2 = $\pm \zeta_2$ feedback reference = $\pm \delta$



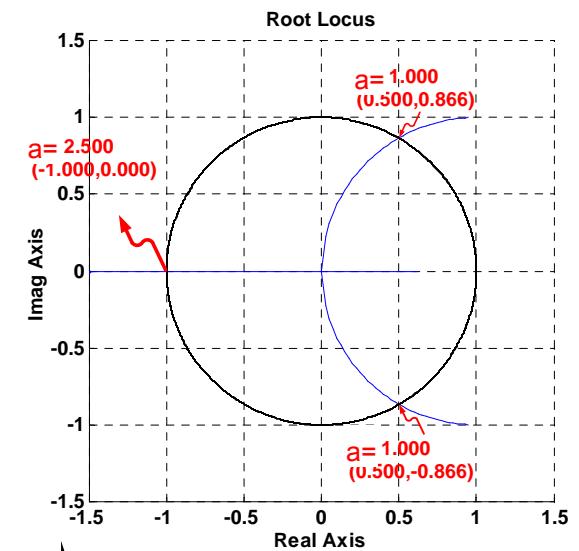
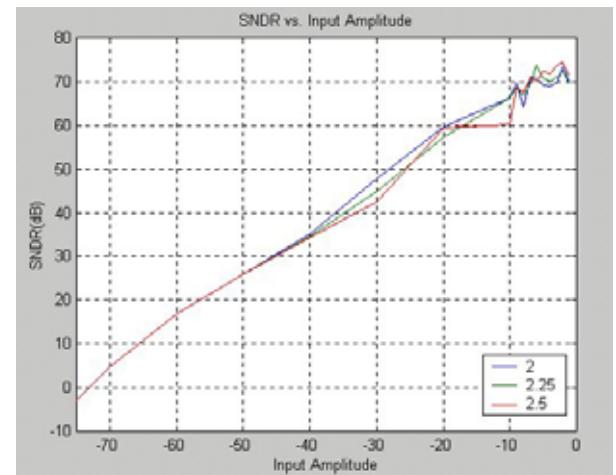
η : a fraction of feedback reference

$$a_1 \leq \frac{\delta \times \eta}{\zeta_1}$$

from the standpoint of circuit noise, power consumption and die area → choose $a_1=b_1$

$$a_2 \leq \frac{\delta \times \eta}{\zeta_2}$$

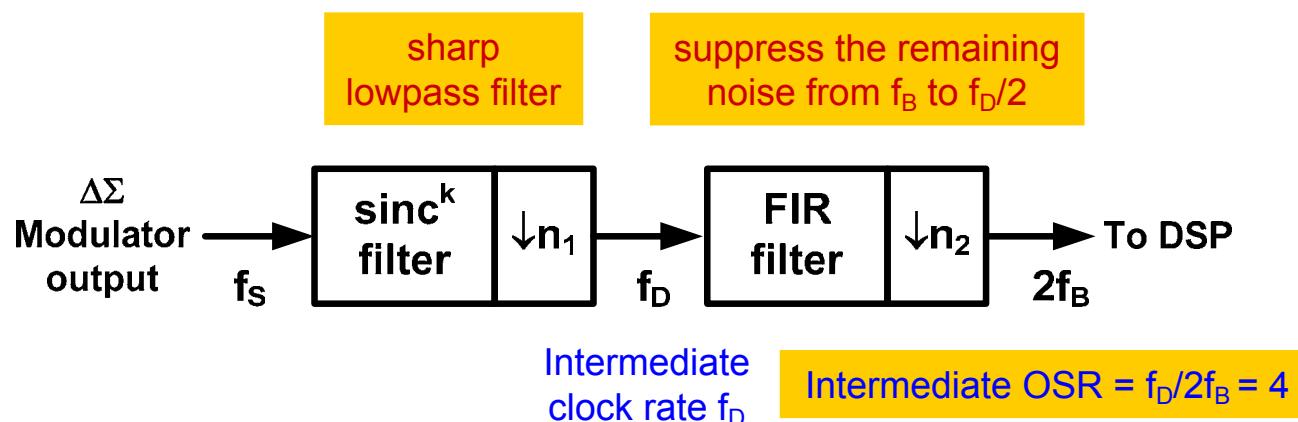
$$\frac{a_2}{a_1 b_2} = a = 2$$



Decimation Filter

- Two-Stage Decimation Filter

- Lowpass filtering
- Down sample
 - It is efficient for high-resolution applications



- The filter should cut off at a feaster rate around f_B than the NTF of the $\Delta\Sigma$ modulator rises
 - Very little out-of-band noise is left unsuppressed around f_B
- Gain response should be flatter around f_s/OSR and its harmonics than the NTF is around dc
 - $K=L+1$ (sinc^k filter for L^{th} -order modulator)

Decimation Filter

- The Sinc Filter

- A running average of the input data stream $y(n)$

$$w(n) = \frac{1}{N} \sum_{i=0}^{N-1} y(n-i)$$

- The z-domain transfer function

$$H_1(z) = \frac{1}{N} \frac{1-z^{-N}}{1-z^{-1}}$$

- The frequency response $|H_1(z)| = \left| \frac{\text{sinc}(Nf)}{\text{sinc}(f)} \right|$

- ▶ Gain ≈ 1 at and near $f=0$
- ▶ Gain ≈ 0 near fs/N and its harmonics [$\text{sinc}(f) \equiv \sin(\pi f)/(\pi f)$]

► Choose $N=OSR$ to attenuate the noise due to down sampling by N

- The output noise of first-order noise shaping

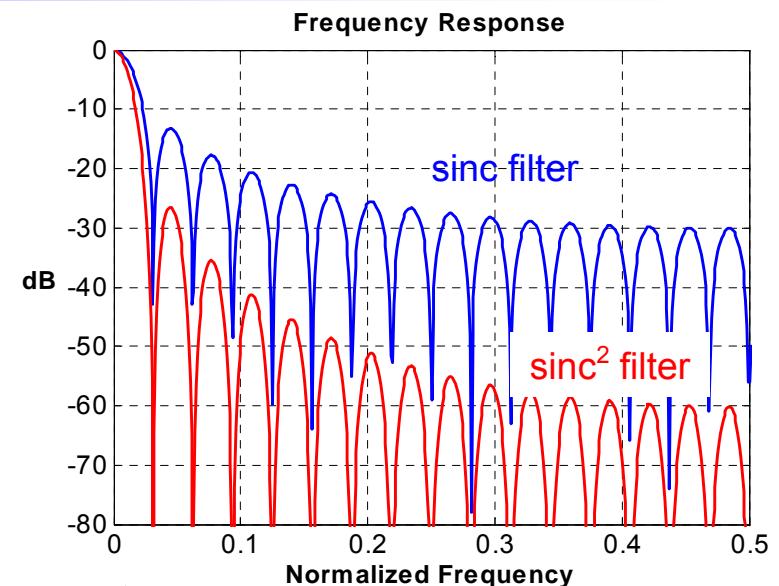
$$Q_1(z) = H_1(z)NTF(z)E(z) = \frac{1}{N}(1-z^{-N})E(z)$$

- ▶ In the time domain

$$q_1(n) = \frac{1}{N}[e(n) - e(n-N)]$$

- ▶ The resulting quantization noise power

$$\sigma_{q_1}^2 = \frac{2\sigma_e^2}{N^2} \quad (\text{rms noise power } \sigma_e^2)$$



- The noise power of the sinc^2 filter

$$\sigma_{q_2}^2 = \frac{2\sigma_e^2}{N^3}$$

a sinc^{L+1} LPF is sufficient for an L^{th} -order loop

N times less effective than the ideal LPF

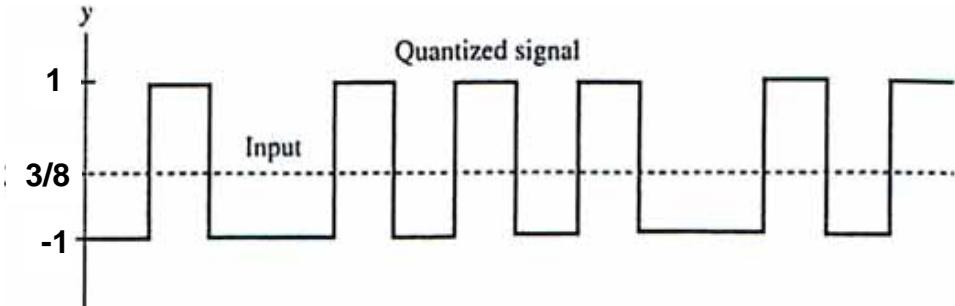


Tones in $\Delta\Sigma$ Modulators

● Pattern Noise

■ Idle Tones

- ▶ With a dc signal input
 - ▶ The output oscillates repetitively
- ▶ Is decided by **output pattern**



▶ Example

- ▶ A dc level of $1/3$ to a first-order $\Delta\Sigma$ modulator having 1-bit quantizer form $\{1,1,-1,\underline{1},\underline{1},-1,\dots\}$
 - ◆ The output power is concentrated at dc and $fs/3$
 - ◆ The post low-pass filter is required to eliminate the high-frequency component
- ▶ A dc level of $3/8$ to a first-order $\Delta\Sigma$ modulator having 1-bit quantizer form $\{1,1,-1,1,1,-1,1,1,-1,1,1,-1,1,1,1,-1,1,1,-1,\dots\}$
 - ◆ The period of this pattern is 16 cycles
 - ◆ The output power is concentrated at dc, $fs/16$
 - ◆ The post low-pass filter will *not* attenuate the idle tone power at $fs/16$ with an OSR of 8

Tones in $\Delta\Sigma$ Modulators

- Second-Order Modulator 1-bit Quantizer

- Step size $\Delta=2$ for output levels {1, -1}

A dc level of 1/256 is applied

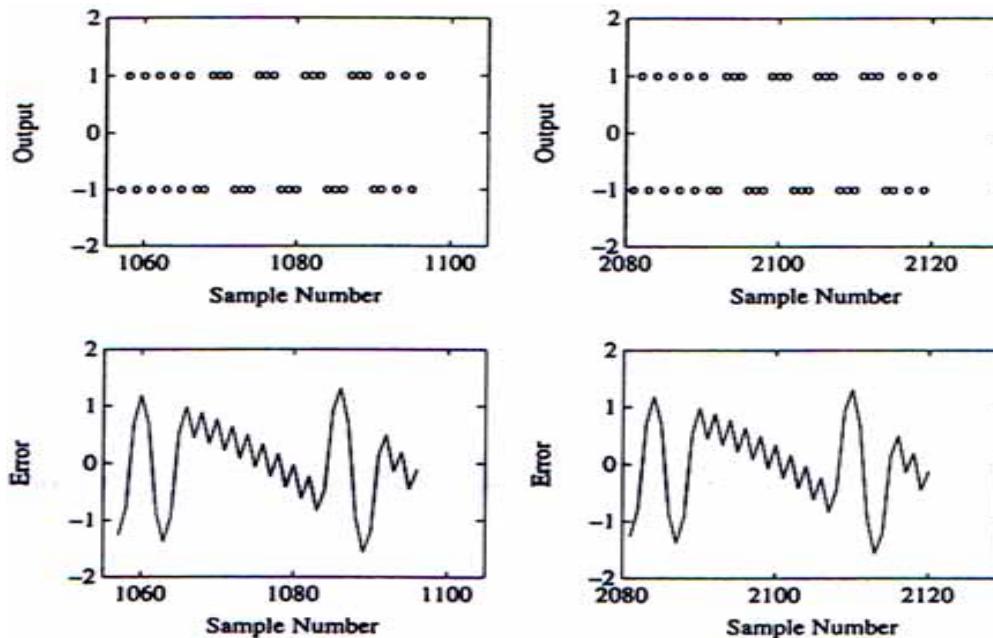
- The power spectrum is concentrated at

$$\textcolor{red}{\rightarrow} f_0 = \frac{n f_s |A_{dc}|}{2\Delta} \quad n = \{0, 1, 2, \dots\}$$

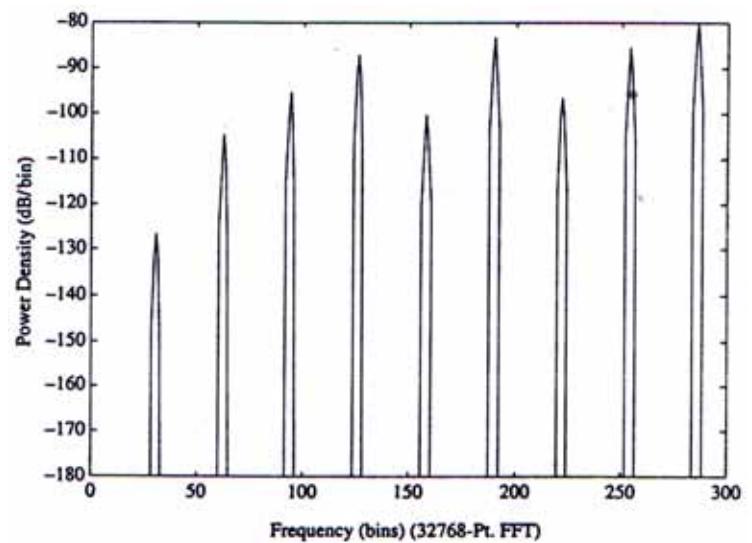
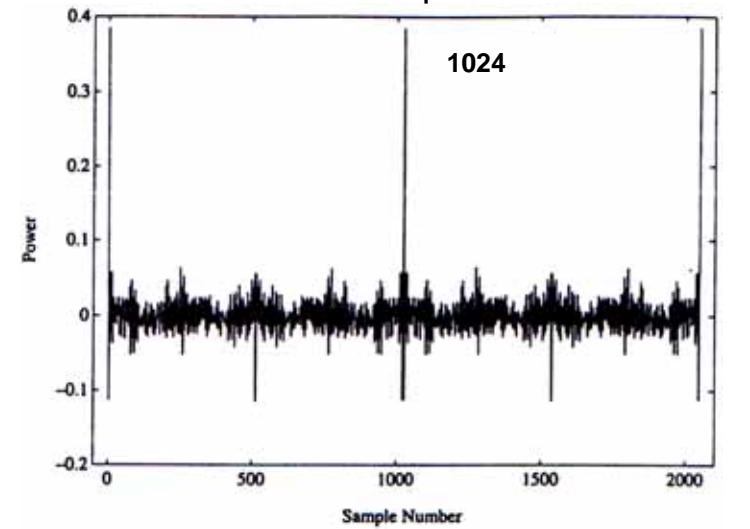
$|A_{dc}|$: the magnitude of the dc input level

- Other parameters affect the tonal behavior

$\textcolor{blue}{\rightarrow}$ Finite-gain amplifier, switch charge injection, ...



Autocorrelation of quantization error



Higher-Order Delta-Sigma Modulators

Department of Electrical Engineering

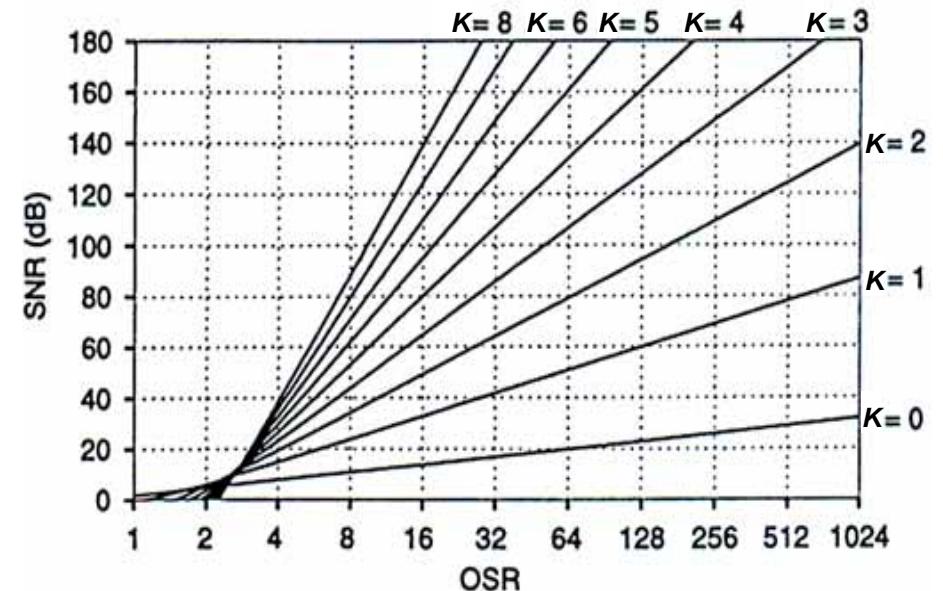
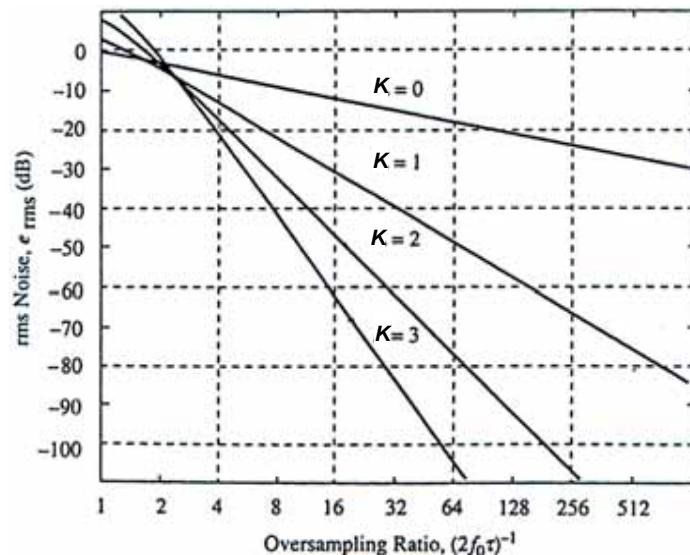
Higher-Order Noise-Shaping

- K-order Noise-Shaping

$$\text{NTF}(z) = (1 - z^{-1})^K$$

$$|\text{NTF}(z)|_{z=e^{j2\pi f}} \approx [2 \sin(\frac{\pi f}{f_s})]^K$$

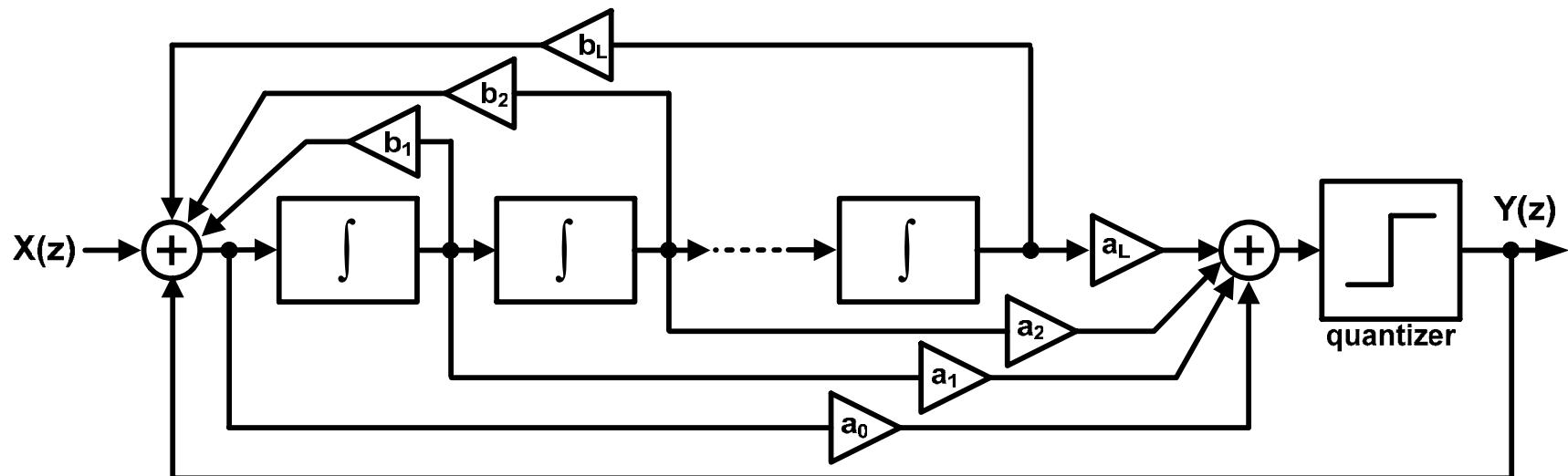
- The quantization noise power $P_n \approx (\frac{\Delta^2}{12}) \frac{\pi^{2K}}{2K+1} (\frac{1}{\text{OSR}})^{2K+1}$
- The maximum SNR = $6.02 \times B + 1.76 + 10 \log(\frac{2K+1}{\pi^{2K}}) + (20K+10) \log(\text{OSR})$
 - ➡ Doubling the OSR gives an SNR improvement by $3(2K+1)\text{dB}$ or $(K+1/2)\text{bits/octave}$
- Larger order cause a larger out-of-band gain of the NTF



Single-Loop Topology

- Interpolative $\Delta\Sigma$ Modulator

- Additional poles and zeros are introduced in the interest band
- Refined coefficients are required for this modulator makes it is sensitive to the component variation
- There is a stability problem in the modulators

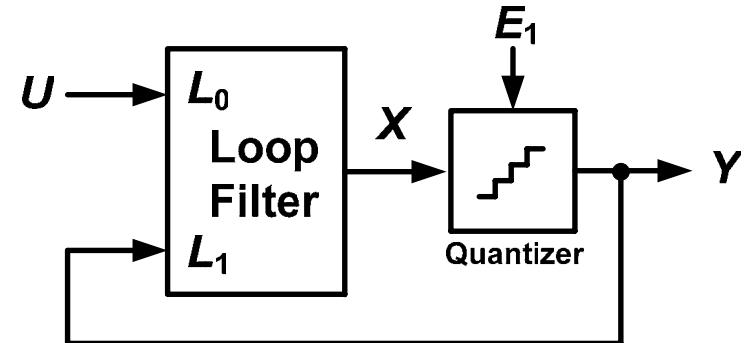


W. L. Lee and C. G. Sodini, "A Topology for Higher-Order Interpolative Coders,"
in Proc. of IEEE International Symposium on Circuits and Systems, pp. 459-462, 1987

Higher-Order Single-Quantizer Modulators

Motivation

- Strong noise shaping - High SNR
- Less prone to idle tones
- Simple circuit design
 - ➡ Issue of stability



Loop Topologies

- A universal $\Delta\Sigma$ structure

$$\Rightarrow Y(z) = STF(z) \cdot U(z) + NTF(z) \cdot E(z)$$

$$L_0(z) = \frac{STF(z)}{NTF(z)} \quad L_1(z) = 1 - \frac{1}{NTF(z)}$$

$$\blacktriangleright \text{Signal transfer function (STF)} : STF(z) = \frac{L_0(z)}{1 - L_1(z)}$$

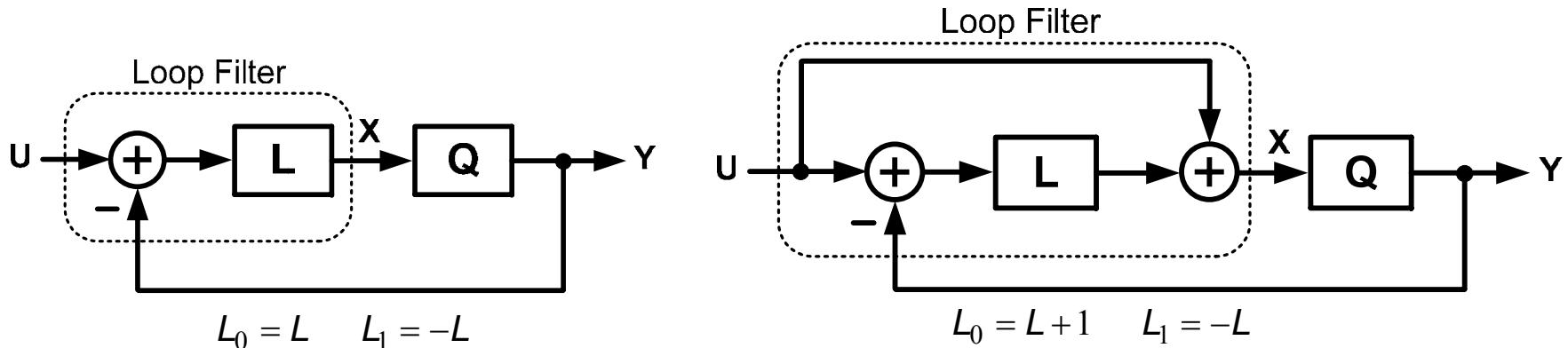
$$\blacktriangleright \text{Noise transfer function (NTF)} : NTF(z) = \frac{1}{1 - L_1(z)}$$

\blacktriangleright poles of L_1 = zeros of NTF

Higher-Order Single-Quantizer $\Delta\Sigma$ Modulators

- Single Feedback Topology

- Loop function along with the quantizer determines all properties
 - Stability, signal and noise transfer function



- Single Feedback Topology with a Feedforward Path

- The input to the filter

$$U - Y = U - (STF \cdot U + NTF \cdot E) = -\frac{E}{1+L} \quad (STF(z) = \frac{L+1}{1+L} = 1)$$

- No longer contains the signal
- Only quantization noise
 - The linearity of loop filter need not be very high

Example for Stability

- The Gain k of the Quantizer

$$k = \frac{\langle y, x \rangle}{\langle x, x \rangle} = \frac{E[|x|]}{E[x^2]} \quad \text{where } y(n) = \text{sign}[x(n)]$$

- The modified noise transfer function with new k

$$NTF_k(z) = \frac{1}{1 - kL_1(z)} = \frac{NTF_1(z)}{k + (1 - k)NTF_1(z)}$$

► The natural mode of linear model = the roots of the denominator of $NTF_k(z)$

- Root Locus of a sixth-order modulator

► $k=0$

► These roots coincides with the zeros of $NTF_1(z)$

► $k=1$

► These roots coincides with the poles of $NTF_1(z)$

► $k < 0.572$

► Unstable

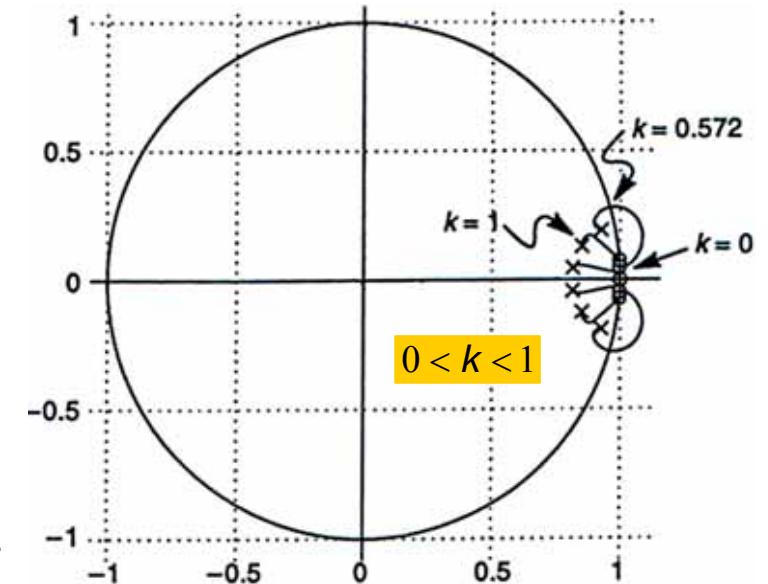
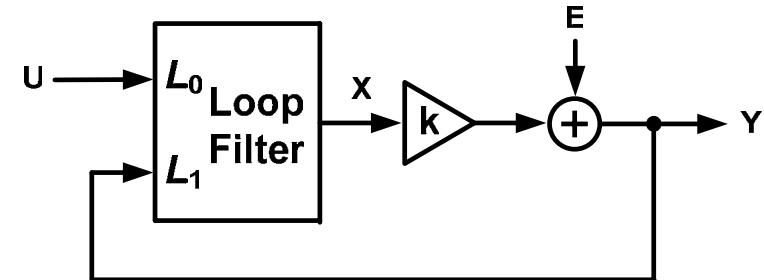
► **Runaway state**

► Large input to quantizer $\rightarrow k$ falls

\rightarrow feedback small \rightarrow larger quantizer input $\rightarrow \dots$

- The input to the quantizer **cannot** be too large

$$X(z) = STF(z) \cdot U(z) + (NTF(z) - 1) \cdot E(z)$$



$$NTF(z)_{peak} = (1 - z^{-1})^n \Big|_{z=-1} = 2^n$$

Design Methodology for Stability

- For High-Order Single-Loop Modulators

- Very large high-frequency noise-shaping gain

- Overloading and instability $NTF(z) = (1 - z^{-1})^N$

- The idling waveform at the comparator input becomes large

- Low comparator gain

- Reduction of input

- Modify the differentiating response

- Adding $D(z)$

$$NTF(z) = \frac{(z-1)^N}{D(z)}$$

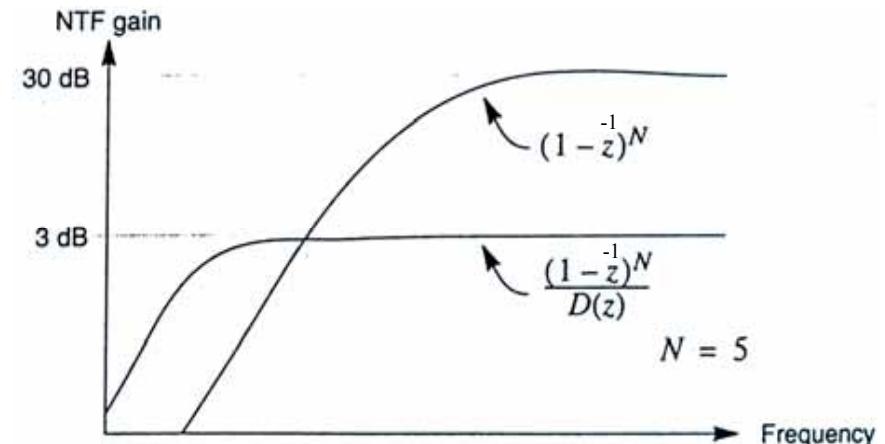
- Flatten the high-frequency portion of $H(z)$

- Ex. Butterworth alignment of the poles can be introduced to $NTF(z)$

- A maximally flat high-frequency region of $NTF(z)$ can be obtained

- The poles of Butterworth NTF are relatively low Q

- Less susceptible to oscillations for a signal with the same frequency as poles



Stability Considerations

- Bounded input

- The stable input range is usually a few dB below the full-scale range of the feed back DAC
 - The loss in range caused from the nonlinear effects of quantizer overload

- Single-Bit Modulators

- A rule of thumb

- Lee's criterion

- A binary $\Delta\Sigma$ modulator with an $NTF(z) = H(z)$ is likely to be **stable** if $\max_{\omega} |H(e^{j\omega})| < 1.5$

- Infinite-norm of H

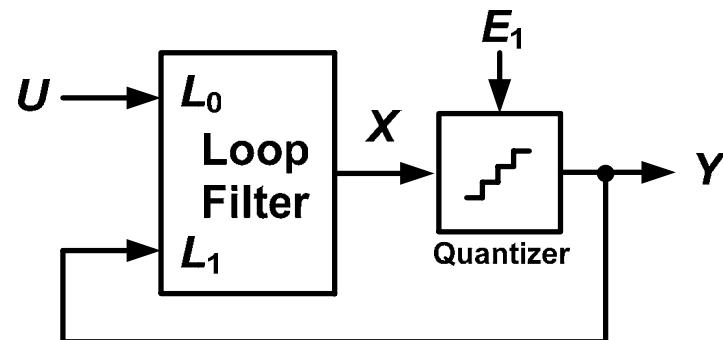
- The maximum gain of NTF over all frequencies $\max_{\omega} |H(e^{j\omega})| = \|H\|_{\infty}$

- 3rd- or 4th-order modulators

- $\bullet \|H\|_{\infty} = 1.5 \sim 2$

- 7th-order↑ modulators

- $\bullet \|H\|_{\infty} < 1.4$

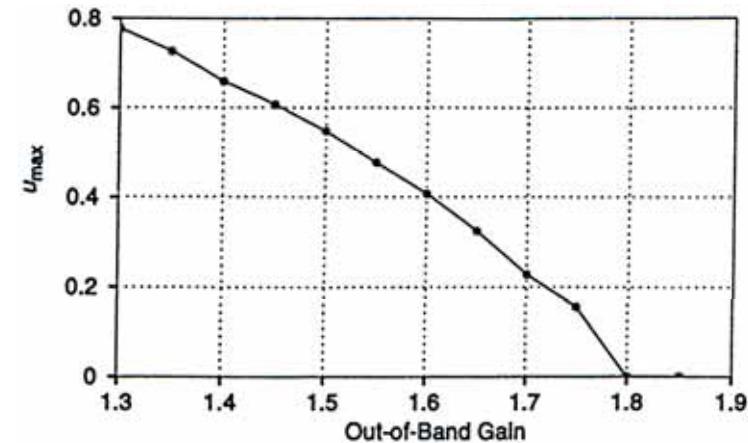
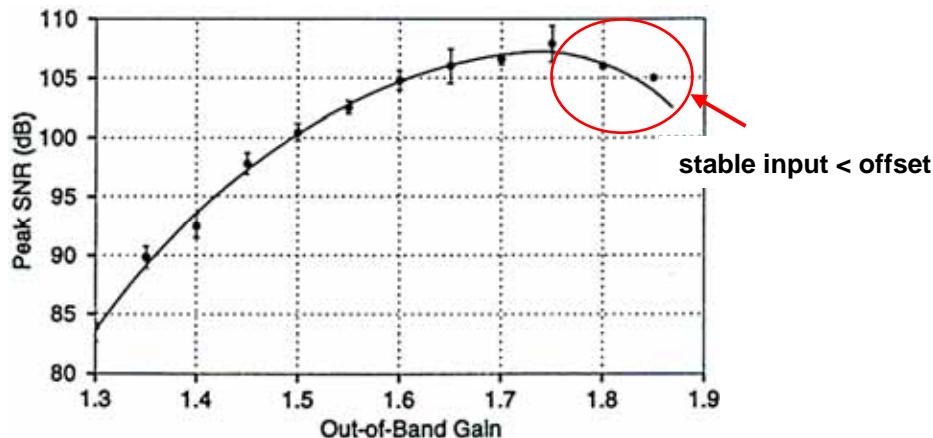


Design Methodology for Stability

Design Trade-offs

- Ex. A sixth-order modulator operated at OSR=40

- Larger out-of-band gain of NTF without causing unstable
 - Higher peak SNR
 - ◆ Decrease in the stable input range
 - ◆ Gain=1.75, peak SNR=107, stable input < 0.2



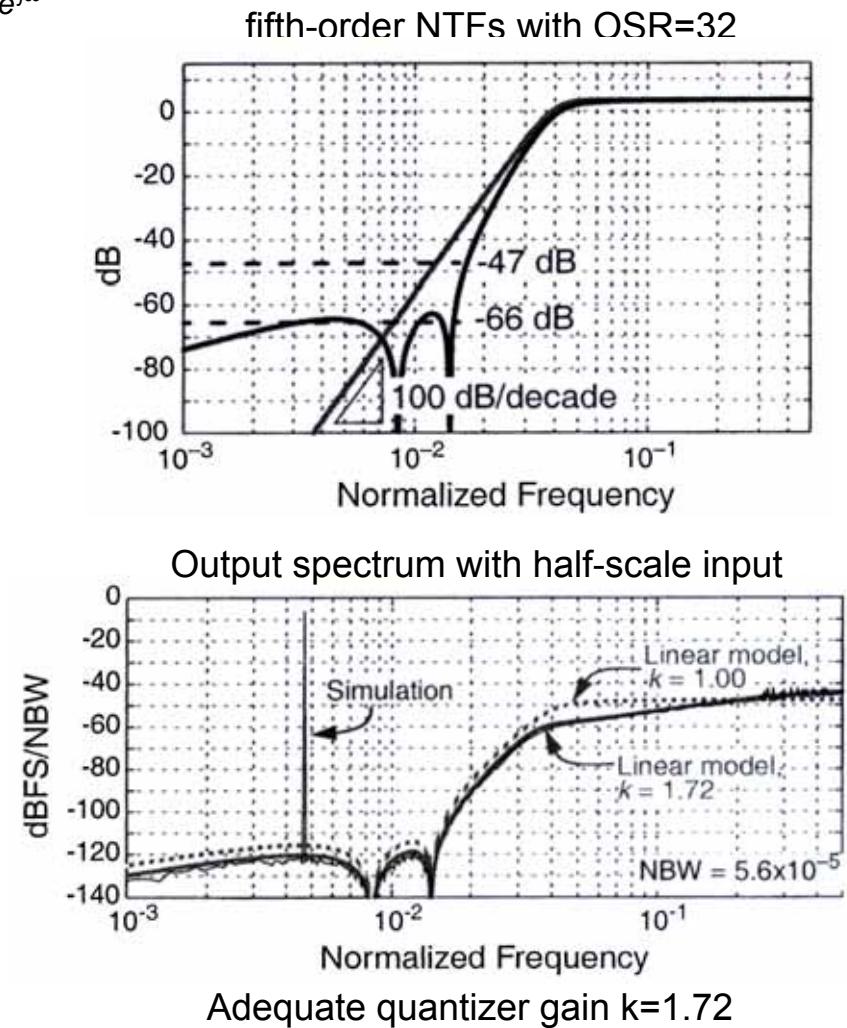
- Maximum specified input signal range: 50%~80% of effective comparator feedback signal
 - <50%: high NTF gain
 - Low stability
 - >80%: NTF is not very aggressive
 - Lose some benefits of higher-order loop

Optimization of the NTF Zeros

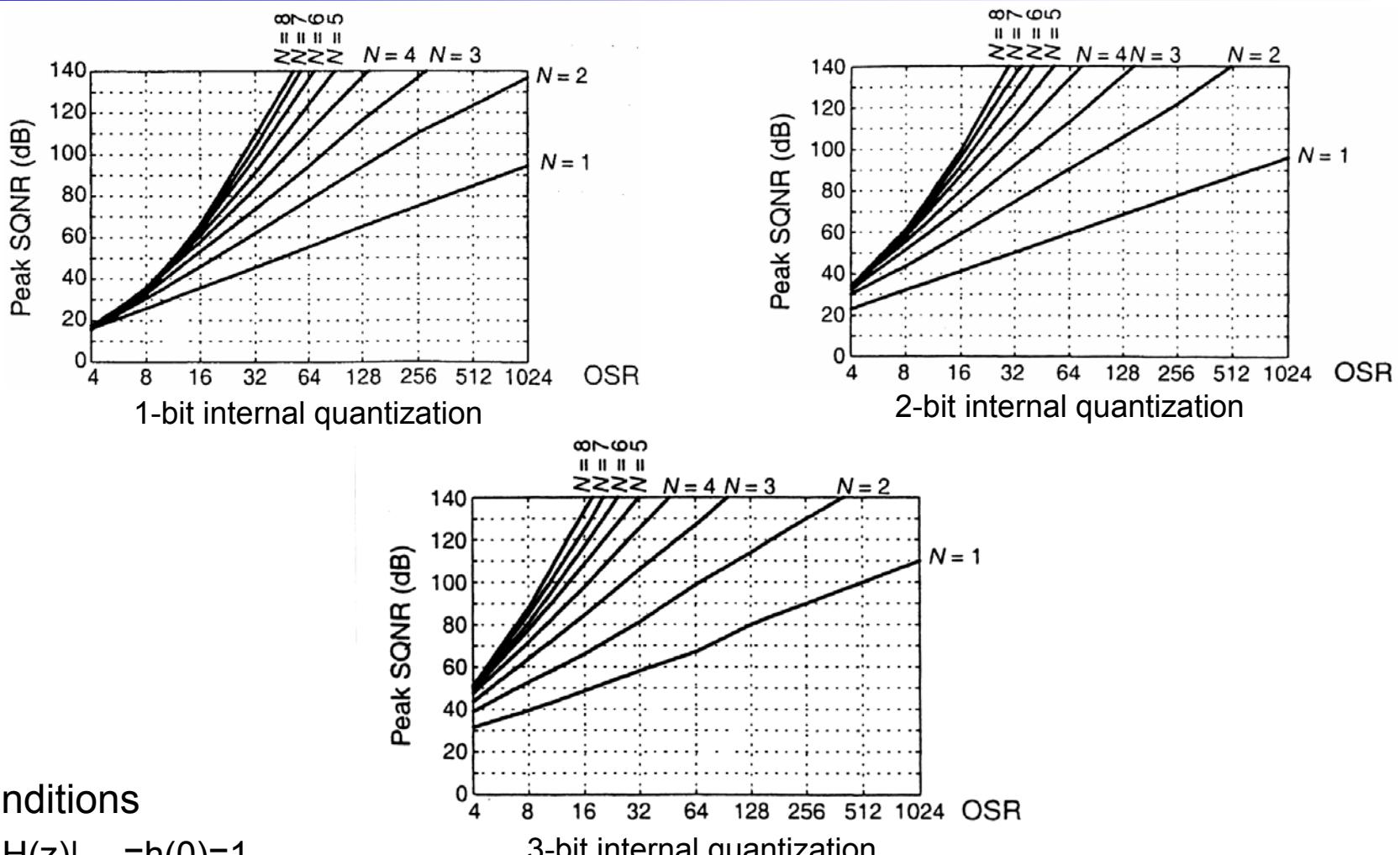
- Spread zeros to reduce the total noise power in the signal band
- Minimize the normalized noise power $\int |NTF(z)|_{z=e^{j\omega}} d\omega$
 - Zero placement for minimum in-band noise

N	zero locations, normalized to ω_B	SQNR improvement
1	0	0 dB
2	$\pm 1/(\sqrt{3})$	3.5 dB
3	$0, \pm \sqrt{3}/5$	8 dB
4	$\pm \sqrt{3}/7 \pm \sqrt{(3/7)^2 - 3/35}$	13 dB
5	$0, \pm \sqrt{5/9} \pm \sqrt{(5/9)^2 - 5/21}$	18 dB
6	$\pm 0.23862, \pm 0.66121, \pm 0.93247$	23 dB
7	$0, \pm 0.40585, \pm 0.74153, \pm 0.94911$	28 dB
8	$\pm 0.18343, \pm 0.52553, \pm 0.79667, \pm 0.96029$	34 dB

- For even-order NTF
 - Double zero at $z=1$ for perfect dc suppression
 - Reproduction of the dc input
 - Reduce the probability of low-frequency tones



Optimization of the NTF Poles



Conditions

- $H(z)|_{z=\infty} = h(0) = 1$
- The locations of the poles should be based on stability conditions (Lee's Rule)
- The magnitude of $H(z)$ should be flat over the signal band

Steps of Finding the Complete NTF

- Choose the **order N** of modulator by specified **SNR & OSR** from the above figures
 - Finding **zeros** of the NTF
- Choose the NTF approximation type
 - Butterworth highpass
 - Inverse Chebyshev highpass
 - Maximally-flat all-pole highpass
- Place the **cutoff frequency ω_{3dB}** of the NTF slightly above the edge of the signal band

$$H(z) = \prod_{i=1}^N \frac{z - z_i}{z - p_i}$$

- Predict the **stability** of the modulator (Lee's Rule) $|H(z)|_{z=-1} = \prod_{i=1}^N \frac{z - z_i}{z - p_i} < 1.5$

- Confirm the stability estimation under other practical conditions

- **Unstable**

- ▶ Shift the poles away from $z=-1$ (reducing the cutoff frequency ω_{3dB})
 - ▶ Reduce the peak NTF gain
 - ▶ Enhance the stability

- **Stable**

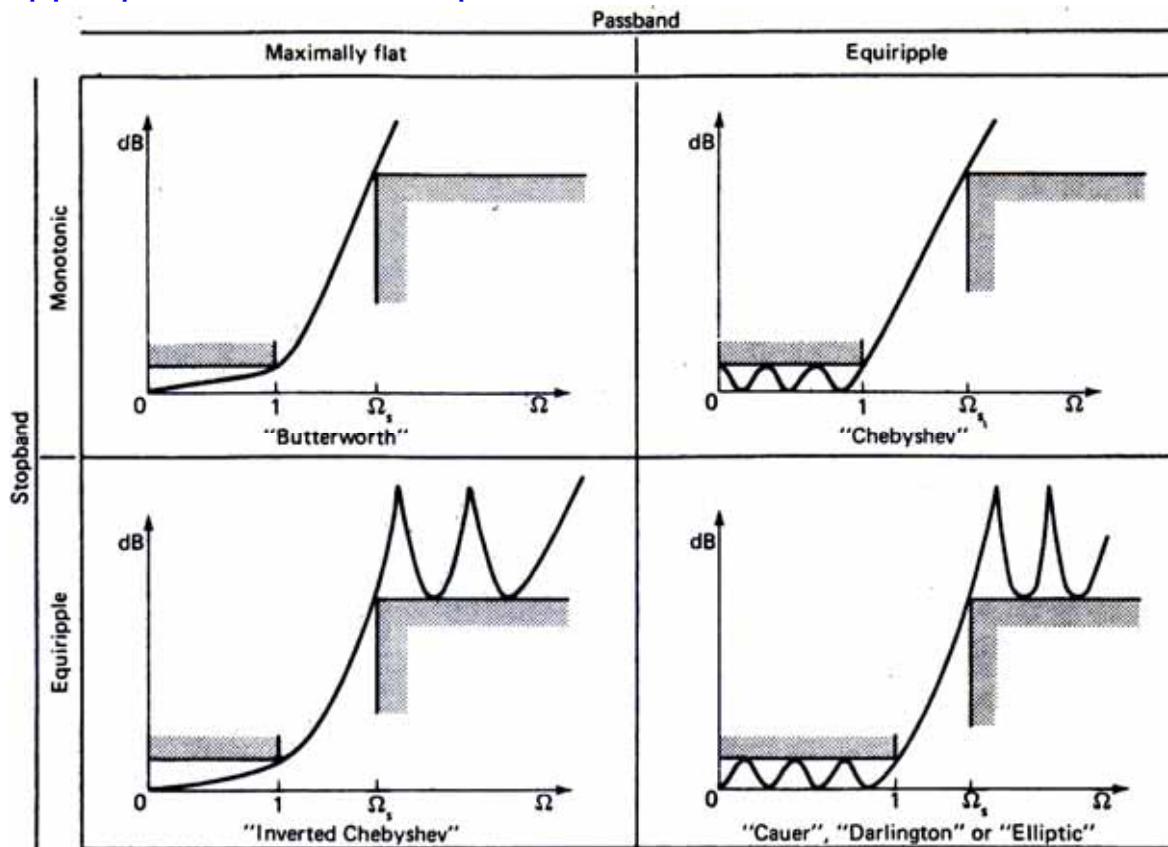
- ▶ More aggressive NTF (increasing the cutoff frequency ω_{3dB})
 - ▶ Repeating the stability tests – iterated until the maximum SNR is approached



NTF Approximation Types for Higher-Order Single-Bit Modulators

- Four Filter Types

- Butterworth – maximally flat passband
- Chebyshev – equiripple passband and monotonically increasing attenuation stopband
- Inver Chebyshev – maximally flat passband and equiripple stopband
- Elliptic – equiripple passband and stopband

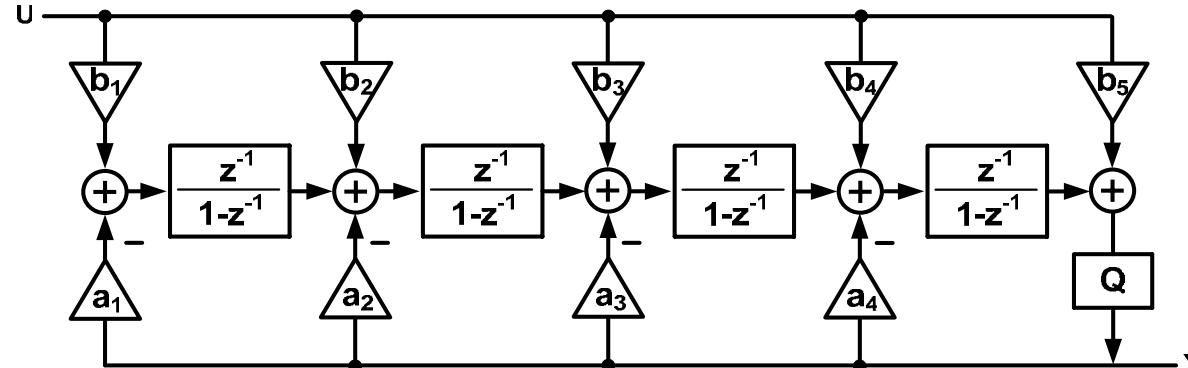


Loop Filter Architectures

- Loop Filters with Distributed Feedback and Input Coupling

■ Cascaded Integrators with distributed FeedBack as well as distributed input coupling (CIFB)

► Cascade N delaying integrators ($N = 4$)



$$NTF(z) = H(z) = \frac{(z-1)^N}{D(z)} \quad \text{where} \quad D(z) = a_1 + a_2(z-1) + a_3(z-1)^2 + \dots + a_N(z-1)^{N-1} + (z-1)^N$$

$$STF(z) = \frac{b_1 + b_2(z-1) + b_3(z-1)^2 + \dots + b_{N+1}(z-1)^N}{D(z)}$$

► All zeros of NTF lie at $z=1$ (dc)

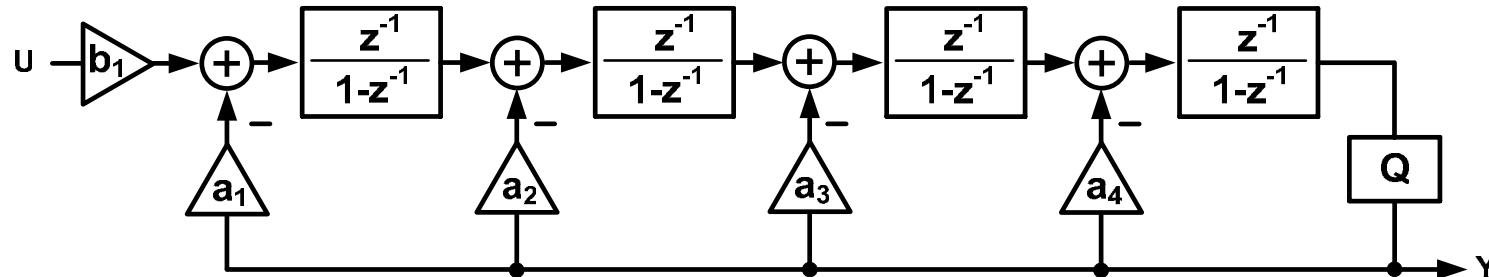
- a_i can introduce nonzero poles for stable operation
- The poles are shared

◆ Ex. If NTF is designed as a fifth-order Butterworth high-pass function
STF would be a fifth-order Butterworth low-pass

- b_i determine the zeros of STF – coefficient matching with the specified STF

CIFB

- The case all $b_i = 0$ except b_1



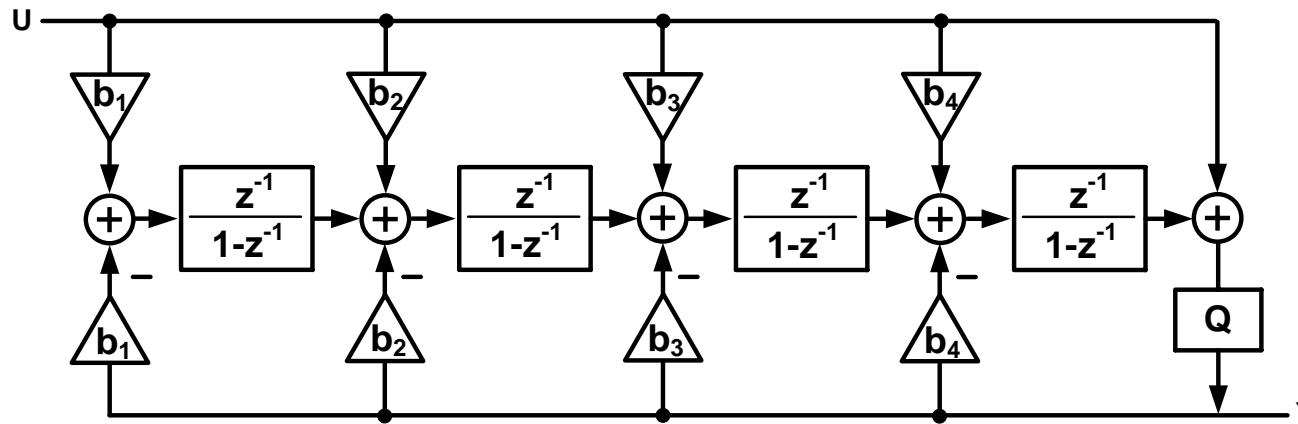
$$STF(z) = \frac{b_1}{D(z)}$$

$$NTF(z) = H(z) = \frac{(z-1)^N}{D(z)}$$

- All zeros of STF lie at $z=\infty$
- $D(z)$ should be flat in the signal band
 - ▶ Butterworth filter is chosen
 - ◆ STF flatness does not yield significant peaking
- Significant amount of input signal and filtered quantization error contained in each integrator output
 - ▶ High dc gain of opamp required
 - ▶ To keep reasonable output swing
 - ◆ Larger circuits
 - ◆ More power hungry

CIFB

- The case $b_i = a_i$ for $i \leq N$, $b_{N+1} = 1$



➡ STF=1

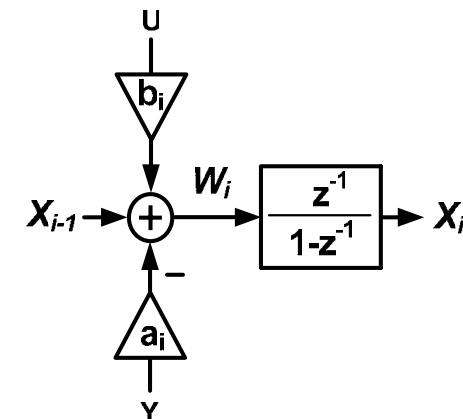
$$Y(z) = U(z) + H(z)E(z)$$

➡ The input signal to the i^{th} integrator

$$W_i(z) = X_{i-1}(z) - a_i Y(z) + b_i U(z) = X_{i-1}(z) - a_i H(z)E(z)$$

➡ Since U is absent

▶ Process quantization noise only

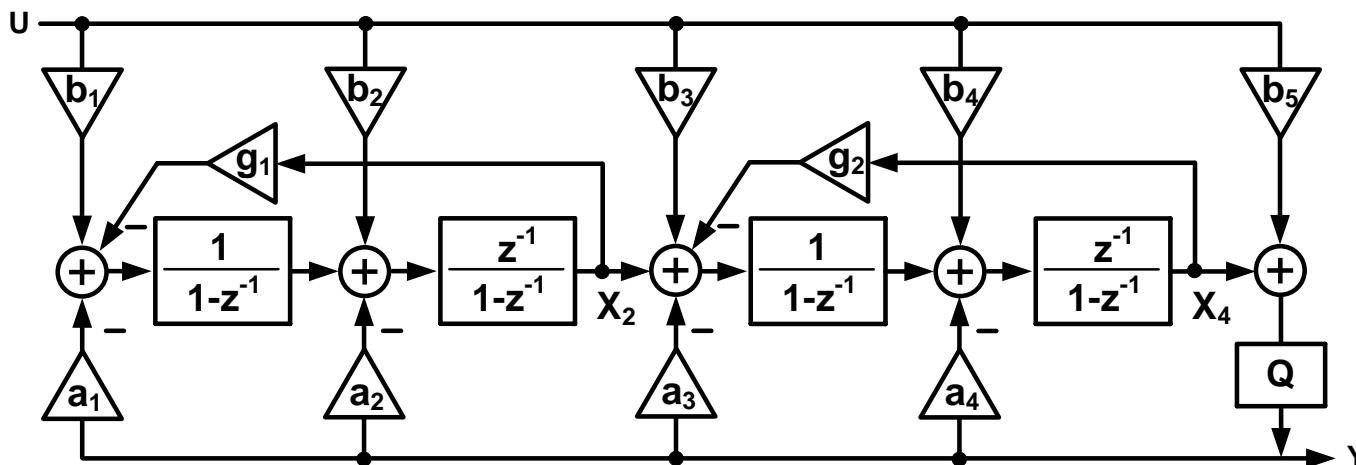


- ☺ Reduced output swing at the output of the integrators (especially for m-bit quantizer)
less extensive dynamic range scaling
- ☺ Unavoidable nonlinearities of the integrators does not introduce harmonic distortion into output

Cascade of Resonators with distributed FeedBack (CRFB)

- Modified Interpolative $\Delta\Sigma$ Modulators

- Local feedback paths around pairs of integrators – resonators
 - One of the integrator needs to be a delay-free one for stabilizing resonator¹
 - Move the zeros of NTF to finite positive frequencies for much better SNR
 - Exhibit one or more notches in interest band to reduce the in-band noise (tones)



- Reduce the sensitivity to component variation

$$R_1(z) = \left. \frac{X_2(z)}{Y(z)} \right|_{U(z)=0} = -\frac{a_1 z + a_2(z-1)}{z^2 - (2-g_1)z + 1}$$

$$\cos \omega_i = 1 - g_i / 2 \quad i = 1, 2$$

$$\omega_1 \ll 1, \omega_1 \approx \sqrt{g_1}$$

$$\omega_2 \ll 1, \omega_2 \approx \sqrt{g_2}$$

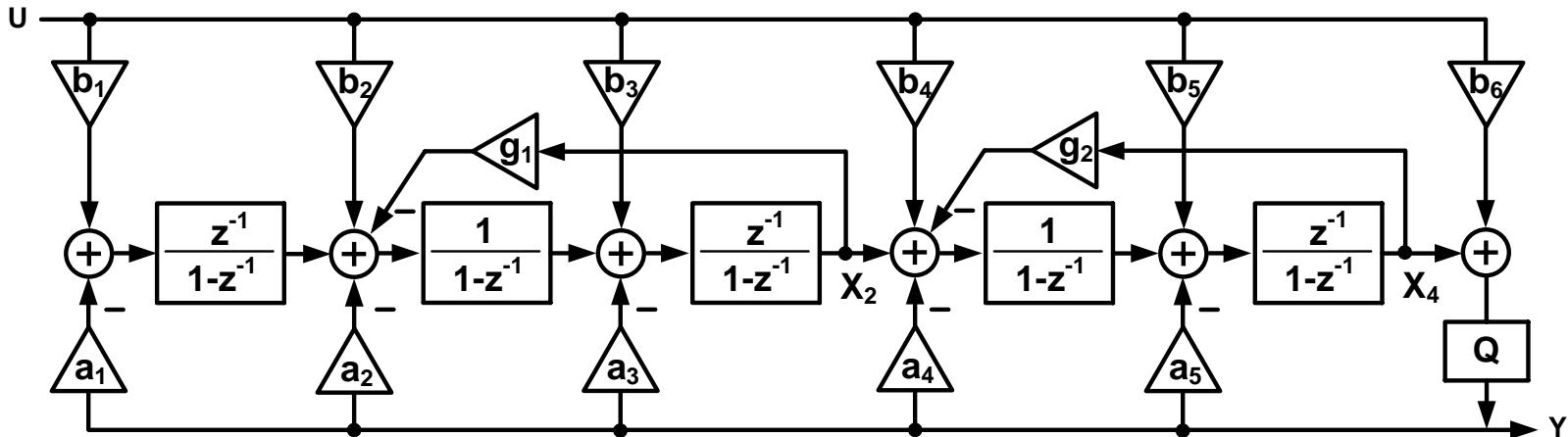
¹ Have a delay in each integrator can also be implemented to reduce the speed requirement of opamp

CRFB

- For odd N

- Make the integrator the input stage

- Minimize the input-referred contribution of noise sources from the subsequent stages



- A delay associated with each SC integrator for wideband ADC

- Reduce the speed requirement of the opamp used

$$R_1(z) = \left. \frac{X_2(z)}{Y(z)} \right|_{U(z)=0} = -\frac{a_2 + a_3(z-1)}{z^2 - 2z + (1+g_1)}$$

$$z = 1 + j\sqrt{g_i} \quad i = 1, 2$$

$$\omega_1 \ll 1, \omega_1 \approx \sqrt{g_1}$$

$$\omega_2 \ll 1, \omega_2 \approx \sqrt{g_2}$$

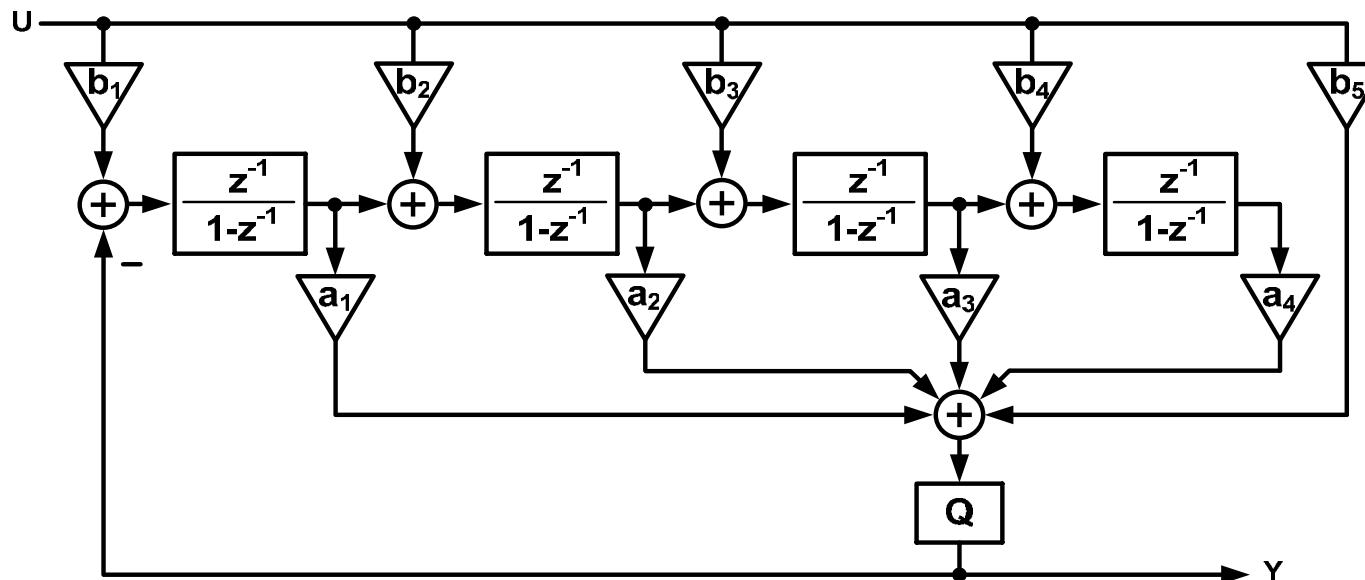
Cascade Integrators with distributed FeedForward (CIFF)

- Loop Filters with Distributed Feedforward and Input Coupling

 - The transfer function of the feedback filter

$$L_1(z) = -a_1 I(z) - a_2 I(z)^2 - \cdots - a_N I(z)^N \quad \text{where } I(z) = 1/(z-1)$$

$$L_0(z) = b_1 \cdot (a_1 I + a_2 I^2 + \cdots + a_N I^N) + b_2 \cdot (a_2 I + \cdots + a_N I^{N-1}) + b_3 \cdot (a_3 I + \cdots + a_N I^{N-2}) + \cdots + b_{N+1}$$

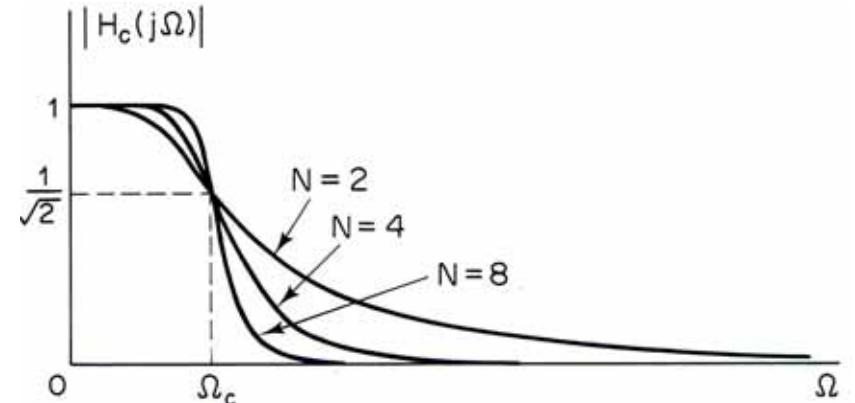
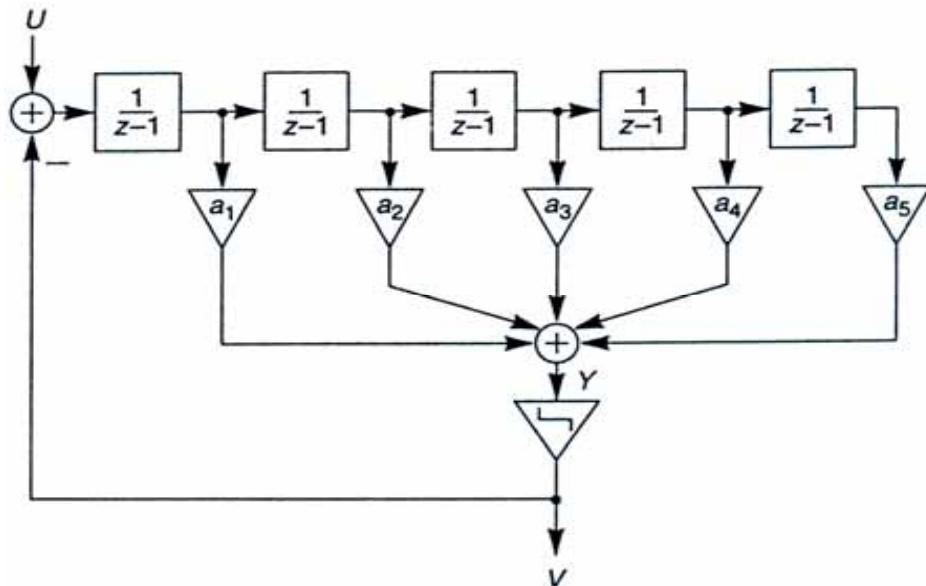


- All N poles of $L_1(z)$ lie at dc ($z=1$)
- All the zeros of the NTF at dc
 - Inverse Chebyshev NTF *cannot* be implemented
 - Butterworth high-pass NTF

Cascade Integrators with distributed FeedForward (CIFF)

- Chain of Integrators with Weighted Feedback Summation

Set $b_1=1$, $b_2=b_3=b_4=b_5=0$



Loop filter $L_0(z) = -L_1(z) = \frac{a_1}{z-1} + \frac{a_2}{(z-1)^2} + \frac{a_3}{(z-1)^3} + \dots$

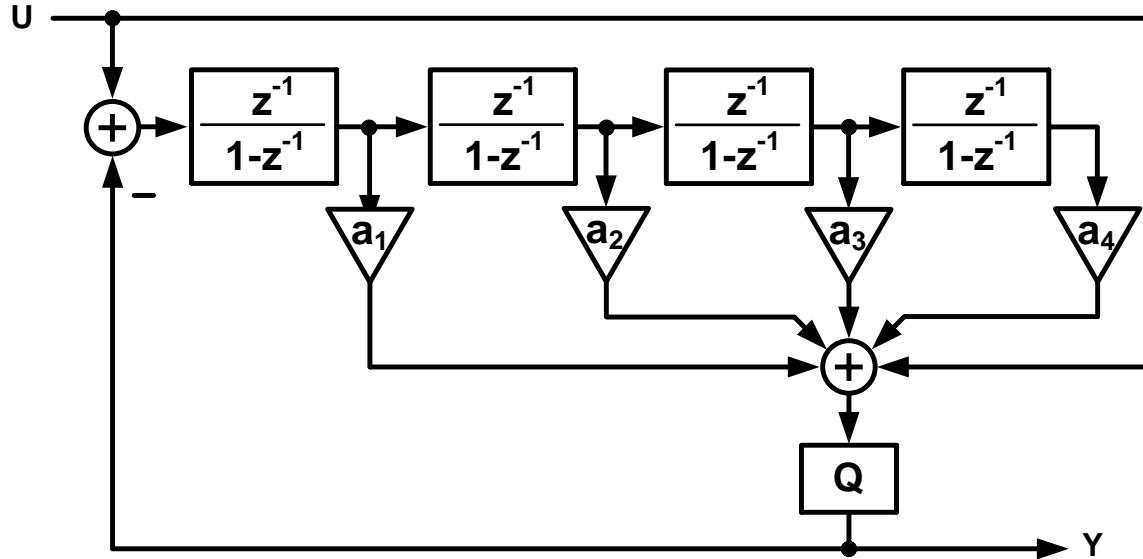
$STF(z) = 1 - NTF(z)$

Cause peaking at high frequencies for Butterworth filter

Prefilter should be added

Cascade Integrators with distributed FeedForward (CIFF)

- The case $b_2 = b_3 = \dots = b_N = 0$ and $b_1 = b_{N+1} = 1$



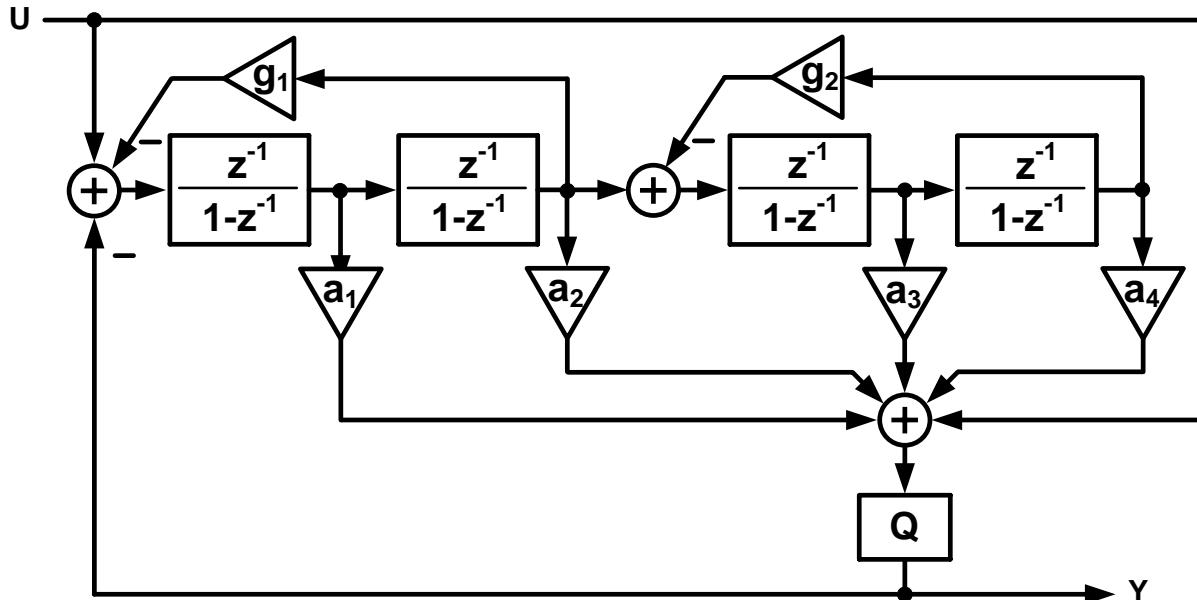
■ $L_0(z) = 1 - L_1(z)$
■ STF=1

$$U(z) - V(z) = U(z) - [U(z) + H(z)E(z)] = -H(z)E(z)$$

- ➡ The loop filter does not process the input signal
- ➡ Low-distortion property

Cascade of Resonators with distributed FeedForward (CRFF)

- The case $b_2 = b_3 = \dots = b_N = 0$ and $b_1 = b_{N+1} = 1$



- Low-distortion property
- Optimized zeros of $H(z)$
 - Moves the open-loop poles (the zeros of NTF) away from dc
 - Inverse Chebyshev NTF can be implemented
 - Attenuate the in-band noise

► The poles of the resonators $\omega_1 = \cos^{-1}\left(1 - \frac{g_1}{2}\right) \approx \sqrt{g_1}$ for $g_1 \ll 1$

$$\omega_2 = \cos^{-1}\left(1 - \frac{g_2}{2}\right) \approx \sqrt{g_2} \text{ for } g_2 \ll 1$$

Higher-Order Single-Bit $\Delta\Sigma$ Modulators

- Example

- Design a third-order A/D converter. All zeros of NTF are placed at $z=1$ so that the converter can be used for various oversampling ratios.

- The form of the NTF

- $$NTF(z) = \frac{(z-1)^3}{D(z)}$$

- A thumb of rule $|NTF(z)| < 1.5$ for stability

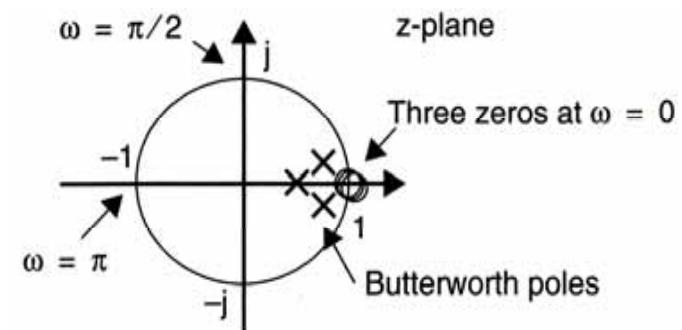
- Choose $|NTF(z)| < 1.4$
 - A passband edge at $fs/20$

- Derive a third-order Butterworth high-pass filter with a peak gain 1.37

- $$NTF(z) = \frac{(z-1)^3}{z^3 - 2.3741z^2 + 1.9294z - 0.5321}$$

- A loop filter can be found

- $$-L_1(z) = \frac{1 - NTF(z)}{NTF(z)} = \frac{0.6259z^2 - 1.0706z + 0.4679}{(z-1)^3}$$



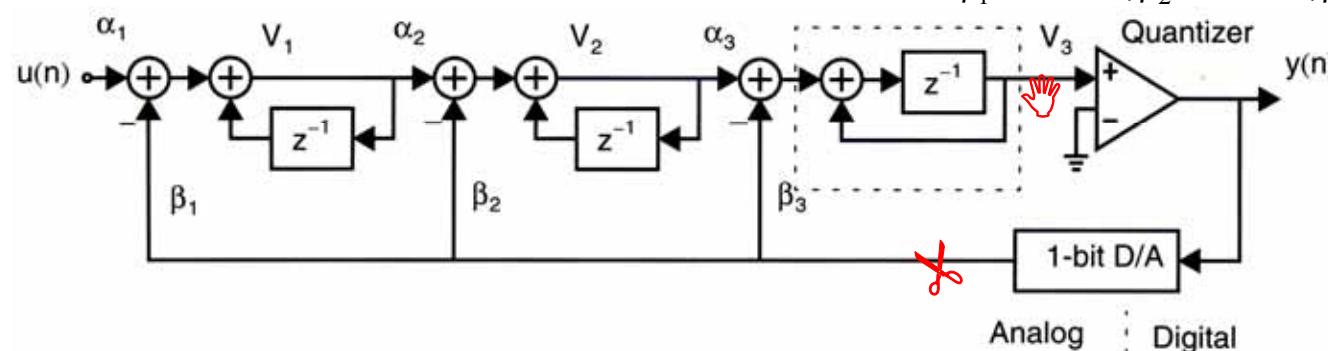
- $$\text{Stable}$$
 - $$\text{Initially set } \alpha_1 = \beta_1, \alpha_2 = \alpha_3 = 1$$

$$-L_1(z) = \frac{(\beta_1 + \beta_2 + \beta_3)z^2 - (\beta_2 + 2\beta_3)z + \beta_3}{(z-1)^3}$$

$$\Rightarrow \alpha_1 = 0.0232, \alpha_2 = 1.0, \alpha_3 = 1.0$$

$$\Rightarrow \beta_1 = 0.0232, \beta_2 = 0.1348, \beta_3 = 0.4679$$

Initial set

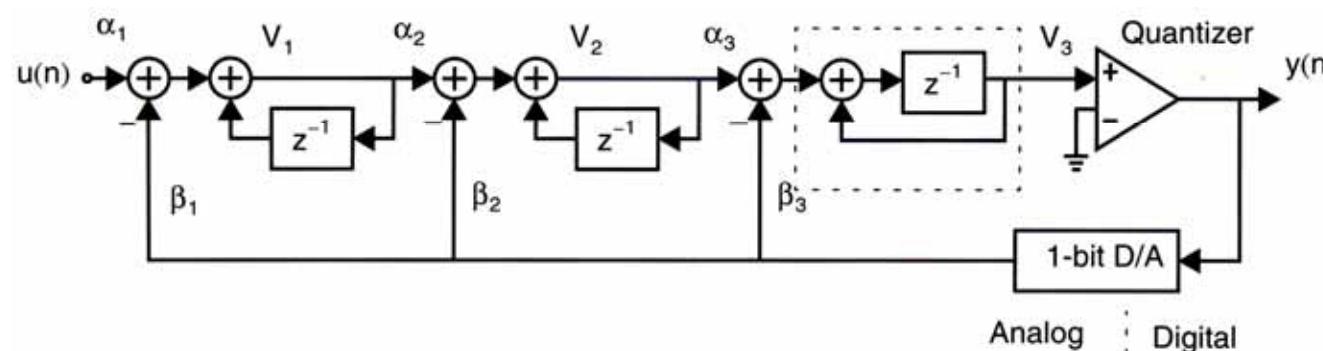


Higher-Order Single-Bit $\Delta\Sigma$ Modulators

► Dynamic range scaling

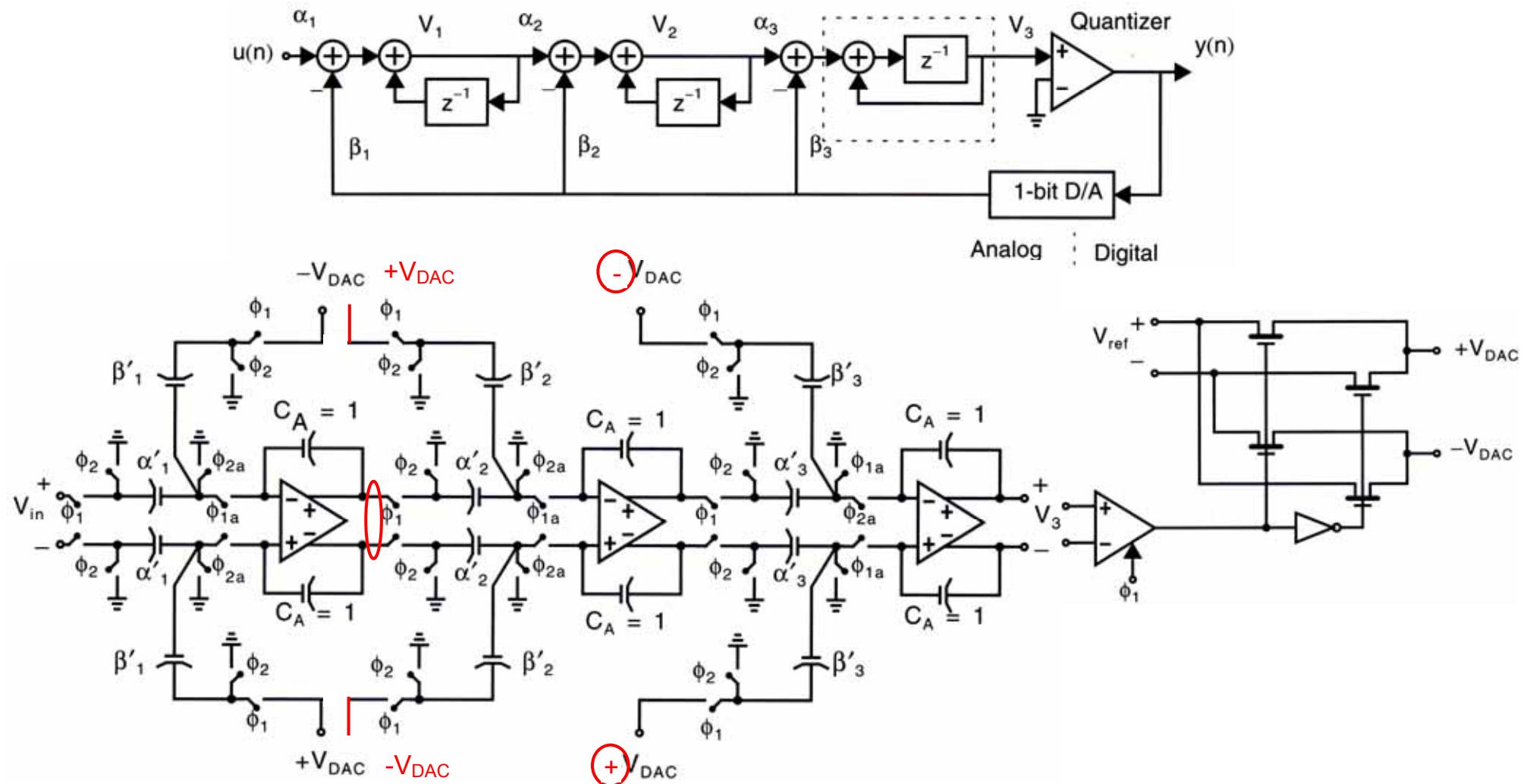
- ▶ Adding gain to each integrator stage
 - Ensure all nodes have approximately the same power level to prevent large noise gain with small signal levels
- ▶ To increase the output level of a node by a factor k
 - Input branches should be multiplied by k
 - Output branches should be divided by k
- ▶ Given a peak value of input 0.7 with $\pi/256$ rad/sample
 - $V_1=0.1256$, $V_2=0.5108$, and $V_3=1.004$
 - To increase the maximum value of V_1 to unity
 - $\alpha_1 \times 1/0.1256 = \beta_1 \times 1/0.1256$, $\alpha_2 \div 1/0.1256$
 - $0.1256\alpha_2 \times 1/0.5018$, $\beta_2 \times 1/0.5018$ and $\alpha_3 \div 1/0.5018$

$$\Rightarrow \begin{aligned} \alpha'_1 &= 0.1847, \alpha'_2 = 0.2459, \alpha'_3 = 0.5108 \\ \beta'_1 &= 0.1847, \beta'_2 = 0.2639, \beta'_3 = 0.4679 \end{aligned}$$



Higher-Order Single-Bit $\Delta\Sigma$ Modulators

Circuit implementation



Multi-Stage Delta-Sigma Modulators

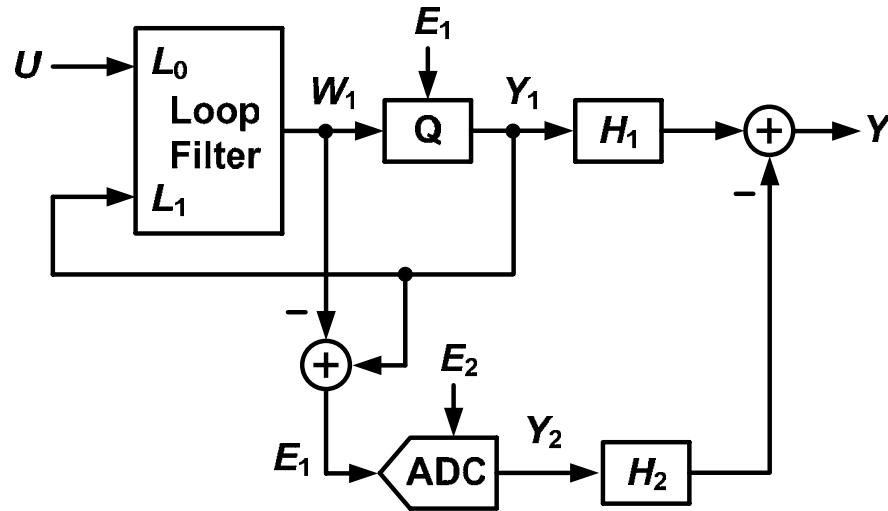
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Multi-Stage Modulators

- For Low OSR

- Stability limits the input amplitude and SNR for higher-order loops

- The Leslie-Singh (L-0 Cascade) Structure



$$Y_1 = W_1 + E_1$$

$$E_1 = Y_1 - W_1$$

$$\begin{cases} Y_1 = STF_1 \cdot U(z) + NTF_1 \cdot E_1 \\ Y_2 = z^{-k}(E_1 + E_2) \end{cases}$$

$$H_1 = z^{-k} \quad H_2 = NTF_1$$

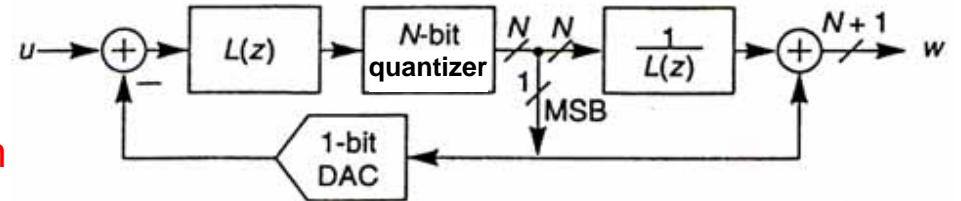
$$\Rightarrow Y = z^{-k}[STF_1 \cdot U(z) - NTF_1 \cdot E_2(z)]$$

$$E_2 \ll E_1$$

- Enhance the SNR by 25~30 dB
- The operation of the first quantizer must be delay-free
 - W₁ must be delayed before subtraction
- W₁ can be the only input of the second stage
 - Handle a larger input signal
 - Increase the requirement of low distortion

The Leslie-Singh Architecture

- Multi-bit Quantization in the Forward Path
 - Most significant bit (MSB) in the feedback path
 - Ensuring the linearity of the signal transmission



Dual-Quantizer Modulators

- The outputs in each quantizer

$$V_1 = \text{STF} \cdot U + \text{NTF} \cdot E_1 \quad V_2 = V_1 - E_1 + E_2$$

E_1 and E_2 are quantization errors of 1-bit and N -bit quantizer, respectively

- The output signal

$$\begin{aligned} W &= H_1 V_1 + H_2 V_2 \\ &= \text{STF} \cdot (H_1 + H_2)U + (H_1 \cdot \text{NTF} + H_2 \cdot \text{NTF} - H_2)E_1 + H_2 E_2 \end{aligned}$$

Setting $H_1 \cdot \text{NTF} + H_2 \cdot \text{NTF} - H_2 = 0 \Rightarrow$

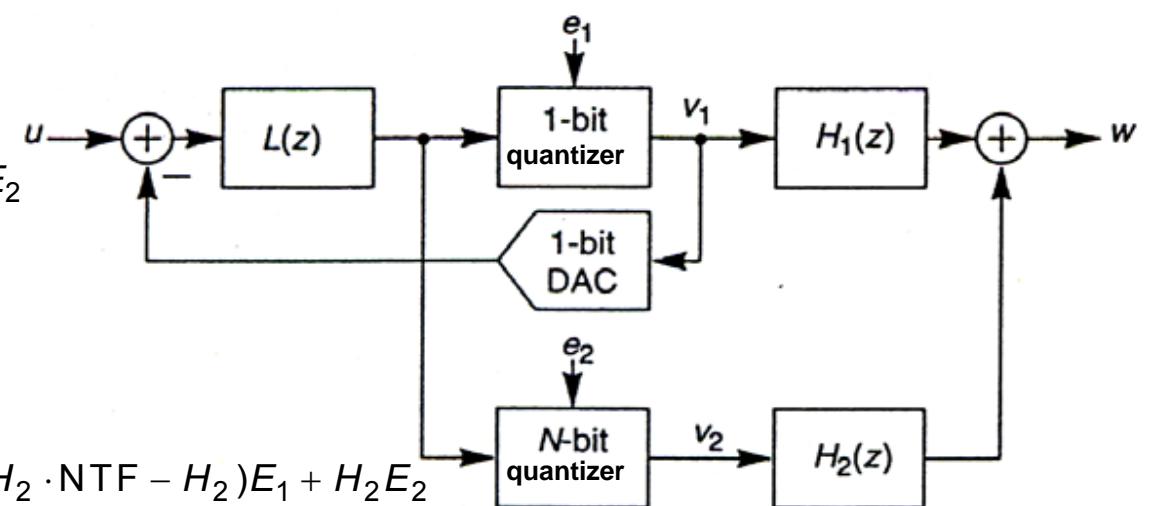
Choosing $\text{STF} = \text{STF} \cdot (H_1 + H_2) = z^{-k}$

► The digital filters $H_1 = 1 - \text{NTF}$ $H_2 = \text{NTF}$

► The output signal $W = z^{-k}U + \text{NTF} \cdot E_2$

► 1-bit quantization error E_1 is cancelled

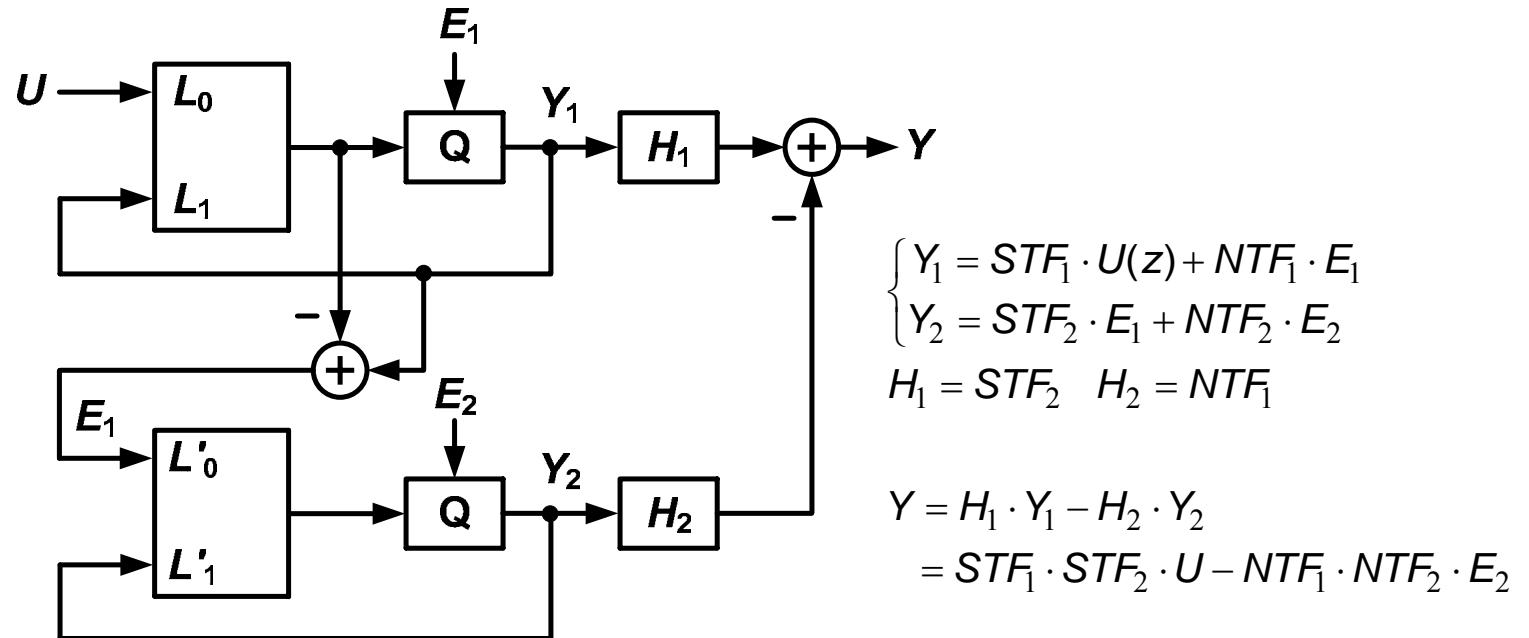
► N -bit quantization error E_2 is filtered by NTF of the upper path loop



Cascade Modulators

- Multi-stage noise SHaping (MASH) Architecture

- Cascade low-order (L_1 th- and L_2 th-order) stages to perform high-order noise-shaping



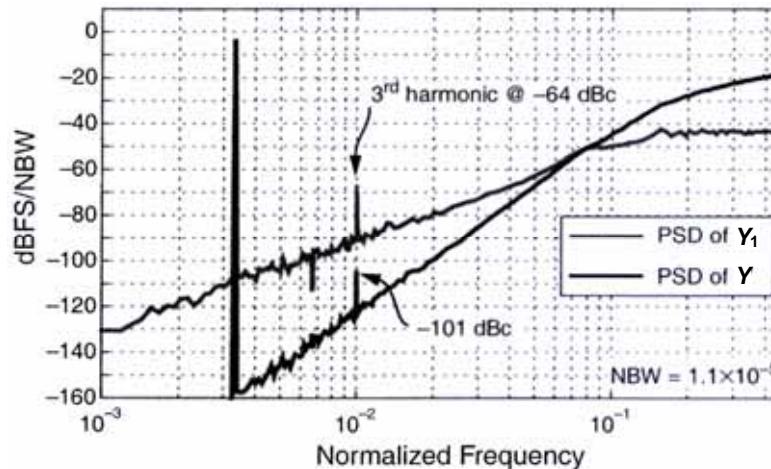
- The quantization error of the former stages could be eliminated in digital domain
 - Obtain an L th-order ($L=L_1+L_2$) noise-shaping of quantization error of the last integrator
- The first stage of the cascade should be a second-order modulator
- Each of the low-order modulators is stable, the overall system will be stable
 - Digital coefficients amplify the last stage quantization error must be minimized

Multi-stAge noise SHaping (MASH) Structure

Advantage

- Input E_1 is noise-like (even contains tones), E_2 is hence very similar to a true white noise
- less likely to need dithering than single-stage modulator

2-2 MASH with single-bit quantization



- Use a low-distortion loop filter structure in all stages without subtraction
 - No harmonic distortion in the second stage
- Use multi-bit quantizer in the second stage $Y = H_1 \cdot Y_1 - H_2 \cdot Y_2 = STF_1 \cdot STF_2 \cdot U - NTF_1 \cdot NTF_2 \cdot E_2$
 - Without any dynamic or other correction of the DAC nonlinearity
 - Since the error E_2 is suppressed by digital highpass filter NTF_1 in the baseband

Imperfections

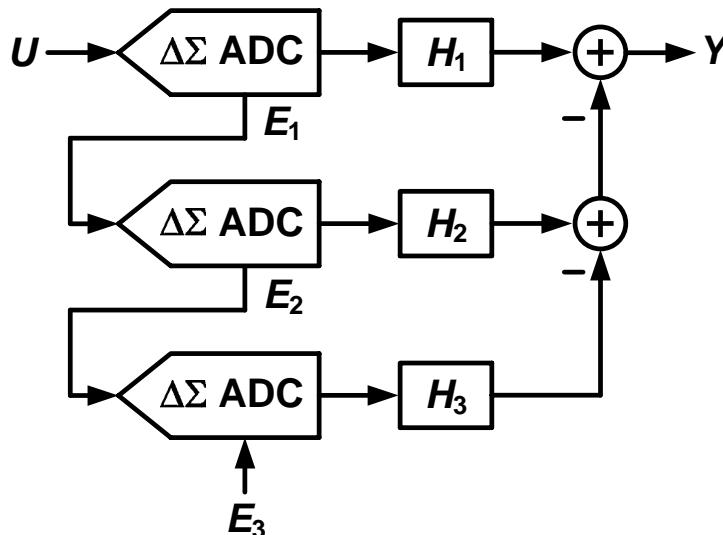
- E_1 appears at the output if $STF_2 \cdot NTF_{1a} - NTF_1 \cdot STF_{2a} \neq 0$
 - “a”: actual value of the analog function



Extended MASH Structure

● Cascade $\Delta\Sigma$ Modulator

- A multi-step converter for high SNR



$$H_1 \cdot NTF_1 - H_2 \cdot STF_2 = 0$$

$$H_2 \cdot NTF_2 - H_3 \cdot STF_3 = 0$$

$$Y = STF_1 \cdot H_1 \cdot U + NTF_3 \cdot H_3 \cdot E_3$$

$$= STF_1 \cdot H_1 \cdot U + \left(\frac{H_1 \cdot NTF_1 \cdot NTF_2 \cdot NTF_3}{STF_2 \cdot STF_3} \right) \cdot E_3$$

- Digital cancellation logics cancel the quantization errors of the prior modulators
 - ➔ Only the final quantization error at the output
- Only feedforward paths and no feedback between modulators
 - ➔ Stable modulator \Rightarrow stable system inherently

● Imperfect cancellation

- Uncancelled noise from the first modulator
- Using second-order modulator in the first stage

Noise Leakage in Cascade Modulators

- To keep the leakages of E_1 and E_2 acceptably low
 - How accurately the components need to be matched
 - The minimum acceptable gain for the opamps

$$H_{l1} = H_1 \cdot NTF_1 - H_2 \cdot STF_2$$

$$H_{l2} = H_2 \cdot NTF_2 - H_3 \cdot STF_3$$

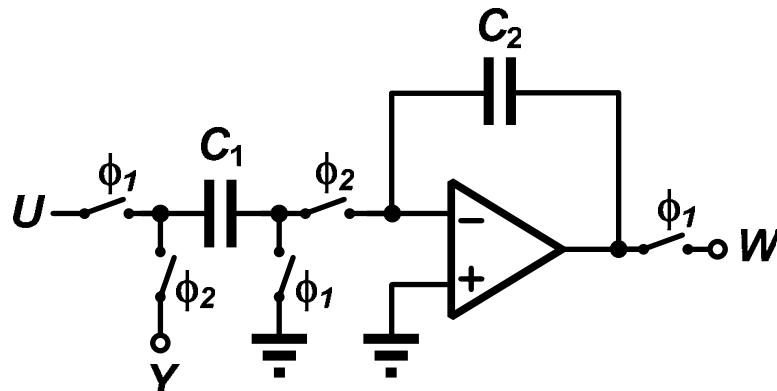
● Assumptions

- H_{l2} represents higher-order shaping
 - ▶ The leakage of E_2 is less important than E_1
- $H_2 = NTF_1$ and $H_1 = z^{-1}$ or 1 in signal band
 - ▶ The effect of an imperfect NTF_1 dominates that of STF_2
 - ▶ The error signals due to STF_2 are inherently noise shaped
- If $STF_2 = H_1 = 1$ and $NTF_1 = 1/(1-L_1) \approx -1/L_1$
 - ▶ $H_{l1} = NTF_1 - H_2 = NTF_{1a} - NTF_{1i}$
 $\approx 1/L_{1i} - 1/L_{1a}$



Noise Leakage in Cascade Modulators

- 1-1-1 MASH



$$I_{ideal}(z) = \frac{g \cdot z^{-1}}{1 - z^{-1}}$$

$$\begin{aligned} I_{actual}(z) &= \frac{g' \cdot z^{-1}}{1 - p' \cdot z^{-1}} = \frac{g \cdot [1 - D - (1 + g)/(A + 1 + g)] \cdot z^{-1}}{1 - [1 - g/(A + 1 + g)] \cdot z^{-1}} \\ &\approx \frac{g \cdot [1 - D - (1 + g)/A] \cdot z^{-1}}{1 - (1 - g/A) \cdot z^{-1}} \end{aligned}$$

g : the nominal gain of integrator

D : capacitance error $\ll 1$

A : the finite dc gain of the opamp

$$L_1(z) = -I(z)$$

$$H_{l1} \approx 1/L_{li} - 1/L_{la} = (1/A) + (1-z) \cdot [D/g + (1+1/g)/A]$$

Unfiltered leakage

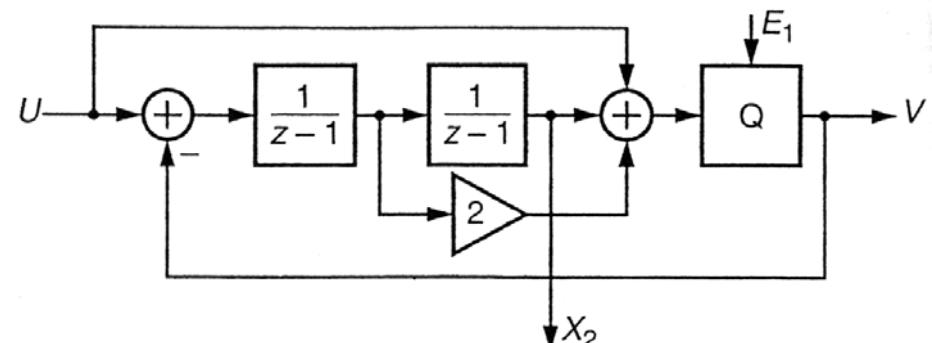
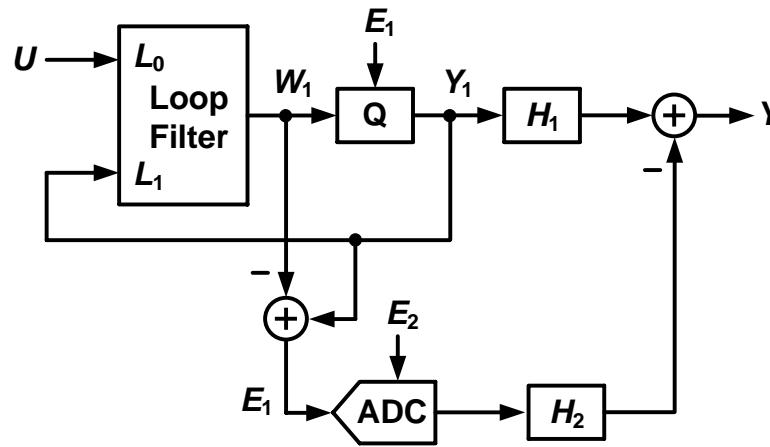
First-order-filtered

- A very-high-gain opamp with excellent settling is required ($A \gg 1$) for high SNR
- Matching accuracy of the capacitors must be very high ($D \ll 1$) for low OSR

Noise Leakage in Cascade Modulators

2-1 MASH

- Reduce the leakage of E_1 for a second-order first stage



- The leakage transfer function $H_{l1} = A_0 + A_1 \cdot (1 - z^{-1}) + A_2 \cdot (1 - z^{-1})^2 + \dots$

→ Unfiltered leakage $A_0 = 1/A^2$

→ Linear filtered error leakage $A_1 = [1/g_1 + 1/g_2]/A$

→ Quadratically filtered leakage $A_2 = 1/(g_1 g_2) - 1 + 2[1 - 1/(g_1 g_2) - 1/g_2^2]/A + 2D/(g_1 g_2)$

g_i : the nominal gain of integrator

D : capacitance error $\ll 1$ (0.5%)

A : the finite dc gain of the opamp (1000)

Noise-shaped for OSR=64

A_1 is reduced by 1/30

A_2 is reduced by 1/1000

A_3 is reduced by 1/30,000

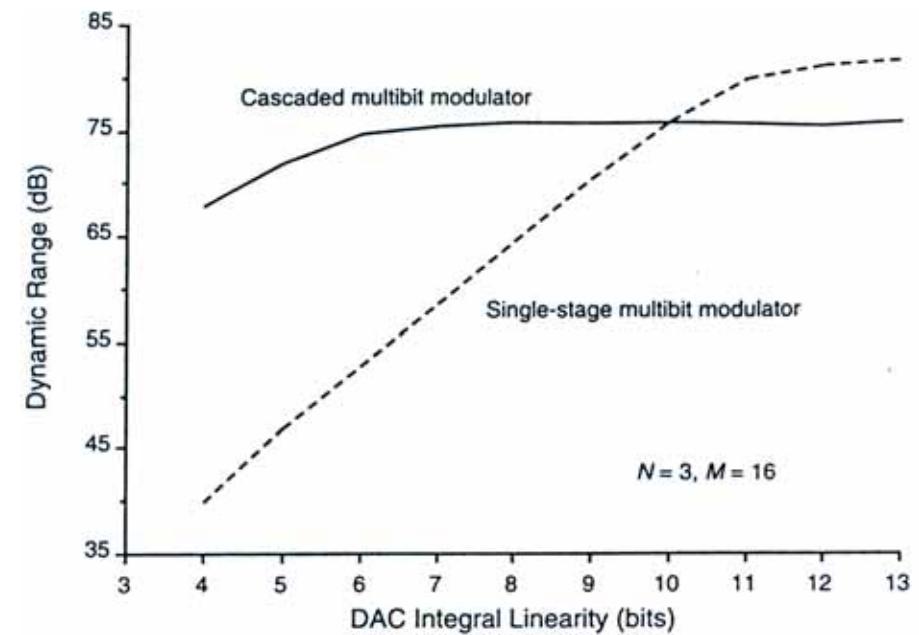
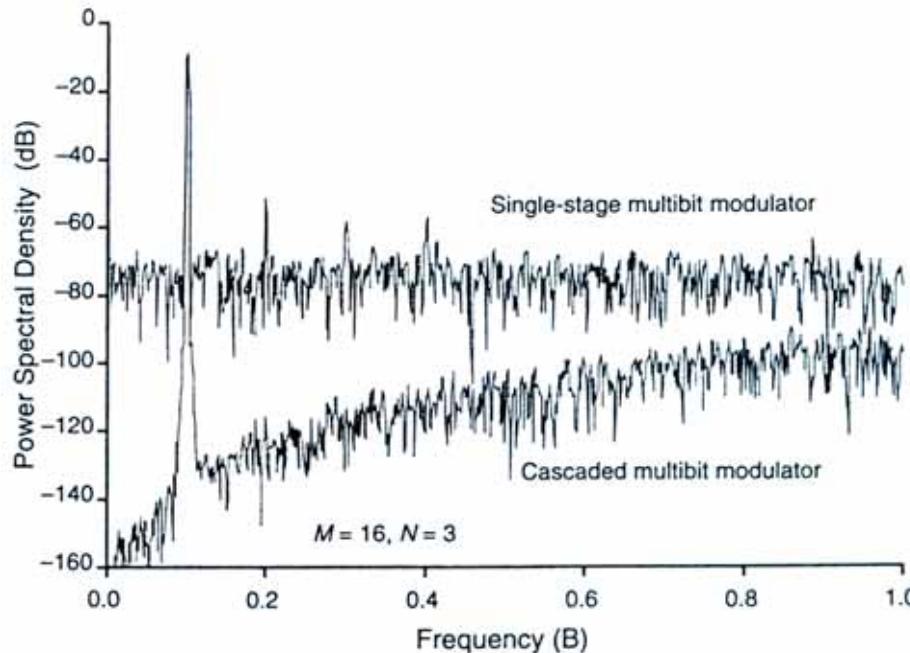
Cascade vs. Single-Stage Modulators

- More Tolerant of DAC nonlinearity

- Third-order modulators under 5-bit DAC linearity
 - Increase in the noise floor and harmonic distortion in single-stage modulator (1-bit)
- To achieve 12-bit dynamic range
 - Cascade - DAC linearity > 6bits
 - Single-stage - DAC linearity > 10bits

- Imperfect integrators

- Incomplete quantization error cancellation



Modulators with Multi-Bit Internal Quantizers

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Multi-Bit $\Delta\Sigma$ Modulators

- The Most Flexibility for Fitting Various Specs.

- Smaller quantization error Δ_N for N-bit internal quantizer

► Quantization noise power spectral density is lowered

$$\frac{\Delta_N^2}{12} \frac{1}{f_s} = \frac{\Delta_1^2}{12} \frac{1}{(2^N - 1)^2} \frac{1}{f_s}$$

steps

Δ_1 : quantization error of single-bit quantizer

► Improve SNR by $6.02 \times N$ ($= 20 \log(2^N - 1)$)

- Quantization error is reduced by 6dB for every bit added

- Ex. 4-bit quantizer \Rightarrow 24 dB improvement

- The stopband performance of the decimator can be relaxed

► Better stability for high-order loops

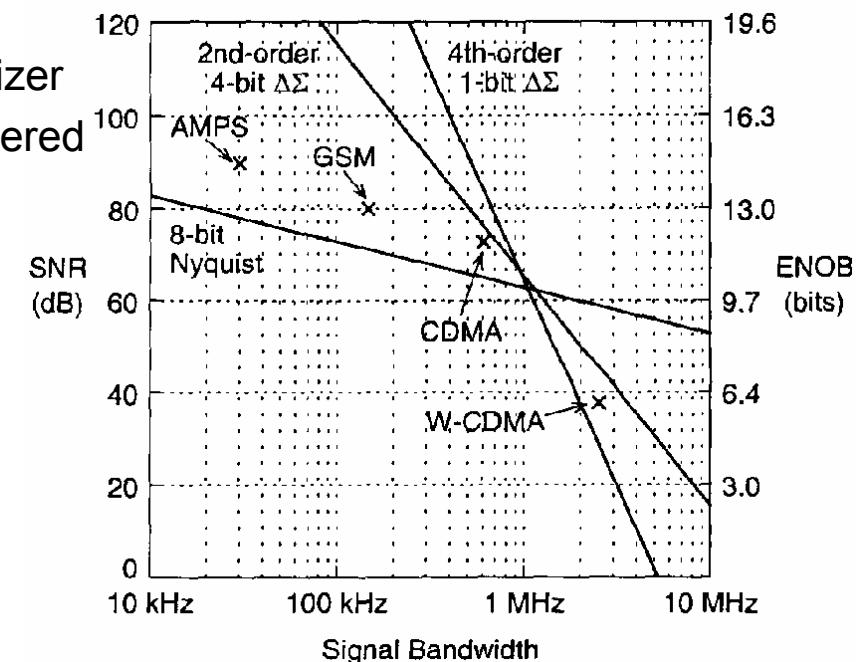
► Better fitting the white noise error model

► Integrator setting requirements are greatly relaxed

► The difference between input and DAC signals is smaller

- The linear requirements on the input stage of the filter is eased

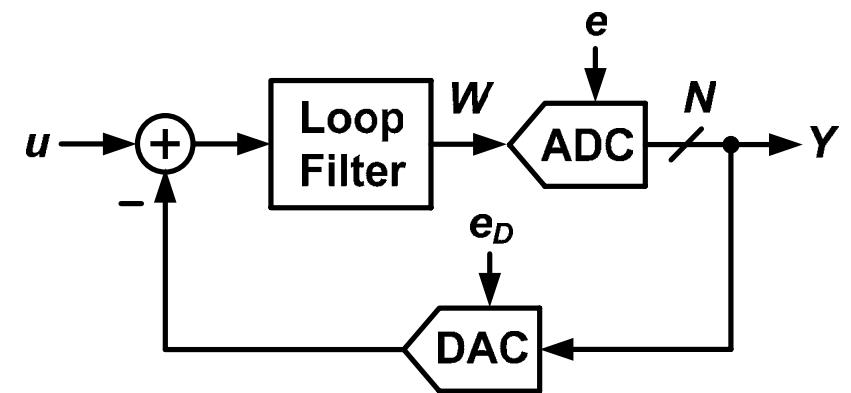
- The spurious tones which are repeated patterns at the output of the quantizer in response to dc references, or ac input, can also be suppressed



Multi-Bit $\Delta\Sigma$ Modulators

- The Effective Gain of the Quantizer is Reduced

- The stability is more robust
- NTF can be chosen more aggressively
 - OSR=16, 5th-order
 - single-bit modulator, SNR=60dB (stability)
 - 4-bit quantizer, SNR=120dB



Gain deviation from the nominal gain 1 at most $\Delta/|2 \cdot w(n)|$

Δ : LSB voltage of the quantizer

small

$$k(n) = \frac{y(n)}{w(n)} = \frac{w(n) + e(n)}{w(n)} = 1 + \frac{e(n)}{w(n)}$$

1-bit quantizer has an instantaneous gain $k(n)=1/w(n)$

Small values of $k(n)$ result in instability for higher-order loops

- DAC input changes less from sample to sample

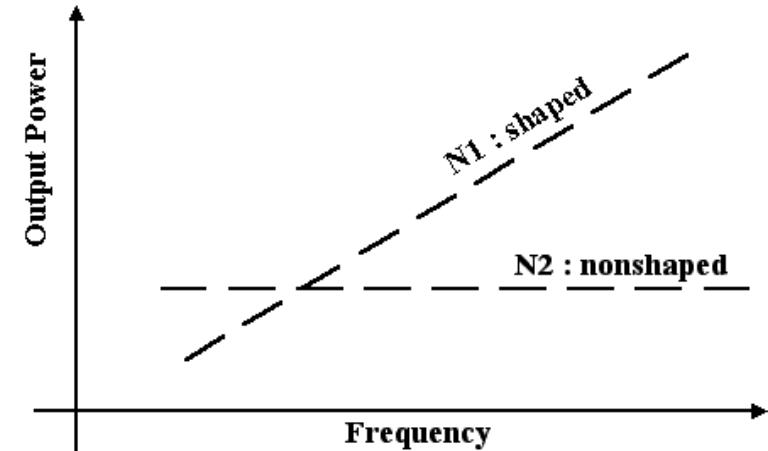
- The SR of the opamp is reduced

- Less sensitive to clock jitter for continuous-time loop filters

Multi-Bit $\Delta\Sigma$ Modulators

● Disadvantage

- Any error in the DAC will appear at the output
- Nonlinearity of the DAC corrupts the signal
 - ▶ Nonlinear error distributed in the DAC due to the mismatching among DAC elements
 - ▶ Capacitors and switches
 - ▶ Introduces extra noise and distortion at the input
 - ▶ Dynamic element matching (DEM)

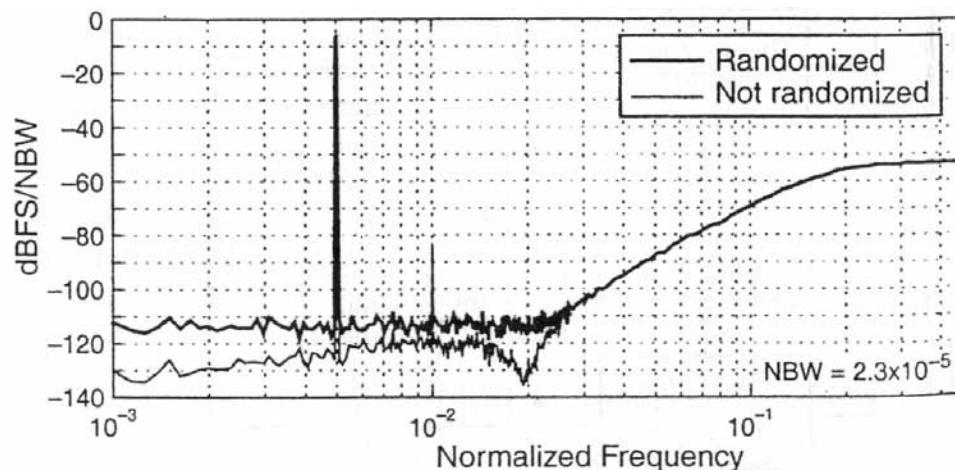
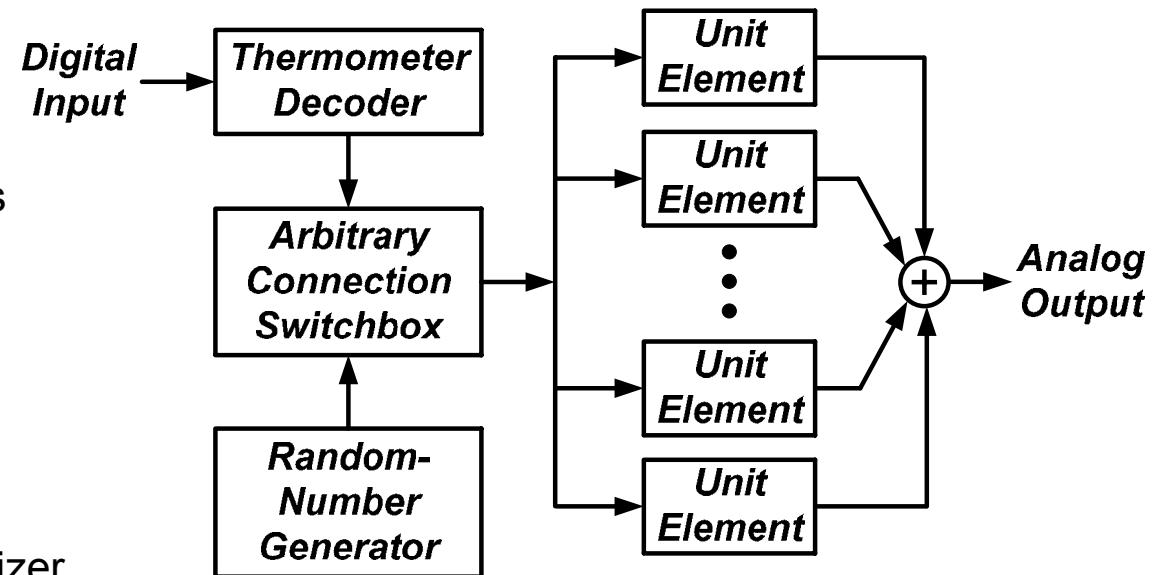


● N-bit ADC linearity

- N-bit DAC (it is hard to realize better than 10 ~ 12 bits)
 - ▶ Dual-Quantization
 - ▶ Mismatch-Shaping
 - ▶ Digital Correction Schemes

Dynamic Element Matching (DEM)

- Element mismatches
 - Harmonic signal distortion
 - Increased noise floor
 - Uneven spacing of DAC levels
 - Signal distortion is replaced by random noise
 - A third-order ADC with 3-bit quantizer
 - [-0.1% , $+0.1\%$] linear-gradient mismatch



Dynamic Element Matching

- Assumption

- Offset and gain error of the DAC are acceptable
- Only DAC nonlinearity is our concern
- “ideal” M -element input-output characteristics

$$w(k) = OS + \frac{FS - OS}{M} \cdot k, \quad k = 0, 1, 2, \dots, M$$

$$u_i = U + d_i \quad (i = 1, 2, \dots, M)$$

$$U = \sum_{i=1}^M u_i / M$$

$$\sum_{i=1}^M d_i = 0$$

- The full-scale output $FS = OS + \sum_{i=1}^M u_i = OS + M \cdot U$
- Ideal output for an input k

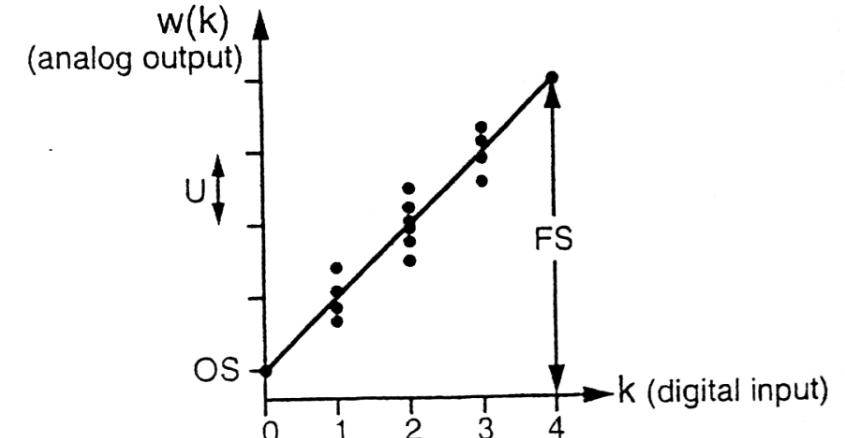
$$w(k) = OS + k \cdot U$$

- A DAC with $M=4$

► For input codes $k=0$ and $k=M=4$ the analog output is unique

► For $k=2$

$$\bar{w}(k) = OS + 3 \cdot \sum_{i=1}^4 u_i / 6 = OS + 2U + 0.5 \cdot \sum_{i=1}^4 d_i = OS + 2U$$

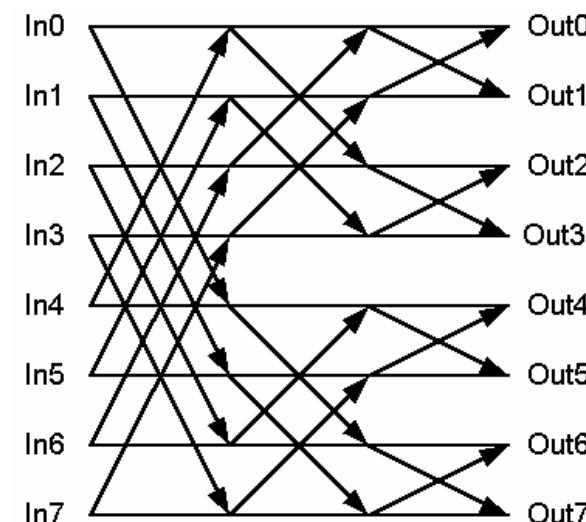


U : the average element

d_i : the deviations of the u_i from the average

Dynamic Element Matching

- Convert the Static Error into Wideband Noise
 - Select different element at different time
 - ▶ Averaging Algorithm – reduce the in-band power of mismatch error
 - ▶ Makes a first-order shaping of mismatch error
 - ▶ CLA
 - ▶ ILA
 - ▶ DWA
 - ▶ Noise-shaping DEM – second-order highpass shaping of mismatch error
 - ▶ Incorporate a filter into the element selection logic : high-order shaping
 - ▶ Complicated hardware
 - Clocked Averaging Algorithm (CLA)
 - ▶ Flips the DAC elements in a period fashion
 - ▶ Cannot cancel DAC error effectively
 - ▶ Ex. 8 elements

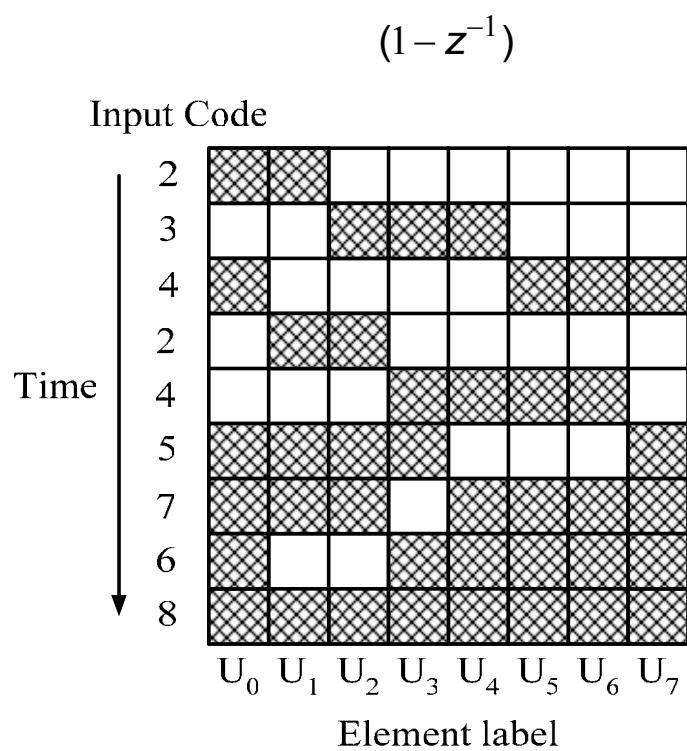
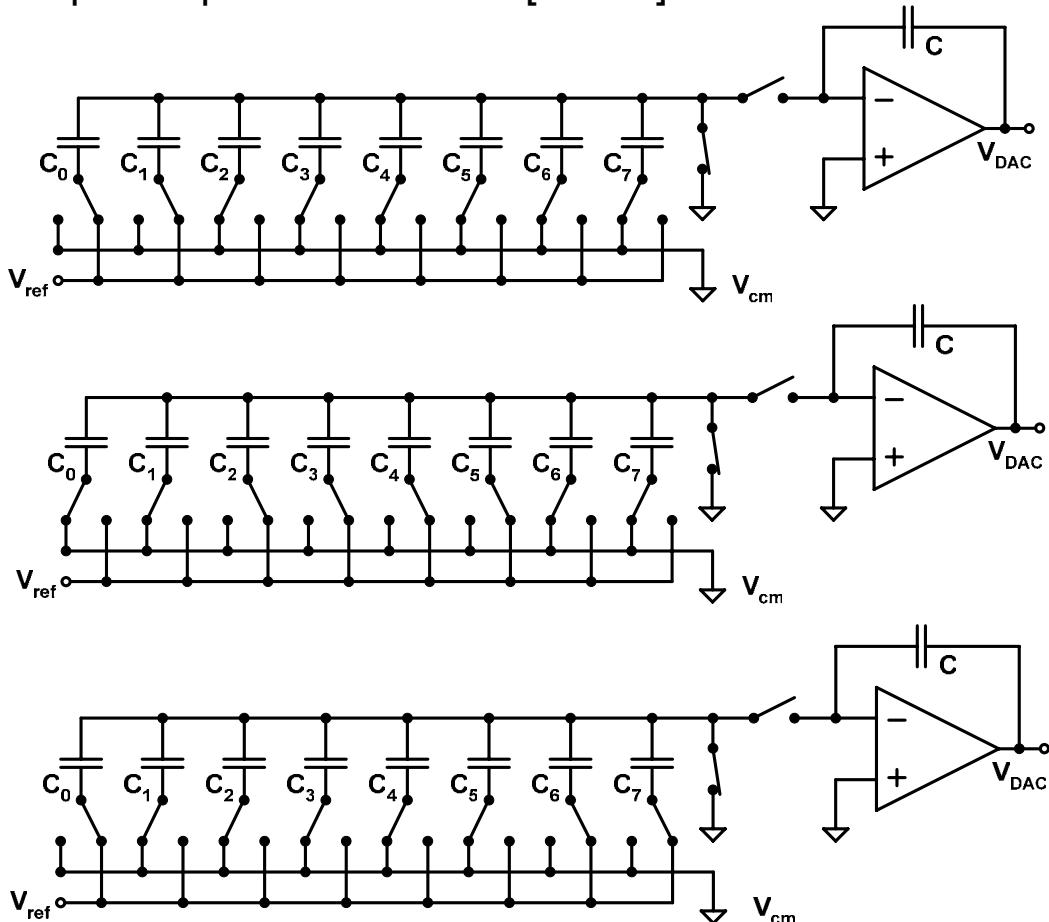


L. R. Carley, "A noise-shaping coder topology for 15+ bit converters," JSSC, vol.24, pp.267-273, Apr. 1989



Element Rotation or Data-Weighted Averaging (DWA)

- Selects DAC components cyclically one by one
 - No unit is reselected before all the others are selected
 - Input sequence of DAC = [2 4 3]



→ Introduces tones in the baseband due to limit cycle oscillation under the guide of a single pointer

R. T. Baird and T. S. Fres, "Improved DAC linearity using data weighted averaging," ISCAS, 1995

Element Rotation or Data-Weighted Averaging (DWA)

- Make the long term average use of each element in the DAC the same

- For the sum of all errors over N clock periods

- Mismatch noise $e(n)$: the sequence of DAC output errors over N clock cycles

$$s(N) = \sum_{n=1}^N e(n)$$

- P : the sum of the absolute values of the errors in the 8 unit elements

$$|s(N)| \leq P/2 \quad \leftarrow \text{Bounded white noise}$$

$$|e(N)|_{\text{ave}} = |s(N)|/N \leq P/(2N) \rightarrow 0 \text{ as } N \rightarrow \infty \quad [\text{The average values of the error samples } e(n)]$$

- The mismatch noise is **first-order highpass filtered**

- $S(\omega)$: The power spectrum of $s(n)$

- Is a uniform noise spectrum

$$e(n) = s(n) - s(n-1)$$

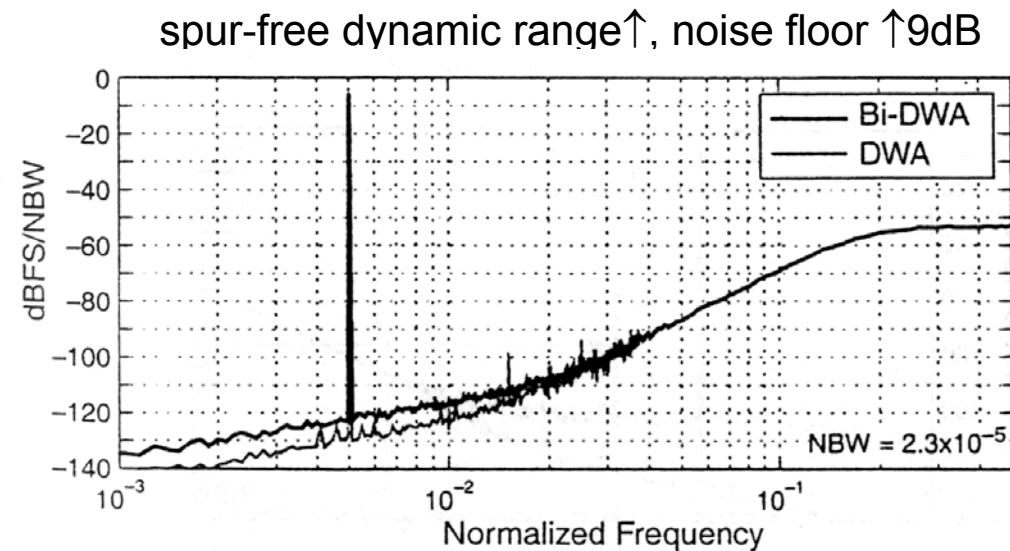
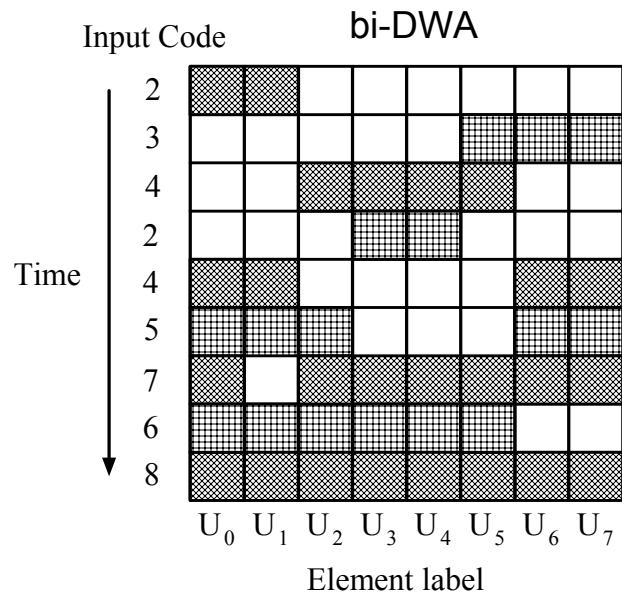
$$\Rightarrow E(\omega) = \left| 1 - e^{-j\omega} \right|^2 \cdot S(\omega)$$



Element Rotation or Data-Weighted Averaging (DWA)

- Tonal Character of $e(n)$

- exhibits tones for a dc or low-frequency periodic input
- 8-element DAC for a value of 6
 - ➡ $S_1=(1, 2, 3, 4, 5, 6); S_2=(7, 8, 1, 2, 3, 4); S_3=(5, 6, 7, 8, 1, 2); S_4=(3, 4, 5, 6, 7, 8)$
 - ➡ $S_5=S_1, S_6=S_2$, etc.
- Introducing a random or pseudo-random effect into the process
 - ➡ Bi-Directional Data-Weighted Averaging (bi-DWA)

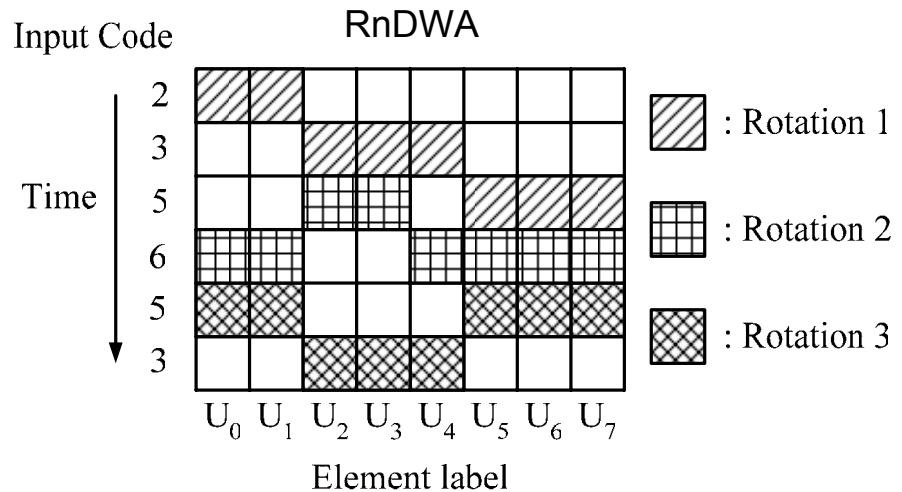
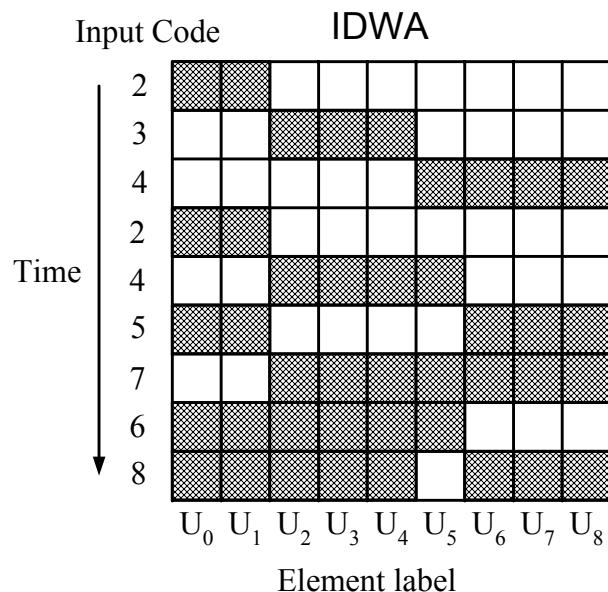


R. T. Baird and T. S. Fres, "Improved DAC linearity using data weighted averaging," ISCAS, 1995



Element Rotation or Data-Weighted Averaging (DWA)

- Incremental Data Weighted Averaging (IDWA)
- Offset technique for Data Weighted Averaging (ODWA)
 - Add a small dc offset to the input to shuffle digital codes
 - ▶ The first tone frequency increases with the amplitude of injected offset (< 0.8 LSB)
 - ▶ Most of mismatch tones are outside the baseband



T. H. Kuo and K. D. Chen, and H. R. Yeng, "A wideband CMOS sigma-delta modulator with incremental data weighted averaging," JSSC, Jan. 2002

Element Rotation or Data-Weighted Averaging (DWA)

- Randomized Data Weighted Averaging (RnDWA)

- Randomization + DWA

- No unit is reselected before all the others are selected

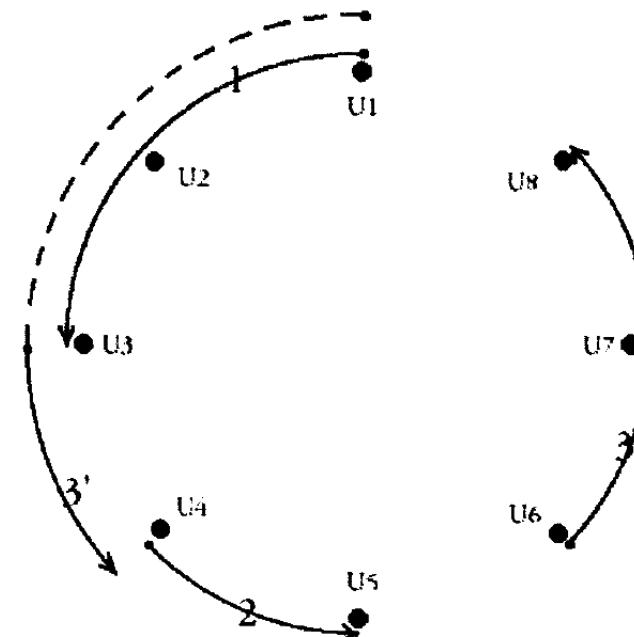
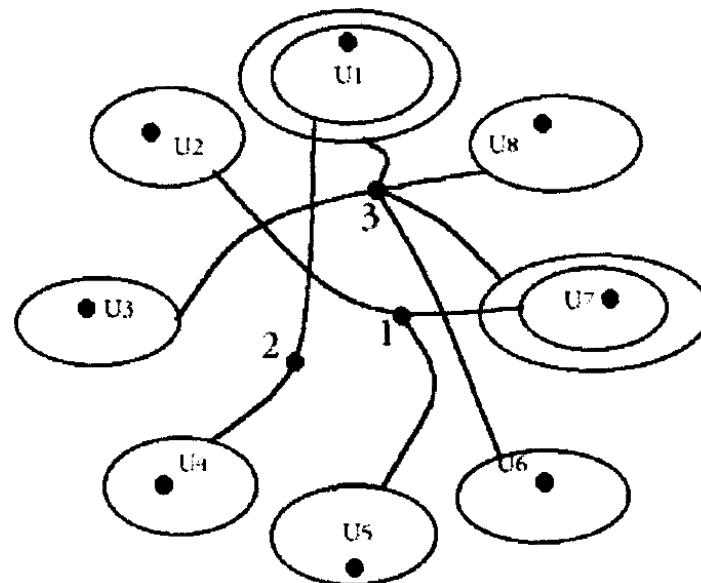
- Ex. Codes 3, 2, 5

- Partially Randomized Data Weighted Averaging (PRnDWA)

- Compatible with rotation process

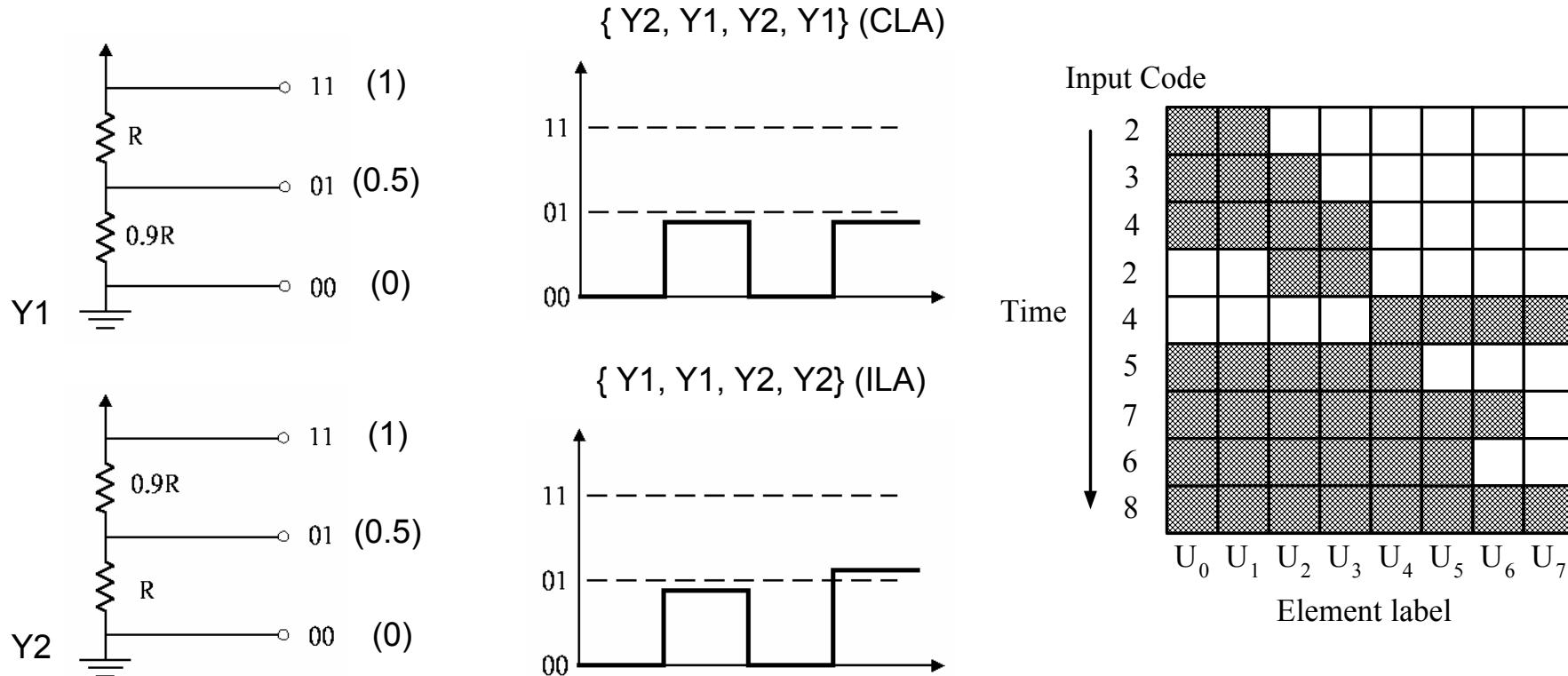
- Benefit from the simplicity

- Ex. Codes 3, 2, 5



Individual Level Averaging (ILA)

- Guarantee each element is used with equal probability for each code
 - Remember each state of each level
 - Ex. 3 levels, two elements and the output sequence : {00, 01, 00, 01}



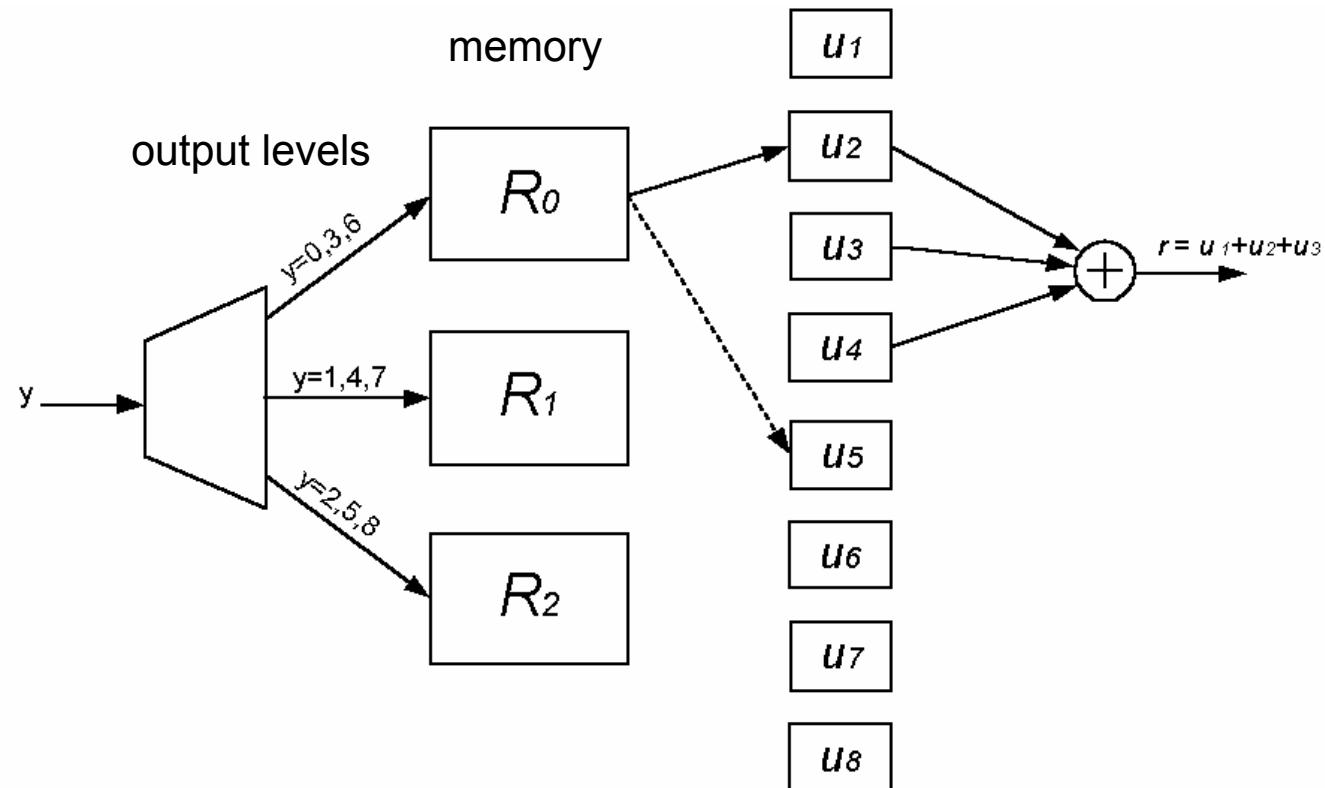
- More slowly to the zero-average than DWA
- Be less likely to generate tones even for dc or periodic inputs

Grouped Level Averaging (GLA)

- Three State Registers

- No adjacent output levels are assigned to the same state register

- Ex. $y=3 \Rightarrow u_2 u_3 u_4 \Rightarrow \text{pointer} \rightarrow u_5$



Vector-Based Mismatch Shaping

- Noise-Shaping DEM

- Vector quantizer uses the information in the $sy(n)$ to select which v elements to be enabled

► v : input digital code

► d_i : M -element column vector

- The difference between the actual element value and the average of all elements

- $[1 \dots 1] \cdot d_i = 0$

► To minimize sy while keeping all components positive

- Scalar value $f = -\min\{H_2 \cdot se\}$

- Vector quantizer sets those components of sv to one that corresponds to the v largest components of sy

$$SV(z) = su \cdot [1 \dots 1] + H_2(z) \cdot SE(z)$$

$$DV(z) = SV(z) \cdot \begin{bmatrix} 1 \\ \vdots \\ 1 \end{bmatrix} + e_d = SV(z) \cdot \begin{bmatrix} 1 \\ \vdots \\ 1 \end{bmatrix} + SV(z) \cdot e_d = V(z) + H_2(z) \cdot (SE(z) \cdot e_d)$$

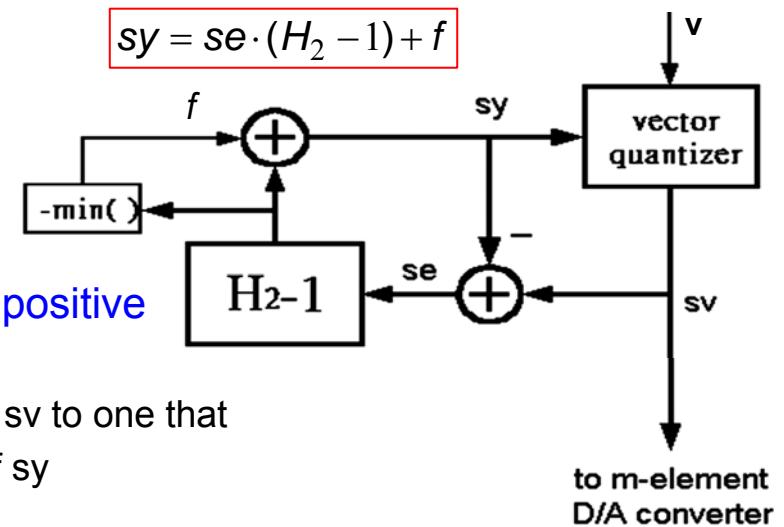
- DAC output is composed of digital input v + a noise term that is shaped by H_2

► Ex. $H_2 = 1 - z^{-1}$

- System is stable

- Selection logic is a circular fashion

- Starting from the element adjacent to that which was mostly used



Vector-Based Mismatch Shaping

- M -element involves M digital noise shaping loops

- For the i th unit element

$$SV_i(z) = F(z) + H(z)E_i(z)$$

$$sv_i(n) = f(n) + [h * se_i](n)$$

* : discrete convolution

- The output of the DAC

$$y(n) = \sum_{i=1}^M u_i(n) = \sum_{i=1}^M sv_i(n)[U + d_i]$$

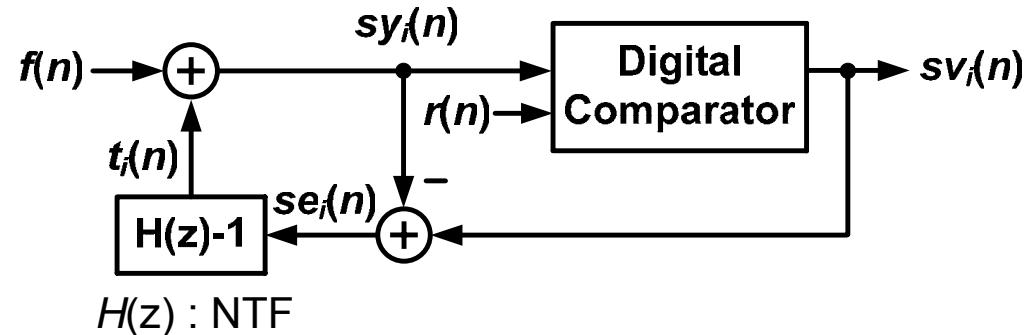
$$= U \sum_{i=1}^M sv_i(n) + \sum_{i=1}^M \{f(n) + [h * se_i](n)\} \cdot d_i$$

$$= U \sum_{i=1}^M sv_i(n) + f(n) \sum_{i=1}^M d_i + h * \sum_{i=1}^M [se_i(n) \cdot d_i] = \text{ideal DAC} + \text{DAC error } e_D(n)$$

$$e_D(n) = h * \sum_{i=1}^M [se_i(n) \cdot d_i]$$

$$sy_i(n) > r(n), sv_i(n)=1$$

$$sy_i(n) < r(n), sv_i(n)=0$$

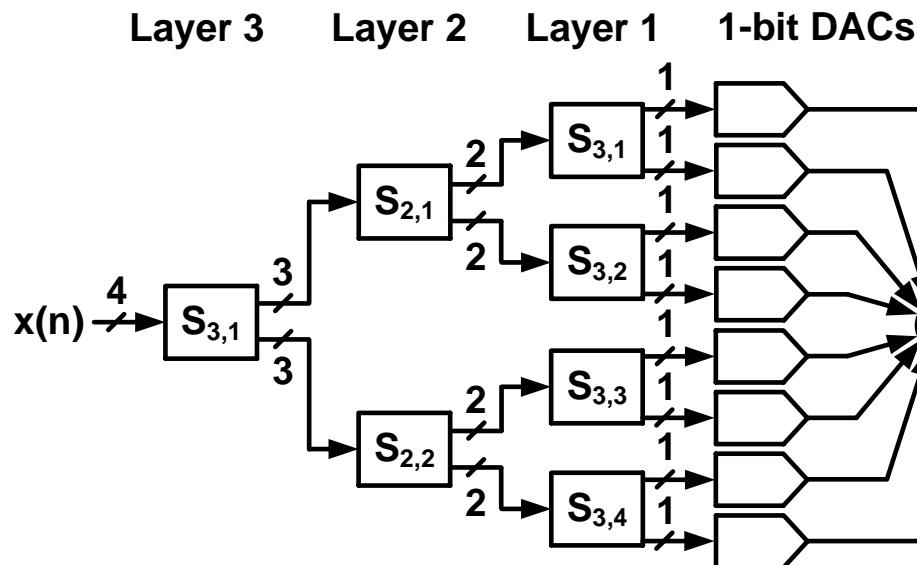


- The DAC error is filtered by $H(z)$
 - Dither may be injected at the inputs of the comparators

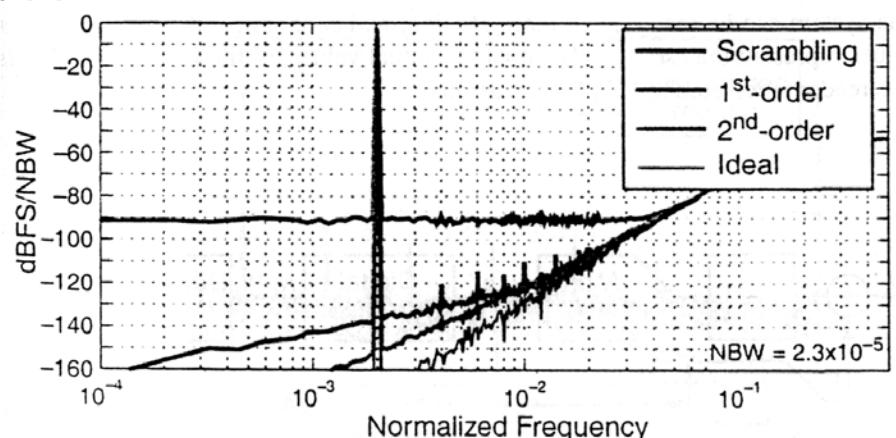
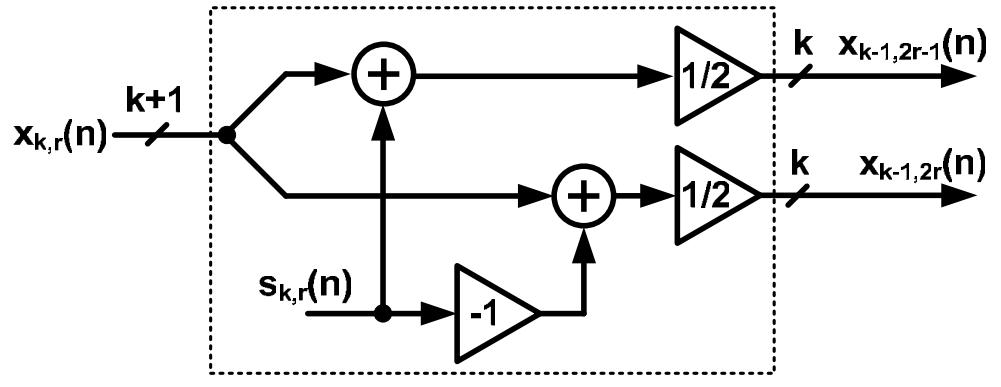


Tree Structure

- $\log_2(M)$ layers of switching blocks
 - 4-bit words for 9 possible values



- Switching Block
 - The sum of the two output signals = the input
 - DAC mismatch noise will be a weighted sum of 1-bit sequence $s_{k,r}(n)$
 - ➡ The sequence $s_{k,r}(n)$ has an L^{th} -order spectral shaping

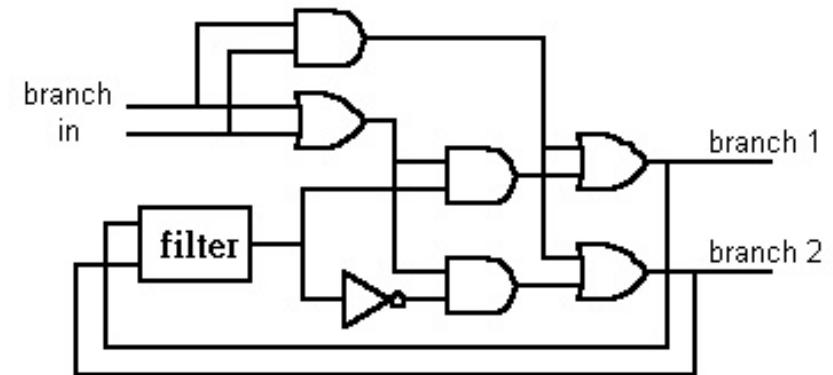
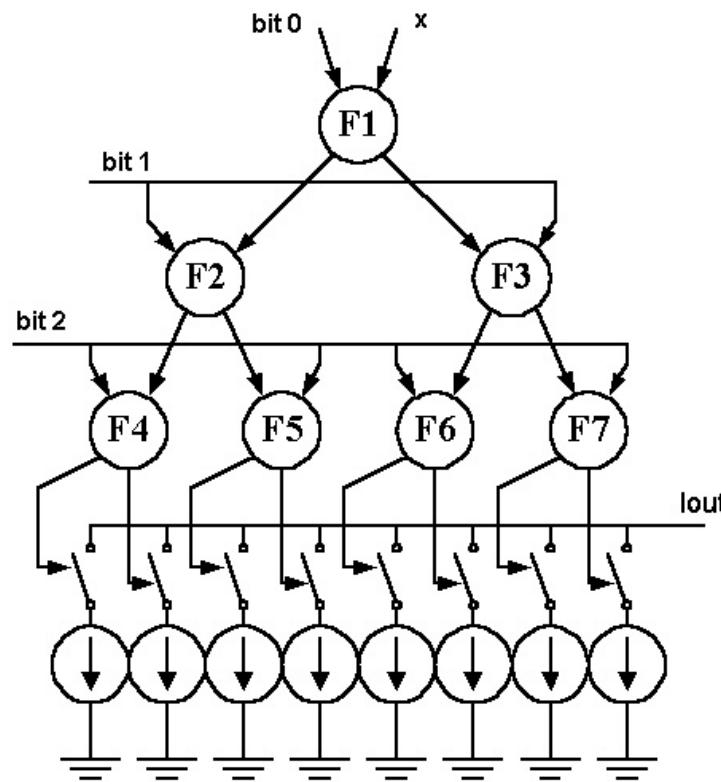


for M elements
comparator : $2M-3$
filter : $2M$



Multibit $\Delta\Sigma$ Modulators

ex. 101



for N unit elements

N-1 nodes
N-1 filters

Drawbacks

- Cumbersome for quantizers larger than 5 bits
- The effectiveness is limited for low oversampling ratio

The Leslie-Singh Architecture

- Second-Order Dual-Quantizer Modulator Case

- Internal delay is assumed in each quantizer

$$STF = z^{-1} \quad NTF = (1 - z^{-1})^2$$

- Limitation of the achievable accuracy

$$\Rightarrow H_1 = 2z^{-1} - z^{-2} \quad H_2 = (1 - z^{-1})^2$$

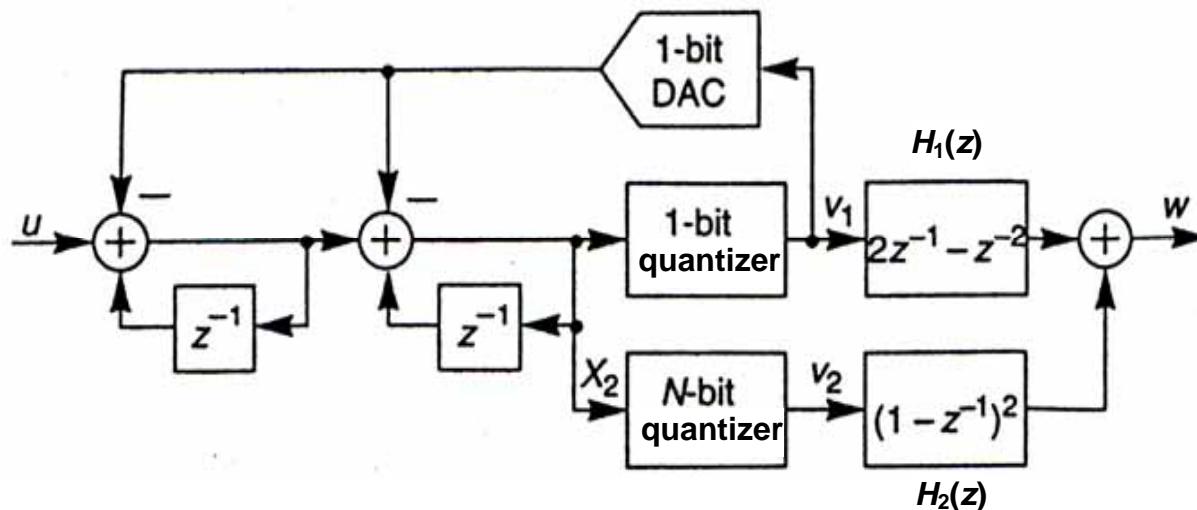
- Mismatch between analog and digital circuits

- NTF depends on the analog components of 1-bit loop
- H_1 and H_2 are digital filter
- Inaccurate H by an amount dH is assumed
- An added noise leaks to the output*

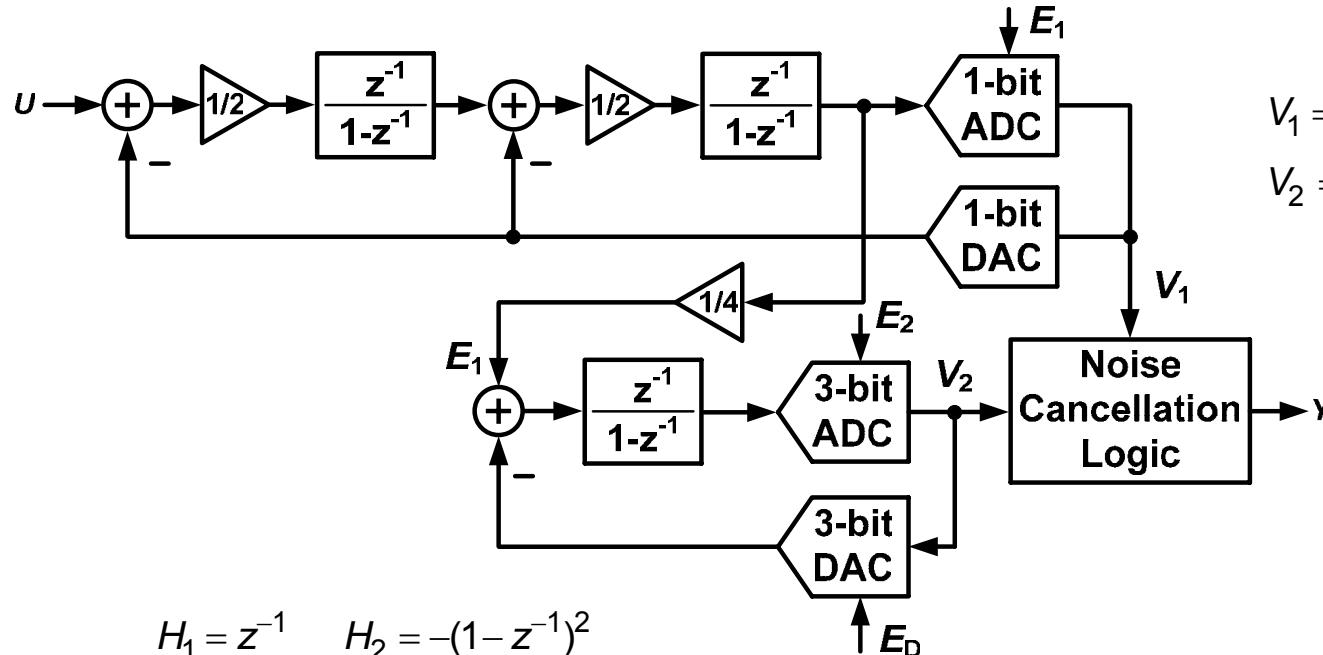
$$\frac{H_1}{H_2} = \frac{1}{H} - 1$$

$$W = \dots + [(H_1 \cdot NTF + H_2 \cdot NTF) - H_2] \cdot E_1$$

$$dE = [(H_1 + H_2) \cdot (H + dH) - H_2] \cdot E_1 = (H_1 + H_2) \cdot dH \cdot E_1 = dH \cdot E_1$$



Dual-Quantizer MASH Structure



$$V_1 = z^{-1} \cdot U + (1-z^{-1})^2 E_1$$

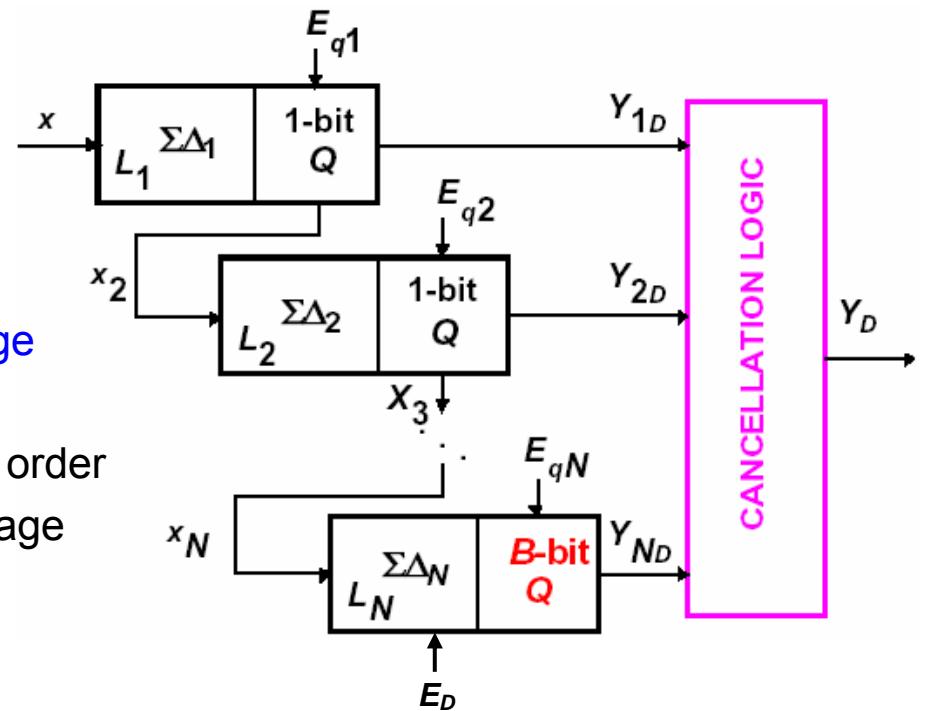
$$V_2 = z^{-1}(E_1 - E_D) + (1-z^{-1})E_2$$

- The nonlinearity of multi-bit DAC in the second stage
 - ▶ will not introduce signal distortion
 - ▶ will be filtered by digital highpass filter H_2

Dual-Quantizer MASH Structure

- In General Form

- One-bit quantization except the final stage
 - $E_{qN}(z)$: quantization error of the N -th stage
- Multibit quantization in the last stage
 - $E_D(z)$: DAC nonlinearity error in the last stage
- $L=L_1+L_2+\dots+L_N$ denotes the total noise-shaping order
 - L_i denotes the order of the i -th modulator stage
- d : digital function in cancellation logic



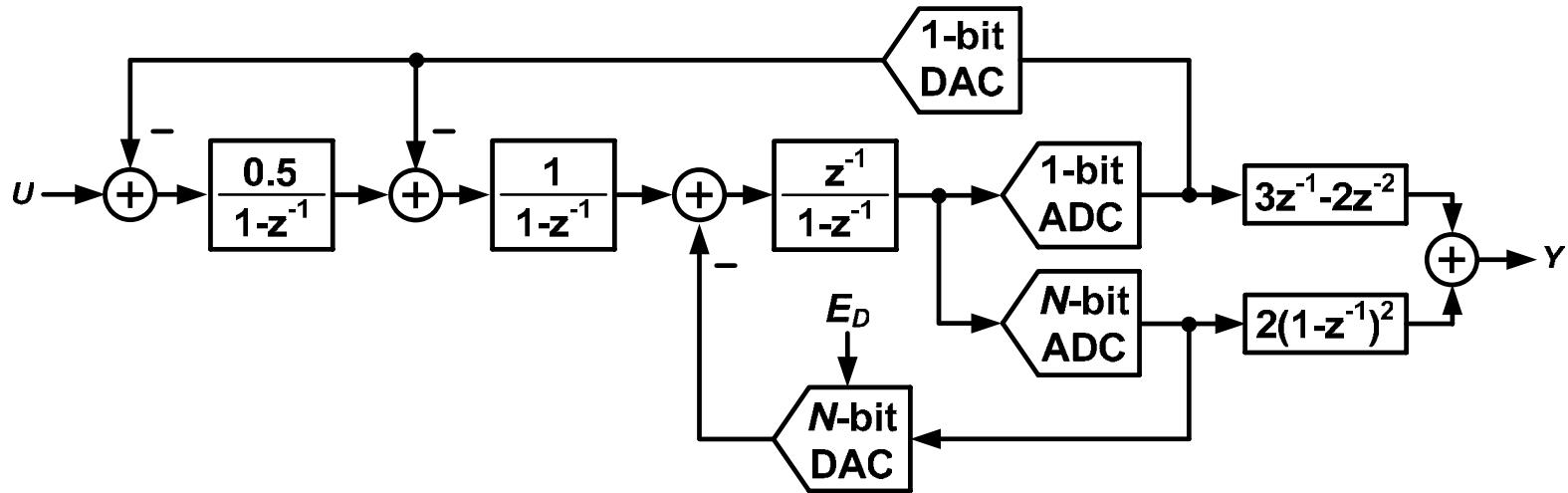
$$Y(z) = z^{-L} X(z) + d(1 - z^{-1})^L E_{qN}(z) - d(1 - z^{-1})^{(L-L_N)} E_D(z)$$

Signal
 ↗
 Lth-order shaping in last-stage quantization error
 ↗
 (L-L_N)th-order shaping in last-stage DAC error

The multibit DAC error is attenuated by the previous stages

Dual-Quantizer Modulators

- Dual-Quantizer Single-Stage Dual-Feedback Structure



$$Y(z) = z^{-1}U(z) + 2(1 - z^{-1})^3 \cdot E_2(z) - 2z^{-1} \cdot (1 - z^{-1})^2 E_D(z)$$

- High linearity in the first and the second integrators
- The nonlinear distortion of N-bit DAC is divided by the product of the transfer functions of the first two integrators

Example Studied of Cascade $\Delta\Sigma$ Modulators

- Example: Design a third-order $\Delta\Sigma$ modulator for audio bandwidth 25KHz

■ 2-1 architecture is the most robust implementation (1-1-1 and 1-2)

■ Take $b=2$

$$Y_1(z) = z^{-2}X(z) + (1 - z^{-1})^2 \cdot E_{Q1}(z)$$

$$Y_2(z) = z^{-1}X_2(z) + (1 - z^{-1}) \cdot E_{Q2}(z)$$

$$X_2(z) = \beta \cdot [(1 - \lambda)Y_1(z) - E_{Q1}(z)]$$

► λ : error mixing coefficient

► β : error gain coefficient

$$Y(z) = [z^{-2}H_1(z) + z^{-3}H_2(z)\beta(1 - \lambda)]X(z)$$

$$+ \{(1 - z^{-1})^2[H_1(z) + z^{-1}H_2(z) \cdot \beta(1 - \lambda)] - z^{-1}H_2(z) \cdot \beta\} \cdot E_{Q1}(z)$$

$$+ (1 - z^{-1})H_2(z)E_{Q2}(z)$$

■ Choose

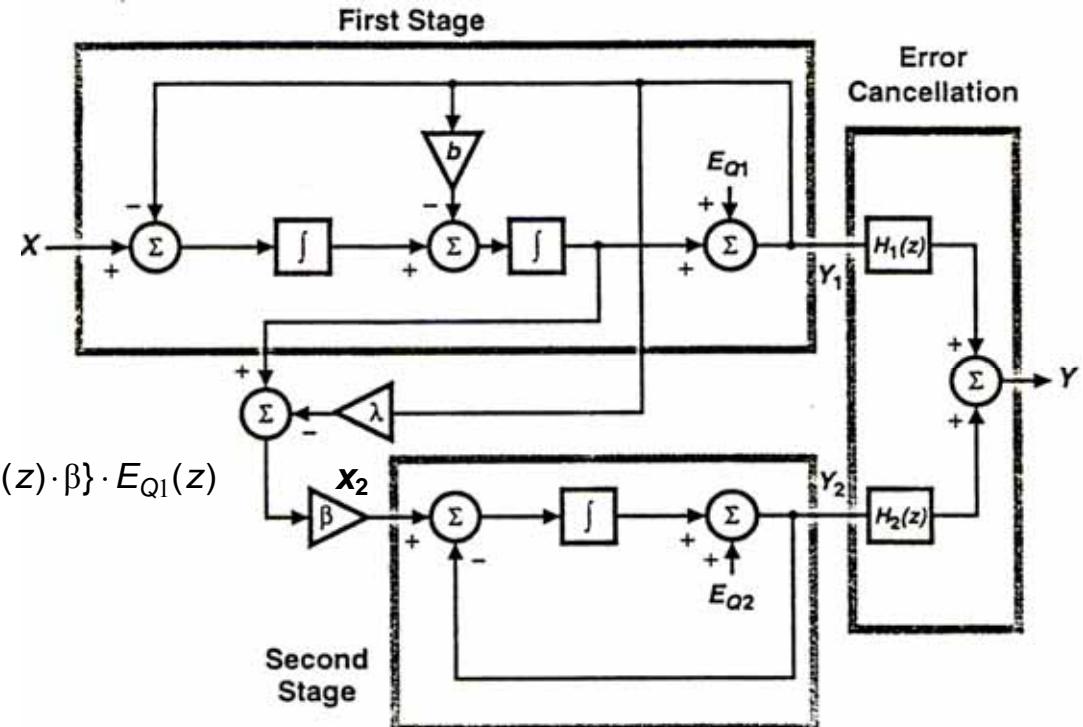
$$H_1(z) = z^{-1} - (1 - \hat{\lambda})(1 - z^{-1})^2 z^{-1}$$

$$H_2(z) = \frac{1}{\hat{\beta}}(1 - z^{-1})^2$$

► $\hat{\lambda}$ and $\hat{\beta}$ are digital estimates of the analog coefficients λ and β , respectively

► Mismatch between the analog components and their digital counterparts

◆ Degrade the performance of modulator



Example Studied of Cascade $\Delta\Sigma$ Modulators

► Define the mismatch errors

$$\blacktriangleright \beta = \hat{\beta}(1 + \delta_\beta)$$

$$\blacktriangleright \lambda = \hat{\lambda}(1 + \delta_\lambda)$$

► The modulator output $Y(z) = z^{-3} X(z) - \delta_\beta (1 - z^{-1})^2 z^{-1} E_{Q1}(z) + \frac{1}{\hat{\beta}} (1 - z^{-1})^3 E_{Q2}(z)$

► Typical values of $\hat{\beta}$: 0.25~0.5

► Insensitive to mismatching error in estimating λ

► Errors in estimating β cause noise from the first stage $E_{Q1}(z)$

● Leaks to the output with second-order shaping

► The baseband noise power $P_n = \delta_\beta^2 \frac{\pi^4}{5 \cdot \text{OSR}^5} \sigma_{Q1}^2 + \frac{1}{\hat{\beta}^2} \frac{\pi^6}{7 \cdot \text{OSR}^7} \sigma_{Q2}^2$

● σ_{Q1}^2 and σ_{Q2}^2 are quantization noise powers of the first- and second-stage quantizers

► To limit the increase in the baseband noise < 1dB above that predicted with perfect matching

$$\bullet 10 \log\left(\frac{P_n}{\frac{1}{\hat{\beta}^2} \frac{\pi^6}{7 \cdot \text{OSR}^7} \sigma_{Q2}^2}\right) < 1 \Rightarrow \delta_\beta < \sqrt{\frac{5(10^{0.1} - 1)}{7}} \frac{\pi}{\hat{\beta} \cdot \text{OSR}} < 0.43 \frac{\pi}{\hat{\beta} \cdot \text{OSR}}$$

● Ex. $\beta=0.25$ and $\text{OSR}=80 \Rightarrow$ the mismatch error $\delta_\beta < 6.8\%$



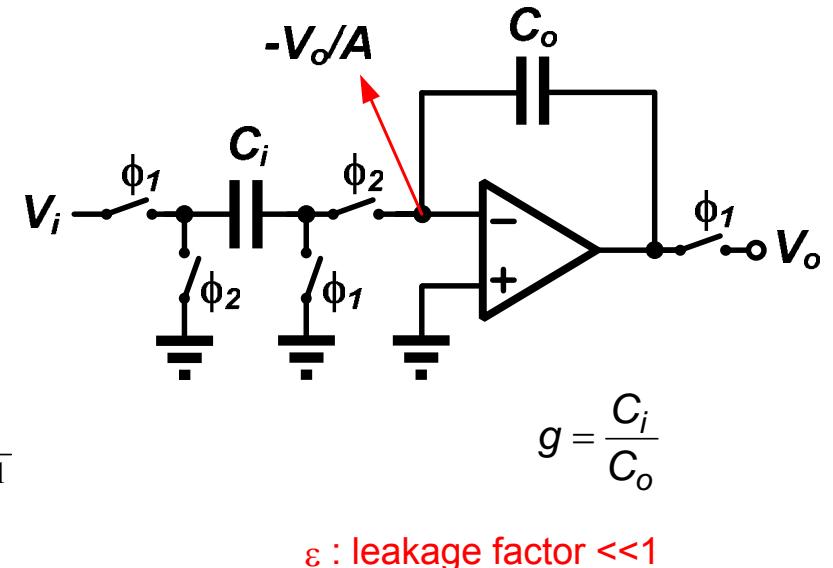
Example Studied of Cascade $\Delta\Sigma$ Modulators

Integrator Leakage

- Finite opamp open loop gain at dc A
 - Increase the in-band noise power

Integrator transfer function

$$\begin{aligned} H(z) &= \frac{z^{-1}}{\left[\frac{C_o}{C_i}\left(1+\frac{1}{A}\right) + \frac{1}{A}\right] - \frac{C_o}{C_i}\left(1+\frac{1}{A}\right)z^{-1}} \\ &\approx \frac{gz^{-1}}{1 - \frac{A+1}{A+1+g}z^{-1}} = \frac{gz^{-1}}{1 - (1 - \frac{g}{A+1+g})z^{-1}} = \frac{gz^{-1}}{1 - (1 - \varepsilon)z^{-1}} \end{aligned}$$



- The modulator output $Y(z) = z^{-3}X(z) + z^{-2}[(1-z^{-1})(\varepsilon_1 + \varepsilon_2) + z^{-1}\varepsilon_1\varepsilon_2]E_{Q1}(z)$
 $+ \frac{1}{\beta}[(1-z^{-1})^3 + (1-z^{-1})^2z^{-1}\varepsilon_3]E_{Q2}(z)$
- The baseband noise power $P_n = [\frac{\varepsilon_1^2\varepsilon_2^2}{\text{OSR}} + (\varepsilon_1 + \varepsilon_2)^2 \frac{\pi^2}{3 \cdot \text{OSR}^3}] \sigma_{Q1}^2 + \frac{1}{\hat{\beta}^2} [\varepsilon_3^2 \frac{\pi^4}{5 \cdot \text{OSR}^5} + \frac{\pi^6}{7 \cdot \text{OSR}^7}] \sigma_{Q2}^2$
- To limit the increase in the baseband noise < 1dB beyond that obtained with ideal integrators
 - $\varepsilon_1, \varepsilon_2 < \sqrt{\frac{3(10^{0.1} - 1)}{7}} \frac{\pi^2}{\hat{\beta} \cdot \text{OSR}^2} < 0.33 \frac{\pi^2}{\hat{\beta} \cdot \text{OSR}^2}$ $\varepsilon_3 < \sqrt{\frac{5(10^{0.1} - 1)}{7}} \frac{\pi}{\text{OSR}} < 0.43 \frac{\pi}{\text{OSR}}$
 - Ex. $\hat{\beta} = 0.25$, OSR=80, $\varepsilon_1, \varepsilon_2 < 0.002$, $\varepsilon_3 < 0.017$
 - Opamp open loop gains > 500 and 59 for the first and second stages

Example Studied of Cascade $\Delta\Sigma$ Modulators

Opamp open loop gain required

Let $g=1$ and $A_{01}=A_{02}>>1$ ($\varepsilon_1=\varepsilon_2=\varepsilon$)

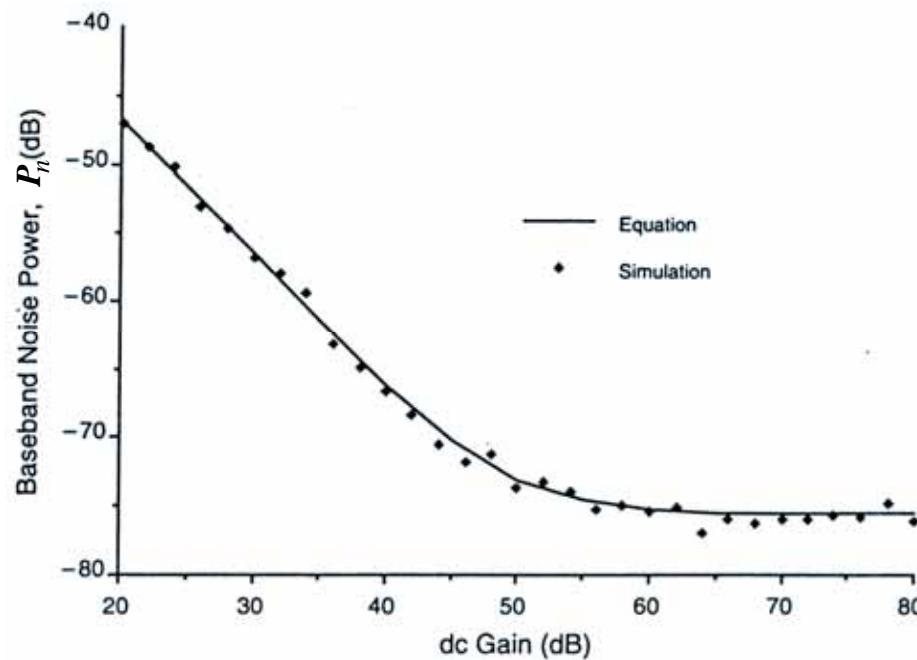
The transfer function of the first stage can be expressed as

$$Y_1(z) = z^{-2} X(z) + [(1 - z^{-1})^2 + 2\varepsilon \cdot z^{-1}(1 - z^{-1}) + \varepsilon^2 \cdot z^{-2}] \cdot E_{Q1}(z)$$

The resulting baseband quantization error power

$$P_n = \left(\frac{\varepsilon^4}{\text{OSR}} + \frac{4\pi^2\varepsilon^2}{3 \cdot \text{OSR}^3} \right) \sigma_{Q1}^2$$

Approximately 60dB of dc gain is required for 12-bit dynamic range for the second-order modulator



Example Studied of Cascade $\Delta\Sigma$ Modulators

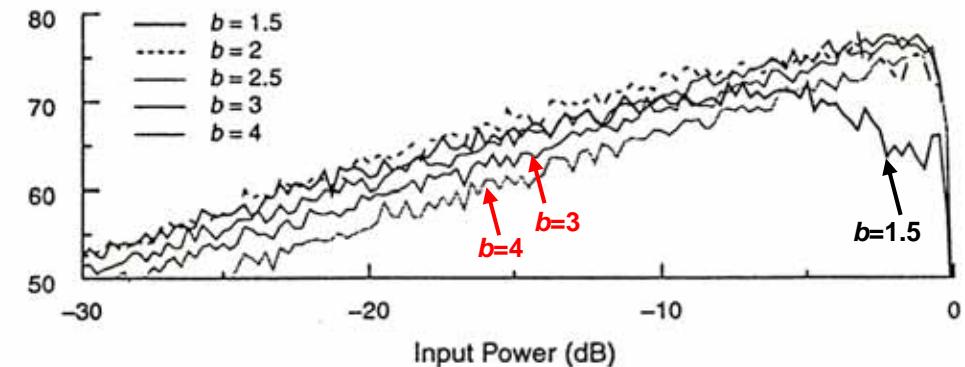
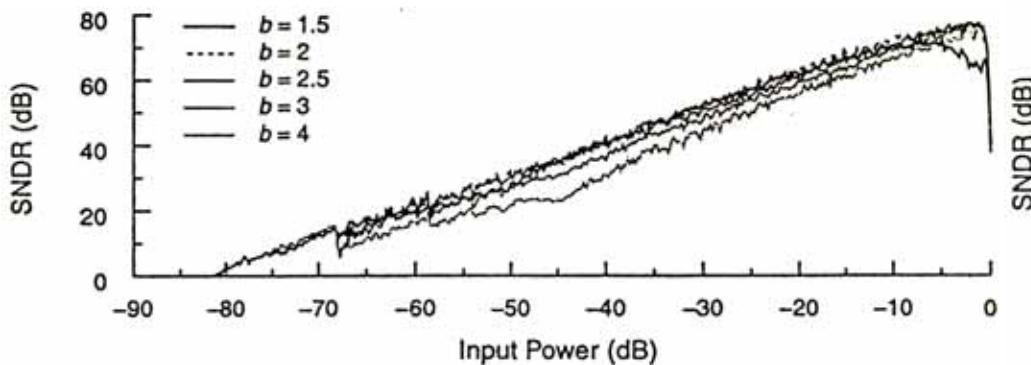
- Second-Order Low-Pass $\Delta\Sigma$ Modulator

- Determine the feedback factor b

- Significantly impact the peak SNDR and overload level
 - The dynamic range can be increased by maximizing the feedback
 - $V_{in} = -6 \text{ dB}$, $f_{in} = 1.01 \text{ KHz}$, $f_s = 2.56 \text{ MHz}$, OSR=80 with $b=1.5\sim4$
 - $2 < b < 4$ peak SNDR and overload level are high
 - $b \geq 3$ signal dependence
 - $b = 2$ strong tones appear near the zero input level
 - Take $b=2.5$ due to the reduction in spectral tones

- Root locus method predicts the modulator unstable for $b \geq 2.5$

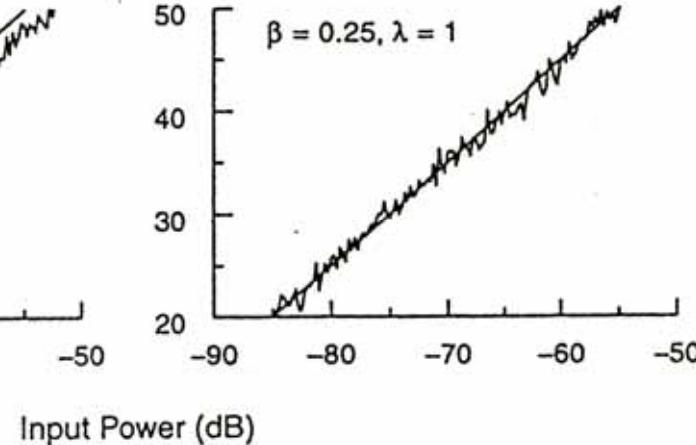
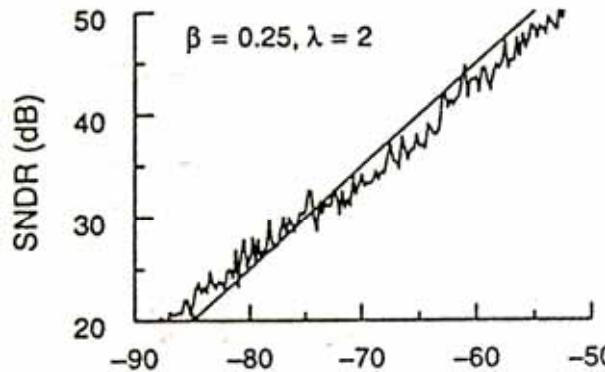
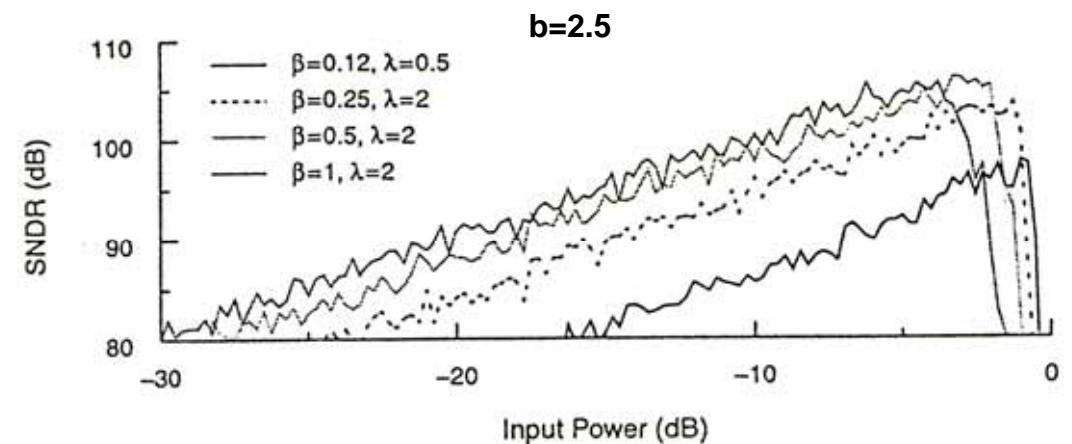
L. Williams and B. A. Wooly, "A third-order sigma delta modulator with extended dynamic range," IEEE J. SSC, vol. SC-29, pp. 193-202, Mar.1990.



Example Studied of Cascade $\Delta\Sigma$ Modulators

Determine the coefficients β and λ

- ➡ $\beta=0.12$ and $\lambda=0.5 \Rightarrow$ the highest overload level -0.65dB
 - ▶ Increase the quantization noise floor
- ➡ $\beta=0.25$ and $\lambda=2.0 \Rightarrow$ the highest overload level -1.0dB
 - ▶ the quantization noise floor = -105dB < -100dB
- ➡ $\beta=0.5, \lambda=2.0$ and $\beta=1.0, \lambda=2.0 \Rightarrow$ lower noise floor, lower overload level
- ➡ $\beta=0.25$ and $\lambda=1.0$
 - ▶ Lower overload level = -1.3dB
 - ▶ Very nearly independent of signal power



Example Studied of Cascade $\Delta\Sigma$ Modulators

- Investigation on the Occurrence of Spectral Tones

 - $b=2.5$, $\beta=0.25$ and $\lambda=1.0$

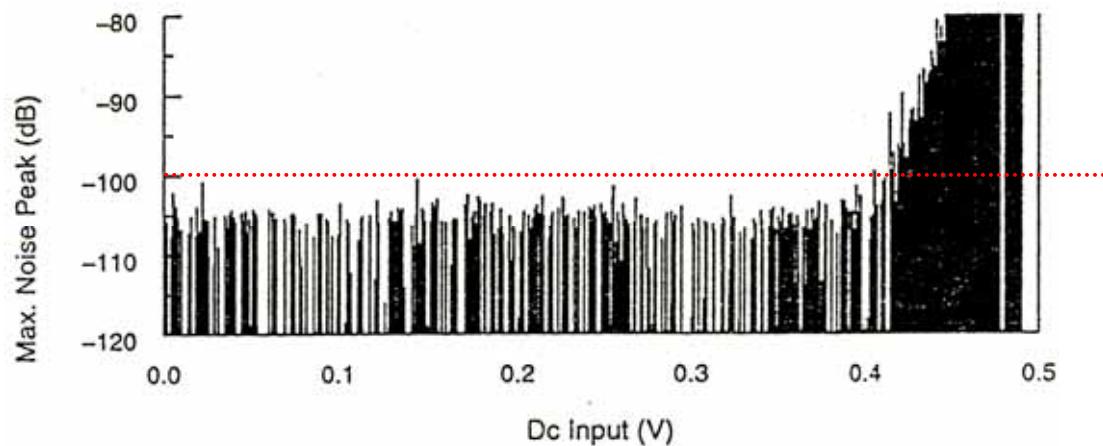
 - Feedback reference levels = ± 0.5

 - In fine increments across the positive input range of the modulator

 - The power of the strongest spectral component were recorded

 - Dc input < 0.416

 - No tones whose power > -100dB



Example Studied of Cascade $\Delta\Sigma$ Modulators

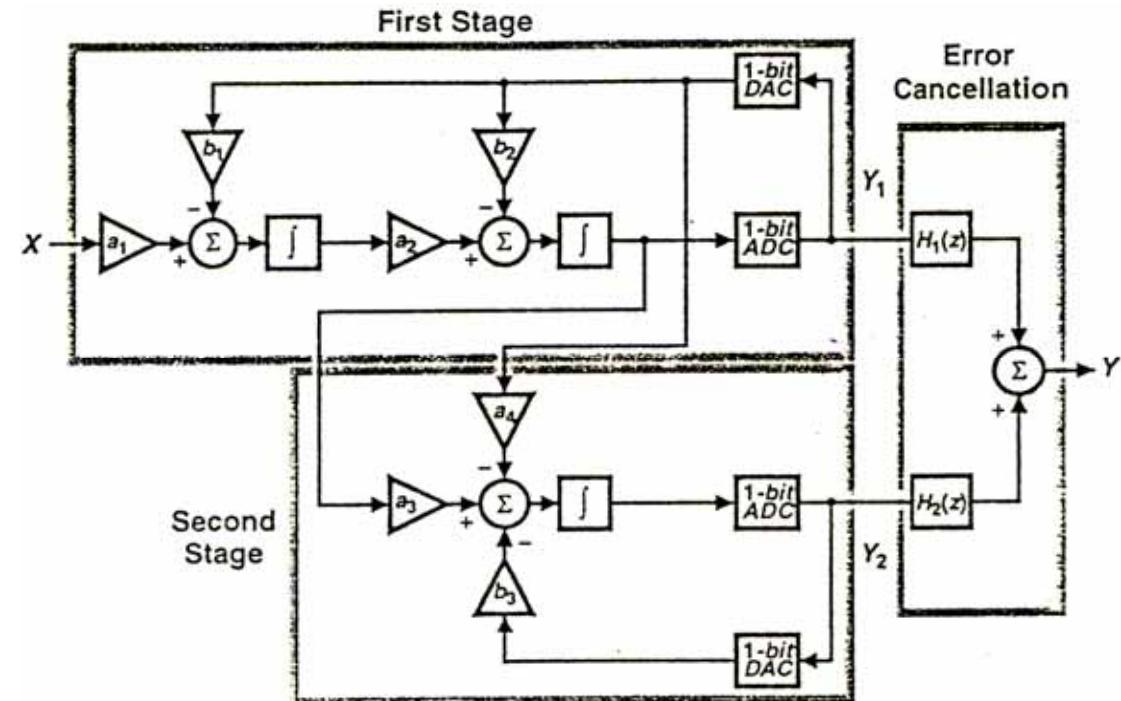
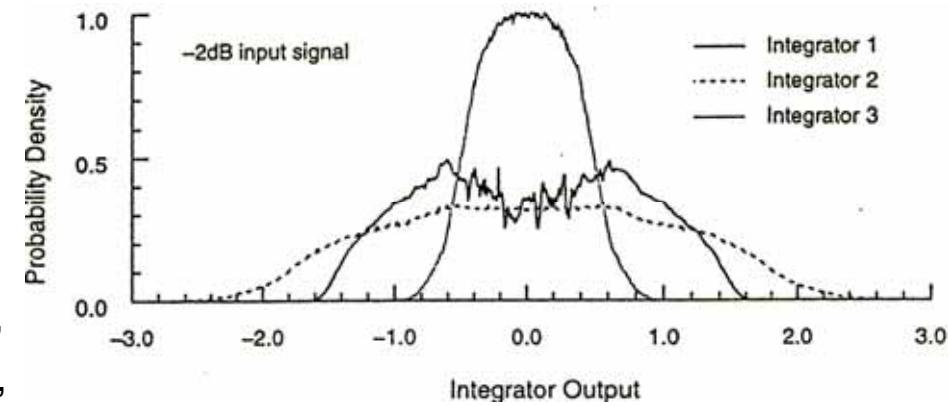
Signal Scaling

- Limit the output swing of integrators not to exceed the linear range
- -2dB input power relative to an input with an amplitude of ± 0.5
 - ▶ The output swings of the first, the second, and the third integrators are ± 1.66 , ± 2.98 , and ± 1.30 respectively
 - ▶ Assume maximum linear output range equal to a fraction η of the feedback reference levels
 - The feedback factors

$$b_1 < \frac{\eta}{2 \times 1.66}$$

$$b_2 < \frac{\eta}{2 \times 2.98}$$

$$b_3 < \frac{\eta}{2 \times 1.30}$$



Example Studied of Cascade $\Delta\Sigma$ Modulators

■ Integrator gains

► From the standpoint of circuit noise, power dissipation and die area

► Sampling network can be shared with feedback signal

$$\bullet \quad a_1 = b_1$$

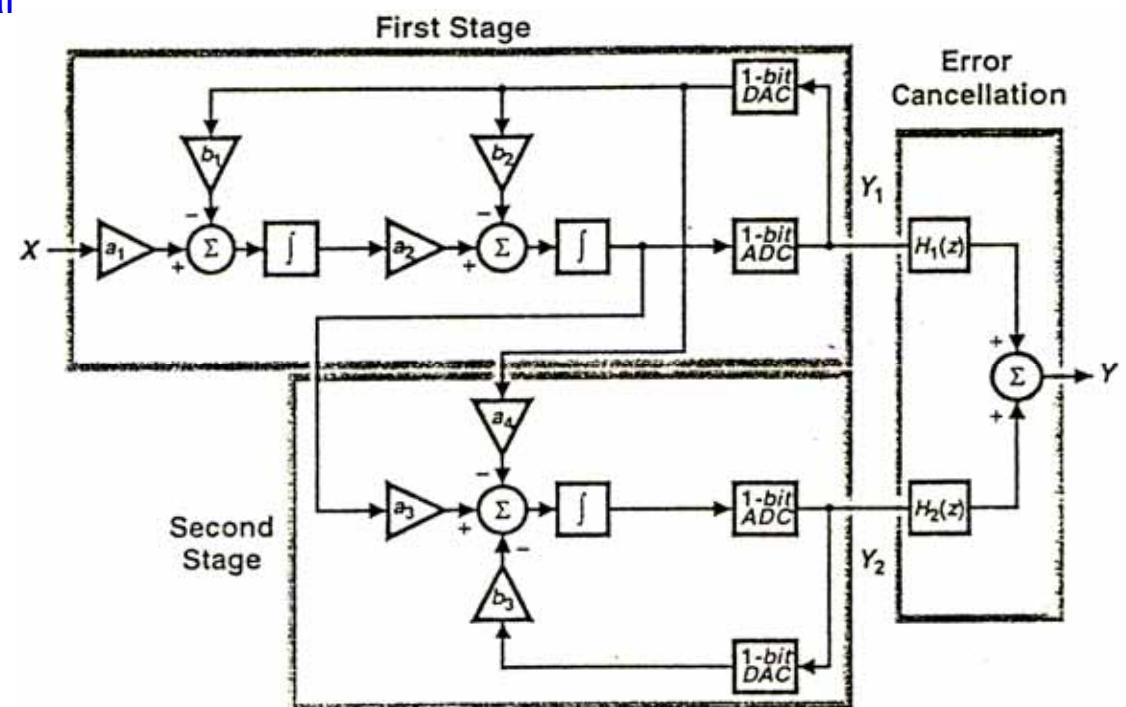
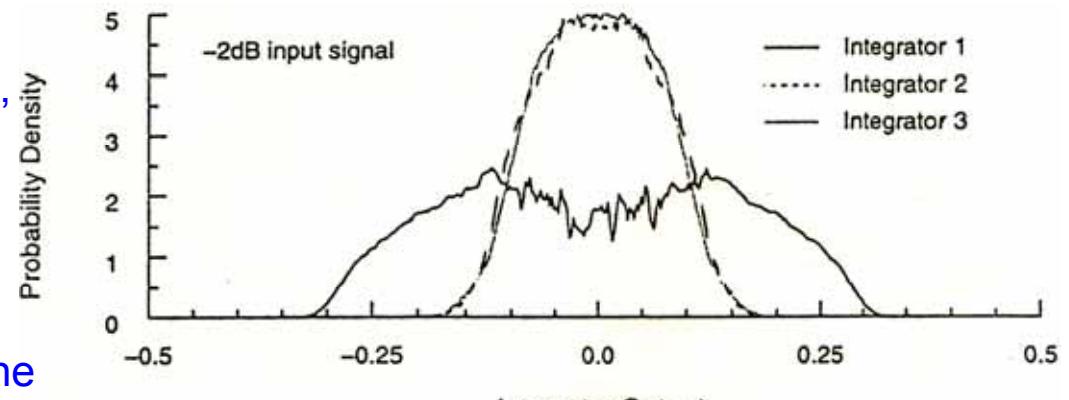
► Assume the feedback levels from the outputs of two stages are identical

$$\bullet \quad a_2 = \frac{1}{b} \times \frac{b_2}{b_1}$$

$$a_3 = b\beta \times \frac{b_3}{b_2}$$

$$a_4 = \lambda\beta \times b_3$$

Integrator gain	value
a_1	1/5
b_1	1/5
a_2	1/3
b_2	1/6
a_3	3/4
a_4	1/20
b_3	1/5

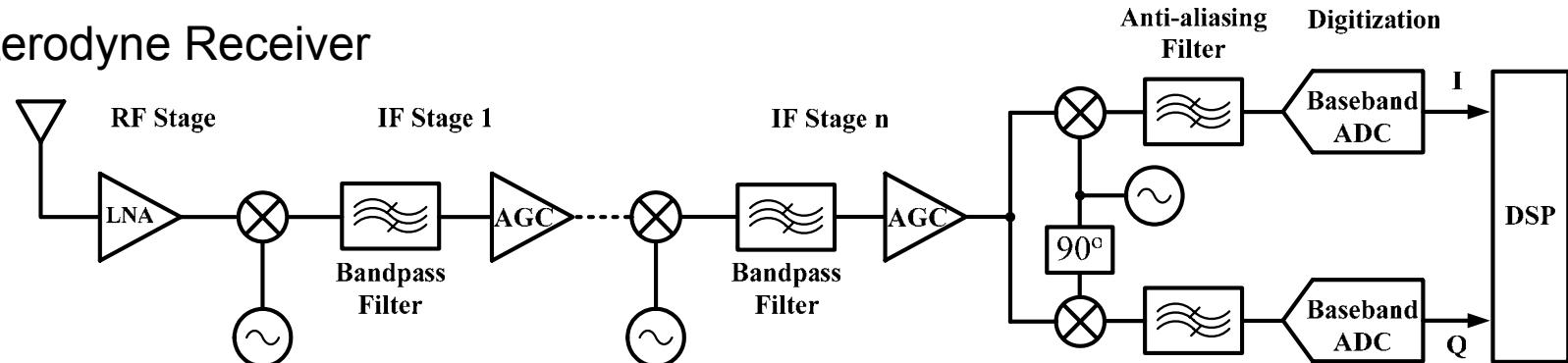


Bandpass Delta-Sigma Modulation

Department of Electrical Engineering

Receiver Architectures

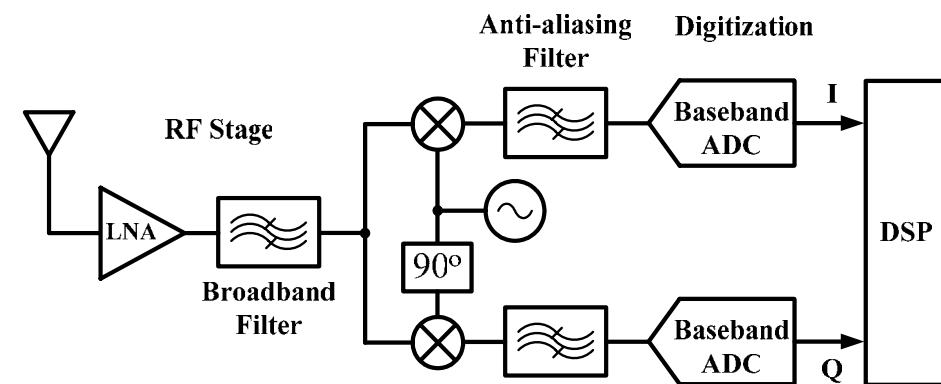
● Superheterodyne Receiver



- Too much analog circuits

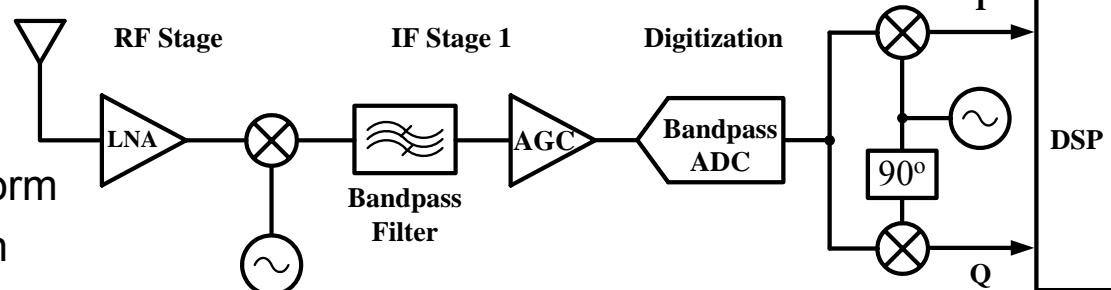
● Direct Conversion — Zero IF

- Lowpass $\Delta\Sigma$ modulators
- Minimize the number of the IF stage
- Be suitable for integrated system
- Suffers from the low frequency noise
 - ➡ I/Q mismatch, flicker noise, offset



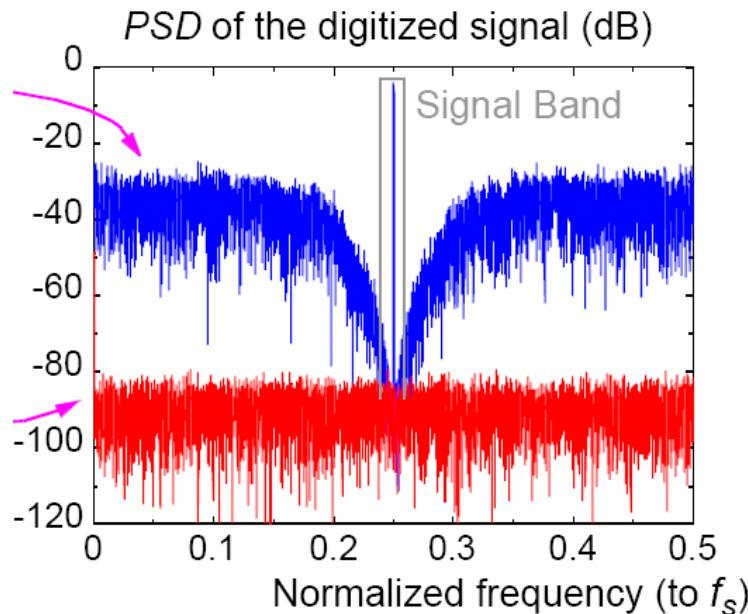
● Single IF Receiver

- Bandpass $\Delta\Sigma$ modulators
 - ➡ high resolution
 - ➡ IF mixing realized in digital form
 - ➡ narrow band data conversion



Bandpass Analog-to-Digital Converter

- Bandpass Delta-Sigma Modulators

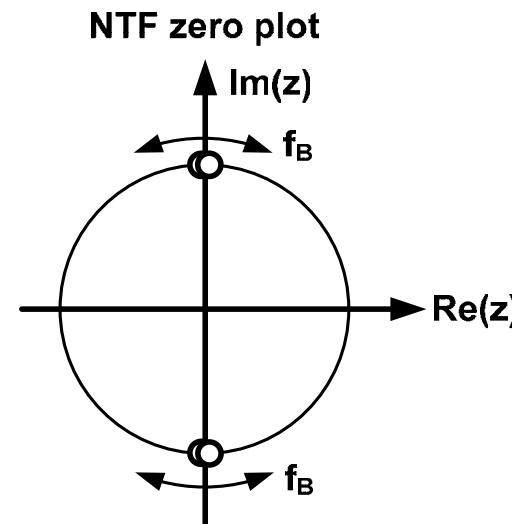
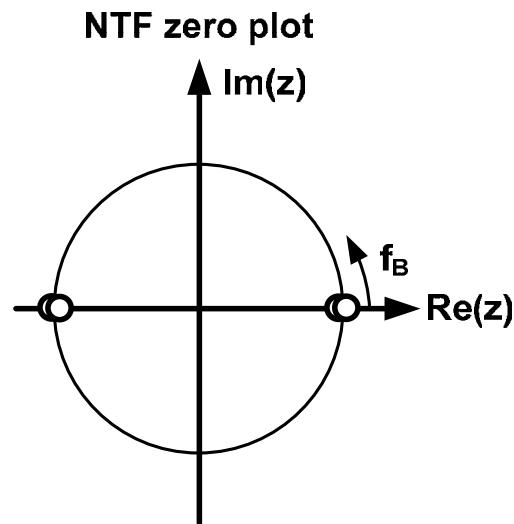


- Quantization noise is small in signal band, rather the whole Nyquist band
- Oversampling and noise-shaping reduce the noise in the signal band
- In-band
 - $\rightarrow \lim_{f \rightarrow f_0} |NTF| = 0$
- Out-of-band
 - $\rightarrow |NTF| < 1.6$ for stability

- Advantages
 - ➔ Eliminate one or more analog downconversion operations
 - ➔ Separate the signal from various low-frequency noise

Bandpass Delta-Sigma Modulators

- Bandpass Modulator has NTF zeros on $z = \pm j$
 - $f_0 = f_s/4$
 - n NTF zeros requires $(2n)^{\text{th}}$ -order converter due to complex conjugate zeros
 - $\text{OSR} = f_s/(2f_B)$
 - f_B : two-sided bandwidth
 - Lowpass
 - Minimum sample rate at the output of the decimator is $2f_B$
 - Bandpass
 - Minimum sample rate at the output of the decimator is f_B
 - The data can be decimated by $2 \times \text{OSR}$



Pseudo N-path Transformation

Pseudo 2-path Transformation

- Lowpass Modulator → Bandpass Modulator

- $z \rightarrow -z^2$

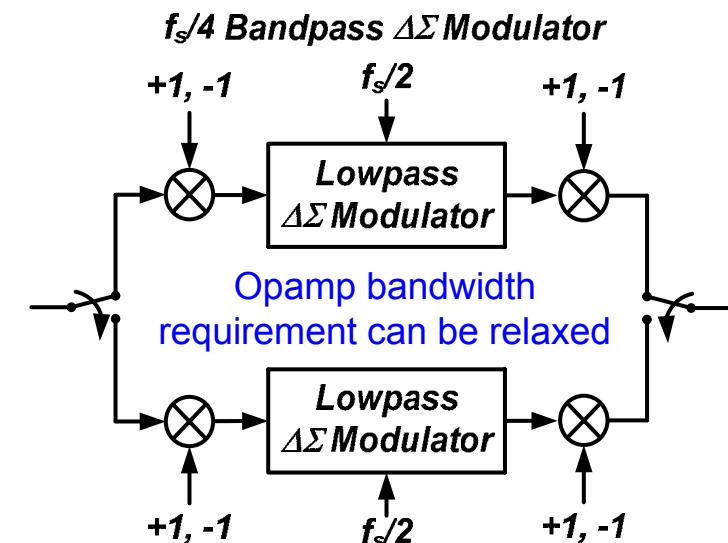
$$\left. \frac{z^{-1}}{1-z^{-1}} \right|_{z=e^{j2\pi f}} \rightarrow \left. \frac{z^{-2}}{1+z^{-2}} \right|_{z=e^{j2\pi f}}$$

- The zeros of NTF

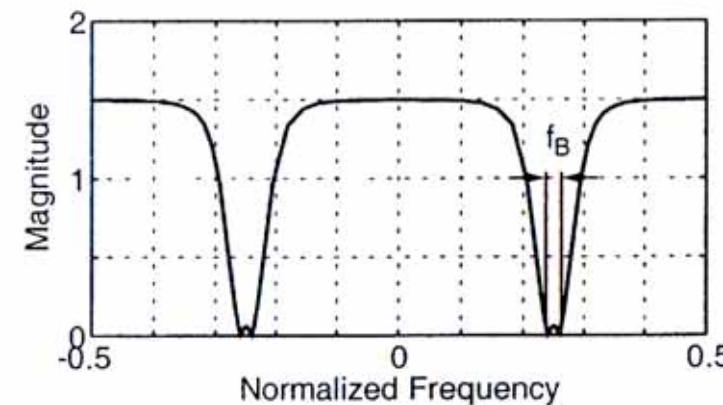
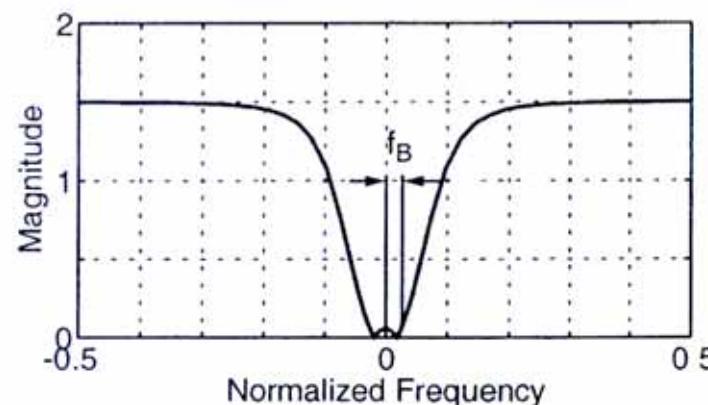
- $f = 0 \rightarrow f = \frac{1}{4} \times f_s$

- All features of LP Modulator are preserved

- SNR, DR, Stability



Each lowpass modulator in 2-path architecture is subsampled with alternating polarities



Influence of Bandpass Noise-Shaping

- NTF

$$NTF = [1 - 2\cos(2\pi f_0 T_s)z^{-1} + z^{-2}]^L$$

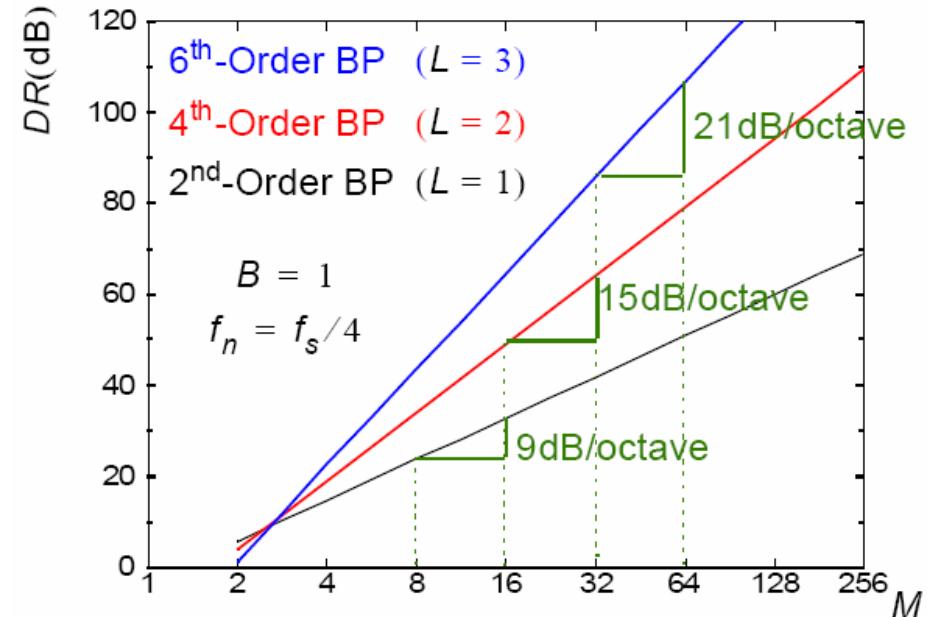
- In-band quantization noise power

$$P_Q = \frac{[\sin(2\pi f_0 T_s)]^{2L} \pi^{2L} X_{FS}^2}{12(2^B - 1)^2 (2L+1) M^{(2L+1)}}$$

- Dynamic range

$$DR \approx \frac{3(2^B - 1)^2 (2L+1) M^{(2L+1)}}{2\pi^{2L} [\sin(2\pi f_0 T_s)]^{2L}}$$

$$= \frac{3(2^B - 1)^2 (2L+1) M^{(2L+1)}}{2\pi^{2L}} \quad \text{for } f_0 = f_s/4$$



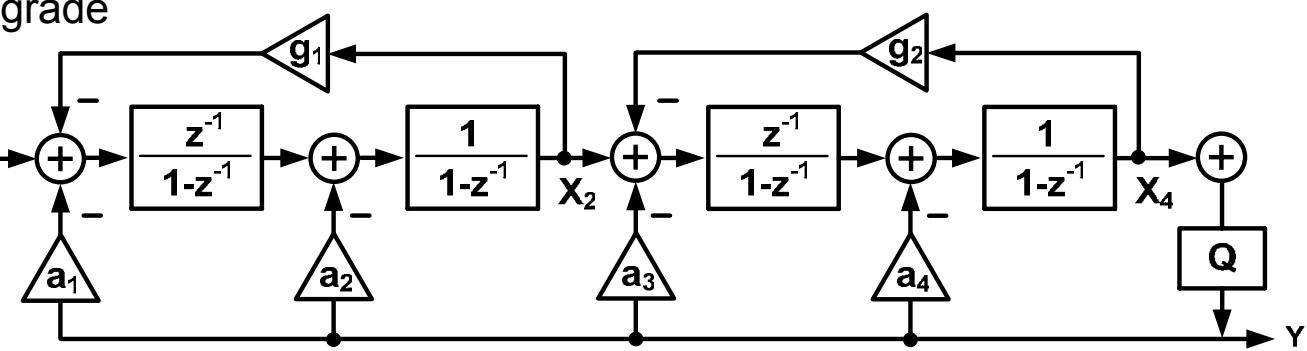
- Standard Feedback Topology

- Quality factor Q in the resonator (finite dc gain in the integrator)

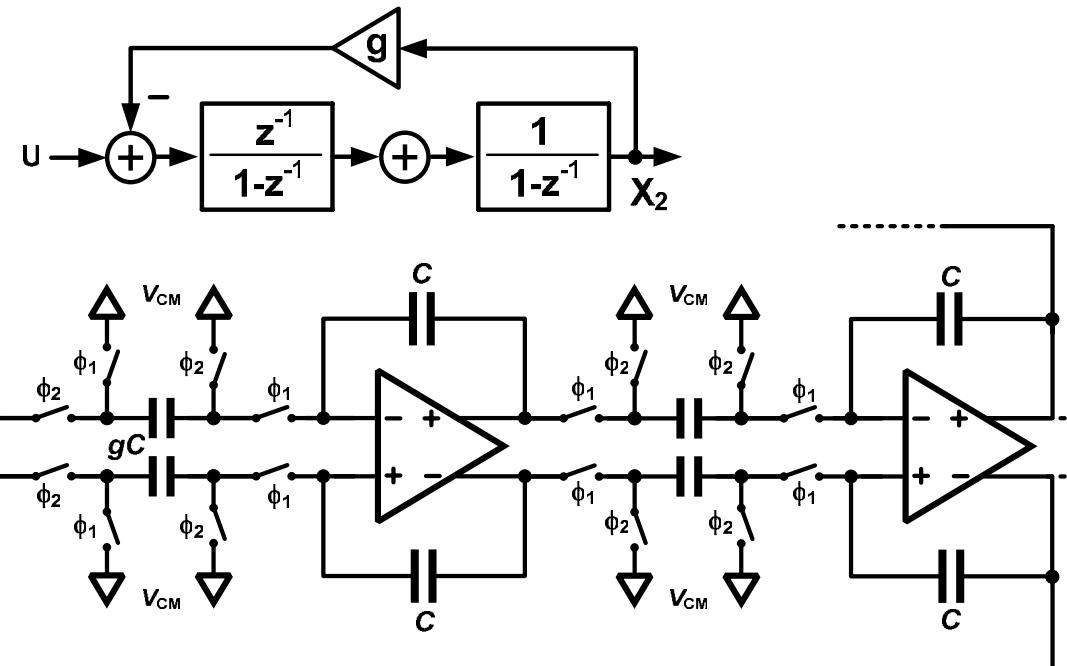
→ $Q < f_0/f_B \rightarrow$ SNR degrade

→ OSR↑ → Q↑

→ $Q > 100$ (readily)



Lossless Discrete Integrator (LDI)



- The poles of the LDI loop lies on the unit circle

$$1 - (2 - g)z^{-1} + z^{-2} = 0$$

$$z = \sigma \pm j\sqrt{1 - \sigma^2} \text{ where } \sigma = 1 - g/2$$

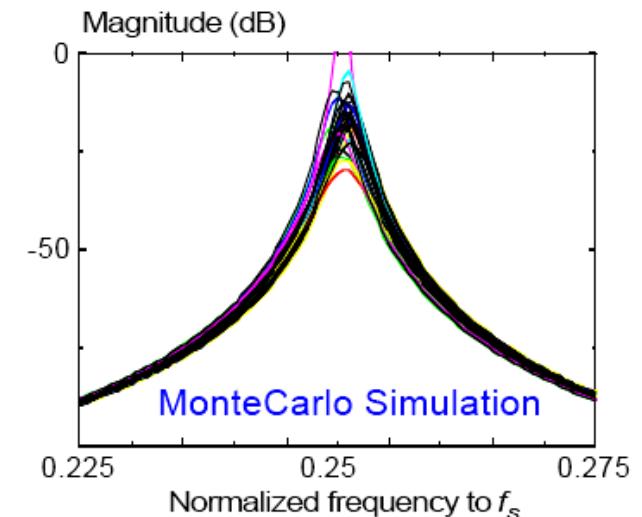
$$|\sigma| \leq 1 (0 \leq g \leq 4) \Rightarrow Q \rightarrow \infty$$

- Arbitrary resonator frequency

- Requires the use of two opamps

$$(u - g \cdot x_2) \frac{z^{-1}}{(1 - z^{-1})^2} = x_2$$

$$\Rightarrow \frac{x_2}{u} = \frac{z^{-1}}{1 - (2 - g)z^{-1} + z^{-2}}$$

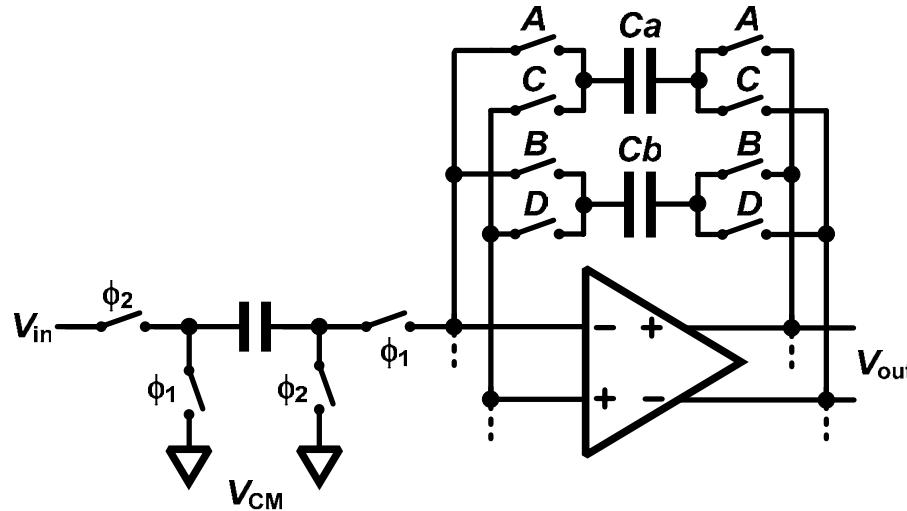


$$\omega_0 = \cos^{-1}(\sigma)$$

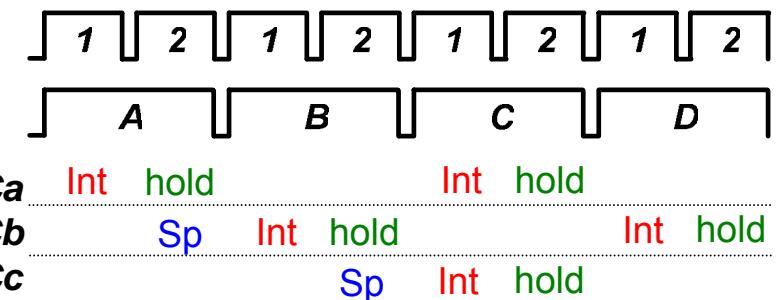
1% shift in capacitor ratio \rightarrow 0.6% shift in ω_0

Resonator with a Single Opamp

- Pseudo 2-Path Switched-Capacitor $fs/4$ Resonator



$$\frac{V_{out}}{V_{in}} = \frac{z^{-1}}{1+z^{-2}} \Rightarrow V_{out} = V_{in}z^{-1} - V_{out}z^{-2}$$

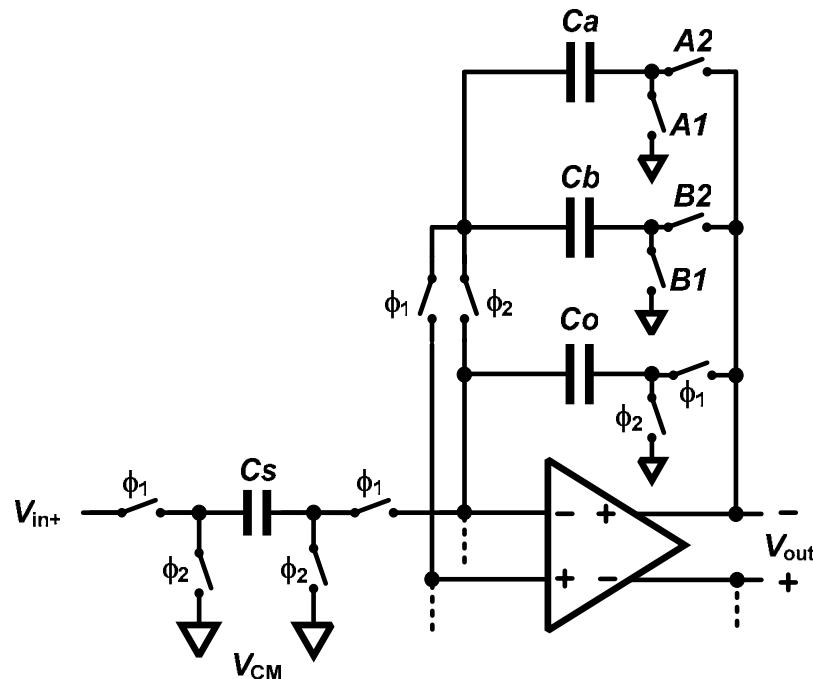


- Mismatch in the paths (Ca and Cb capacitors) causes the ckt to be periodically time-varying
 - Mixing of the signal of $fs/4$ and its harmonics
 - Mixing of the signal with $fs/2 \rightarrow$ image signal
- $fs/4$ clocks (A, B, C, and D) leak into the signal band
 - A tone at band-center

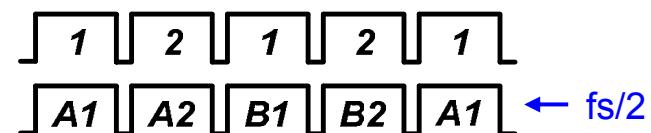
Resonator with Reduced Sensitivity to Capacitor Mismatch

- 2-Path Switched-Capacitor fs/4 Resonator

- Suppose the opamp gain is high enough
- The conversion of charge to voltage is performed by the C_o capacitor
- Capacitors C_a and C_b are used for charge storage
- Avoid the spur-generating mechanism (fs/2)



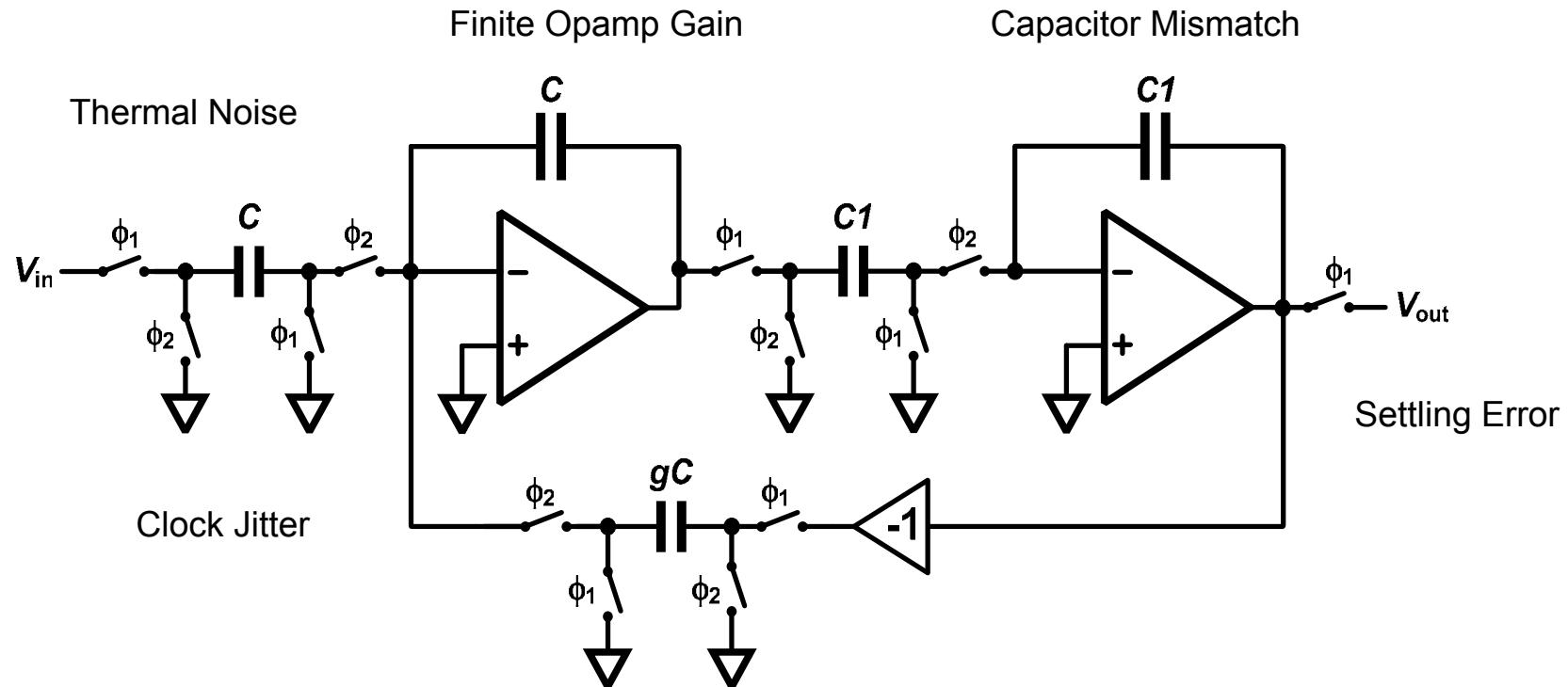
$$\frac{V_{out}}{V_{in}} = \frac{(C_s/C_o)z^{-1}}{1+z^{-2}}$$
$$\Rightarrow V_{out} = (C_s/C_o) \cdot V_{in}z^{-1} - V_{out}z^{-2}$$



- Double sampling can be used to halve the number of opamps

Circuit Errors

- Switched-Capacitor LDI



Error Sources in SC Circuits

- Finite Opamp DC Gain (A_0)

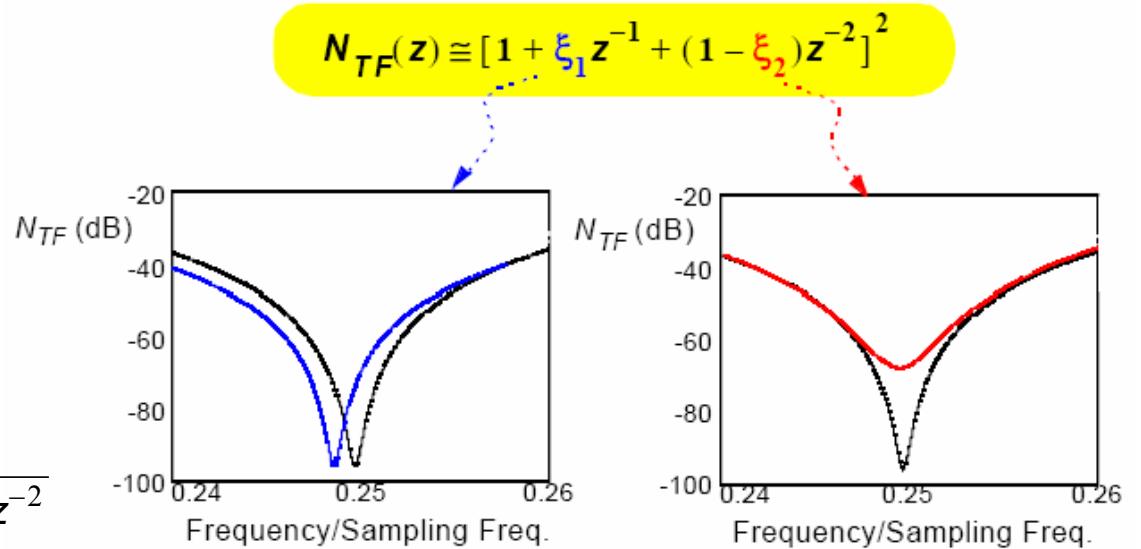
- Integrator

$$I(z) = \frac{(1-\delta)z^{-1}}{1-(1-\gamma)z^{-1}}$$

$$\delta \approx \frac{1}{A_0} \left(1 + \frac{C_1}{C_2}\right), \quad \gamma = \frac{1}{A_0} \frac{C_1}{C_2}$$

- Resonator

$$H_{\text{resonator}}(z) = \frac{z^{-1}}{1 + \xi_1 z^{-1} + (1 - \xi_2) z^{-2}}$$

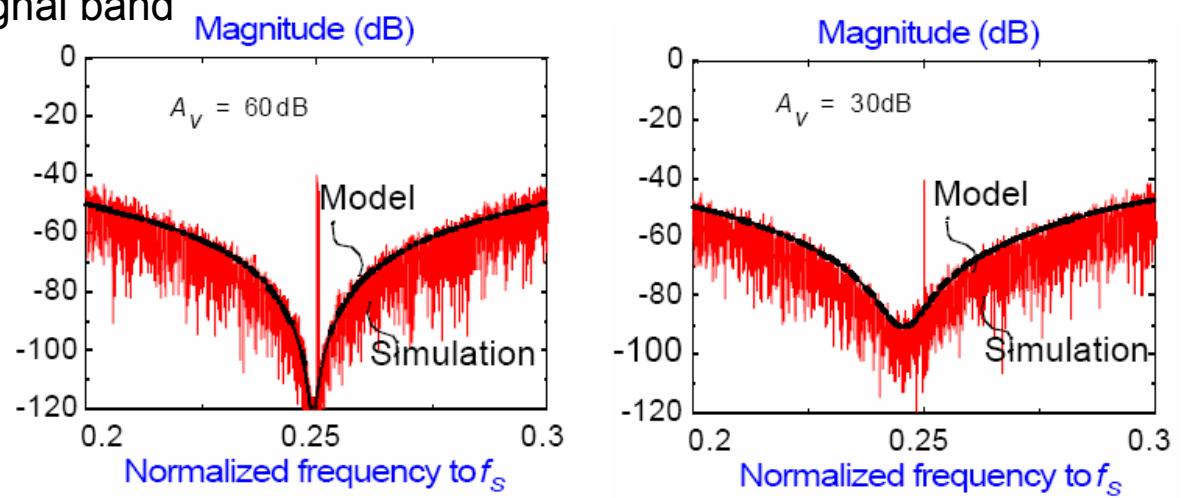


→ ξ_1 : shifts of the notch frequency

→ ξ_2 : loss of attenuation in signal band

$$\xi_1 = 2\gamma - 4\delta$$

$$\xi_2 = 2\gamma$$



Error Sources in SC Circuits

- Settling Error

- SC integrator

→ T_S : the period of the sampling clock

$$I(z) = \frac{(1 - \varepsilon_s) \cdot g z^{-1}}{1 - z^{-1}}$$

$$\varepsilon_s = e^{-T_S/2\tau}, \quad \tau = C_{eq}/g_m$$

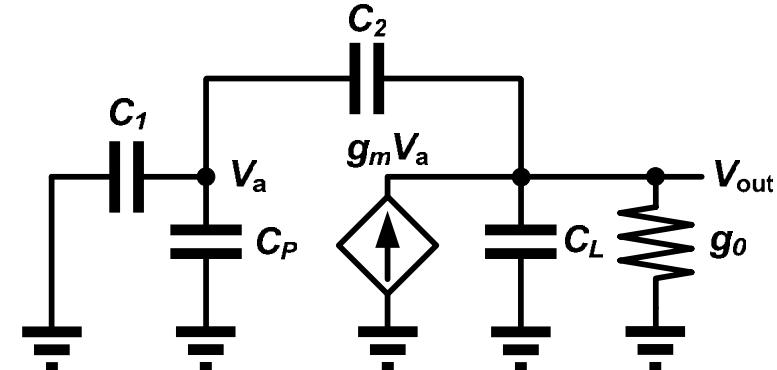
$$C_{eq} = C_1 + C_L \left(1 + \frac{C_1}{C_2}\right)$$

- Transfer function of resonator

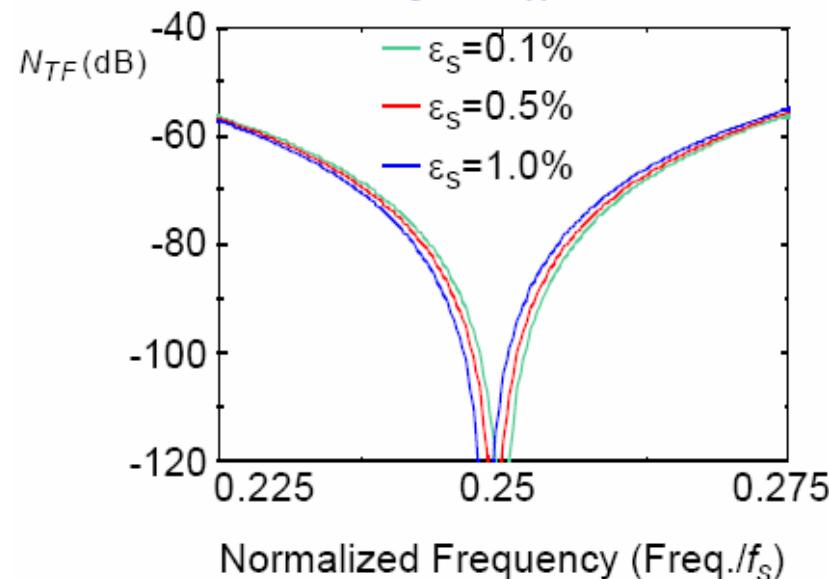
$$H_{resonator}(z) = \frac{z^{-1}}{1 + \xi_1 z^{-1} + (1 - \xi_2) z^{-2}}$$

$$\xi_1 = -4\varepsilon_s$$

$$\xi_2 = 0$$

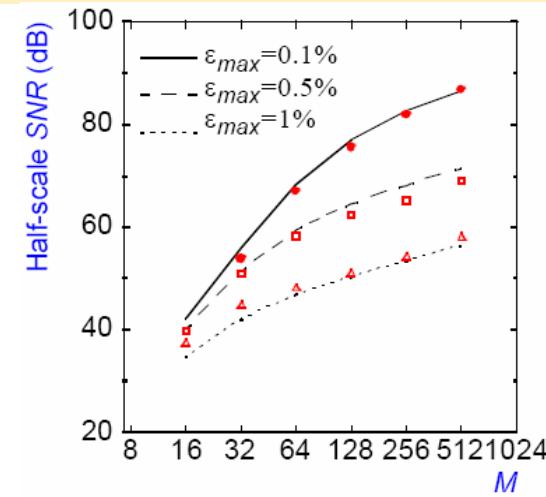
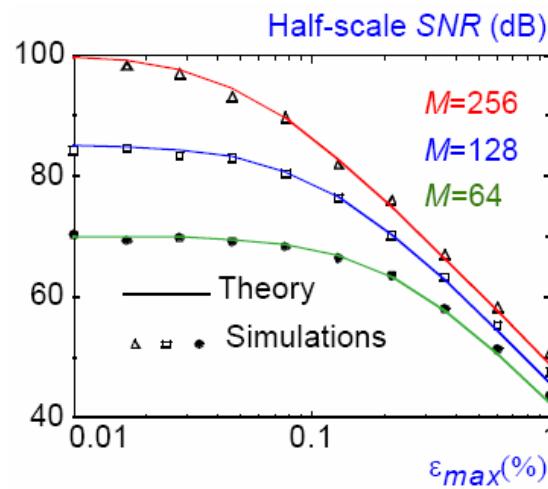
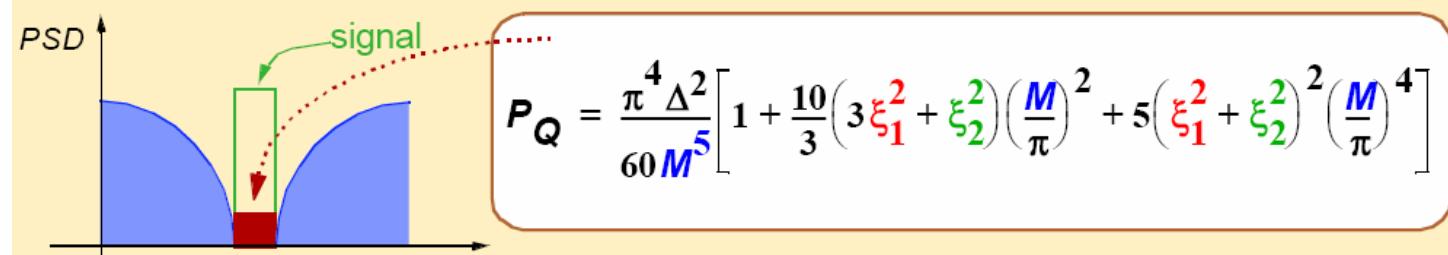
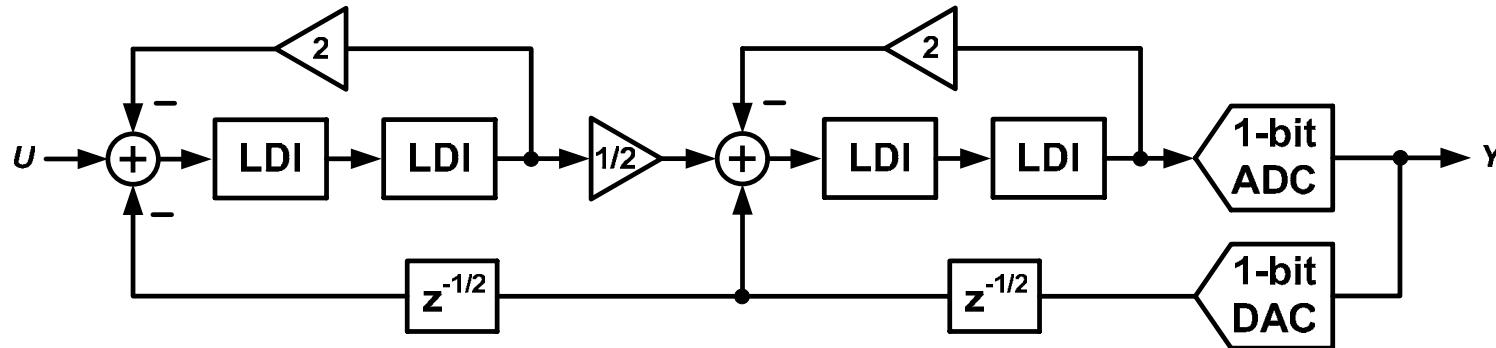


Effect of ε_s on N_{TF} in SC circuits



Error Sources in SC Circuits

- Quantization Noise Power of 4th-order Modulator

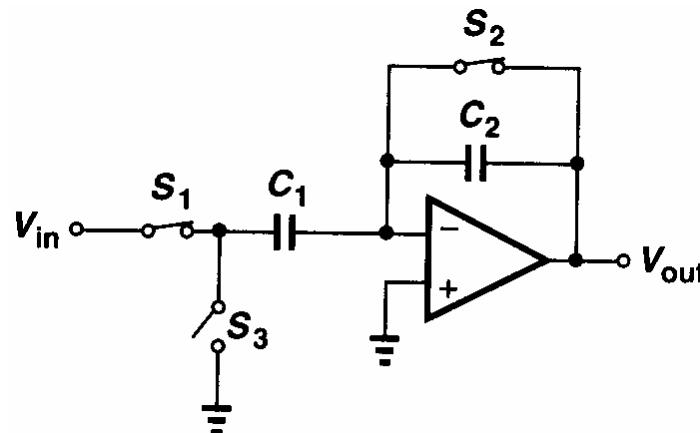


Switched-Capacitor Circuits

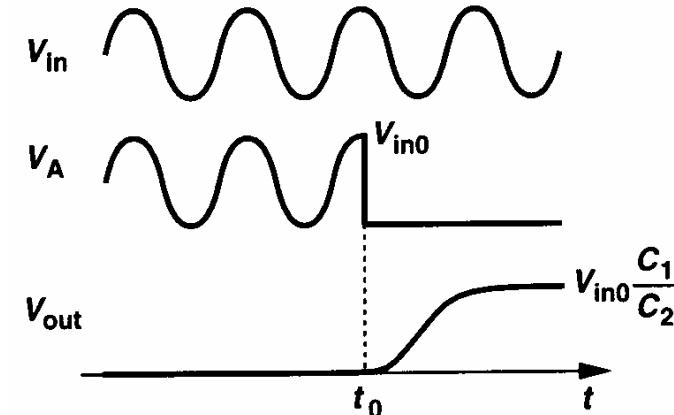
Department of Electrical Engineering

General Considerations

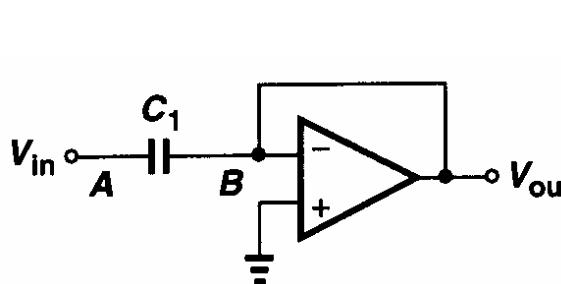
- Switched-Capacitor Amplifier



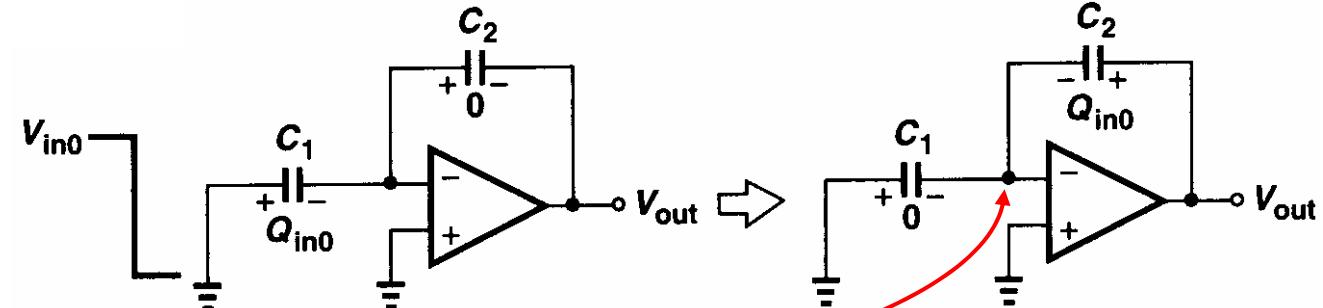
Sampling mode



Amplification mode



Transfer of charge from C_1 to C_2

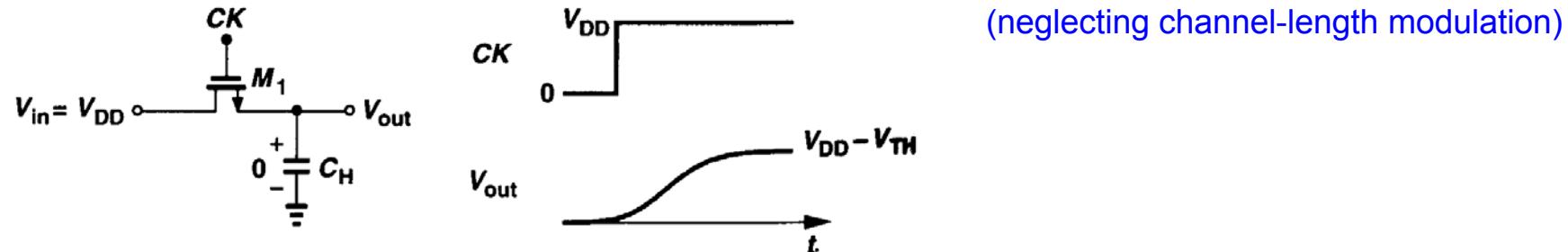


■ Charge conservation equations $Q=CV$

Analog Switches

- Maximum Output Level in an NMOS Sampler

- Since the gate and drain of M_1 are at the same potential, the transistor is **saturated**



$$R_{on} = \frac{1}{\mu_n C_{ox} (W/L) (V_{DD} - V_{in} - V_{TH})}$$

$$V_{out} = V_{DD} - V_{TH} - \frac{1}{2} \frac{\mu_n}{\mu_n} \frac{C_{ox}}{C_H} \frac{W}{L} t + \frac{1}{V_{DD} - V_{TH}}$$

→ implies that as $t \rightarrow \infty$, $V_{out} \rightarrow V_{DD} - V_{TH}$

→ For $V_{out} \approx V_{in}$

► the transistor must operate in **deep triode region** and the **upper bound** of V_{in} equals $V_{DD} - V_{TH}$

- If the variation of R_{on} of device is restricted to a range of 4 to 1

$$\Rightarrow V_{in,max} = \frac{3}{4} (V_{DD} - V_{TH})$$

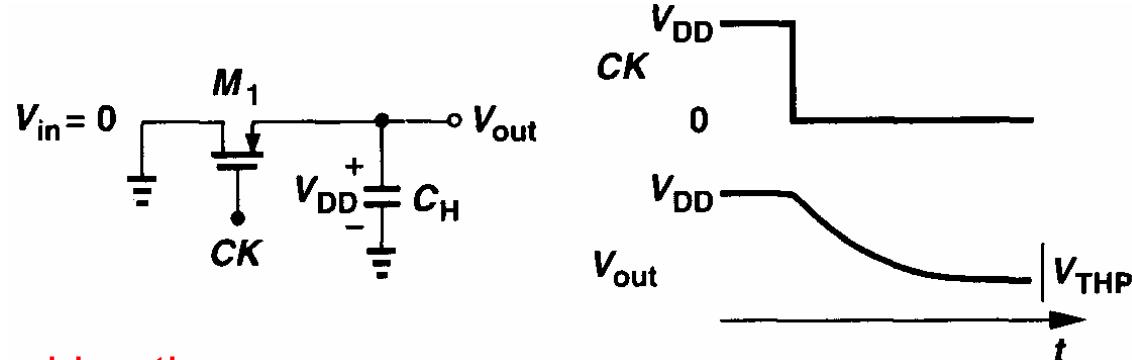
► Note that the device threshold voltage directly limits the voltage swings

Analog Switches

- Minimum Output Level in an PMOS Sampler

MOS devices operating in deep triode region are called “zero-offset” switches

→ to emphasize that no dc shift between the input and output of the sampling circuit *



- Speed Considerations

Definition of Speed in a Sampling Circuit

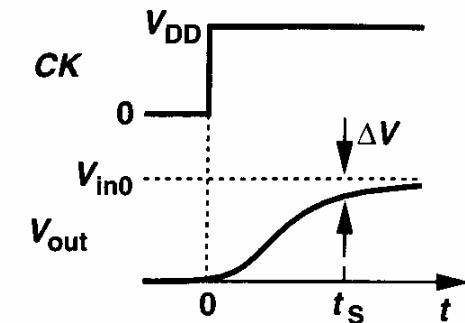
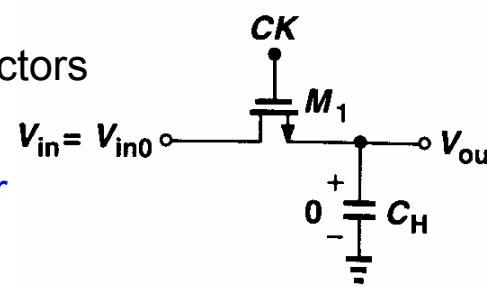
$\Delta V/V_{in0} = 0.1\%$

→ note that after $t = t_s$, we can consider the source and drain voltages be approximately equal

The sampling speed is given by two factors

→ the on-resistance of the switch

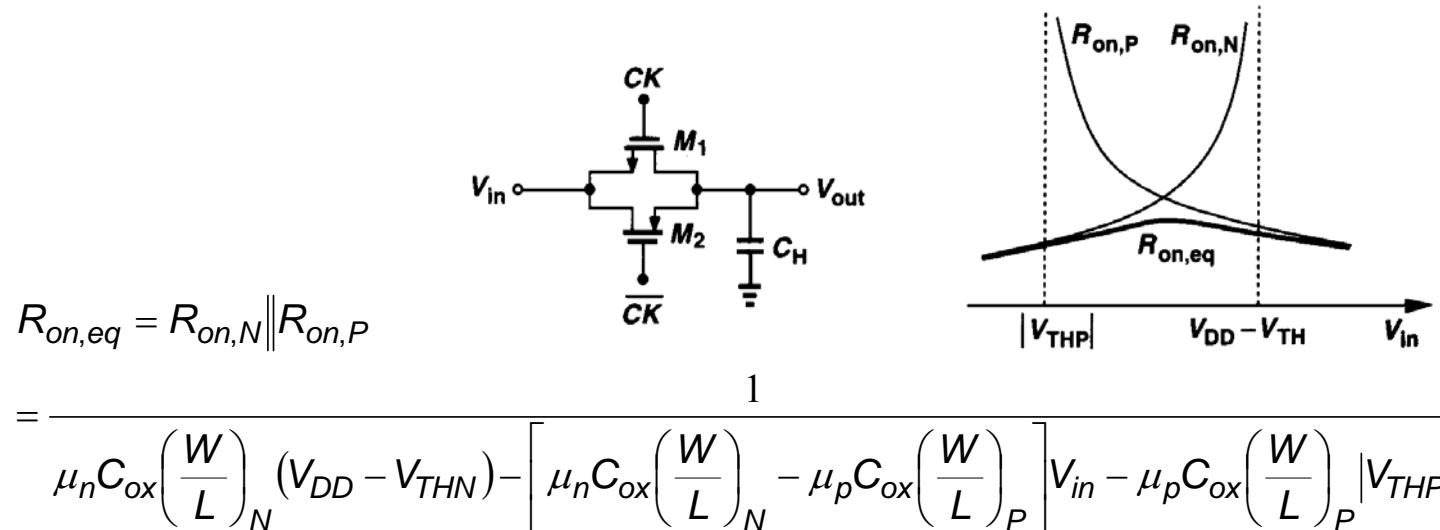
→ the value of the sampling capacitor



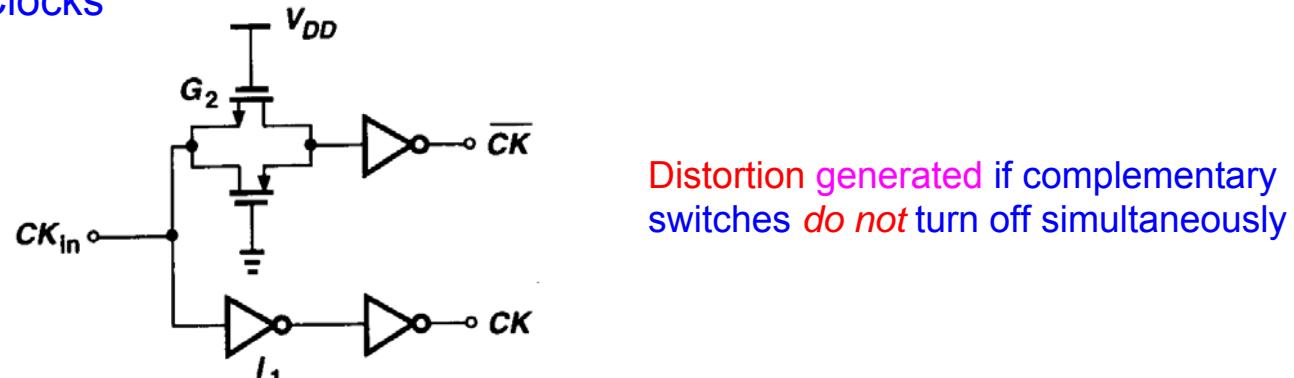
Analog Switches

- On-Resistance of MOS Devices

- On-resistance of NMOS/PMOS devices and complementary switch (transmission gate)



- Complementary Clocks



Switching Errors

Channel Charge Injection

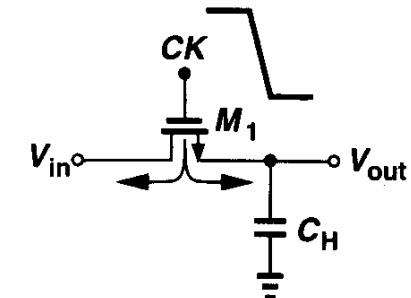
Charge injection when a switch turns off

Assuming $V_{in} \approx V_{out}$, the total charge in the inversion layer is

$$Q_{ch} = WLC_{ox}(V_{DD} - V_{in} - V_{TH})$$

where L denotes the effective channel length

When the switch turns off, Q_{ch} exits through the source and drain terminals, the phenomenon called “channel charge injection”

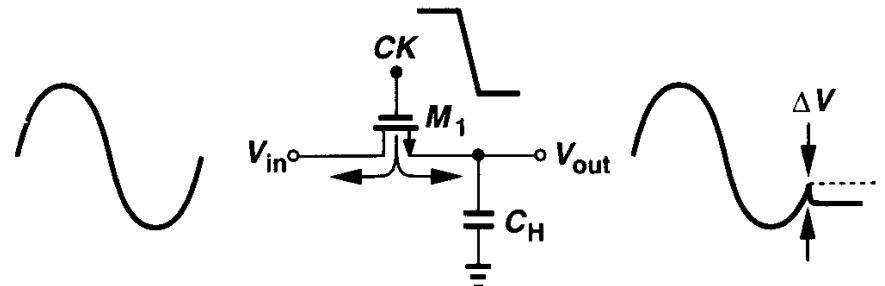


Effect of charge injection

For example, if half of Q_{ch} is injected onto C_H the resulting error equals

$$\Delta V = \frac{WLC_{ox}(V_{DD} - V_{in} - V_{TH})}{2C_H}$$

The error is directly proportional to WLC_{ox} and inversely proportional to C_H



Switching Errors

How Does Charge Injection Affect the Precision

- As a **worst-case** estimate, the entire channel charge is injected onto the sampling capacitor.
The sampled output voltage is

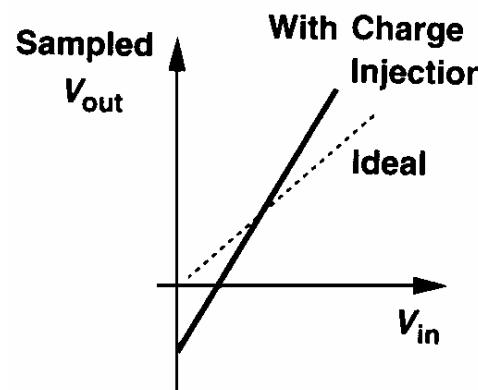
$$V_{out} \approx V_{in} - \frac{WLC_{ox}(V_{DD} - V_{in} - V_{TH})}{C_H} = V_{in} \left(1 + \frac{WLC_{ox}}{C_H} \right) - \frac{WLC_{ox}(V_{DD} - V_{TH})}{C_H}$$

→ where the phase shift between the input and output is neglected

- Two effects

- A non-unity gain equals to $(1 + WLC_{ox}/C_H)$
- A constant offset voltage $-WLC_{ox}(V_{DD} - V_{TH})/C_H$

- Input/output characteristic

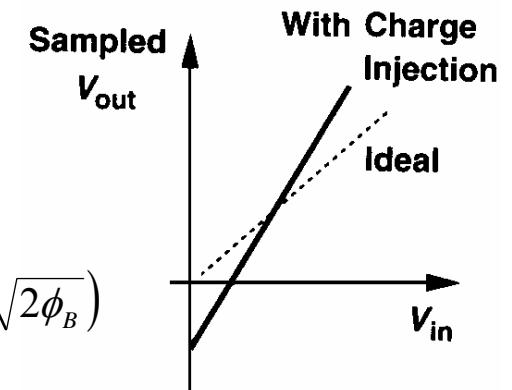


Switching Errors

Body Effect

Since $V_{TH} = V_{TH0} + \gamma(\sqrt{2\phi_B + V_{SB}} - \sqrt{2\phi_B})$ and $V_{BS} \approx -V_{in}$, we have

$$\begin{aligned} V_{out} &= V_{in} - \frac{WLC_{ox}}{C_H} (V_{DD} - V_{in} - V_{TH0} - \gamma\sqrt{2\phi_B + V_{in}} + \gamma\sqrt{2\phi_B}) \\ &= V_{in} \left(1 + \frac{WLC_{ox}}{C_H}\right) + \gamma \frac{WLC_{ox}}{C_H} \sqrt{2\phi_B + V_{in}} - \frac{WLC_{ox}}{C_H} (V_{DD} - V_{TH0} + \gamma\sqrt{2\phi_B}) \end{aligned}$$



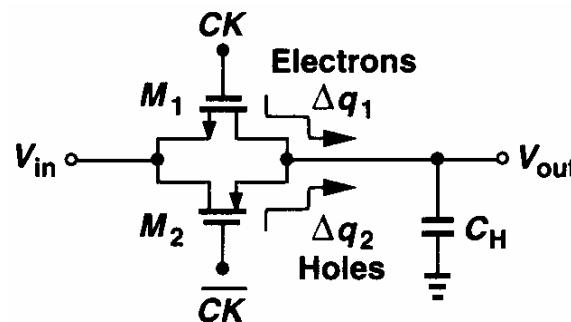
It follows that the **nonlinear** dependence of V_{TH} upon V_{in} introduces nonlinearity in the input/output characteristic

- In summary, charge injection contributes three types of **errors** in MOS sampling circuits
 - ▶ gain error
 - ▶ dc offsets
 - ▶ Nonlinearity
- In many applications, the first two can be tolerated or corrected whereas the last *cannot*

Switching Errors

- The Use of Complementary Switches to Reduce Charge Injection

- The approach to lowering the effect of charge injection incorporates both PMOS and NMOS devices
 - ▶ such that the opposite charge packets injected by the two cancel each other
- For Δq_1 to cancel Δq_2 , we must have $W_1L_1C_{ox}(V_{CK} - V_{in} - V_{THN}) = W_2L_2C_{ox}(V_{in} - |V_{THP}|)$
 - ▶ Thus, the cancellation occurs for only one input level
- Even for clock feedthrough, the circuit does *not* provide complete cancellation
 - ▶ because the gate-drain overlap capacitance of NMOSS is *not equal* to that of PMOSS



Switching Errors

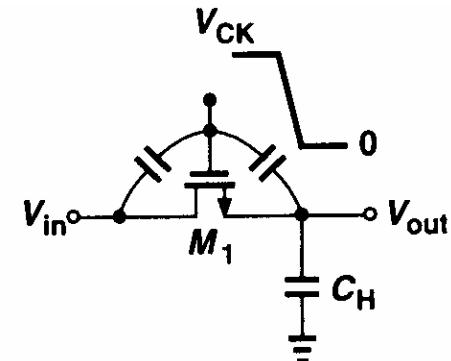
Clock Feedthrough

- Assuming the overlap capacitance is constant, we express the error as

$$\Delta V = V_{CK} \frac{WC_{ov}}{WC_{ov} + C_H}$$

where C_{ov} is the overlap capacitance per unit width

- The error ΔV is independent of the input level
- manifesting itself as a constant offset in the input/output characteristic
- As with charge injection, clock feedthrough leads to a trade-off between speed and precision as well



Switching Errors

- Charge Injection and Clock Feedthrough are Suppression by Dummy Switch

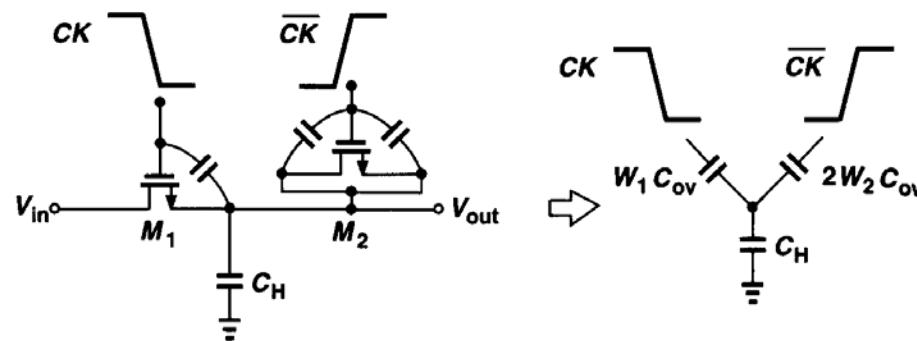
■ A “dummy” switch, M_2 with $W_2 = 0.5W_1$ and $L_2 = L_1$, driven by \overline{CK}

→ the effect of clock feedthrough is suppressed

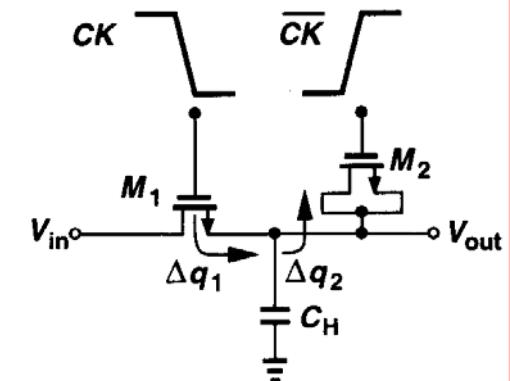
$$\rightarrow \Delta q_2 = W_2 L_2 C_{ox} (V_{CK} - V_{in} - V_{TH2}) = \Delta q_1 = \frac{W_1 L_1 C_{ox}}{2} (V_{CK} - V_{in} - V_{TH1})$$

■ The total charge in V_{out} is zero because

$$-V_{CK} \frac{W_1 C_{ov}}{W_1 C_{ov} + C_H + 2W_2 C_{ov}} + V_{CK} \frac{2W_2 C_{ov}}{W_1 C_{ov} + C_H + 2W_2 C_{ov}} = 0$$



Suppose half of the channel charge of M_1 is injected onto C_H



Sampling Switches

- Channel Charge Injection

- It is instructive to consider the speed-precision trade-off resulting from charge injection
- Representing the speed by a simple time constant τ and the precision by the error ΔV due to charge injection, we define a figure of merit as $F = (\tau \Delta V)^{-1}$

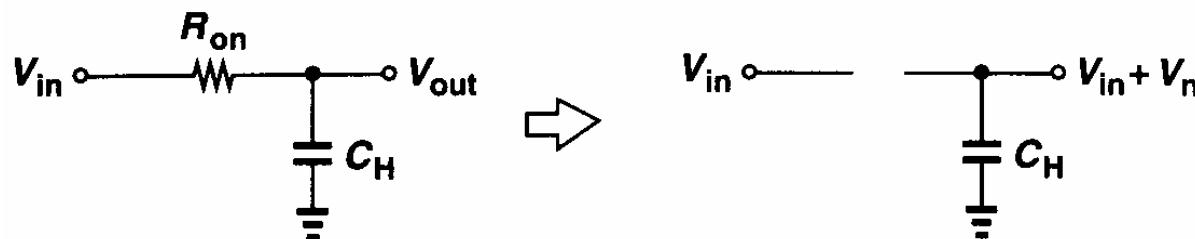
$$\begin{aligned}\tau &= R_{on} C_H = \frac{1}{\mu_n C_{ox} (W/L) (V_{DD} - V_{in} - V_{TH})} C_H \\ \Delta V &= \frac{WLC_{ox}}{C_H} (V_{DD} - V_{in} - V_{TH})\end{aligned}\quad \left. \begin{array}{c} \\ \\ \end{array} \right\} \quad \Rightarrow \quad F = \frac{\mu_n}{L^2}$$

- The trade-off is independent of the switch width and the sampling capacitor

Sampling Noise

● kT/C Thermal Noise

- The on-resistance of the switch introduces thermal noise at the output
- when the switch turns off, this noise is stored on the capacitor along with the instantaneous value of the input voltage



- The rms voltage of the sampled noise is approximately equal to $\sqrt{kT/C}$
- The problem of kT/C noise limits the performance in many high-precision applications
- In order to achieve a low noise, the sampling capacitor must be sufficiently large, thus loading other circuits and degrading the speed

Noise Sources

Thermal Noise

- The thermal motion of the charge carriers in the channel of device

- The power spectral density (PSD)

$$S_v(f) = 4kTR_{on} \text{ (V}^2/\text{Hz)} \quad \text{where } k: \text{Boltzmann constant } 1.38 \times 10^{-23} \text{ J/K}$$

T : absolute temperature

- The sampled thermal noise in switched-capacitor circuits

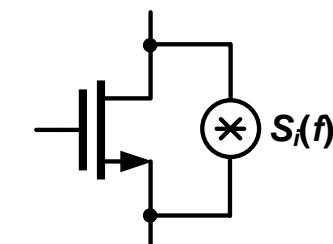
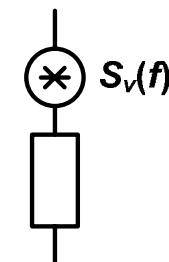
$$V_n^2 = \frac{kT}{C}$$

- MOS in active region

- The noise current

$$S_i(f) = \frac{8}{3}kT g_m \text{ (A}^2/\text{Hz)} \quad \text{for long-channel transistors}$$

$$S_i(f) = 10kT g_m \text{ (A}^2/\text{Hz)} \quad \text{for } 0.25\mu\text{m technology}$$



Flicker Noise

- The charge carriers getting trapped and released as they move in the channel

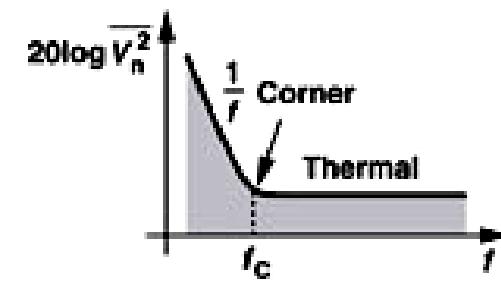
- Large gate area

$$S_v(f) = \frac{K}{C_{ox}WL} \cdot \frac{1}{f} \text{ (V}^2/\text{Hz)}$$

- PMOS

- Correlated Double Sampling (CDS)

- Chopper Stabilized



Sampling Switches

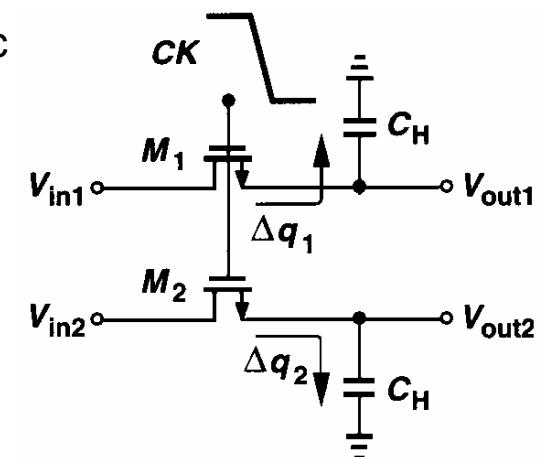
- Differential Sampling Circuit

- The charge injection as a *common-mode disturbance*
- Writing $\Delta q_1 = WLC_{ox}(V_{CK} - V_{in1} - V_{TH1})$ and $\Delta q_2 = WLC_{ox}(V_{CK} - V_{in2} - V_{TH2})$
 - The charge $\Delta q_1 = \Delta q_2$ only if $V_{in1} = V_{in2}$
 - The overall error is *not suppressed* for differential signals

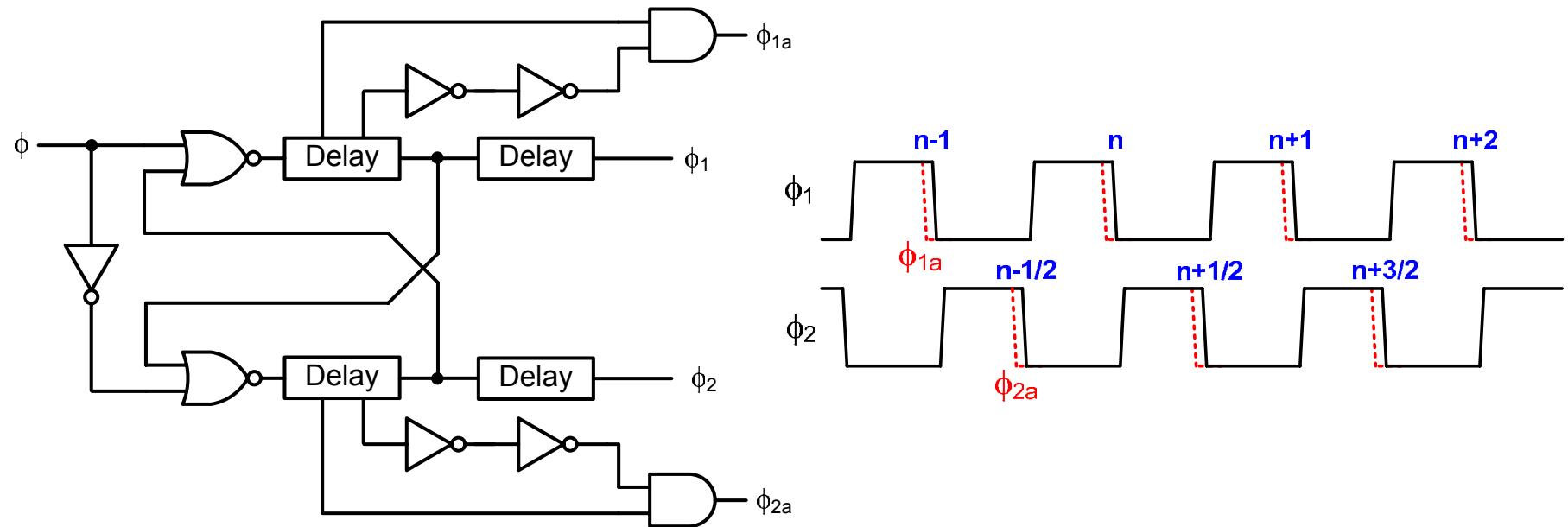
- The differential technique both *removes* the constant offset and *lowers* the nonlinear component

$$\begin{aligned}\Delta q_1 - \Delta q_2 &= WLC_{ox}[(V_{in2} - V_{in1}) + (V_{TH2} - V_{TH1})] \\ &= WLC_{ox}[V_{in2} - V_{in1} + \gamma(\sqrt{2\phi_F + V_{in2}} - \sqrt{2\phi_F + V_{in1}})] \quad \text{---- (A)}\end{aligned}$$

- Since for $V_{in1} = V_{in2}$ (DC), $\Delta q_1 - \Delta q_2 = 0$, the characteristic
 - exhibits *no offset*
 - Also, the *nonlinearity* of body effect *appears* in both *square-root terms* of (A), leading to *only odd-order distortion*



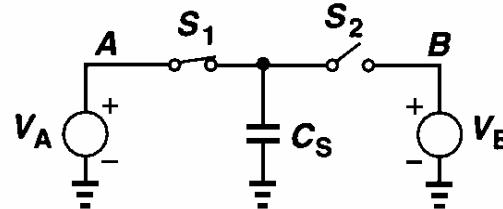
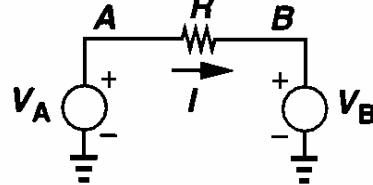
Nonoverlapping Clocks



- Two logic signals running at the same frequency and arranged in such a way that at no time are both signals high
- The locations of the clock edges of and need be moderately controlled to allow for complete charge settling

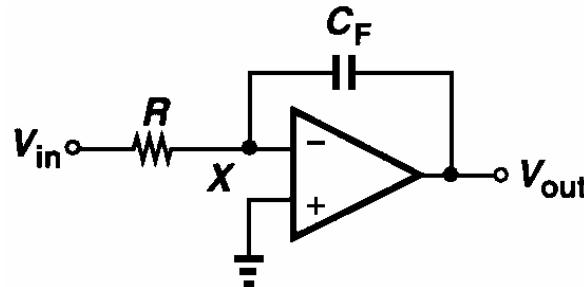
Switched-Capacitor Integrators

- Resistor Equivalence of a Switched Capacitor

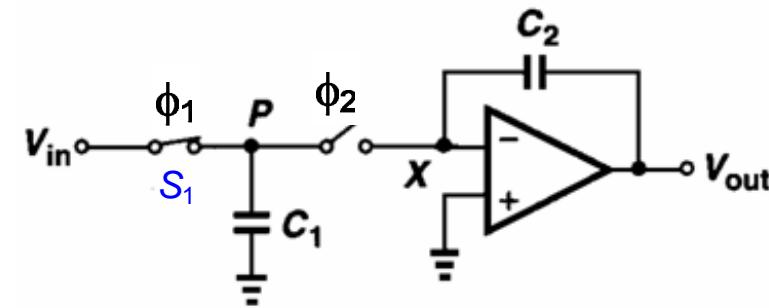


$$\begin{aligned} \overline{I_{AB}} &= \frac{C_S(V_A - V_B)}{T_{CK}} \\ &= C_S f_{CK}(V_A - V_B) \equiv \frac{(V_A - V_B)}{R_{eq}} \\ \Rightarrow R_{eq} &= \frac{1}{C_S f_{CK}} \end{aligned}$$

- Continuous-time and discrete-time resistors



$$V_{out} = -\frac{1}{RC_F} \int V_{in} dt$$



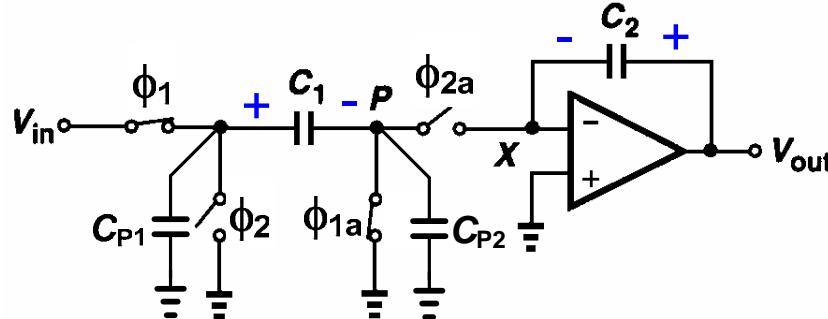
$$V_{out}(z) = V_{out}(z) \cdot z^{-1} - \frac{C_1}{C_2} V_{in}(z) \cdot z^{-1}$$

- The input-dependent charge injection of S_1 introduces **nonlinearity** in the **charge stored** on C_1 and hence the **output voltage**
- The parasitic capacitance at node P resulting from the **source/drain junctions** of S_1 and S_2 leads to a **nonlinear** charge-to-voltage conversion when C_1 is **switched**

Switched-Capacitor Integrators

Parasitic-Insensitive Integrators

- Positive discrete-time integrator for high-accuracy integrated circuits

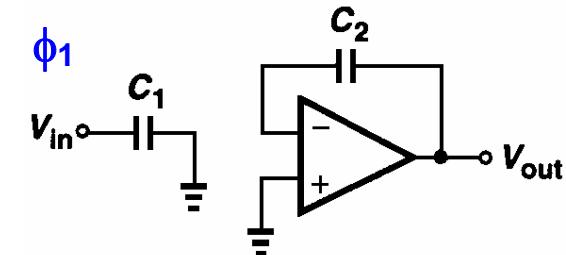


$$V_{out}(z) = V_{out}(z) \cdot z^{-1} + \frac{C_1}{C_2} V_{in}(z) \cdot z^{-1}$$

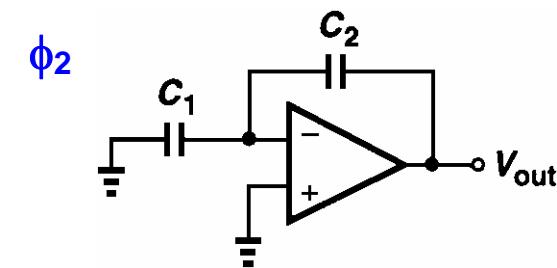
- In the **sampling mode**
 - $\rightarrow C_1$ to track V_{in}
 - \rightarrow the op amp and C_2 hold the previous value
- In the **integration mode**
 - $\rightarrow \phi_{1a}$ turns off first, ϕ_1 turns off next, and subsequently ϕ_2 and ϕ_{2a} turns on

Charge Conservation Equations ($\sum_i C_j \cdot \Delta V_j = 0$)

$$\begin{cases} \phi_1 \rightarrow \phi_2 & C_1(0 - V_{in}(z) \cdot z^{-1}) + C_2[V_{out}(z) \cdot z^{-1/2} - V_{out}(z) \cdot z^{-1}] = 0 \\ \phi_2 \rightarrow \phi_1 & C_2[V_{out}(z) - V_{out}(z) \cdot z^{-1/2}] = 0 \end{cases}$$



sampling mode

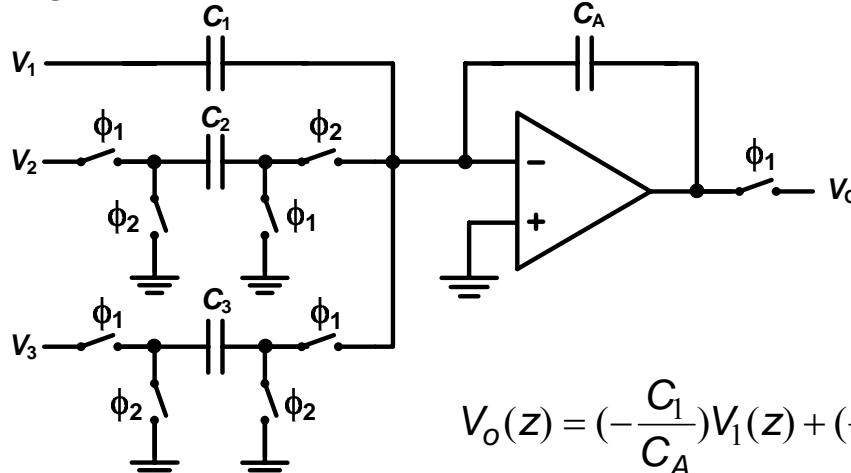


integration mode

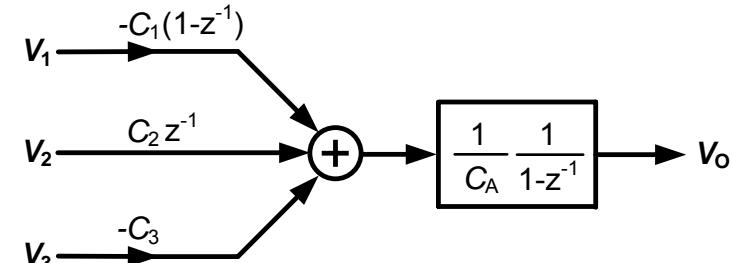
$$\begin{aligned} C_2 \cdot V_{out}(z)[1 - z^{-1}] &= C_1 \cdot V_{in}(z) \cdot z^{-1} \\ \Rightarrow \frac{V_{out}(z)}{V_{in}(z)} &= \frac{C_1}{C_2} \frac{z^{-1}}{1 - z^{-1}} \end{aligned}$$

Signal-Flow-Graph Analysis

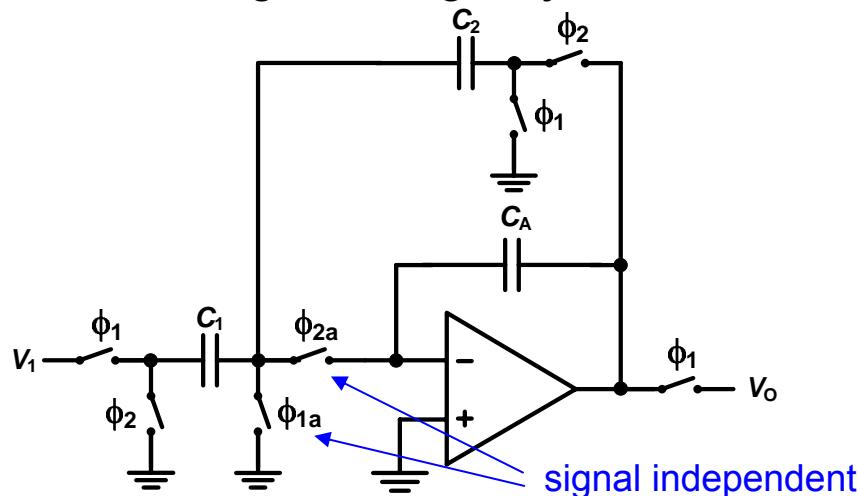
- Using the Principle of Superposition



$$V_o(z) = \left(-\frac{C_1}{C_A}\right)V_1(z) + \left(\frac{C_2}{C_A}\right)\left(\frac{z^{-1}}{1-z^{-1}}\right)V_2(z) - \left(\frac{C_3}{C_A}\right)\left(\frac{1}{1-z^{-1}}\right)V_3(z)$$



- Switch Sharing & Charge Injection

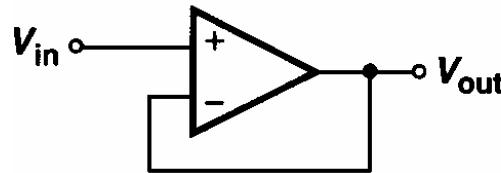


- To reduce the charge injection in SC circuits
 - All switches connected to ground or virtual ground as n-channel switches
- All switches near virtual ground nodes of opamp
 - Turn off early

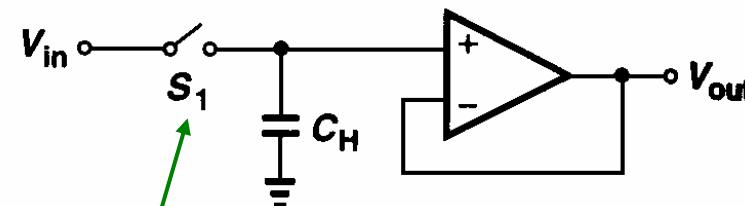
Switched-Capacitor Gain Circuits

- Unity-Gain Buffer

for continuous-time application

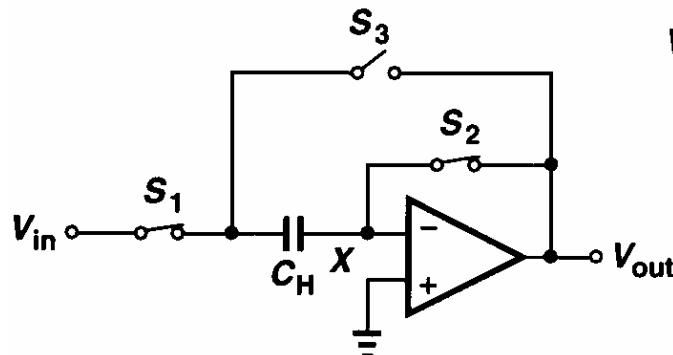


for discrete-time application

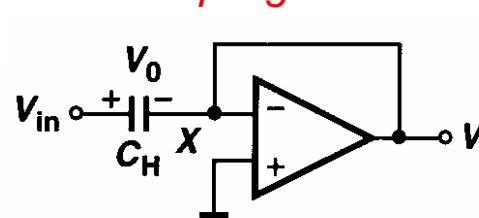


⌚ The input-independent charge injected by S_1 onto C_H limit the accuracy

- Unity-Gain Sampler



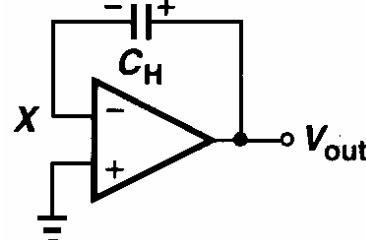
In sampling mode



independent of
the input level

S_2 turns off slightly
before S_1 does

In amplification mode

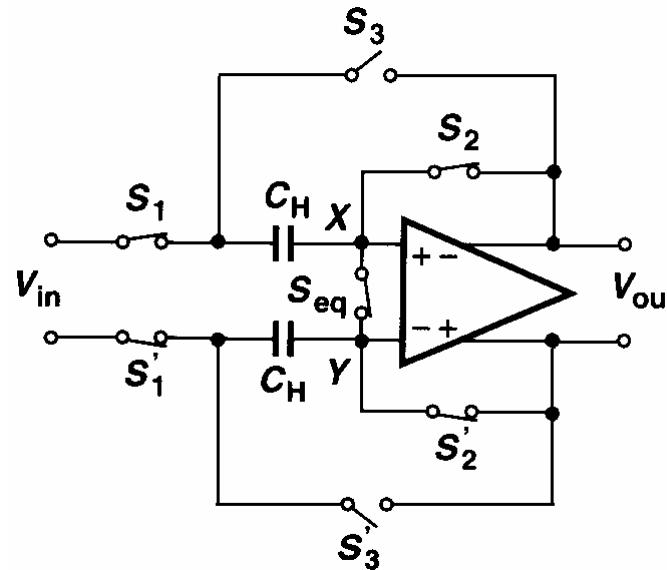


$$\Delta q_2 = WLC_{ox}(V_{CK} - V_{TH} - V_X)$$

Although body effect makes V_{TH} a function of V_X , Δq_2 is relatively constant (offset) because V_X is quite independent of V_{in}

Switched-Capacitor Gain Circuits

- Differential Realization of Unity-Gain Sampler

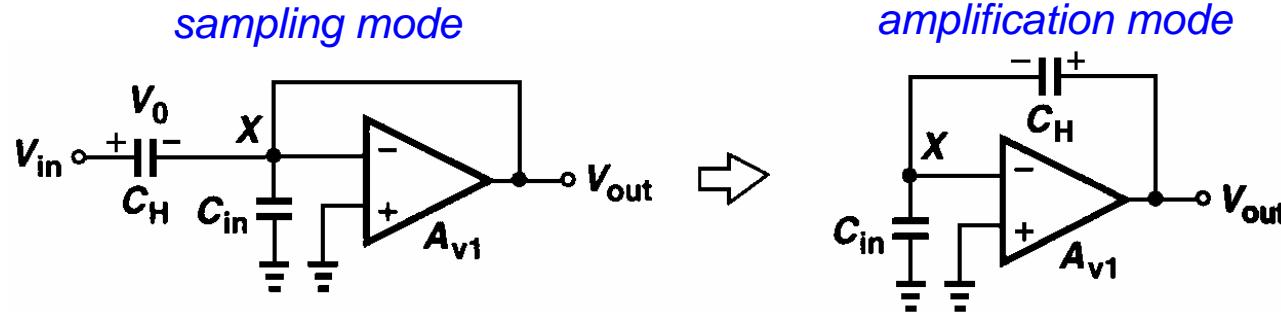


- The charge injected by S_2 and S'_2 appears as a common-mode disturbance at nodes X and Y, where the input(V_{out})-dependent charge injection leads to *nonlinearity*
- In reality, S_2 and S'_2 exhibit a finite charge injection *mismatch*
 - ▶ an issue resolved by adding another switch, S_{eq} , that turns off slightly after S_2 and S'_2 (and before S_1 and S'_1)
 - ▶ thereby equalizing the charge at nodes X and Y

Switched-Capacitor Gain Circuits

Precision Consideration

- Equivalent circuit for accuracy calculations



$$V_X = 0, Q_{CH} = C_H V_0, Q_{Cin} = 0$$

$$V_X \neq 0, Q_{CH} = C_H V_0 + C_{in} V_X, Q_{Cin} \neq 0$$

- In **amplification** mode

$$\left. \begin{aligned} V_{out} - \frac{C_H V_0 + C_{in} V_X}{C_H} &= V_X \\ V_X &= -\frac{V_{out}}{A_{v1}} \end{aligned} \right\} \Rightarrow V_{out} = \frac{V_0}{1 + \frac{1}{A_{v1}} \left(\frac{C_{in}}{C_H} + 1 \right)} \approx V_0 \left[1 - \frac{1}{A_{v1}} \left(\frac{C_{in}}{C_H} + 1 \right) \right]$$

- If $C_{in} / C_H \ll 1$, then $V_{out} \approx V_0 / (1 + A_{v1}^{-1})$

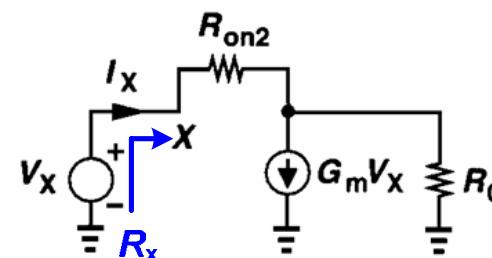
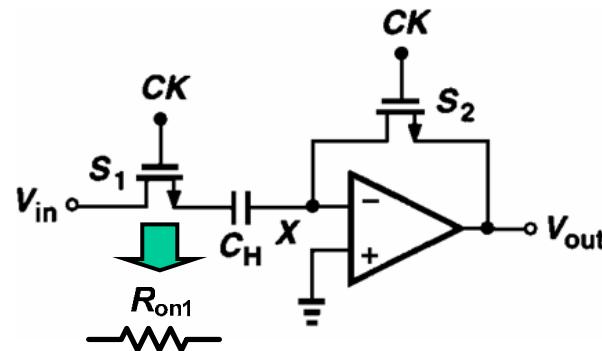
- The circuit **suffers from a gain error** of approximately $-(C_{in}/C_H + 1)/A_{v1}$, suggesting that the **input capacitance** must be **minimized** even if the speed is **not critical**
- To increase A_{v1} , we may choose a **large width** for the **input transistors** of the op amp, but at the cost of **higher input capacitance**

- An **optimum device size** must therefore **yield minimum gain error** rather than **maximum A_{v1}**

Switched-Capacitor Gain Circuits

Speed Consideration of Unity-Gain Sampler

- In sampling mode



$$(I_X - G_m V_X)R_0 + I_X R_{on2} = V_X$$

Input resistance

$$R_X = \frac{R_0 + R_{on2}}{1 + G_m R_0}$$

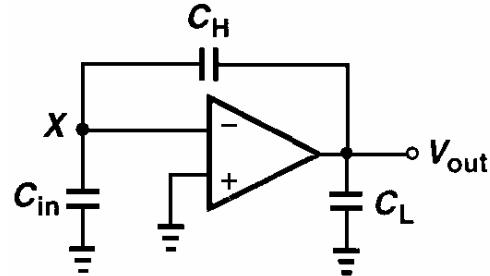
Since typically $R_{on2} \ll R_0$ and $G_m R_0 \gg 1$, $R_X \approx 1/G_m$

The time constant $\tau_{sam} = (R_{on1} + \frac{1}{G_m})C_H$

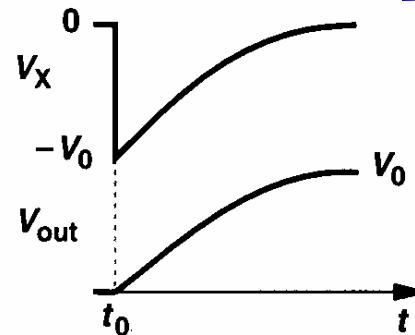
Switched-Capacitor Gain Circuits

Speed Consideration

In amplification mode

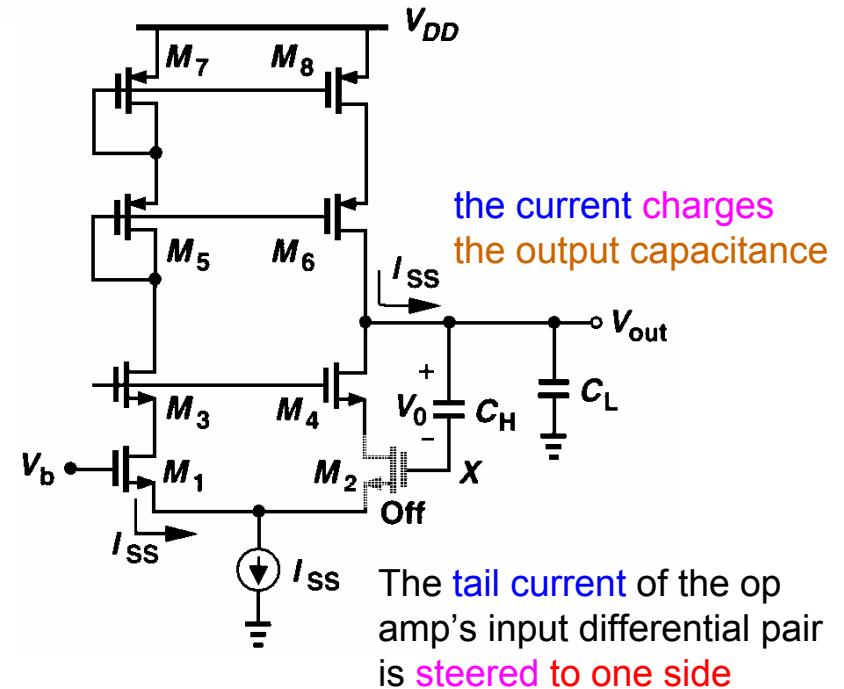


If C_{in} is relatively small
the voltages across C_L and C_H
do not change instantaneously



At the beginning

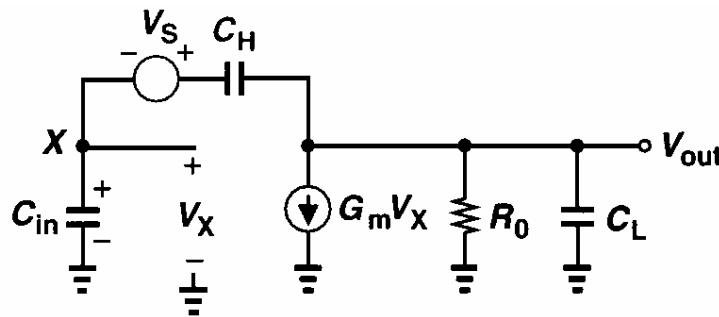
- if $V_{out} \approx 0$ and $V_{CH} \approx V_0$, then $V_X = -V_0$
- The large difference sensed by the op amp, possibly causing the op amp to slew



Switched-Capacitor Gain Circuits

- Speed Consideration of Unity-Gain Sampler

- In amplification mode



$$\left\{ \begin{array}{l} V_{out} \left(\frac{1}{R_0} + C_L s \right) + G_m V_X = (V_S + V_X - V_{out}) \cdot C_H s \\ V_X \frac{C_{in} s}{C_H s} + V_X + V_S = V_{out} \end{array} \right.$$

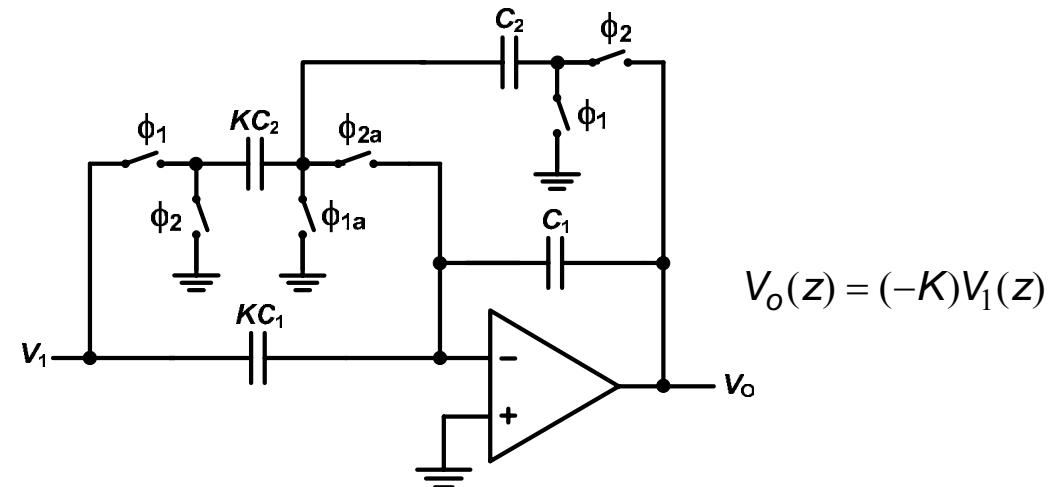
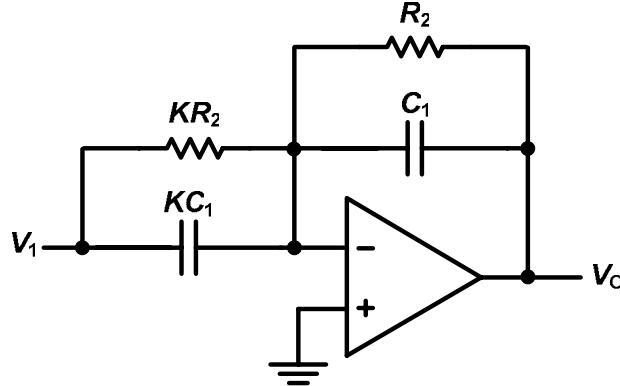
→ $G_m R_0 C_H \gg C_H$ and C_{in}

$$\rightarrow \frac{V_{out}(s)}{V_S} = \frac{(G_m + C_{in} s) \cdot C_H}{(C_L C_{in} + C_{in} C_H + C_H C_L) s + G_m C_H}$$

- The response is characterized by a time constant $\tau_{amp} = \frac{C_L C_{in} + C_{in} C_H + C_H C_L}{G_m C_H}$
 - The response is independent of the op amp output resistance
 - because a higher R_0 leads to a greater loop gain, yielding a constant closed-loop speed
 - If $C_{in} \ll C_L$ and C_H , then $\tau_{amp} = C_L / G_m$

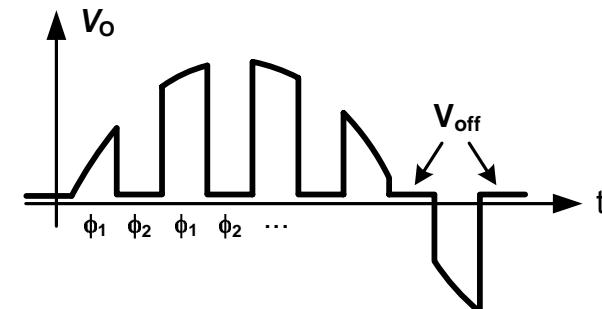
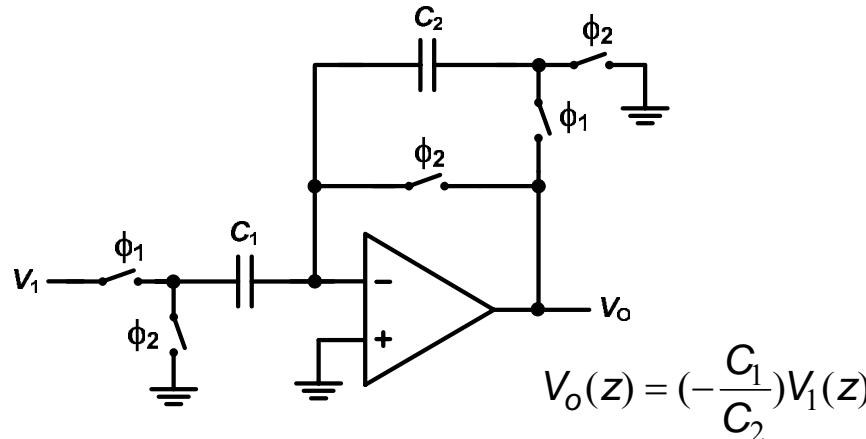
Switched-Capacitor Gain Circuits

- Parallel Resistor-Capacitor Circuit



- 😊 The output does not incur any large slew-rate requirement
- 😢 Amplifier 1/f noise and offset voltage

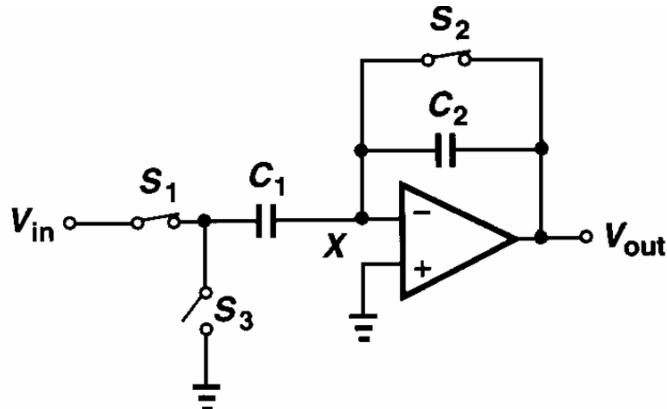
- Resettable Gain Circuit



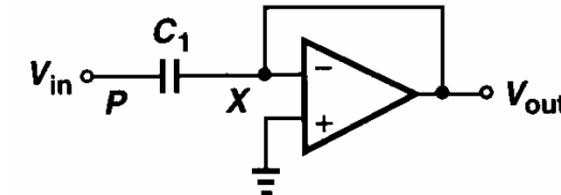
- 😊 The output voltage is independent of the opamp offset voltage
- 😢 high slew-rate opamp

Switched-Capacitor Gain Circuits

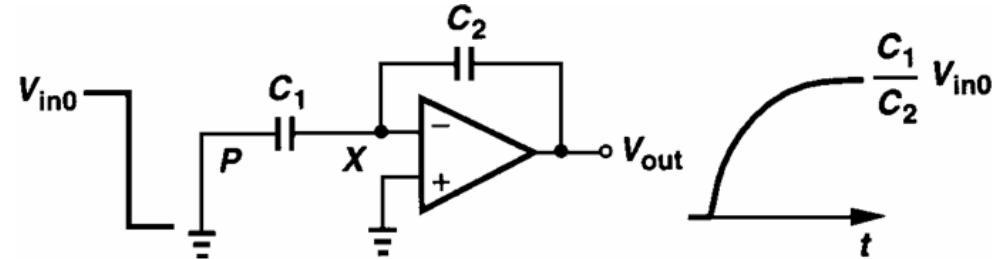
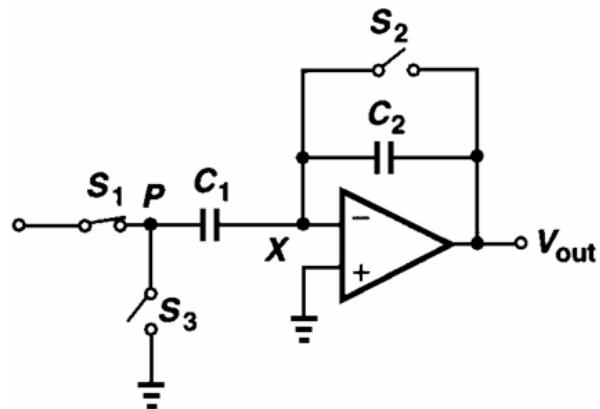
- Noninverting Amplifier



sampling mode



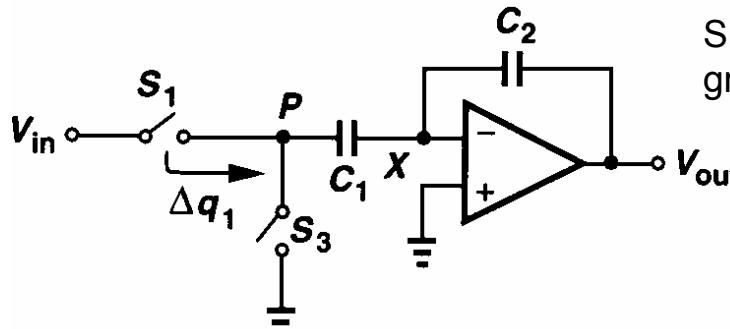
amplification mode



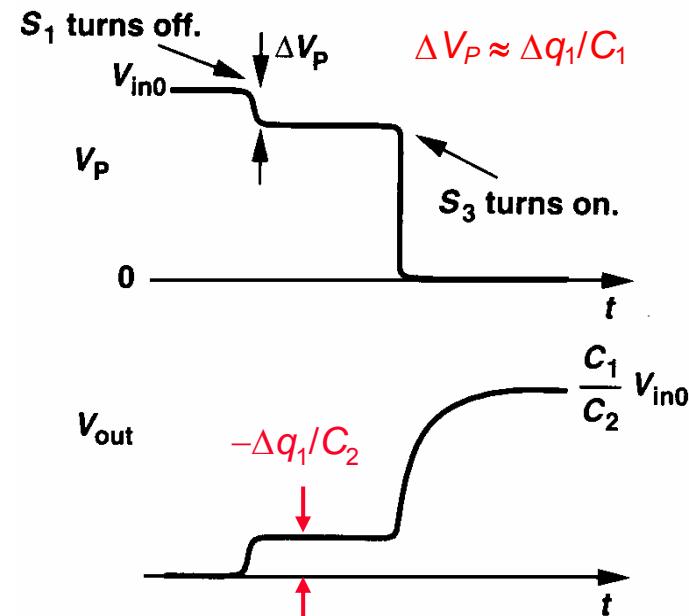
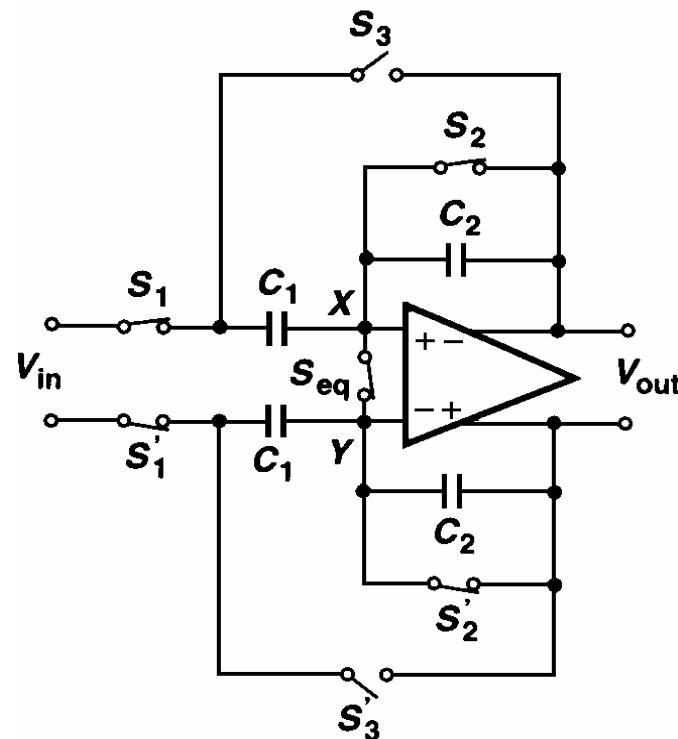
- From the time S_2 turns off until the time S_1 turns off
 - the output voltage may change significantly *without* any error
 - In other words, the sampling instant is defined by the turn-off of S_2

Switched-Capacitor Gain Circuits

- Effect of charge injected by S_1



Since the output voltage is measured after node P is connected to ground, the charge injected by S_1 does **not** affect the final output



☺ The constant offset due to S_2 can be suppressed by differential operation

Switched-Capacitor Gain Circuits

● Precision Consideration

■ Equivalent circuit of noninverting during amplification

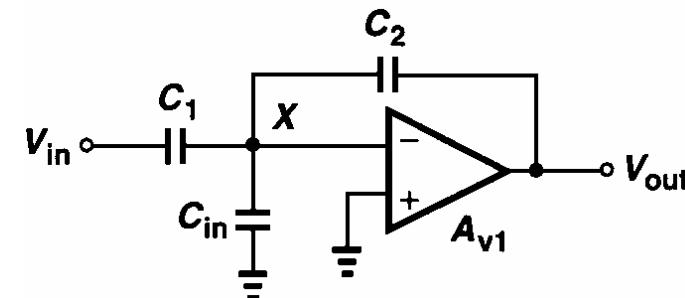
► $(V_{out} - V_x)C_2s = V_xC_{in}s + (V_x - V_{in})C_1s$ and $V_{out} = -A_{v1}V_x$,

► we have

$$\left| \frac{V_{out}}{V_{in}} \right| = \frac{C_1}{C_2 + \frac{C_2 + C_1 + C_{in}}{A_{v1}}}$$

► For large A_{v1}

$$\left| \frac{V_{out}}{V_{in}} \right| \approx \frac{C_1}{C_2} \left(1 - \frac{C_2 + C_1 + C_{in}}{C_2} \cdot \frac{1}{A_{v1}} \right)$$



► implying that the amplifier suffers from a gain error of $(C_2 + C_1 + C_{in})/(C_2A_{v1})$

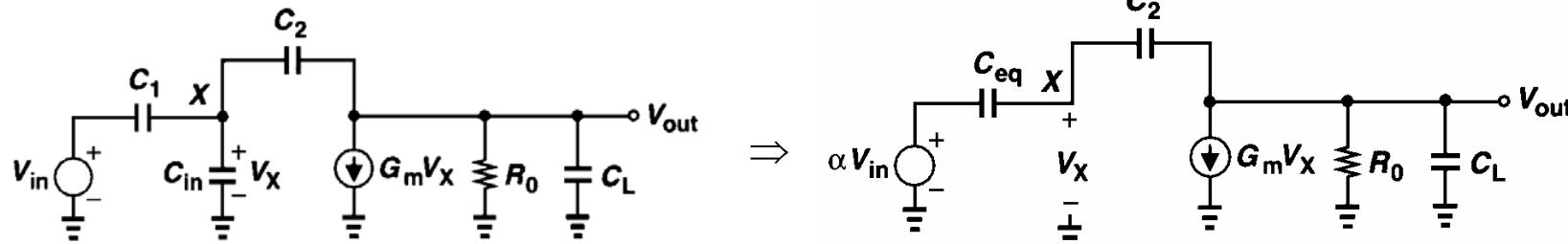
► Note that the gain error increases with the nominal gain C_1/C_2

■ With $C_H = C_2$ and for a nominal gain of unity, the noninverting amplifier exhibits greater gain error than does the unity-gain sampler (p.28)

Switched-Capacitor Gain Circuits

Speed Consideration

- Equivalent circuit of noninverting amplifier in **amplification mode**



where $\alpha = C_1 / (C_1 + C_{in})$ and $C_{eq} = C_1 + C_{in}$

$$\begin{cases} V_X = (\alpha V_{in} - V_{out}) \frac{C_{eq}}{C_{eq} + C_2} + V_{out} \\ V_X G_m + V_{out} \left(\frac{1}{R_0} + C_L s \right) = (\alpha V_{in} - V_{out}) \frac{C_{eq} C_2}{C_{eq} + C_2} \end{cases}$$

$$\rightarrow \frac{V_{out}(s)}{V_{in}} = \frac{-C_{eq} \frac{C_1}{C_1 + C_{in}} (G_m - C_2 s) R_0}{C_2 G_m R_0 + C_{eq} + C_2 + R_0 [C_L (C_{eq} + C_2) + C_{eq} C_2] s}$$

- For a **large $G_m R_0$**

$$\frac{V_{out}(s)}{V_{in}} \approx \frac{-C_{eq} \frac{C_1}{C_1 + C_{in}} (G_m - C_2 s) R_0}{R_0 (C_L C_{eq} + C_L C_2 + C_{eq} C_2) s + G_m R_0 C_2}$$

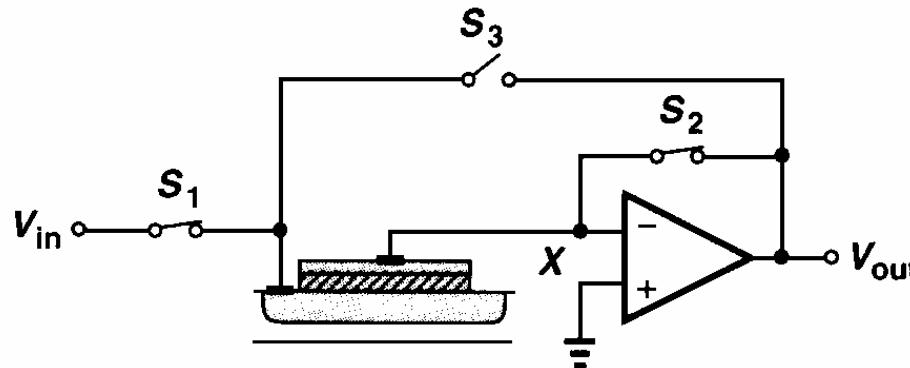
$$\tau_{amp} = \frac{C_L C_{eq} + C_L C_2 + C_{eq} C_2}{G_m C_2}$$

- If $C_L = 0$, then $\tau_{amp} = (C_1 + C_{in}) / G_m$, a value **independent** of the feedback capacitor
 - This because, while a **larger C_2** introduces **behavior loading** at the output, it also provides a **greater feedback factor**

Switched-Capacitor Gain Circuits

Bottom-Plate Sampling

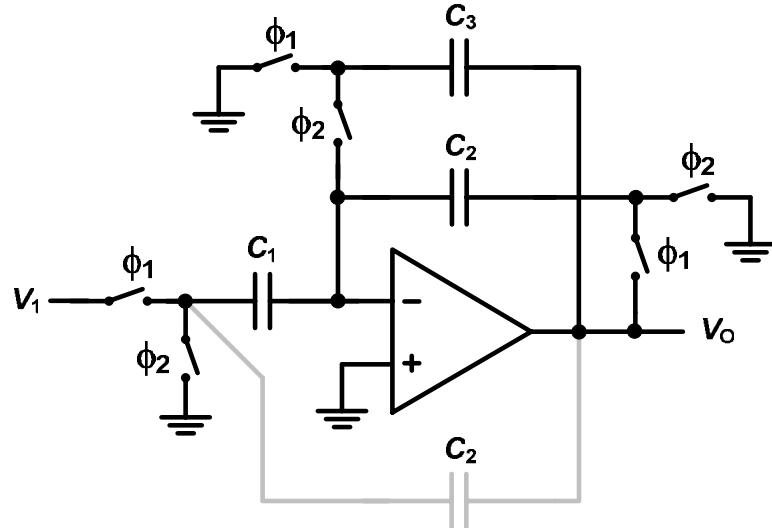
- Connection of capacitor to the unit-gain sampler



- The **input capacitance** of the op amp degrades both the **speed** and the **precision** of the unity-gain sampler/buffer
 - ▶ For this reason, the **bottom plate** of C_H is usually **driven** by the **input signal** or the **output** of the op amp and the **top plate** is **connected** to the node X , **minimizing** the **parasitic capacitance** seen from node X to ground
- Driving the bottom plate by the input or the output also avoids the injection of substrate noise of node X

Switched-Capacitor Gain Circuits

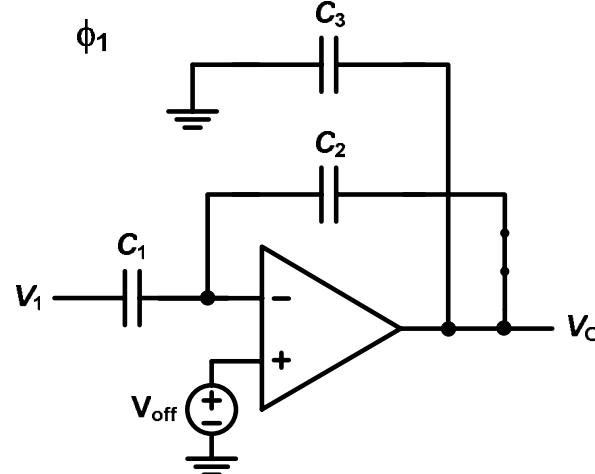
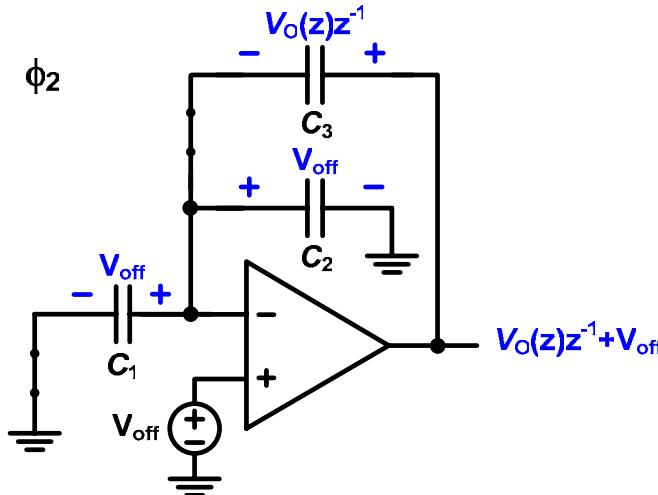
- Capacitor-Reset Gain Circuit



- “Deglitching” capacitor C_2 – 0.5pF or less
- Provide a feedback connection at some instant of time

$$V_o(z) = \left(-\frac{C_1}{C_2}\right)V_1(z)$$

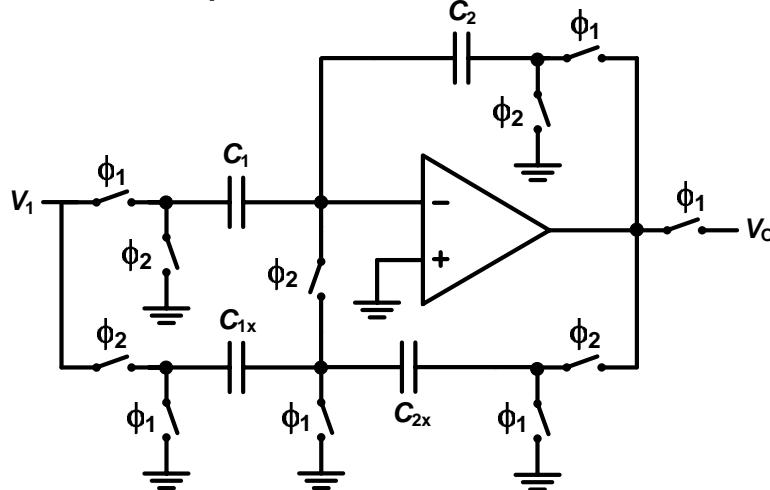
- The error due to finite opamp gain is proportional to $1/A^2$
- Relax the slew-rate requirement of opamp



Correlated Double Sampling (CDS)

- Minimize the error due to finite offset, 1/f noise, and finite opamp gain
- For high accurate gain amplifiers, S/H, integrators

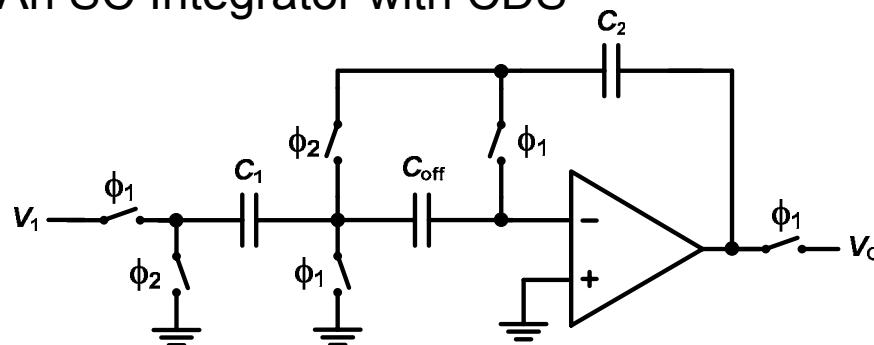
An SC Amplifier with CDS



- During ϕ_2 , the error is sampled and stored
- During ϕ_1 , the error is subtracted from the signal

$$V_o(z) = \left(-\frac{C_1}{C_2}\right)V_1(z)$$

An SC Integrator with CDS

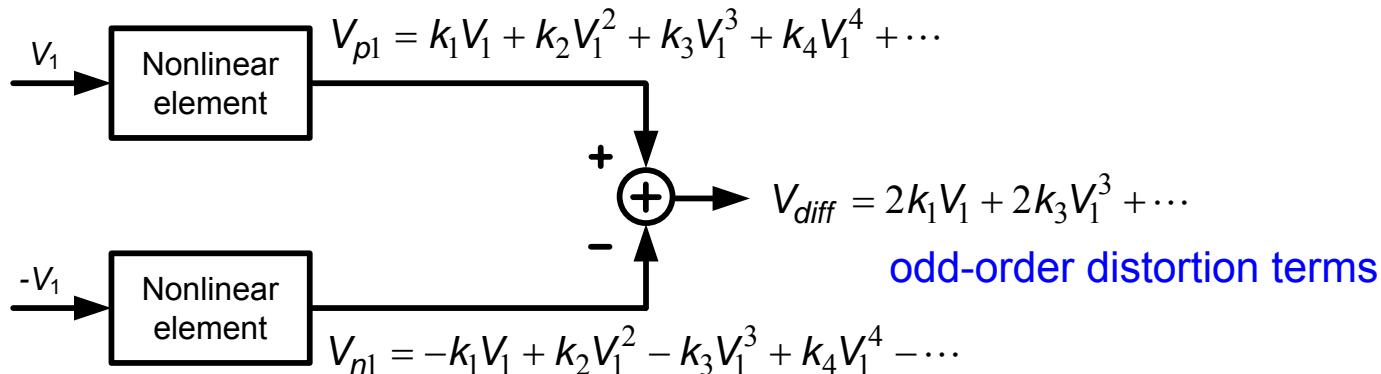


- It is useful for the oversampling A/D converters

$$V_o(z) = \left(\frac{C_1}{C_2}\right) \frac{z^{-1}}{1 - z^{-1}} V_1(z)$$

Full Differential Switched Capacitor Circuits

- Reject much more common-mode noise
- Better distortion performance



- Cancel the clock feedthrough of the switch
- The output swing is doubled
- The sampling capacitors can be half the size of those in single-ended case
 - The same dynamic range due to KT/C noise is maintained
- Common-mode feedback is needed

Operational Amplifiers (Opamps)

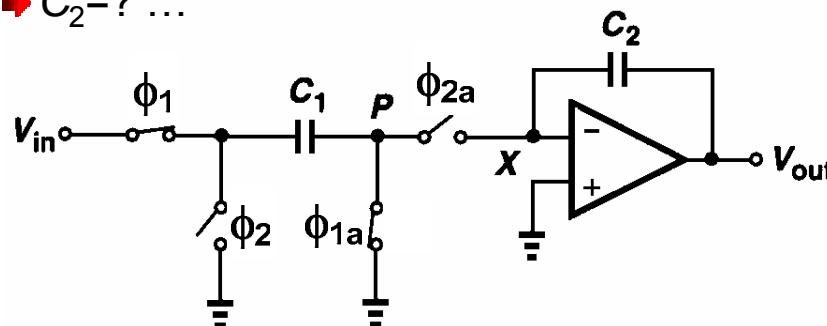
Department of Electrical Engineering

General Considerations

Input Capacitance

- The in-band noise power $P_N = \frac{kT}{C_1 \cdot OSR} = P_S \cdot 10^{-SNR/10}$ ($SNR = 10 \log_{10}(\frac{P_S}{P_N})$)

- Input sampling capacitor
- $C_1 = 1.29\text{pF}$
- $C_2 = ? \dots$



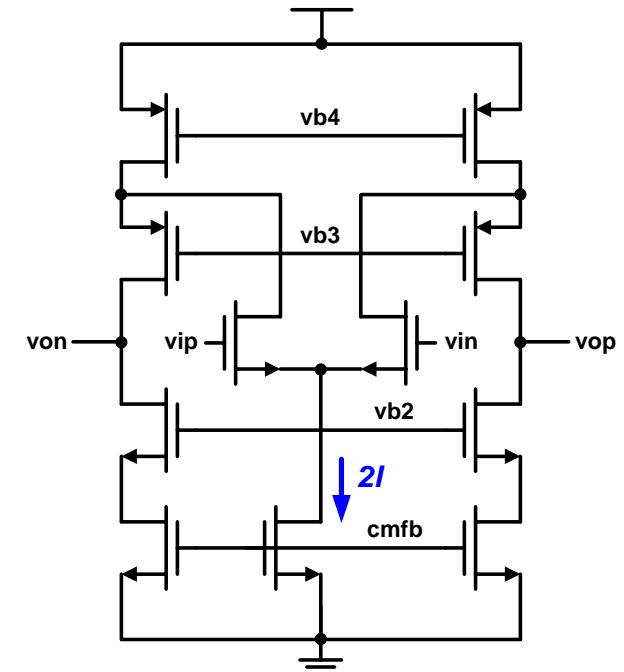
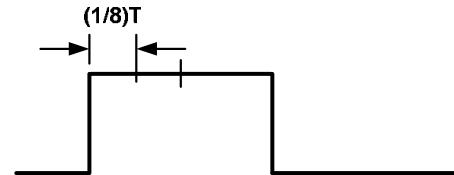
Amplitude = 1.0, SNR=100dB, OSR=64

$$\text{Input-referred thermal noise} = \frac{kT}{C_1}$$

Slew Rate

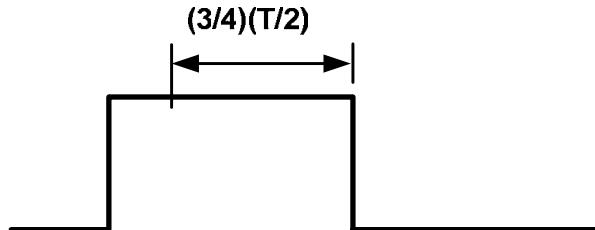
- The slew current I available at each output
- Integrating charge $C_1 V_{SW} = I \times \Delta t$

$$I = 8f_{CK}C_1V_{SW} = 8 \times 2.56\text{MHz} \times 1.29\text{pF} \times 2 = 53\text{ }\mu\text{A}$$



General Considerations

Transconductance of Opamp



$$\frac{T}{2} \times 75\% = 10\tau = 10 \times \frac{C_{load}}{\beta g_m} \Rightarrow g_m = 88 \mu A/V$$

Integrator Leakage

- Finite opamp open loop gain at dc A_0
 - ➡ Increase the in-band noise power
 - ➡ Integrator transfer function

$$\begin{aligned} H(z) &= \frac{z^{-1}}{\left[\frac{C_2}{C_1}\left(1 + \frac{1}{A_0}\right) + \frac{1}{A_0}\right] - \frac{C_2}{C_1}\left(1 + \frac{1}{A_0}\right)z^{-1}} \approx \frac{gz^{-1}}{1 - \frac{A_0 + 1}{A_0 + 1 + g}z^{-1}} \\ &= \frac{z^{-1}}{1 - \left(1 - \frac{g}{A_0 + 1 + g}\right)z^{-1}} = \frac{z^{-1}}{1 - (1 - \varepsilon)z^{-1}} \end{aligned}$$

➡ ε : leakage factor $<< 1$

Operational Amplifiers (Opamp)

- AC Analysis

- Gain、Phase Margin、Unit Gain Frequency
- Gain Margin (GM)
- Common Mode Voltage Gain (Acm)
- Common Mode Rejection Ratio (CMRR)
- Power Supply Rejection Ratio (PSRR \pm)
- Gain vs. Vout (Nonlinearity)
- Noise

- DC Analysis

- Output Swing
- Offset Voltage

- Tran Analysis

- Slew Rate and Settling Time
- Total Harmonic Distortion

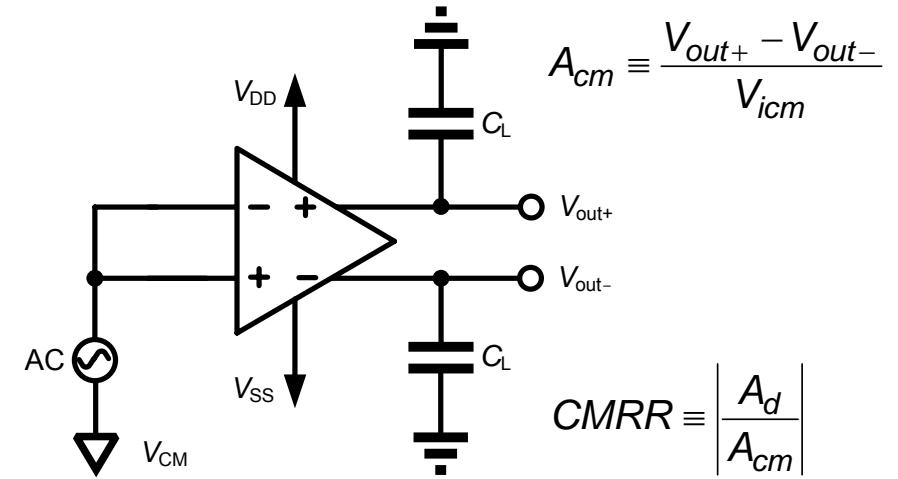
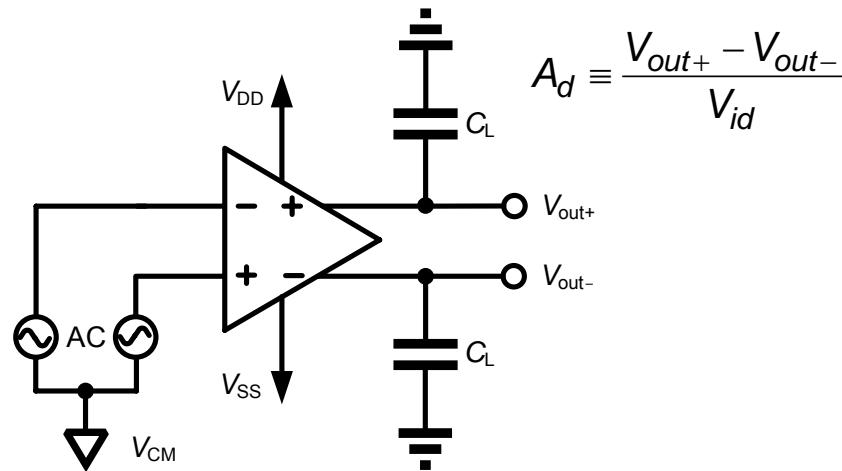
- Normal Analysis

- Average Power

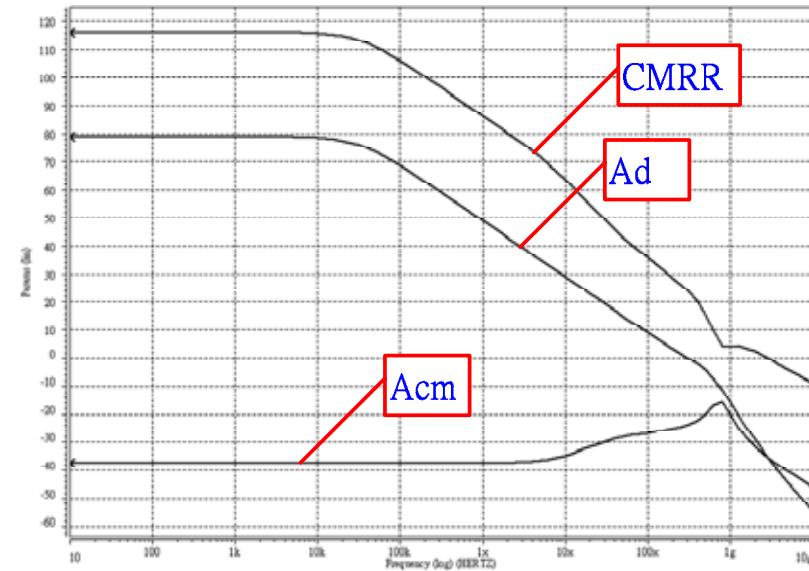
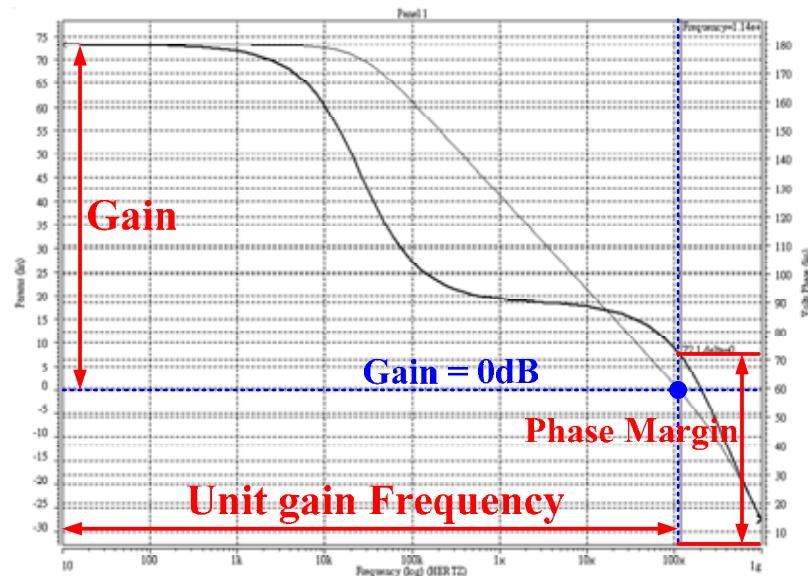


AC Response

- Differential Gain, Common-Mode Gain, Common Mode Rejection Ratio (CMRR)

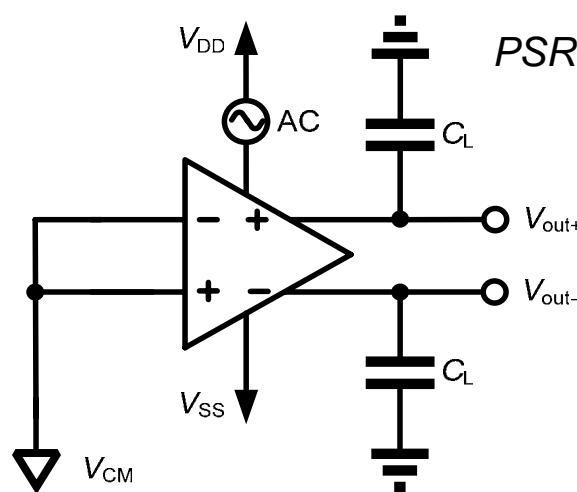


$$CMRR \equiv \left| \frac{A_d}{A_{cm}} \right|$$

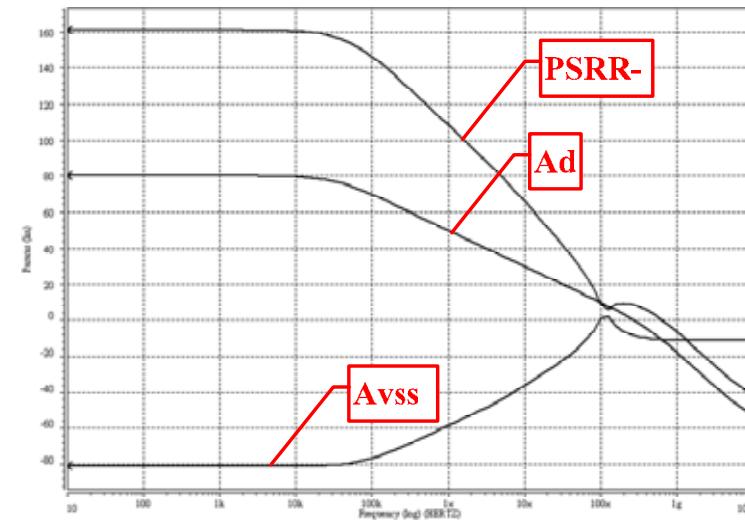
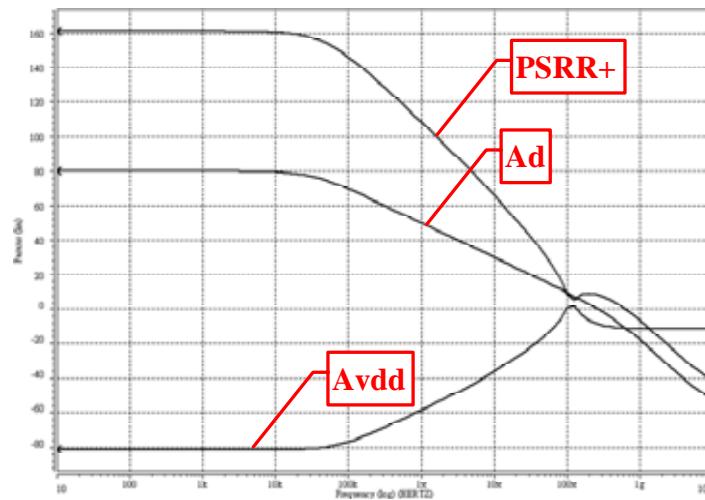
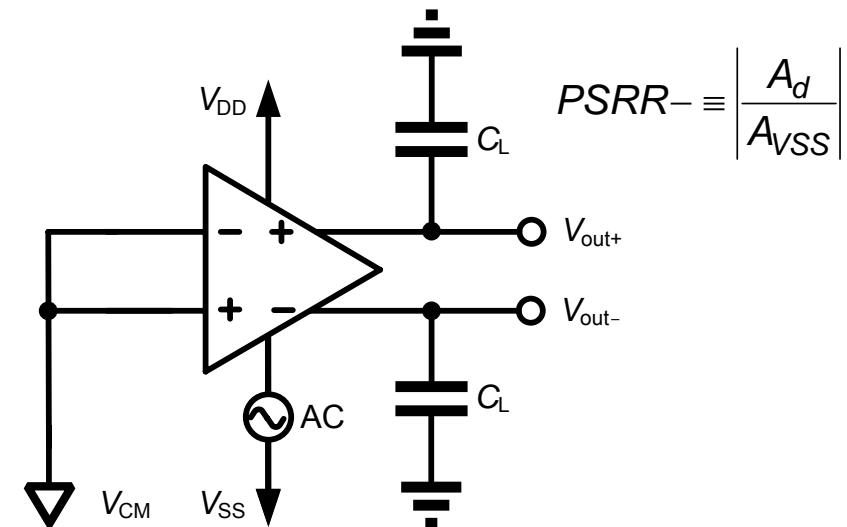


AC Response

● Power Supply Rejection Ratio (PSRR+)

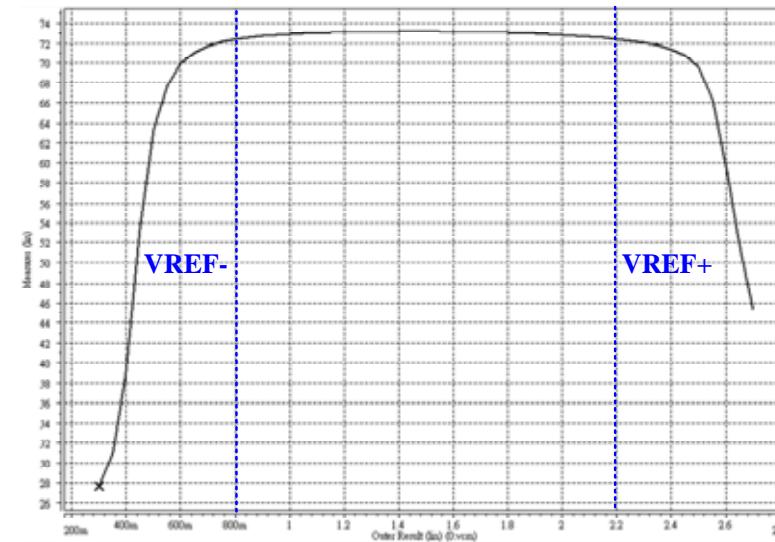
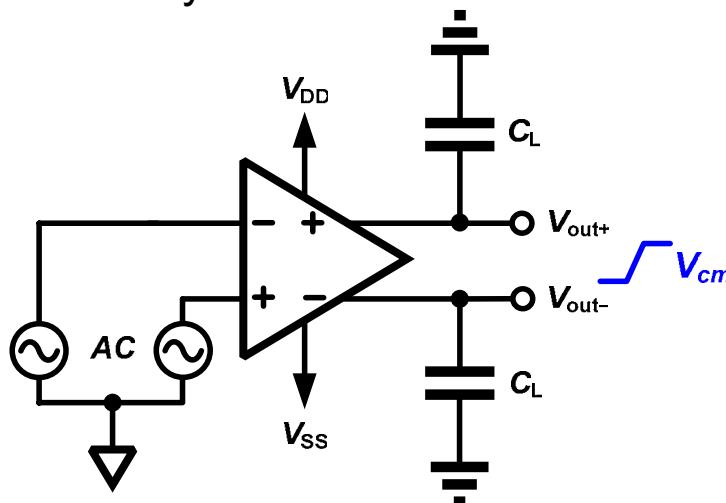


● Power Supply Rejection Ratio (PSRR-)

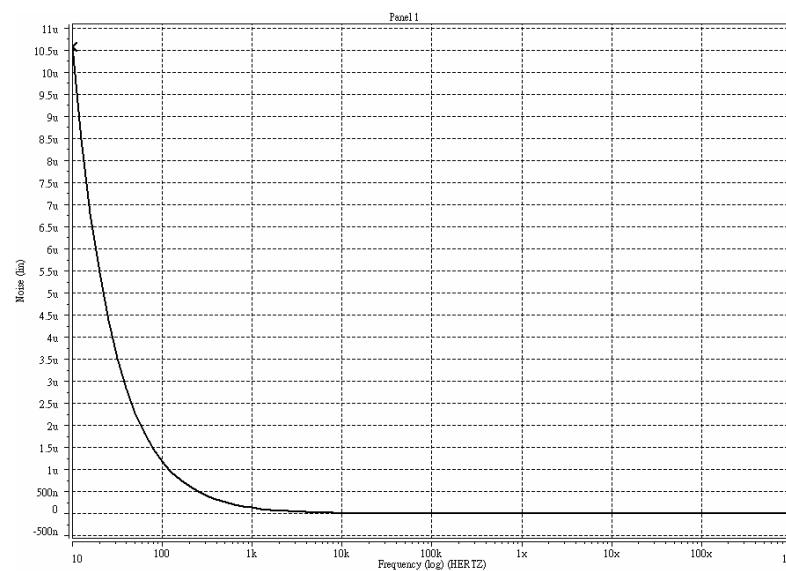
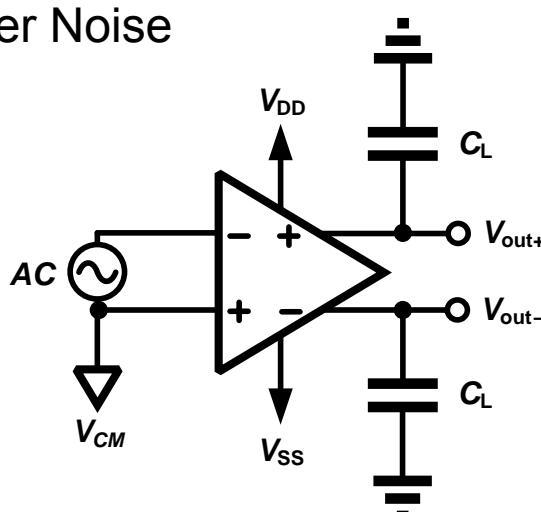


Differential Gain vs. Vout

- Nonlinearity

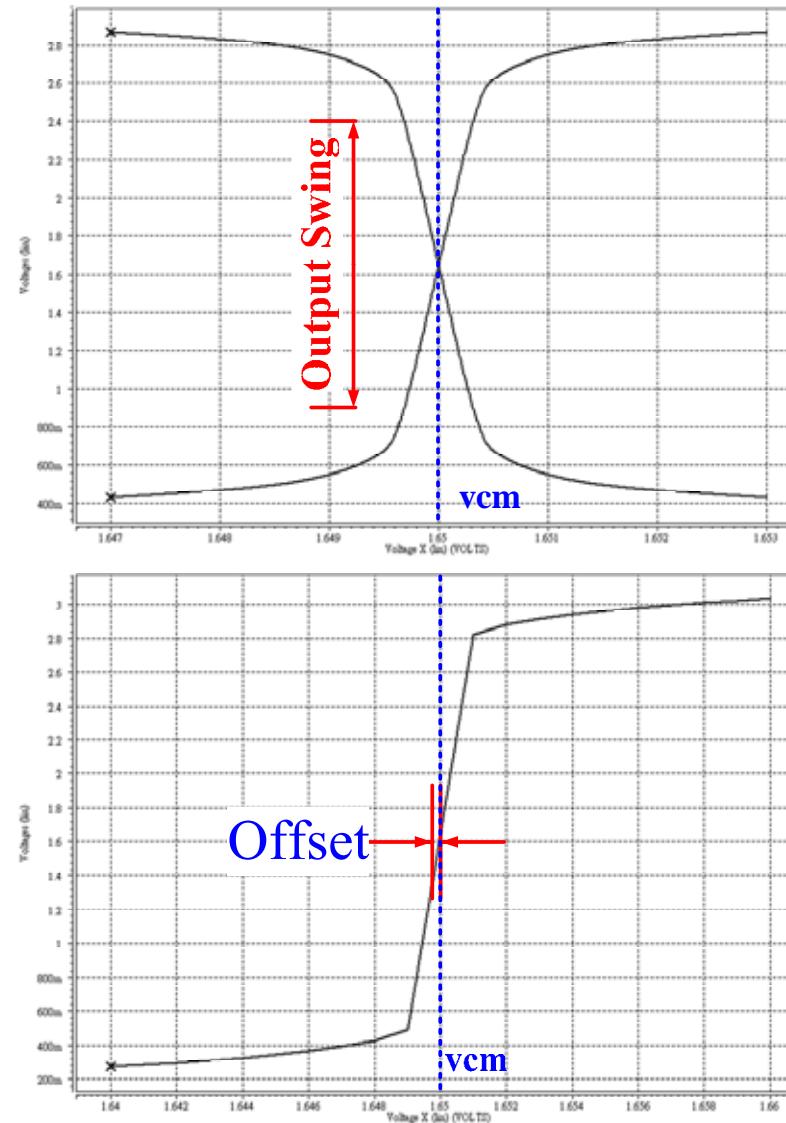
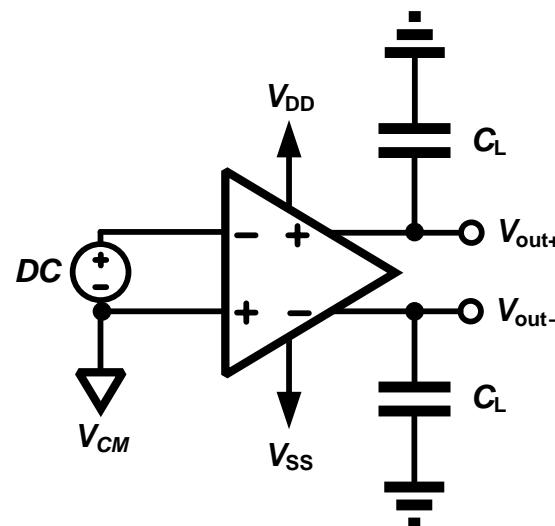


- Flicker Noise



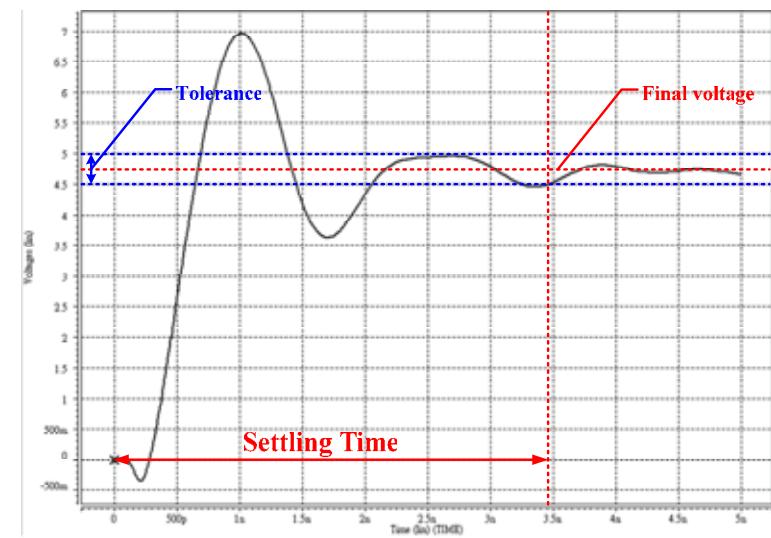
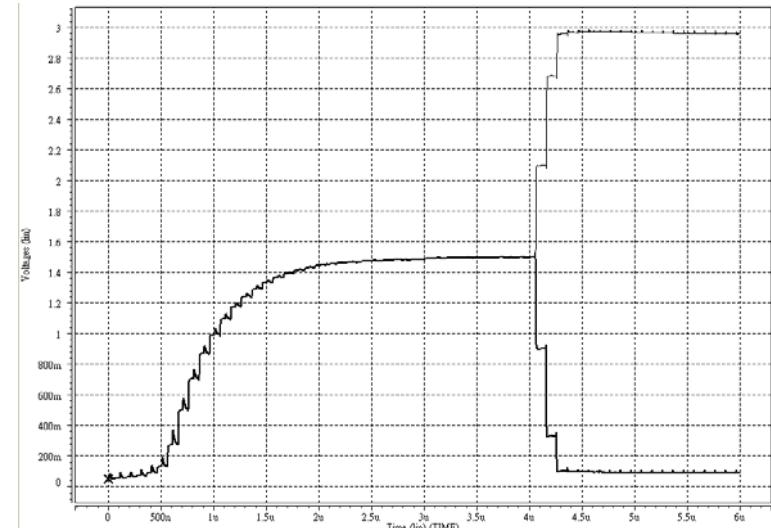
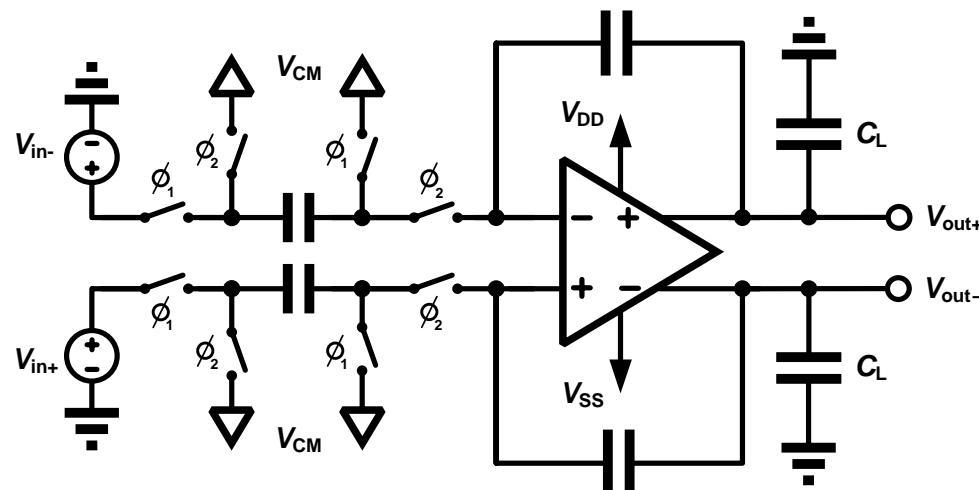
DC Analysis

- Output Swing
- Input Offset



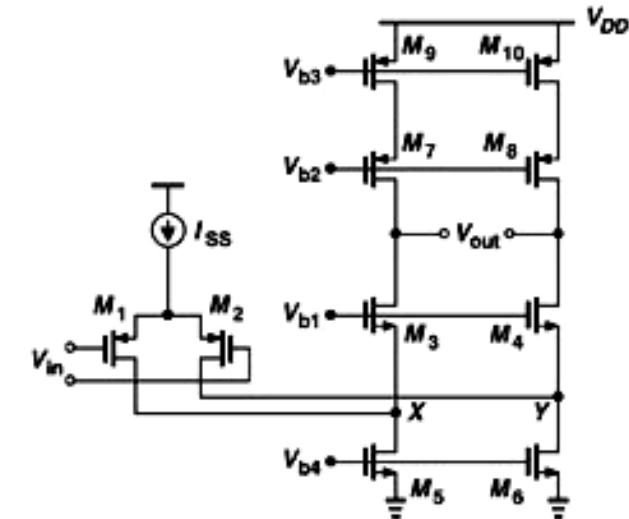
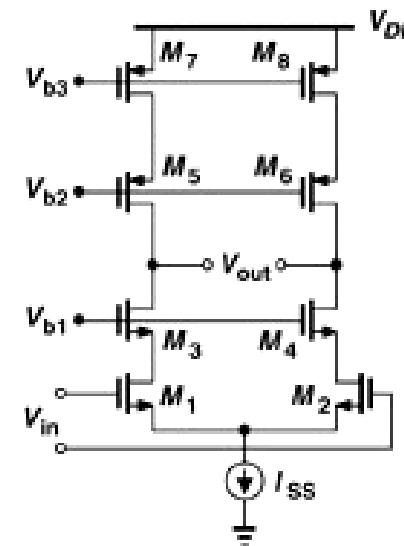
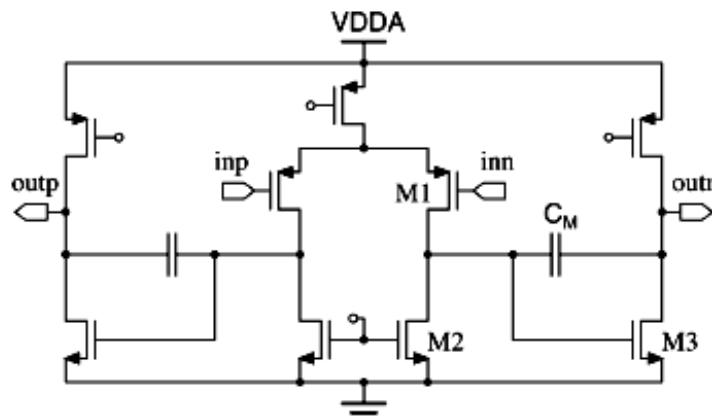
Transient Response

- Slew Rate
- Settling Time



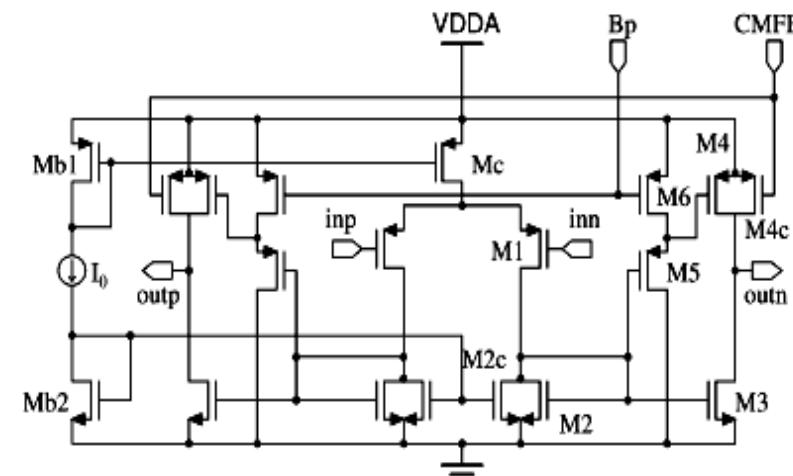
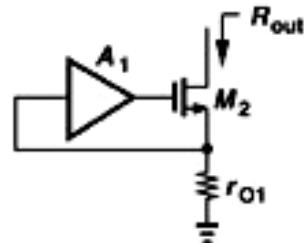
Fully Differential Operational Amplifier

- Two-Stage, Telescopic and Folded Cascode



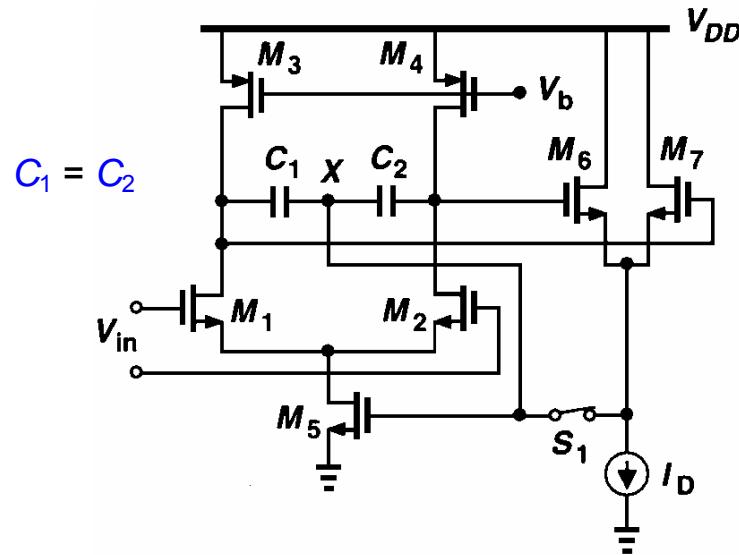
- Gain boosting in cascode output stage

Output swing is our concern



Switched-Capacitor Common-Mode Feedback

- The Definition of the Voltage across C_1 and C_2
 - In the sampling (or reset) mode - CM level definition



- The amplifier differential input is zero and S_1 is on
- $V_{GS6} = V_{GS7}$
- The output CM level = $V_{GS6,7} + V_{GS5}$

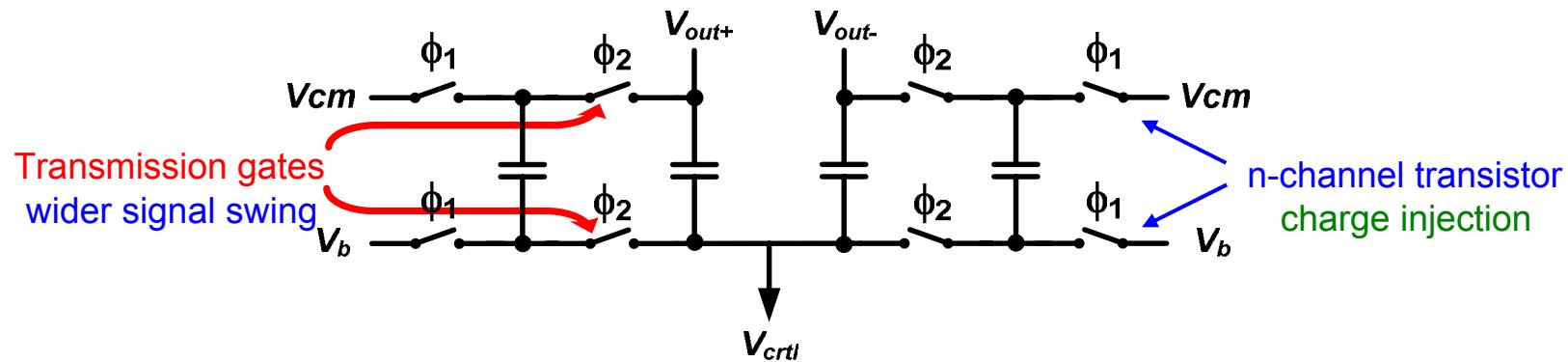
- At the end of the sampling mode
 - S_1 turns off, leaving a voltage equal to $V_{GS6,7}$ across C_1 and C_2

- In the amplification mode (S_1 is off)
 - reproduce the average of the changes in each output stage at node X
 - EX. if V_{out1} and V_{out2} experience a positive CM change
 - then V_X and hence I_{D5} increase
 - pulling V_{out1} and V_{out2} down
 - M_6 and M_7 may experience a large nonlinearity but they do not impact the performance of the main circuit

Switched-Capacitor Common-Mode Feedback

- Alternative Topology for Definition of Output CM Level

- SC low-pass filter



- C_C is used to generate the average of the output voltages
 - Control the current source
 - C_S determines the bias voltage across C_C
 - $C_S \approx (1/4 \sim 1/10) C_C$

Quantizer

Department of Electrical Engineering

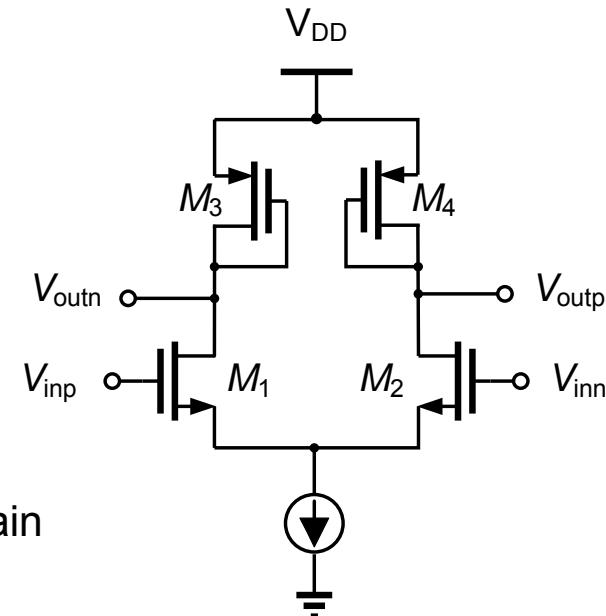
Comparators

- Design issue

- Resolution (gain)
- Speed
- Accuracy (offset)
- Power consumption
- Kickback noise

- Differential pair comparator

- Higher-mobility NMOS transistors to achieve higher gain
- Low input offset in differential pair
- Low gain



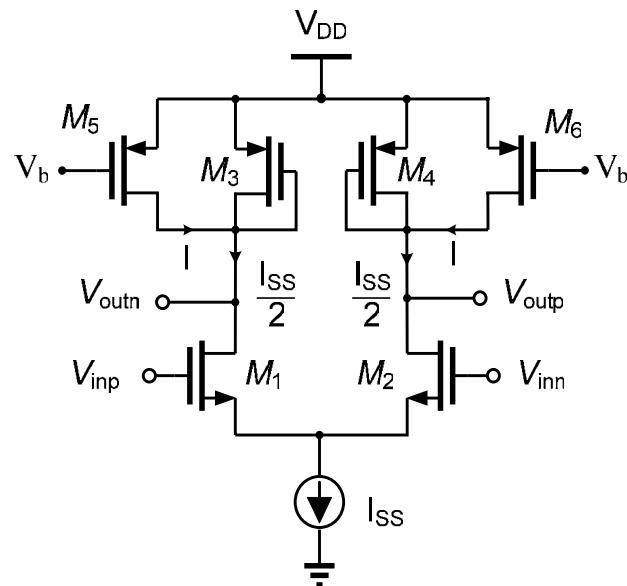
Differential pair with diode connected load devices

$$Av = \sqrt{\frac{\mu_n(W/L)_1}{\mu_p(W/L)_3}}$$

Gain Enhancement Comparator

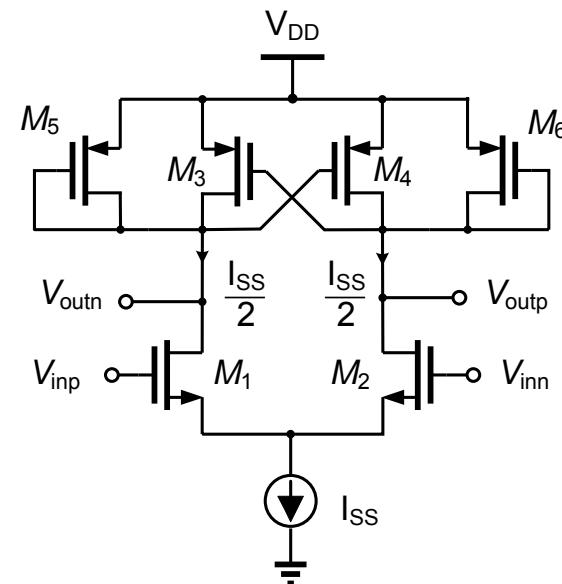
- To increase the gain of comparator

- When $I=0.9 \cdot (I_{SS}/2)$, the gain by a factor of $\sqrt{10}$
- A maximum value of I is 0.9



Gain-enhanced source-coupled differential pair

$$Av = \sqrt{\frac{\mu_n(W/L)_1}{\mu_p(W/L)_3(1 - 2 \cdot I/I_{SS})}}$$



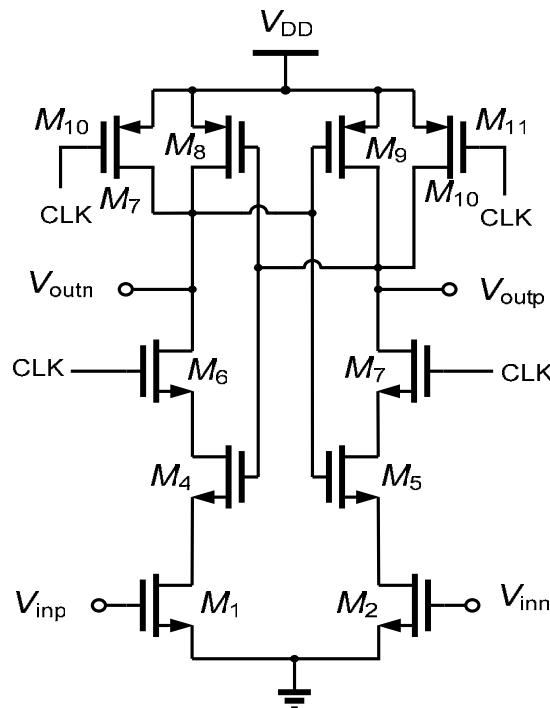
Using positive feedback to provide increased gain

$$Av = \sqrt{\frac{\mu_n(W/L)_1}{\mu_p(W/L)_3}} \frac{1}{1 - \alpha}$$

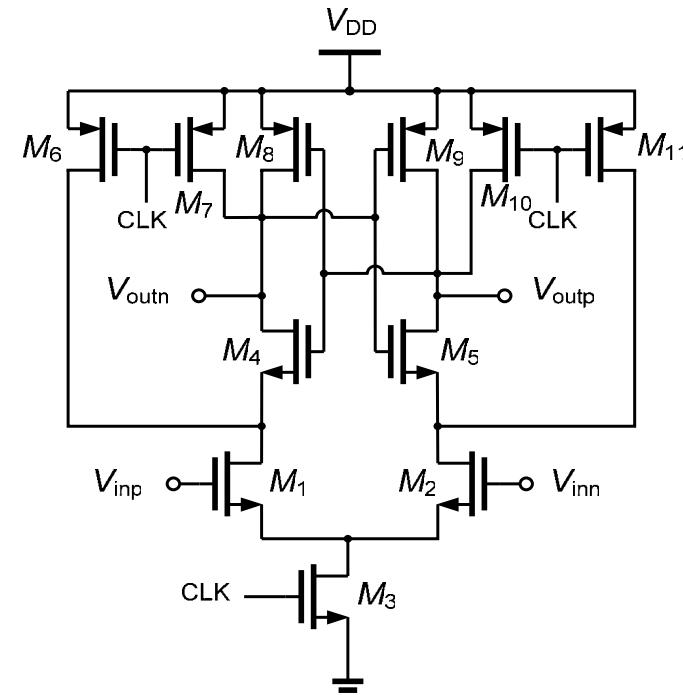
$$=(W/L)_3/(W/L)_5$$

Kickback Noise

- The regeneration is done by two cross-coupled CMOS inverters
 - No power consumption when $CLK=0$
 - The lower input offset with differential pair
 - The architecture of comparator have **kickback** noise problems
 - Caused by the voltage variations on the node



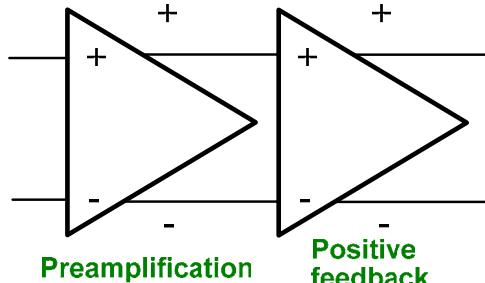
(a) Dynamic latched comparator



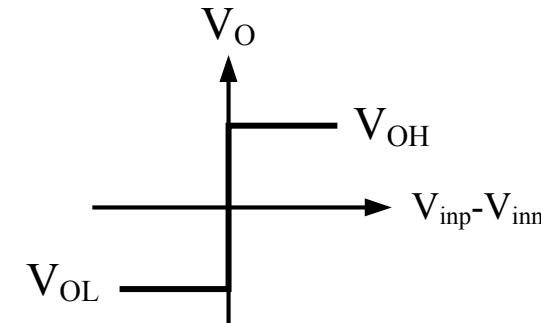
(b) Dynamic latched comparator with differential pair

Circuit Modeling of a Comparator

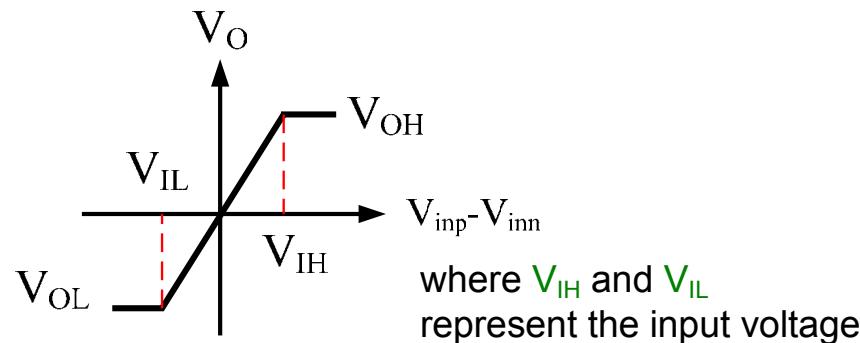
- The comparator consists of the input preamplifier and a positive feedback
 - Prevent the kickback noise from the output to the inputs of the comparator
 - The positive feedback stage is used to determine which of the input signal is larger



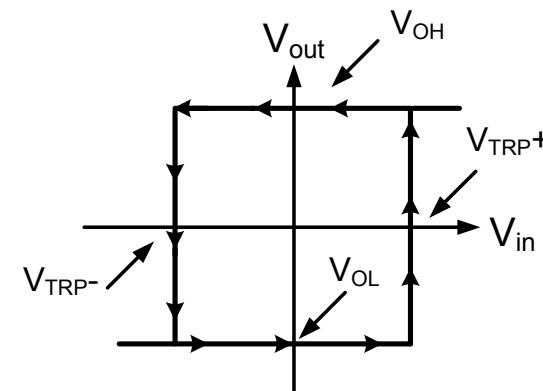
Block diagram of voltage comparator



Transfer curve of ideal comparator



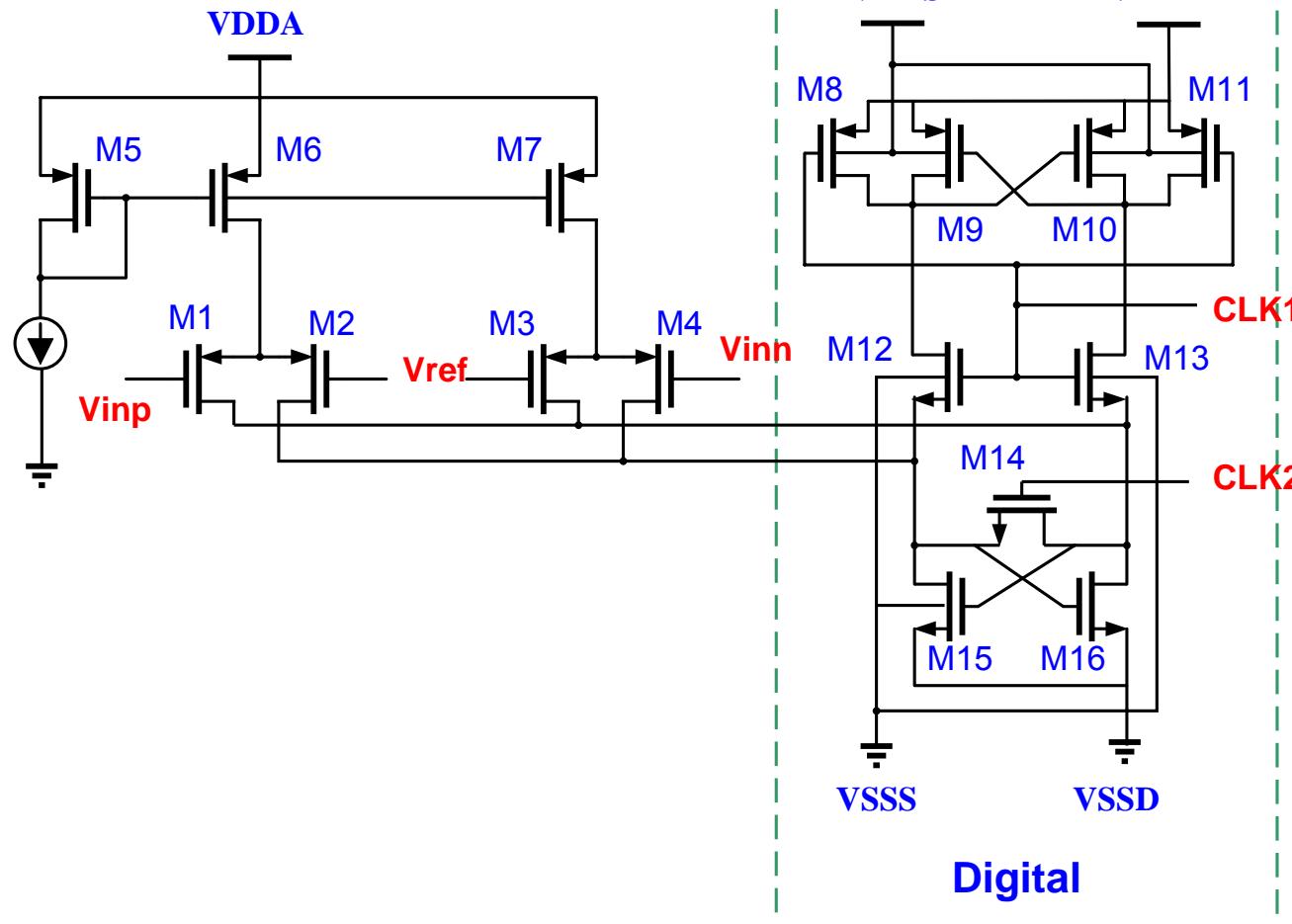
Transfer curve of comparator with finite gain



Transfer curve of comparator with hysteresis

Two Stage Comparator

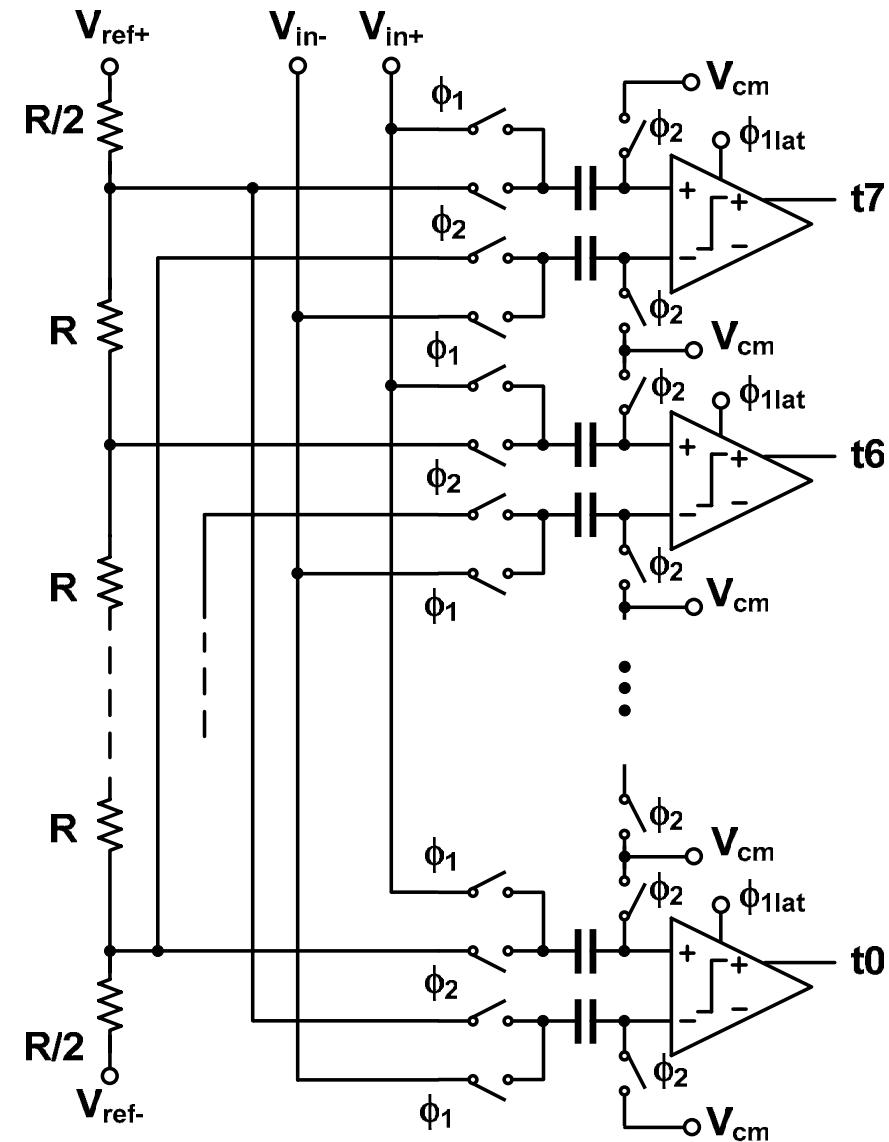
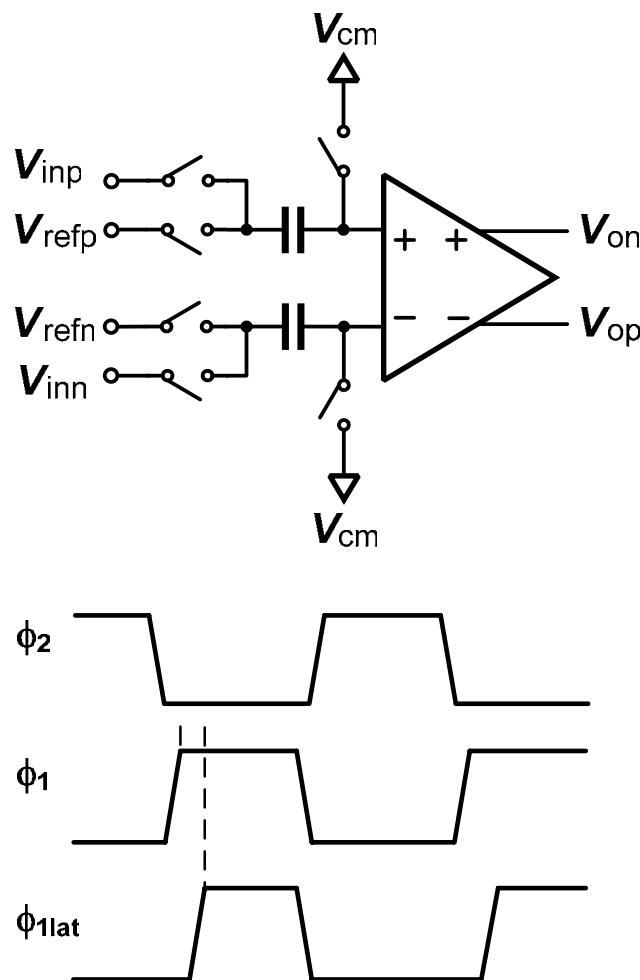
- Isolation on power (VDDA VDDS VDDD)
- Erasing comparator memory->M14



Flash Analog-to-Digital Converter

● SC Quantizer

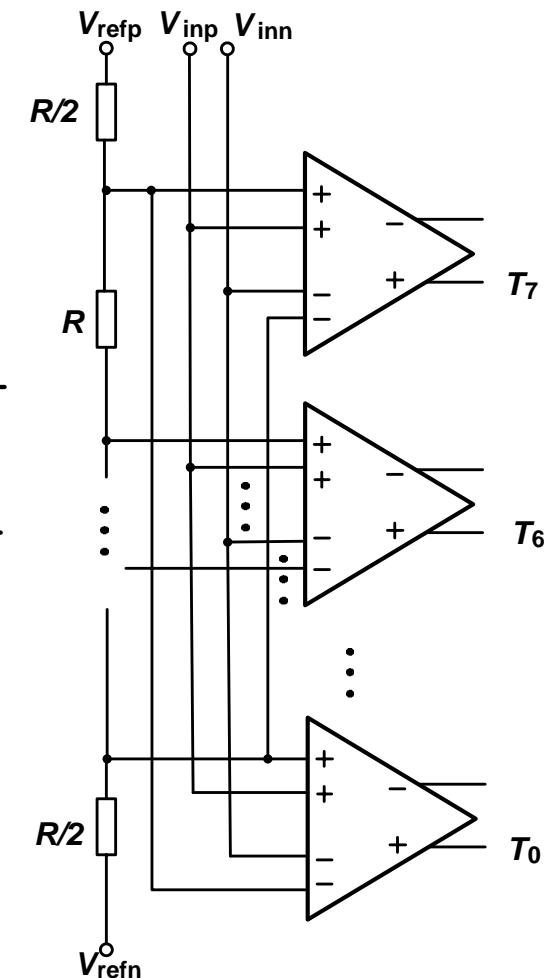
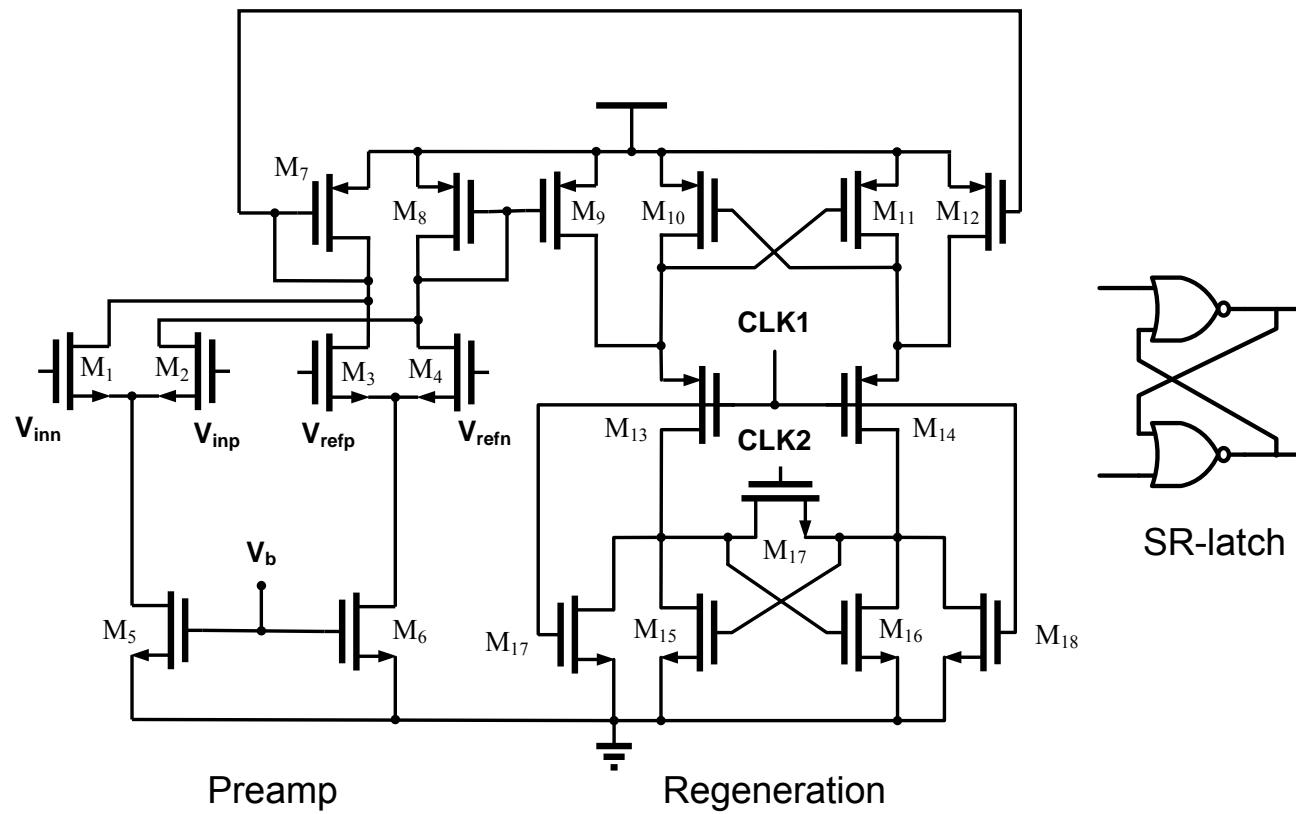
■ Comparator cell



Flash Analog-to-Digital Converter

- Better Isolation (kickback noise)

- One pair of current mirrors is added between the input differential pair and the regeneration stage



Imperfections in Switched-Capacitor Circuits

Department of Electrical Engineering

Error Sources in $\Delta\Sigma$ Modulators

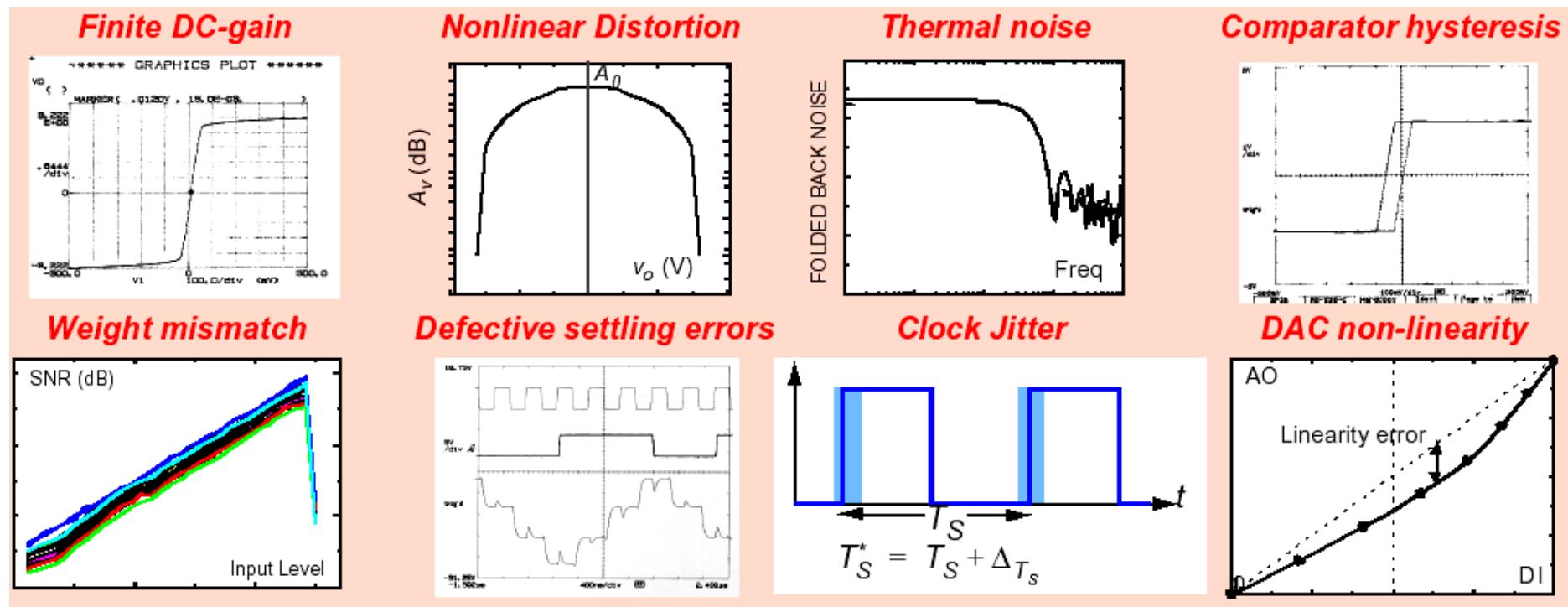
Actual In-band Noise Power

High-frequency applications

- Quantization error, DAC Nonlinearity error, finite DC gain, weight mismatch, defective settling

High-resolution applications

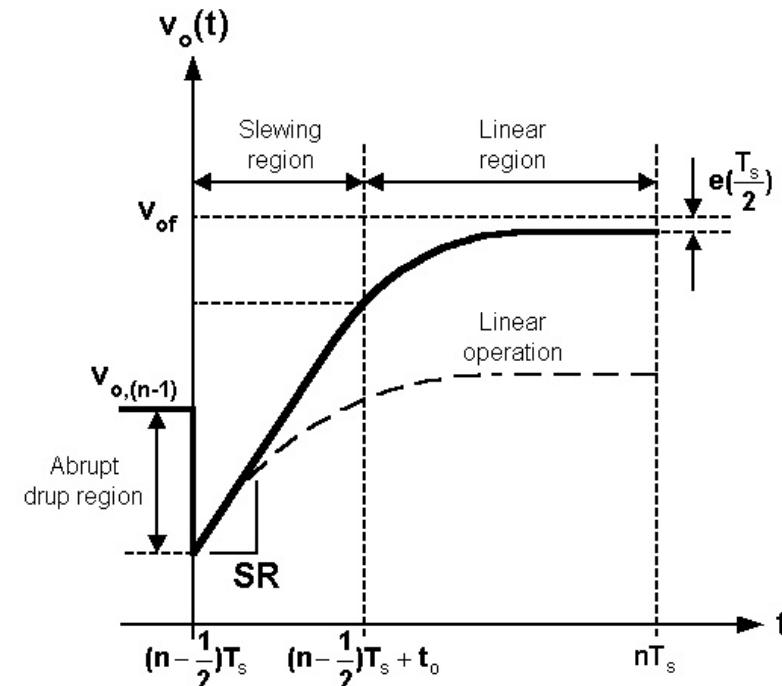
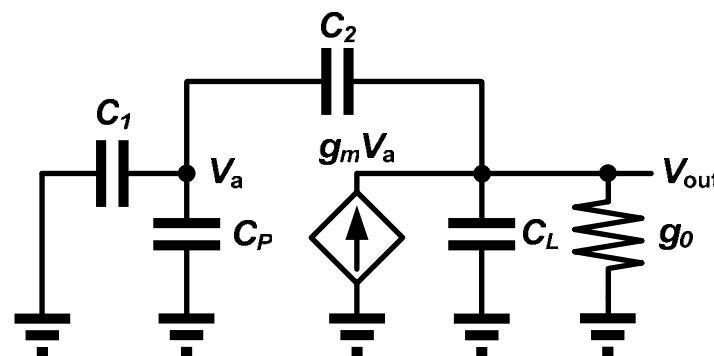
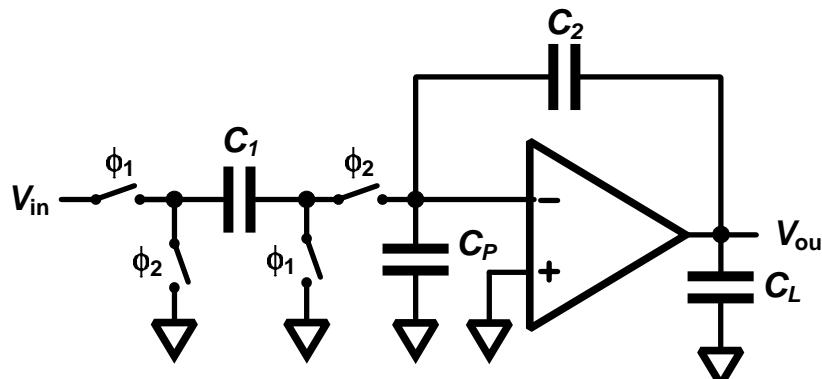
- Thermal noise, component nonlinearity



Error Sources in $\Delta\Sigma$ Modulators

- Incomplete Settling

- The performance of transient response is dominated in the integration phase
- Transient response model



$$v_{ai} = -\frac{C_2}{C_{eq}} \left(1 + \frac{C_L}{C_2}\right) v_i \quad C_{eq} = C_1 + C_P + C_L \left(1 + \frac{C_1 + C_P}{C_2}\right)$$

$$v_{oi} = v_{o,n-1} + \frac{C_2}{C_2 + C_L} v_{ai} = v_{o,n-1} - \frac{C_1}{C_{eq}} v_i$$

Error Sources in $\Delta\Sigma$ Modulators

- $|v_{ai}| \leq I_o/g_m$

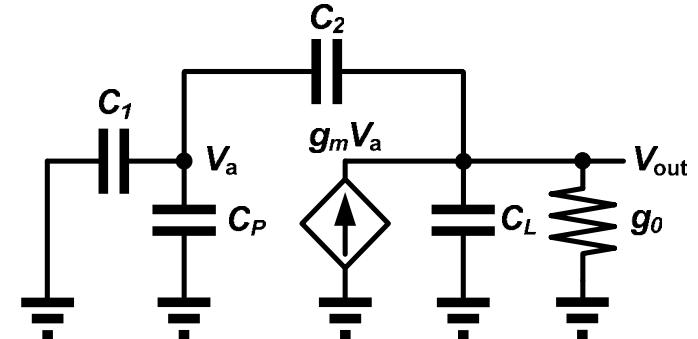
- Linear operation

- I_o : the maximum current that opamp can supply

- g_m : transconductance of opamp

$$v_o(t) = v_{of} - (v_{of} - v_{oi})e^{-t/\tau}$$

$$= \frac{v_{o,n-1} + \frac{C_1}{C_2}v_i}{1 + \frac{g_o}{g_m}(1 + \frac{C_1 + C_P}{C_2})} + \left(-\frac{v_{o,n-1} + \frac{C_1}{C_2}v_i}{1 + \frac{g_o}{g_m}(1 + \frac{C_1 + C_P}{C_2})} + v_{oi} \right) \cdot e^{-\frac{g_m + g_o(1 + \frac{C_1 + C_P}{C_2})}{C_{eq}} \cdot t}$$



- $|v_{ai}| > I_o/g_m$

- Slewling

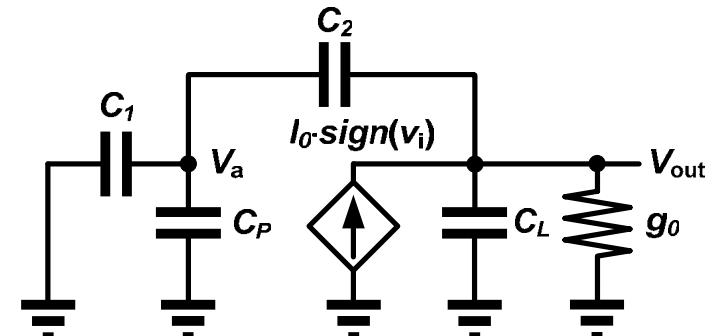
- Integrator gain depends on the input

- Harmonic distortion

- The voltage at node A

$$v_a(t) = v_{af} + (v_{ai} - v_{af}) \cdot e^{-t/\tau} \quad v_o = \left(1 + \frac{C_1 + C_P}{C_2}\right) v_a(t) + v_{o,n-1} + \frac{C_1}{C_2} v_i$$

$$= \frac{I_o \cdot \text{sgn}(v_i)}{g_o \cdot [1 + (C_1 + C_P)/C_2]} - \frac{v_{o,n-1} + (C_S/C_I)v_i}{[1 + (C_1 + C_P)/C_2]} + \left\{ v_{ai} - \frac{I_o \cdot \text{sgn}(v_i)}{g_o \cdot [1 + (C_1 + C_P)/C_2]} + \frac{v_{o,n-1} + (C_1/C_2)v_i}{[1 + (C_1 + C_P)/C_2]} \right\} \cdot e^{-g_o \frac{1 + (C_1 + C_P)/C_2}{C_{eq}} t}$$



Error Sources in $\Delta\Sigma$ Modulators

- $|v_a(t_0)| = I_o/g_m$

■ Enter linear zone

➡ For $g_o \ll 1$

$$v_a(t_0) \approx v_{ai} + \frac{I_o \cdot \text{sgn}(v_i)}{C_{eq}} t_0 = \frac{I_o}{g_m}$$

$$t_0 = -\frac{C_{eq}}{g_m} + \frac{C_1}{I_o} \cdot |v_i| \cdot (1 + \frac{C_L}{C_2})$$

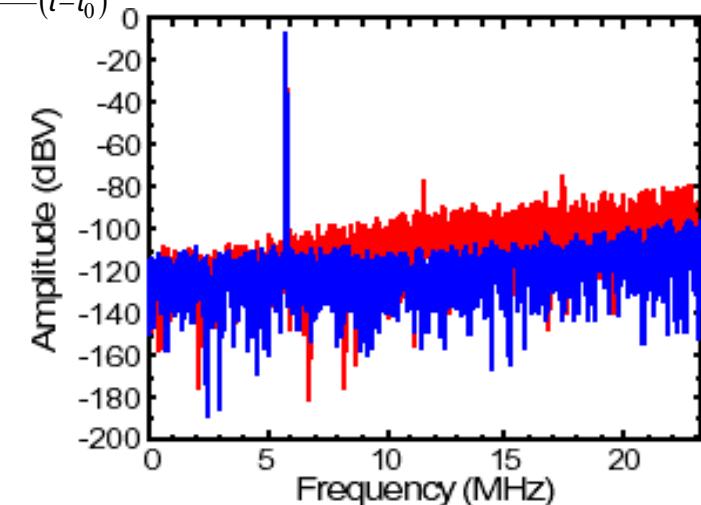
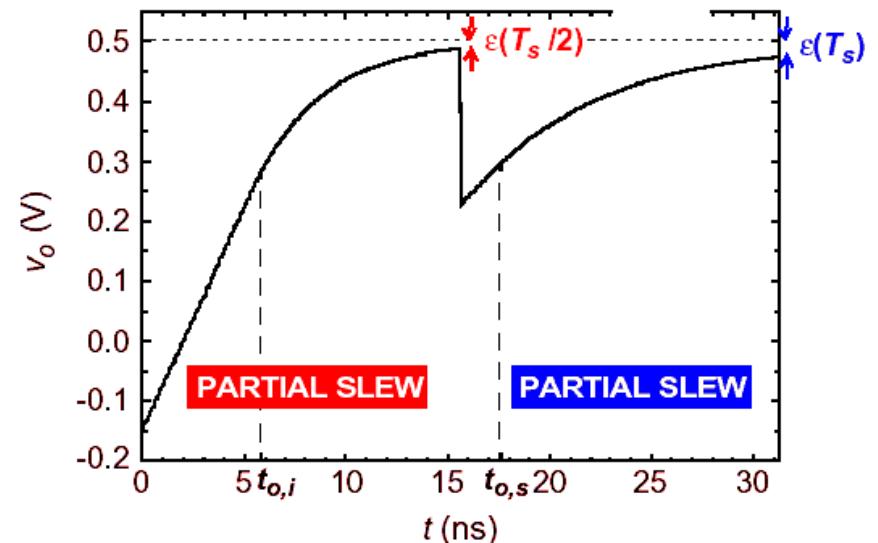
➡ For $t > t_0$

$$v_a \approx -\frac{v_{o,n-1} + (C_1/C_2)v_i}{1 + (g_m/g_o) + (C_1 + C_P)/C_2}$$

$$+ \left[\frac{v_{o,n-1} + (C_1/C_2)v_i}{1 + (g_m/g_o) + (C_1 + C_P)/C_2} - \frac{I_o \cdot \text{sgn}(v_i)}{g_m} \right] \cdot e^{-\frac{g_m + g_o[1 + (C_1 + C_P)/C_2]}{C_{eq}}(t - t_0)}$$

$$v_o = (1 + \frac{C_S + C_P}{C_I})v_a(t) + v_{o,n-1} + \frac{C_S}{C_I}v_i$$

- The relation between v_o and v_a depends nonlinearity on time
- ➡ Increase the noise floor
 - ➡ SNDR degradation



Error Sources in $\Delta\Sigma$ Modulators

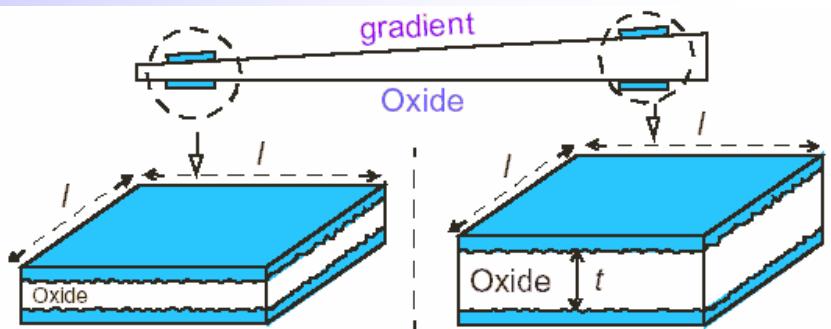
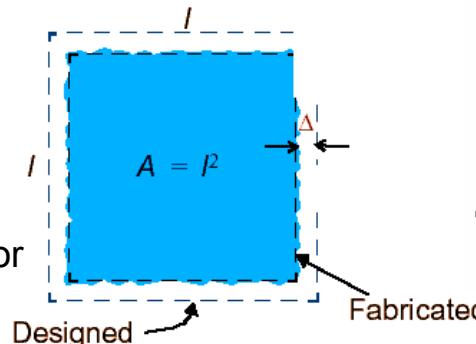
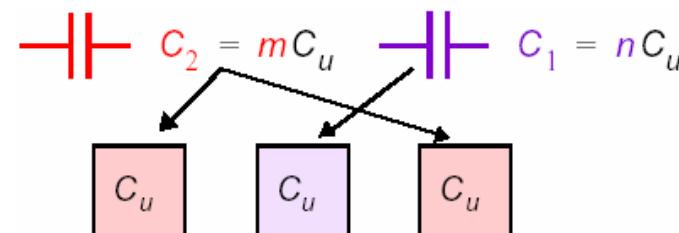
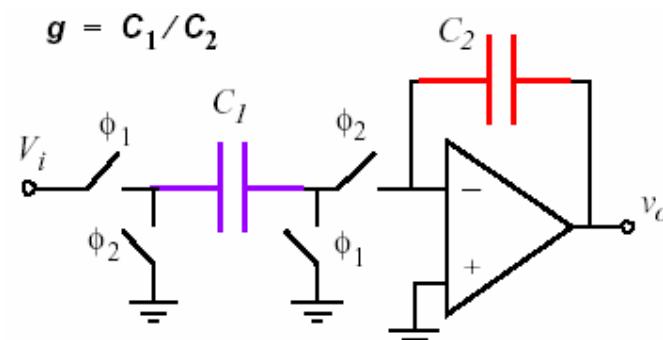
- Weight Mismatch

- Capacitors

- Edge error
 - Diffusing gradient error
 - Dielectric constant error

- Layout strategy

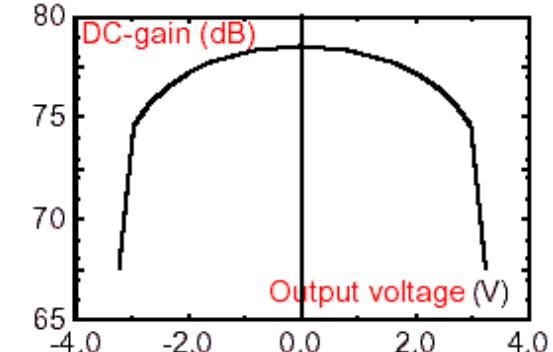
- Common centroid



- Opamp nonlinear gain

- Error Coefficients

- Second- and third-order harmonics at the modulator output
 - Opamp gain depends on the integrator output voltage



$$v_{out} = v_{out} \cdot z^{-1} + \left[\frac{C_i}{C_o} v_{in} + \frac{v_{out}}{A(n-1)} \right] \cdot z^{-1} - \left(1 + \frac{C_i}{C_o} \right) \cdot \frac{v_{out}}{A(n)}$$

Jitter Noise

- The sampling of the signal is not uniform
 - Produce amplitude error
 - Suppose time jitter with amplitude α and frequency ω
 - Sample at time from τ to $\tau + \alpha \sin(\omega t)$
 - Input signal for $\alpha \omega_0 \ll 1$

$$A \cos \omega_0 \tau \rightarrow A \cos[\omega_0(\tau + \alpha \sin \omega \tau)]$$

$$\approx A \cos(\omega_0 \tau) + \frac{A \omega_0 \alpha}{2} [\cos((\omega_0 - \omega)\tau) - \cos((\omega_0 + \omega)\tau)]$$

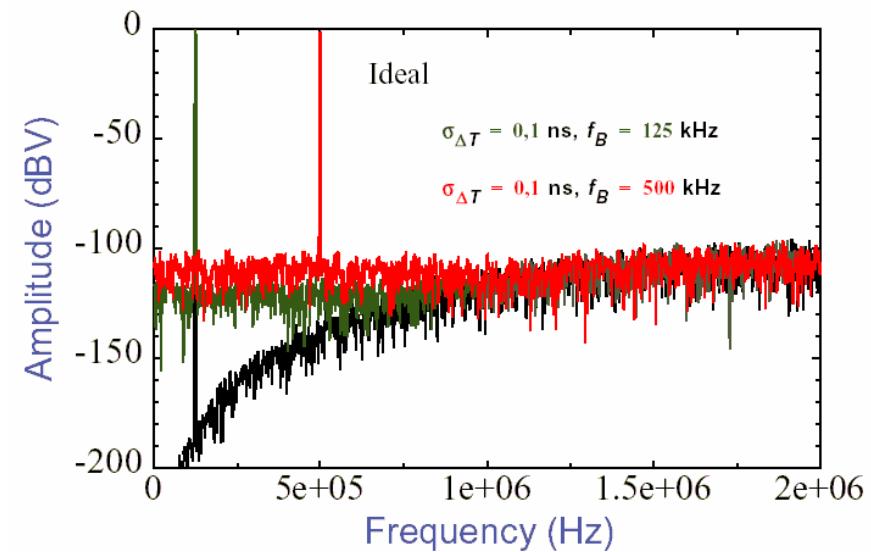
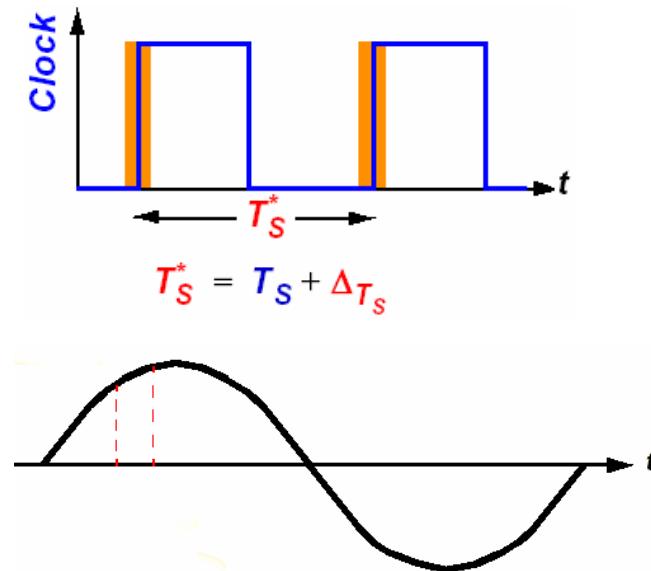
- Jitter is modulated by the input signal
- If jitter is white with a power $(\Delta \tau)^2$

The resulting error power from 0 to $\text{fs}/2$

$$(A \omega_0 \Delta \tau)^2 / 2$$

In-band noise power

$$\frac{A^2 (\omega_0 \Delta \tau)^2}{2 \text{ OSR}}$$



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- [15] R. Schreier, G. C. Temes, "Understanding Delta-Sigma Data Converters," IEEE Press Wiley Interscience 2005.



Low-Voltage Delta Sigma Modulators

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Outline

1. Introduction
2. Low Voltage Circuits for Delta Sigma Modulator
3. Low Voltage Nested-Chopper Delta Sigma Modulator
4. Low Voltage Second-Order Delta Sigma Modulator Using a Single Opamp
5. Low Voltage Fourth-Order Bandpass Delta Sigma Modulator



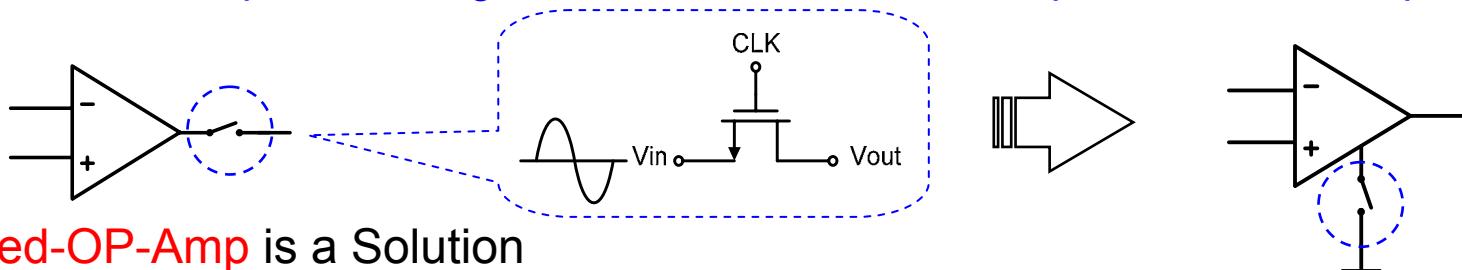
Introduction

● Why Low Supply Voltage

- Reduce the size and weight of the battery
- Low power consumption to prolong the battery lifetime
- Reduced gate oxide breakdown voltage in today's submicron technology
- The Semiconductor Industry Association predicts
 - ▶ 1.5V in 2001, 0.9V in 2006~2009

● The Main Issue — Low Gate Overdrive on Switch and OP-Amp

- Low Gate Overdrive on Switch
 - ▶ Multi-threshold technology (low threshold devices), expensive
 - ▶ Voltage multipliers, devices can not sustain in deep sub-micron technology
- Switched OP-Amp, eliminating the series switch with the output nodes of the Op-Amp



● Switched-OP-Amp is a Solution

- Two-stage OP-Amp topology that turns on and off the output stage for high speed applications
- One terminal of other switches is at V_{DD} (NMOS) or ground (PMOS)

Outline

1. Introduction
2. Low Voltage Circuits for Delta Sigma Modulator
 - Low Voltage Switched Capacitor Circuits
 - Switched Opamp Technique
 - Low Voltage Quantizer
3. Low Voltage Nested-Chopper Delta Sigma Modulator
4. Low Voltage Second-Order Delta Sigma Modulator Using a Single Opamp
5. Low Voltage Fourth-Order Bandpass Delta Sigma Modulator

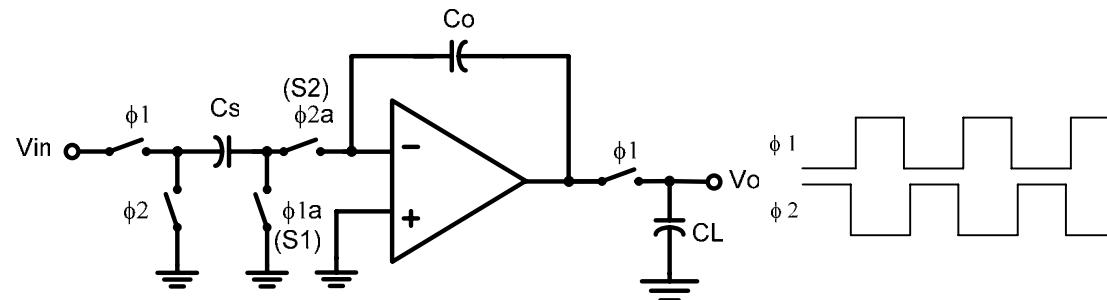


Low Voltage Switched Capacitor Circuits

- Switched Capacitor Circuits

 - Integrator

 - Non-overlapping clocks



$$\frac{V_o(z)}{V_{in}(z)} = \left(\frac{C_s}{C_0} \right) \frac{z^{-1}}{1-z^{-1}} = A_o \frac{z^{-1}}{1-z^{-1}}$$

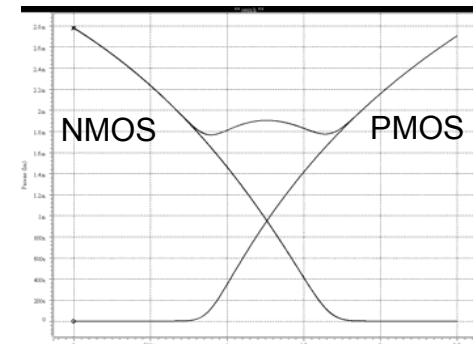
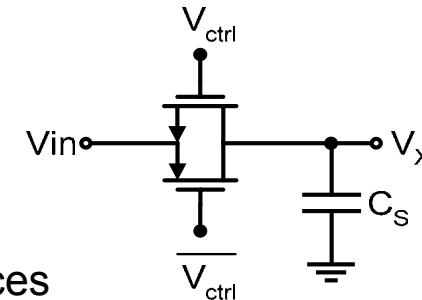
- Low Voltage Switched Capacitor Circuits

 - Driving problem of the switch

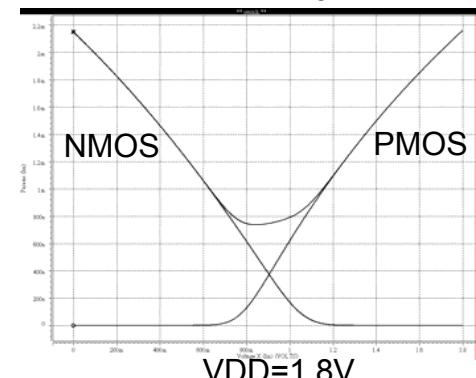
 - Transmission gate

 - Dimensions of the NMOS and PMOS devices

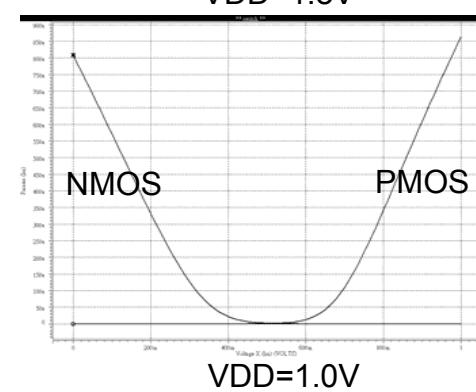
are $W/L=2.5\mu m/0.25\mu m$ with a multiplicand ratio 1:4



$VDD=2.5V$



$VDD=1.8V$

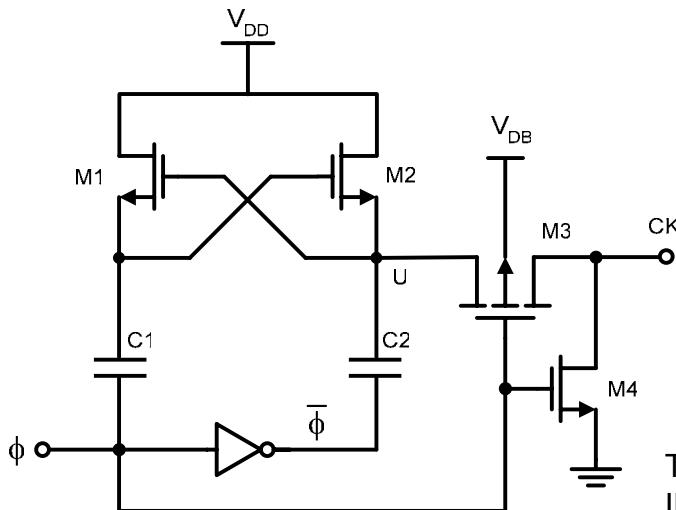


$VDD=1.0V$

Solutions for Driving Problem of Switch

• Voltage Boosting Technique

- The clock ϕ is high
 - ▶ M2 on, C2 is charged to V_{DD}
 - ▶ M4 on, output CK down to low
- The clock ϕ is low
 - ▶ Node U up to $2V_{DD}$
 - ▶ M4 off, M3 on, output CK $\Rightarrow 2V_{DD}$
 - ▶ C_P : parasitic capacitor at node U
 - ▶ $C_{G,switch}$: gate capacitance of the following sampling switches
- not to be suited for future deep submicro technology



$$V_H = 2V_{DD} \frac{C_2}{C_2 + C_P + C_{G,switch}}$$

T. B. Cho and P. R. Gray, "A 10b, 20Msample/s, 35mW Pipeline A/D Converter," IEEE J. Solid-State Circuits, vol. SC-30, pp.166-172, Mar. 1995

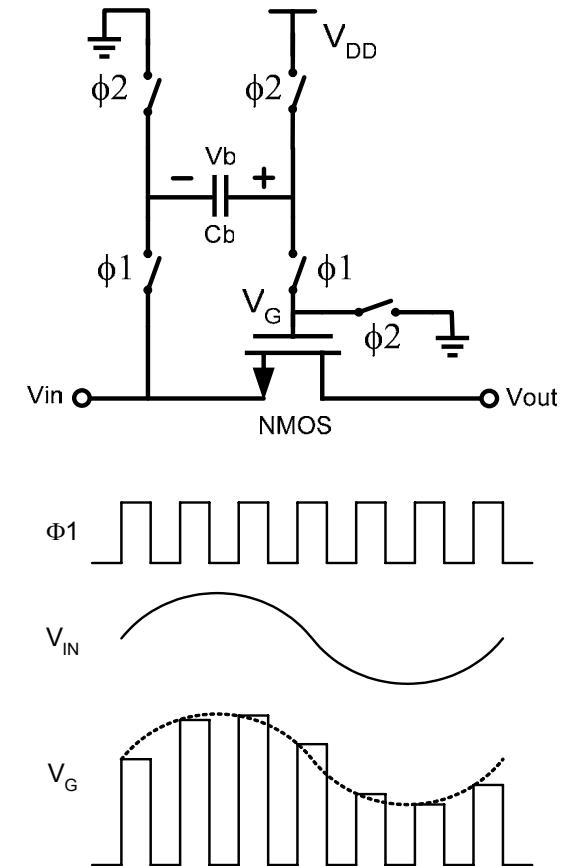
Solutions for Driving Problem of Switch

Multi-Threshold Voltage Technology

- make use of a few extra masking and doping steps to reduce the threshold voltage
- Expensive
- Increase of the leakage current
 - more signal dependent charge loss
 - harmonic distortion resulted

Bootstrapped Switch

- In phase ϕ_2
 - C_b is precharged
 - NMOS off
- In phase ϕ_1
 - driven voltage $V_{in} + V_{DD}$ to ensure a constant V_{GS}
- constant on-resistance



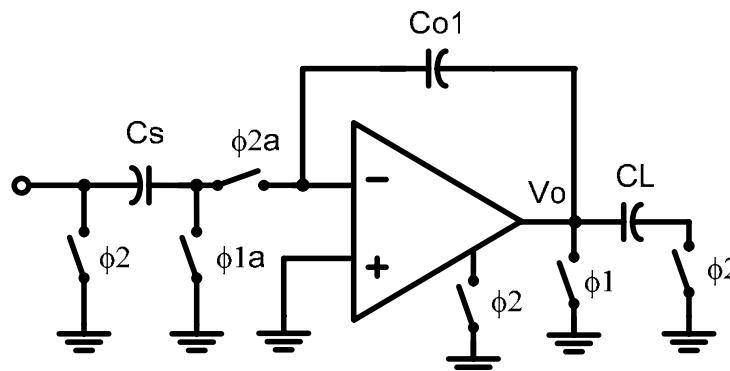
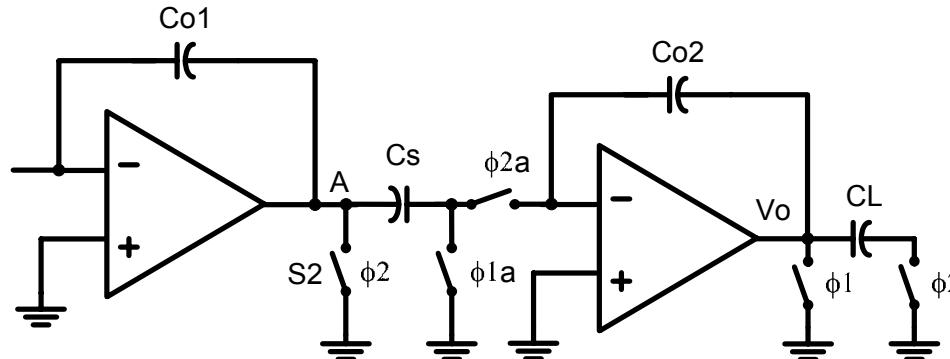
M. Dessouky, A. Kaiser, "Input Switch Configuration for Rail-to-Rail Operation of Switched Opamp Circuits," Electron Letters, vol.35, no. 1, pp. 8-10, Jan. 1999

Switched Opamp Technique

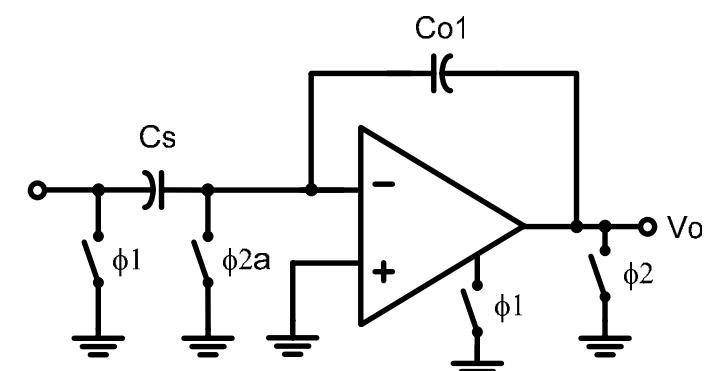
Evolution

Half-delay Switched Opamp Integrator

➡ Avoid node A unstable during charge transfer



Half-delay Switched Opamp Integrator



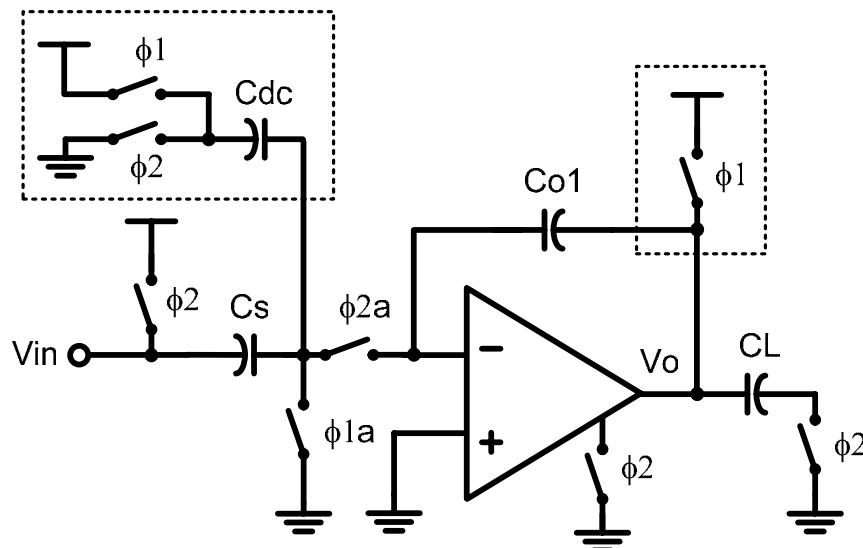
Half delay element

V. Peluso, M. Steyaert, and W. Sansen, "Design of Low-Voltage Low-Power CMOS Delta-Sigma A/D Converters," Kluwer Academic Publishers, 1999.

Switched Opamp Technique

Offset Compensating Circuit

- To avoid the input node of amplifier drop below V_{SS}
- DC offset between the input and output of the amplifier
- This single-ended structure cannot allow an inverting architecture
 - Fully differential
- Operative speed of the circuit is limited
 - Double output stages



Charge conservation

$$\phi_1 \rightarrow \phi_2$$

$$C_{dc} \cdot (0 - V_{DD}) + C_s \cdot (V_{DD} - \frac{V_{DD}}{2} - \tilde{V}_{in}) = 0$$

$$DC : C_{dc} = \frac{C_s}{2}$$

A. Baschirotto and R. Castello, "A 1-V, 1.8MHz CMOS Switched-Opamp SC Filter Rail-to-Rail Output Swing," IEEE J. Solid-State Circuits, vol.32, pp. 1979-1986, Dec. 1997

Fully Differential Switched Opamp with Dual Output

Input Stage

- Input DC level is V_{SS}
 - P-channel device
 - Less flicker noise
 - Large overdrive voltage
 - Body effect

Folded Cascode

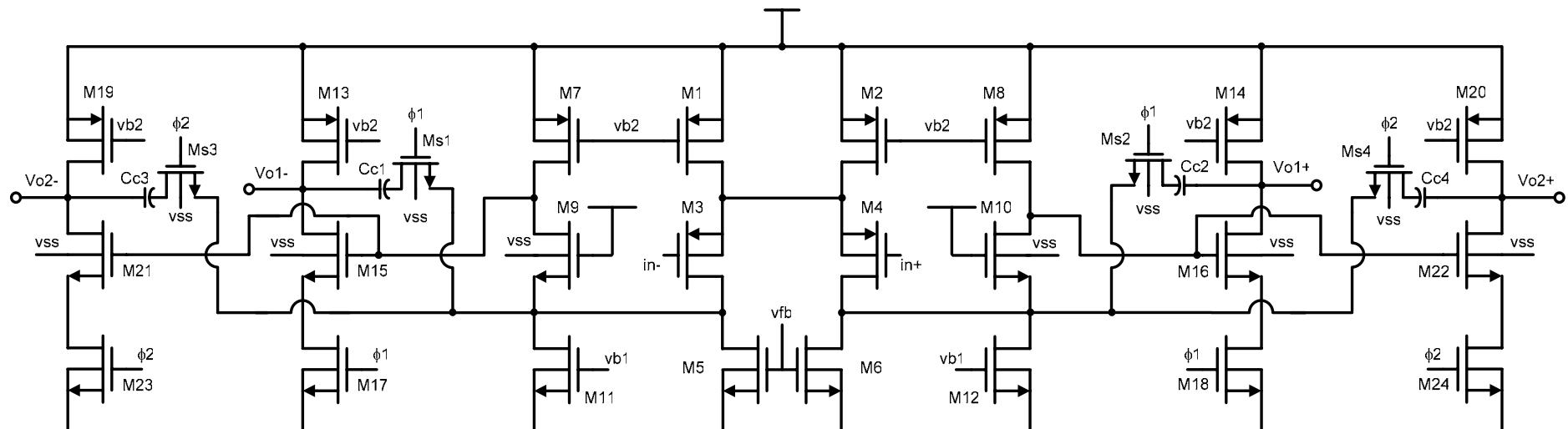
- DC level shift
- CMFB

Double Output Stages

- Switches
 - M17, M18, M23, and M24

Compensate Capacitor

- In off state, switches break off the path to prevent from discharging



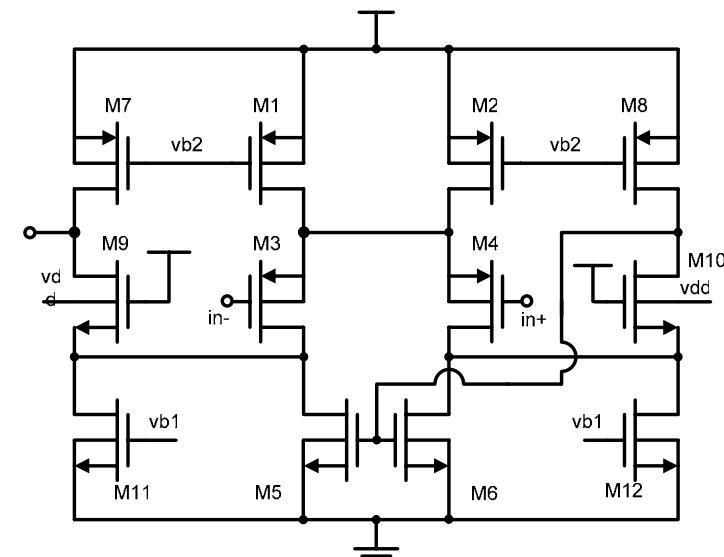
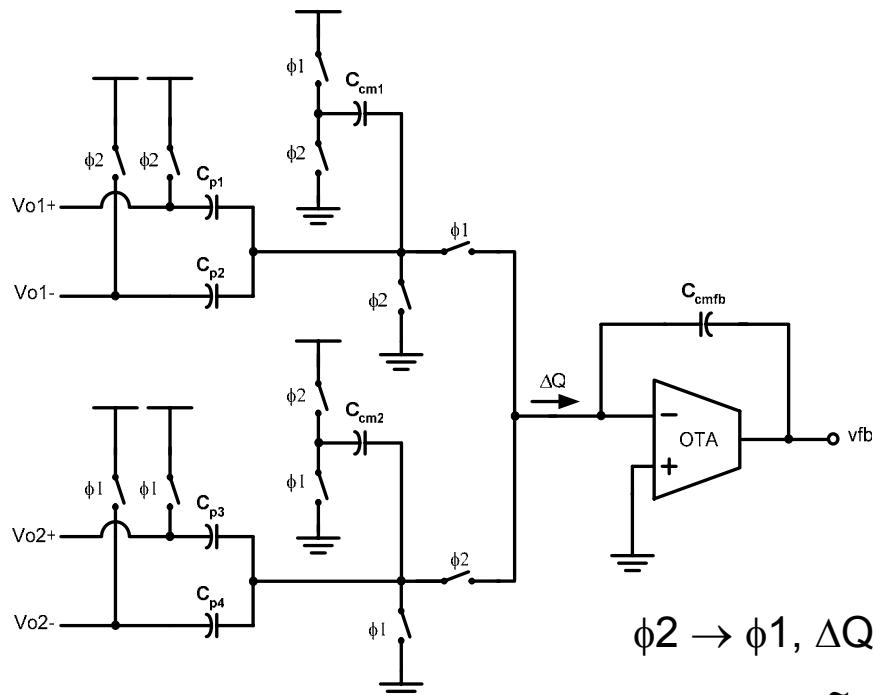
S. L. Cheng, "1V Switched Capacitor Pseudo-2-Path Filter," Hong Kong University, 1999.

Common Mode Feedback (CMFB)

- Dynamic Common Mode Feedback Circuit

 - Keep the common mode of the output signals in the middle of the available output swing

- $C_{cm1} = C_{p1} = C_{p2}$



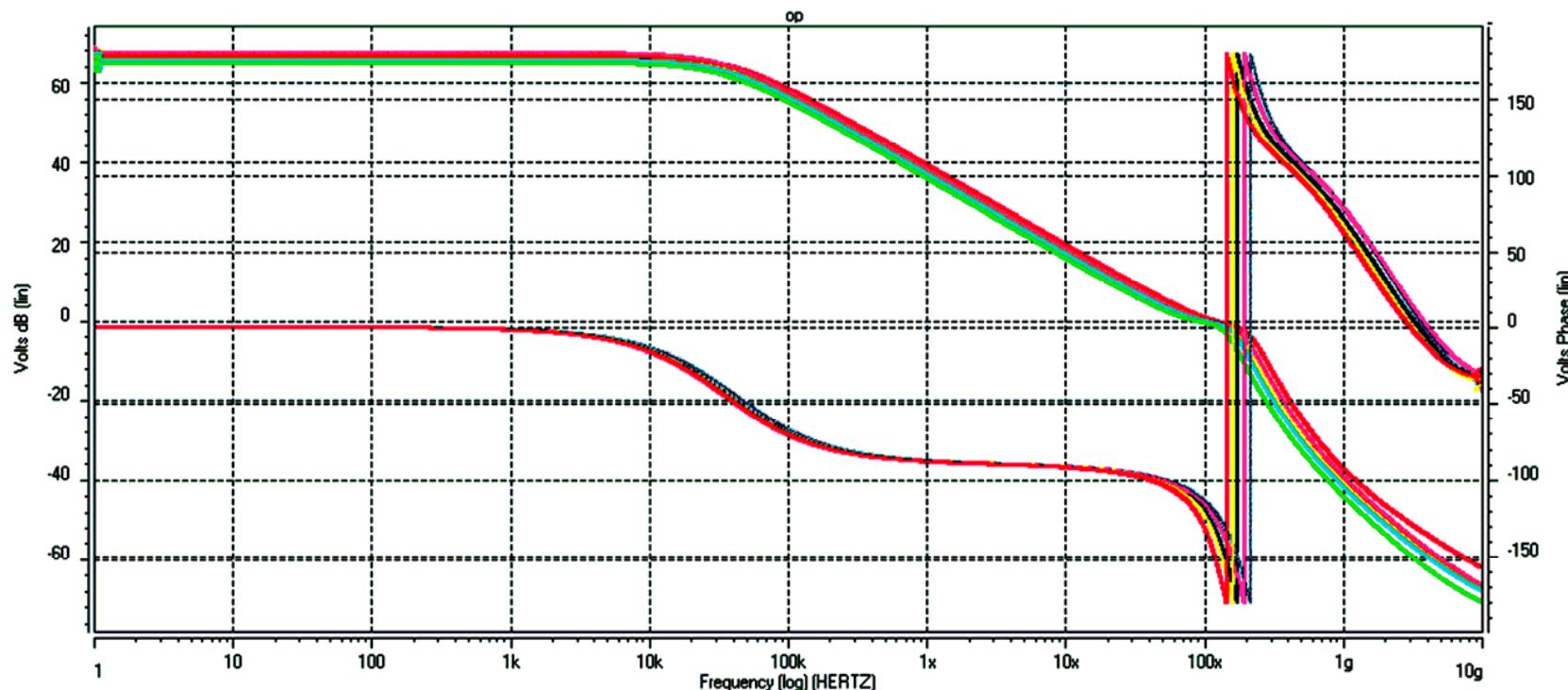
$$C_{p1} \cdot [V_{DC} + \tilde{V}_{o1+} - V_{DD}] + C_{p2} \cdot [V_{DC} + \tilde{V}_{o1-} - V_{DD}] + C_{cm1} \cdot [V_{DD} - 0] = 0$$

$$\Rightarrow V_{DC} = V_{DD}/2$$

M. Waltari and K. Halonen, "Fully Differential Switched Opamp with Enhanced Common Mode Feedback," Electron Letters, vol. 34, no. 23, 12th, pp. 8-10, Jan. 1998

Simulation Results

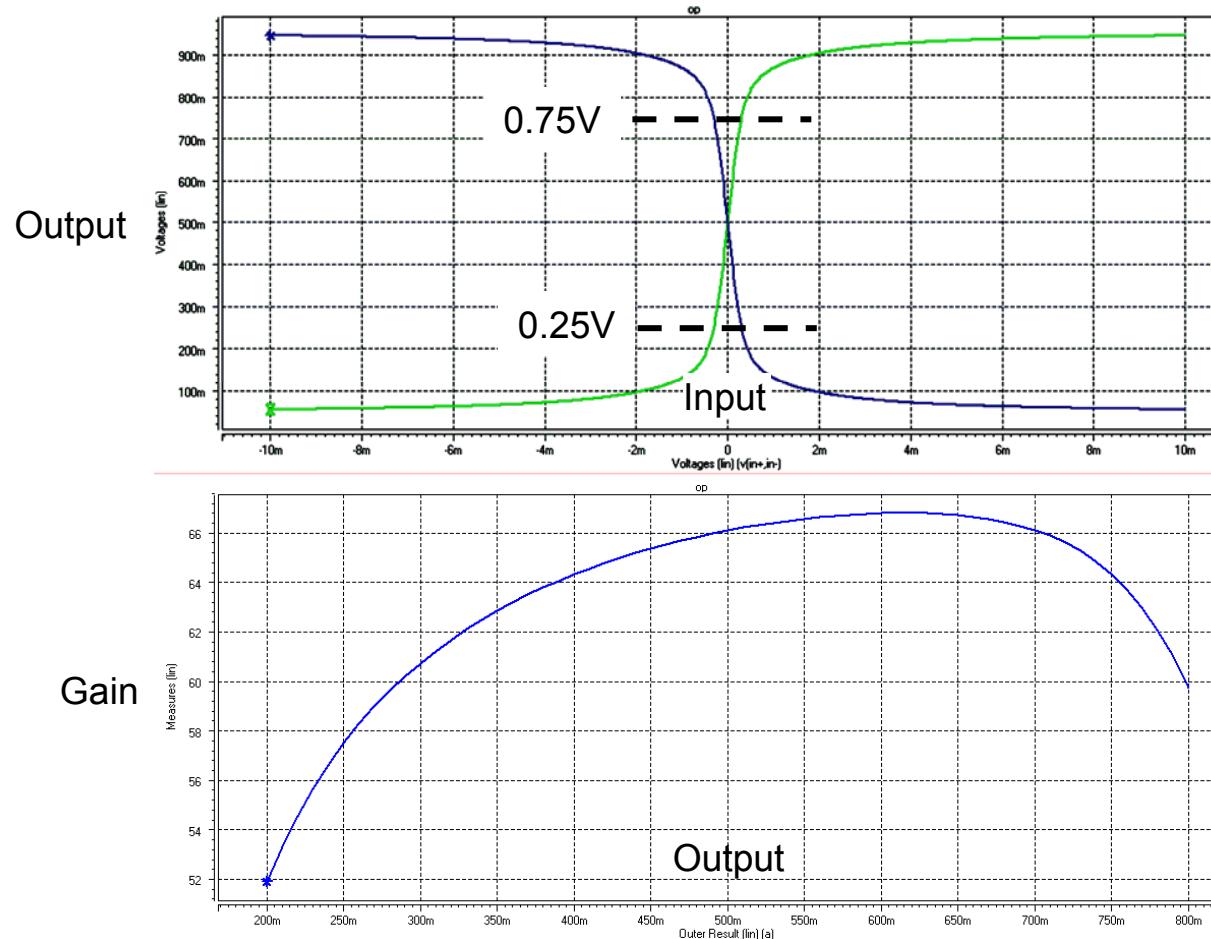
- AC Response (TT, four corners)
 - DC gain = 70 dB
 - Unity Gain Frequency = 100 MHz
 - Phase Margin = 68°



Simulation Results

Output versus Differential Input Transfer Curve

- Reasonable gains of opamp from the output range 0.2V to 0.8V
- $\Rightarrow V_{ref+}=0.75V, V_{ref-}=0.25V$



Low Voltage Quantizer

Comparator

Preamplifier Stage

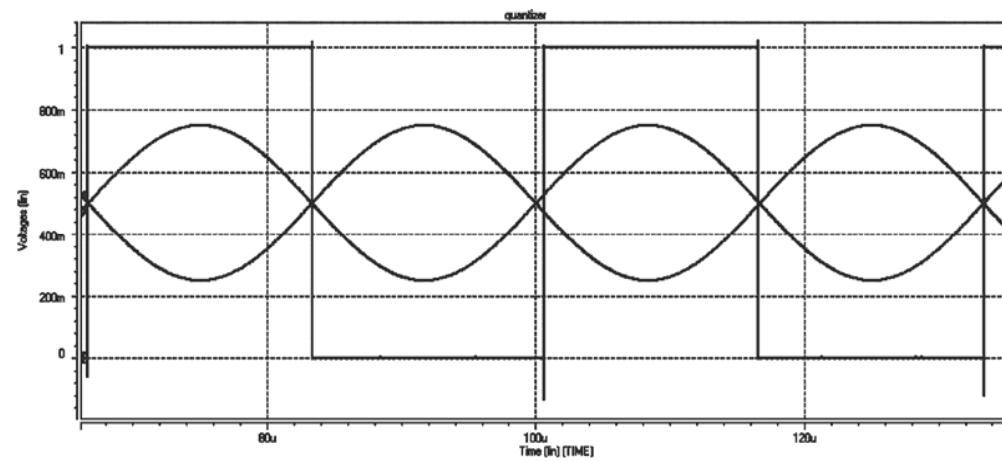
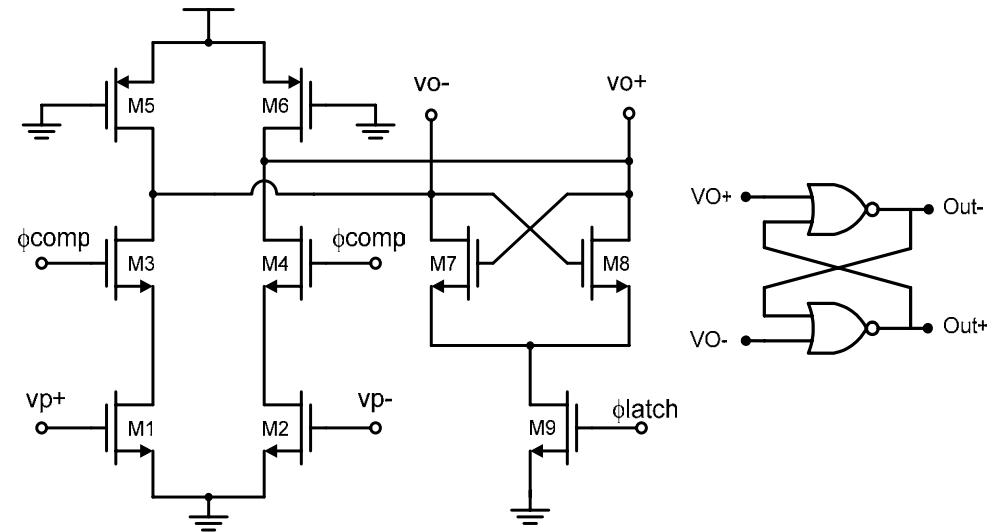
→ Input common mode is set to V_{DD}

Regeneration Stage

→ At the end of ϕ_{comp} , ϕ_{latch} active

→ Introduce Half Delay

RS Latch for Debouncing



V. Peluso, P. Vancorenland, A. Marques, M. Steyaert, and W. Sansen, "A 900mV 40 μ W Switched Opamp Modulator with 77 dB Dynamic Range," ISSCC Digest of Technical Papers, pp. 68 -69, Feb. 1998

Low Voltage Quantizer

- In Phase $\phi 1$
 - Discharged

- In Phase $\phi 2$
 - Compare

- Compensated Capacitors, C_p and C_s
 - Attenuate these voltages of comparator

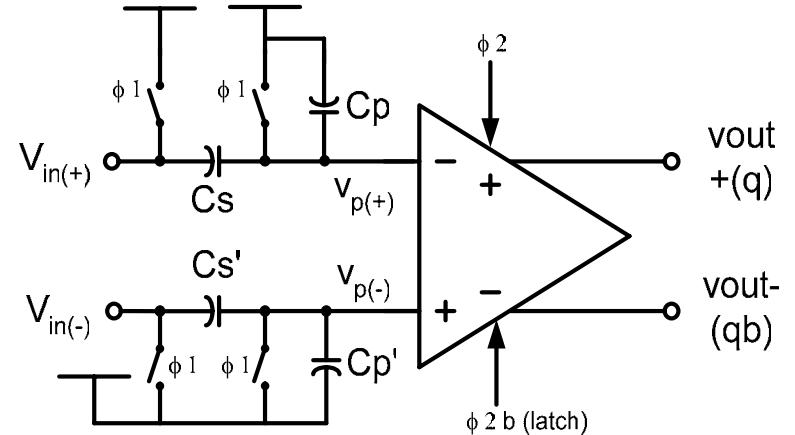
$\phi 1 \rightarrow \phi 2$

$$C_s \cdot [(\tilde{v}_{in(+)} + \frac{V_{DD}}{2}) - (\tilde{v}_{p(+)} + V_{DD}) - 0] - C_p \cdot [(\tilde{v}_{p(+)} + V_{DD} - V_{DD}) - 0] = 0$$

$$\Rightarrow \tilde{v}_{p(+)} = \frac{C_s}{C_p + C_s} \cdot (\tilde{v}_{in(+)} - \frac{V_{DD}}{2})$$

$$V_{p(+)} = \tilde{v}_{p(+)} + V_{DD}$$

$$\Rightarrow V_{p(+)} = \frac{C_s}{C_s + C_p} \cdot \tilde{v}_{in(+)} + \left(1 - \frac{C_s/2}{C_p + C_s}\right) \cdot V_{DD}$$



for example, $C_s=2\text{pF}$ and $C_p=0.5\text{pF}$

$$V_{p(+)} = 0.8 \cdot \tilde{v}_{in(+)} + 0.6 \cdot V_{DD}$$

V. Peluso, P. Vancorenland, A. Marques, M. Steyaert, and W. Sansen, "A 900mV 40 μ W Switched Opamp Modulator with 77 dB Dynamic Range," ISSCC Digest of Technical Papers, pp. 68 -69, Feb. 1998



Outline

1. Introduction

2. Low Voltage Circuits for Delta Sigma Modulator

3. Low Voltage Nested-Chopper Delta Sigma Modulator

- Offset Cancellation Technique
- Nested-Chopper Amplifier
- Chopper-Stabilized $\Delta\Sigma$ Modulator
- Nested-Chopper $\Delta\Sigma$ Modulator

- ▶ System Consideration
- ▶ Implementation
- ▶ Noise Analysis
- ▶ Nonlinear Gain of Opamp
- ▶ Simulation and Experimental Results

4. Low Voltage Second-Order Delta Sigma Modulator Using a Single Opamp

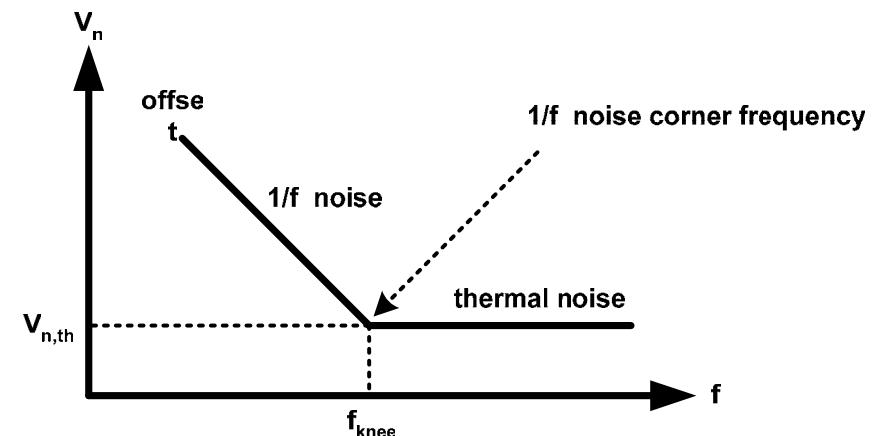
5. Low Voltage Fourth-Order Bandpass Delta Sigma Modulator



Offset Cancellation Technique

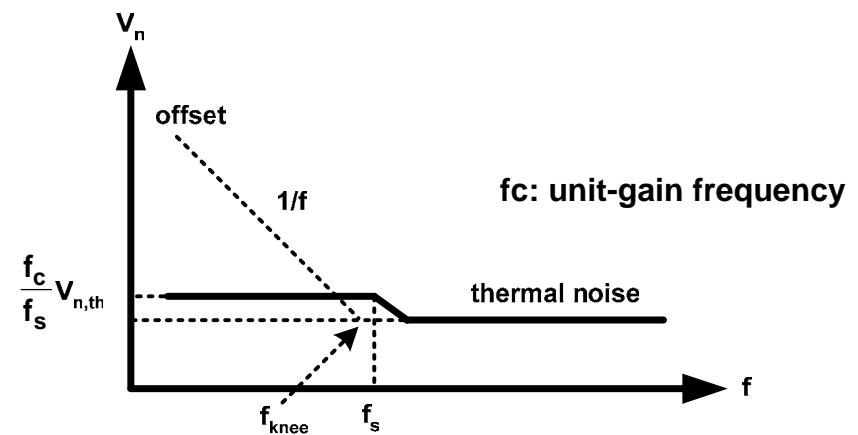
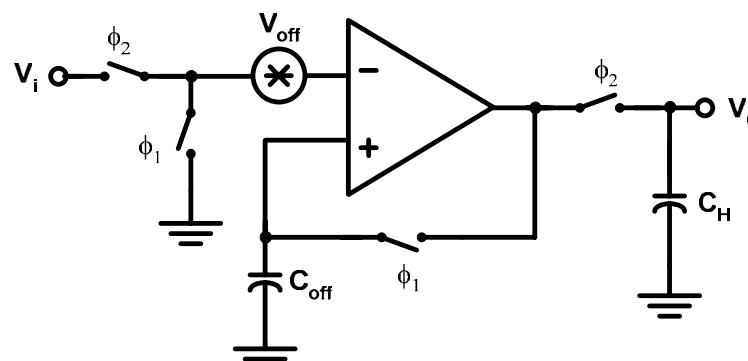
Major Enemies of Analog Front End

- Thermal noise
- Flicker noise ($1/f$ noise)
- DC offset



Dynamic Offset Cancellation Techniques

- Autozeroing and Correlated Double Sampling (CDS)



C. C. Enz, and G. C. Temes, "Circuit techniques for reducing the effect of op-amp imperfections: autozeroing, correlated double sampling, and chopper stabilization," IEEE J. Solid-State Circuits, vol. 84, no. 11, pp. 1584-1614, Nov. 1996

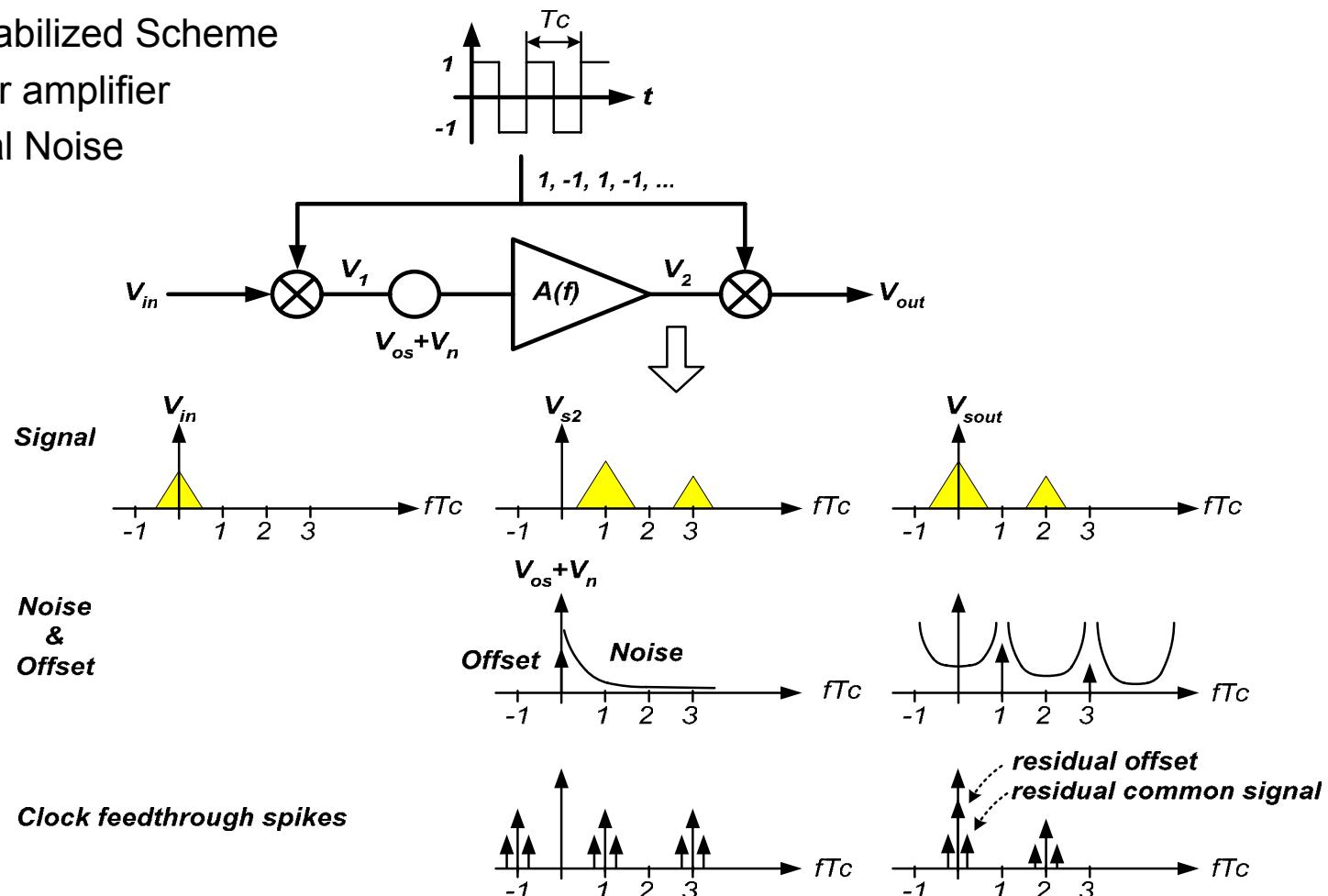
Offset Cancellation Technique

- Dynamic Offset Cancellation Techniques

- Chopper-Stabilized Scheme

- Chopper amplifier

- Residual Noise



C. Menbofi and Q. Huang, "A Fully Integrated, Untrimmed CMOS Instrumentation Amplifier with Submicrovolt Offset," IEEE J. Solid-State Circuits, vol.34, no.3, Mar. 1999

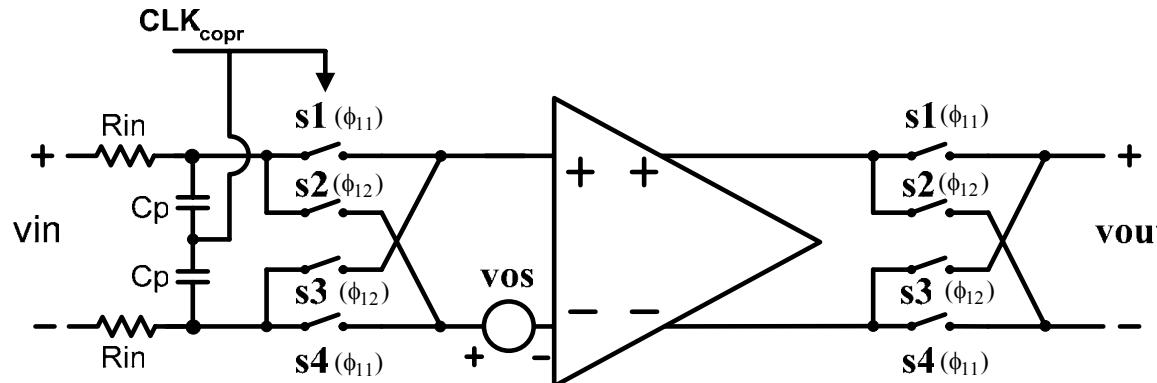
Nested-Chopper Amplifier

● Residual Noise

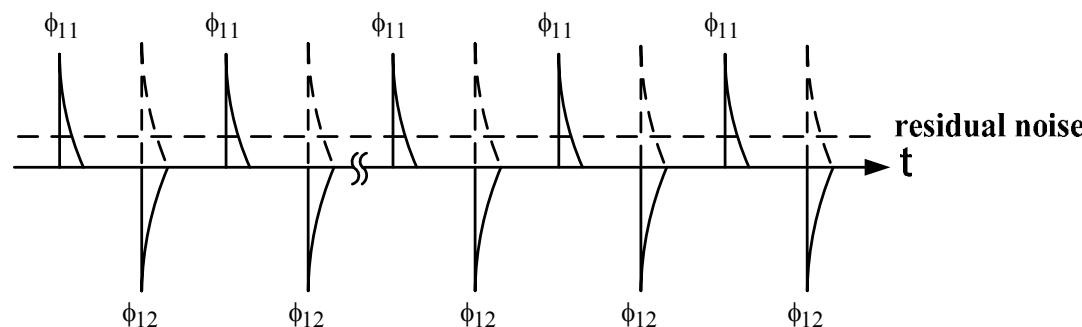
■ Mismatch of the switch paths

- ▶ Clock feedthrough

- ▶ The parasitic capacitors and turn-on resistances of the signal lines



● In Time Domain

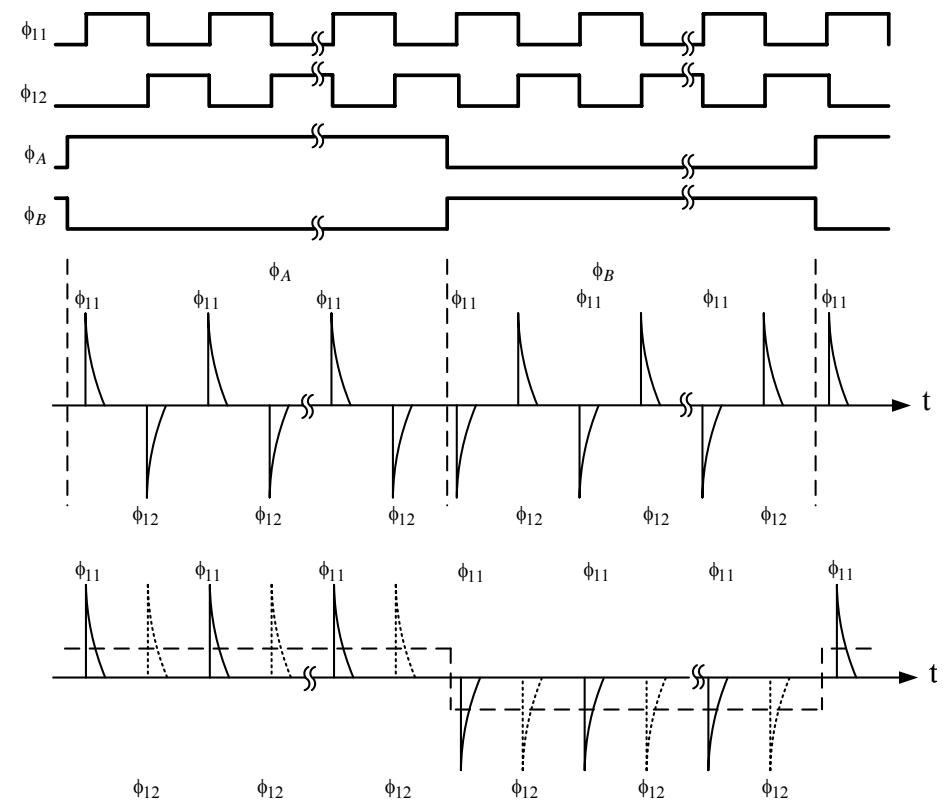
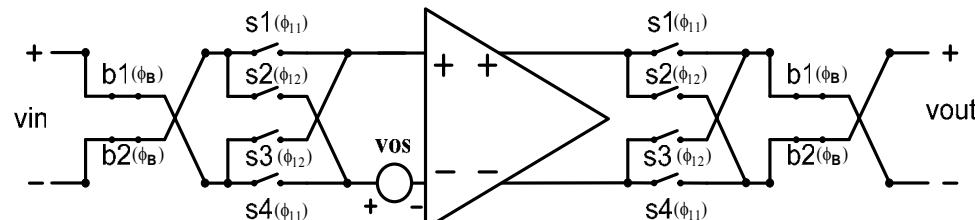
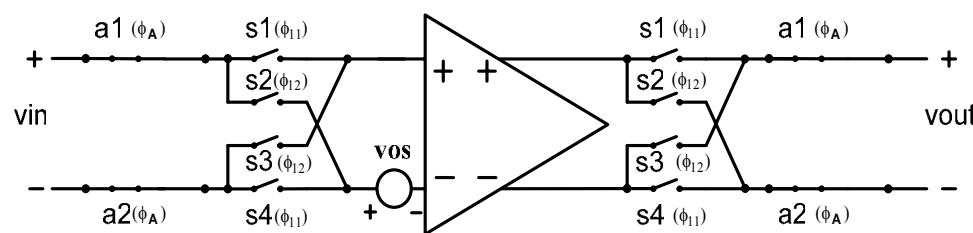
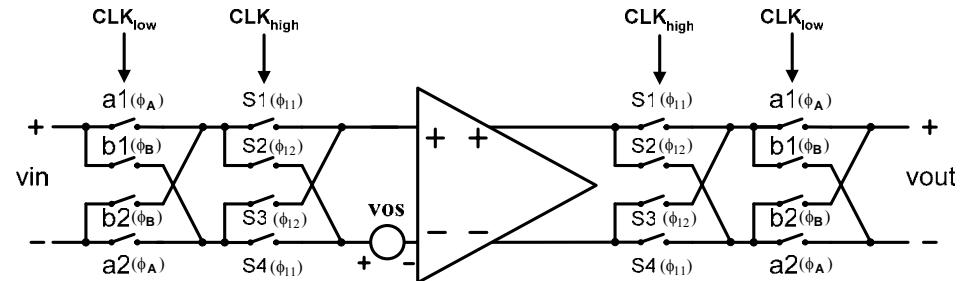


A. Bakker, K. Thiele, and J. H. Huijsing, "A CMOS Nested-Chopper Instrumentation Amplifier with 100-nV Offset," IEEE J. Solid-State Circuits, vol. 35, no. 12, pp. 1877-1883, Dec. 2000

Nested-Chopper Amplifier

● Nested-Chopper Amplifier

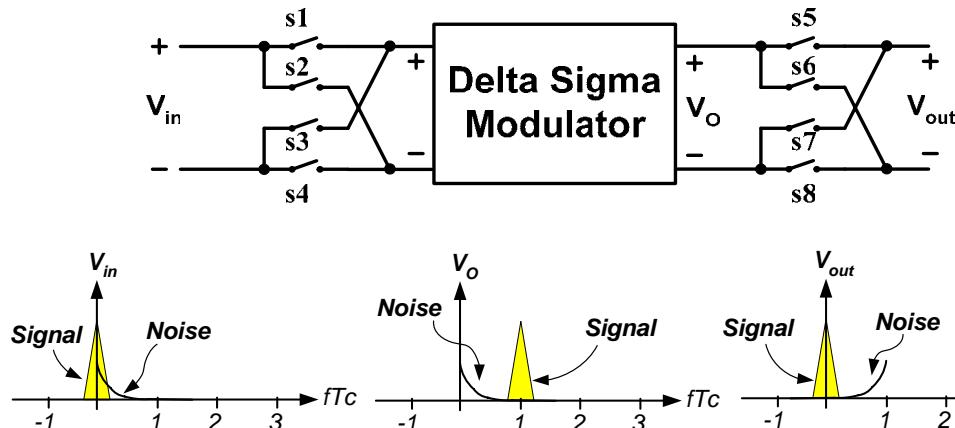
- The operated frequency of the outer chopper is lower than that of the inner one



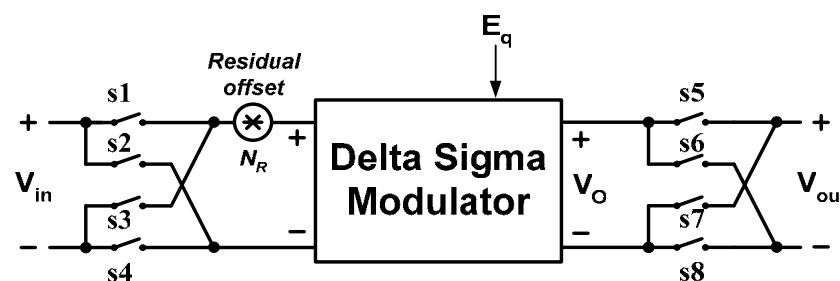
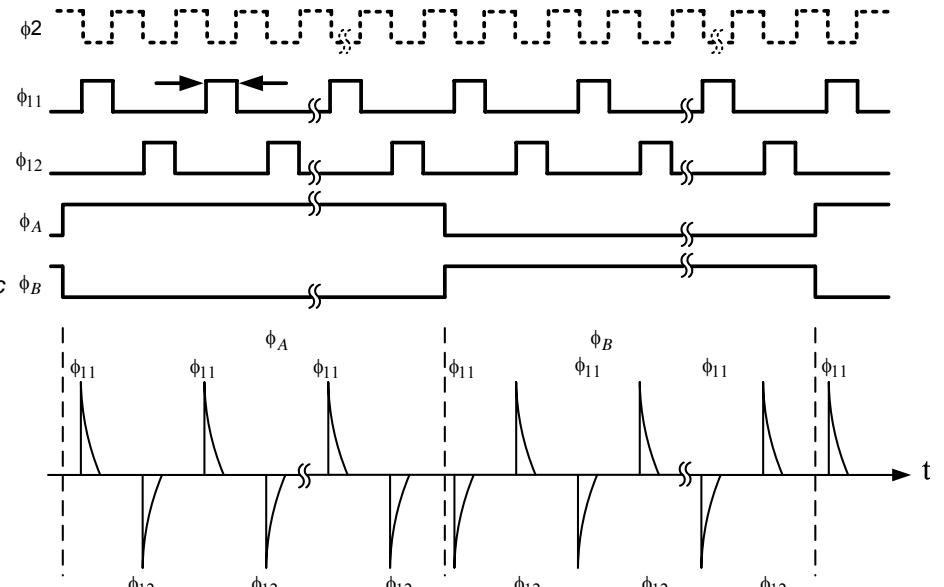
A. Bakker, K. Thiele, and J. H. Huijsing, "A CMOS Nested-Chopper Instrumentation Amplifier with 100-nV Offset," IEEE J. Solid-State Circuits, vol. 35, no. 12, pp. 1877-1883, Dec. 2000

Chopper-Stabilized $\Delta\Sigma$ Modulator

- Low-Frequency Noise is Modulated to High-Frequency Band
 - Chopper frequency = half the sampling frequency



Sample phase, Integration phase



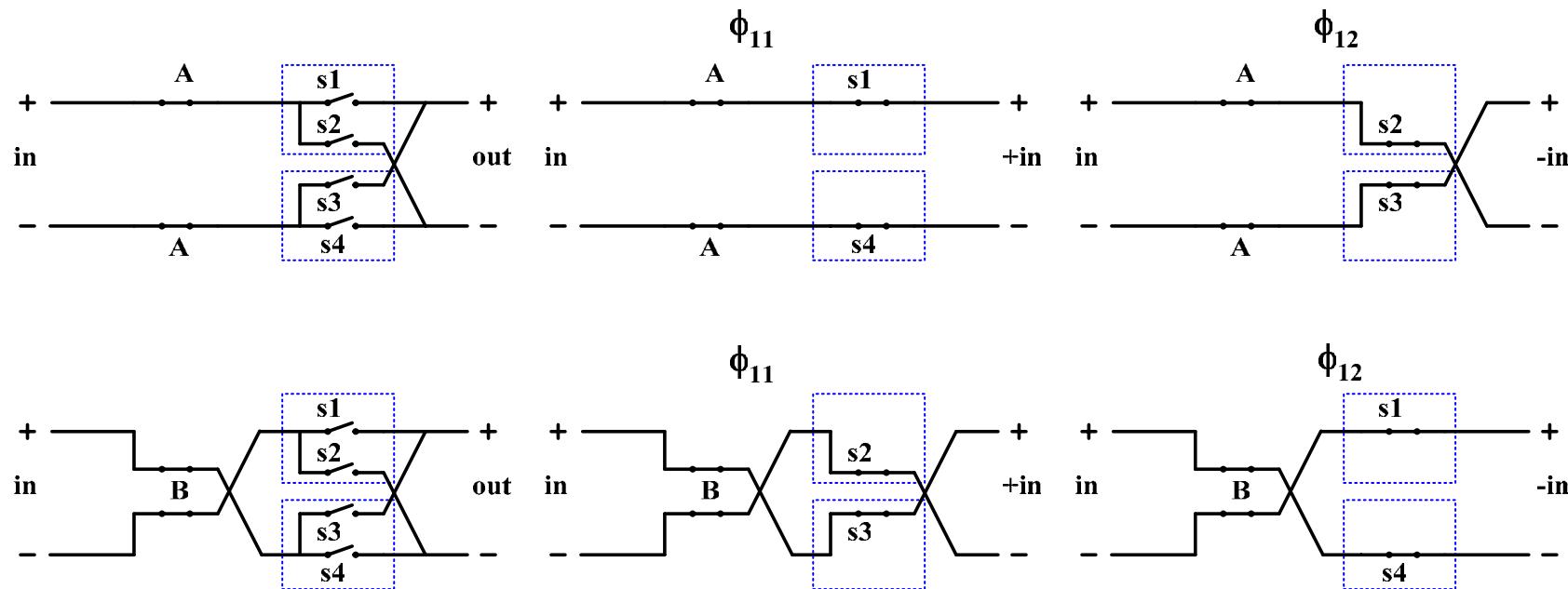
$$V_{out} = V_{in} \cdot STF(z) + E_q \cdot NTF(z) + N_R$$

Y. H. Chang, C. Y. Wu, and T. C. Yu, "Chopper-stabilized sigma-delta modulator," in Proc. IEEE ISCAS, pp. 1286-1289, May. 1993

Nested-Chopper $\Delta\Sigma$ Modulator

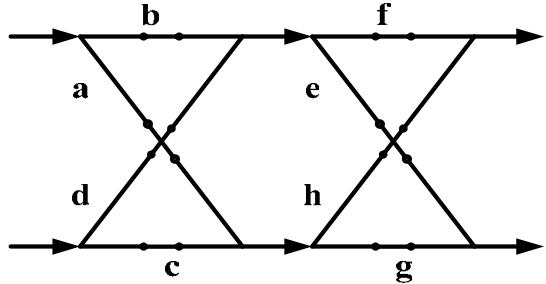
- Nested-Chopper in the Front End

- Phase ϕA is on, as chopper-stabilized modulator does
- Phase ϕB is on, nested-chopper must be still look like one chopper does
 - ▶ Switches s_1 and $s_4 \Leftrightarrow s_2$ and s_3
 - ▶ Boolean function
 - ▶ $s_1, s_4 : \phi A \cdot \phi_{11} + \phi B \cdot \phi_{12}$
 - ▶ $s_2, s_3 : \phi A \cdot \phi_{12} + \phi B \cdot \phi_{11}$



Nested-Chopper $\Delta\Sigma$ Modulator

The Resistance of the Signal Paths

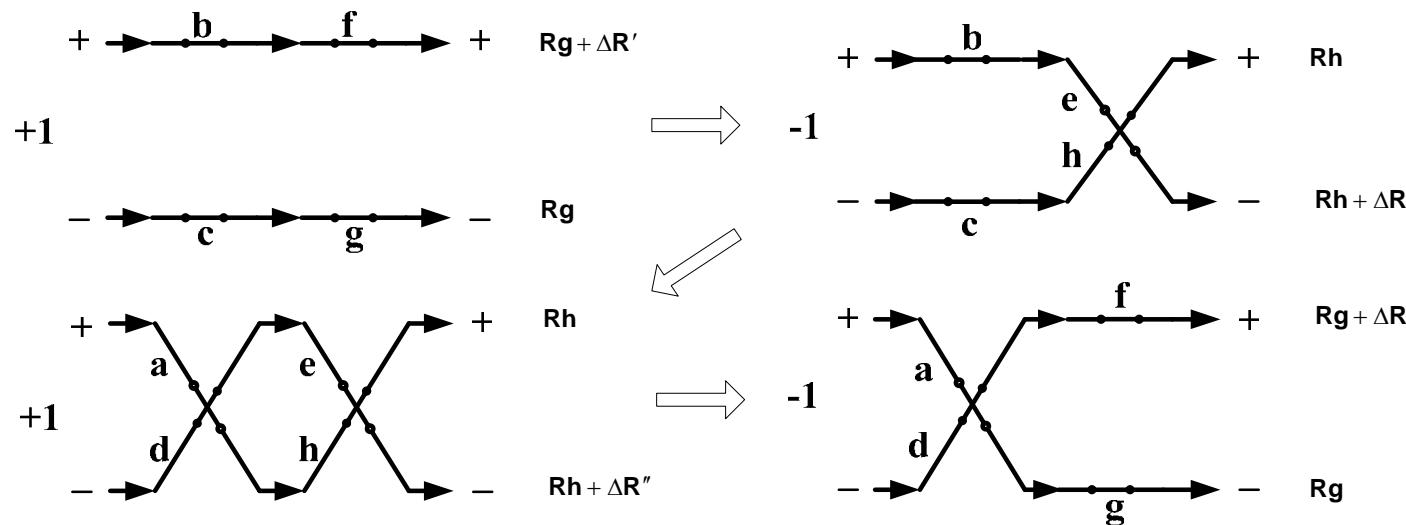


$$R_e = R_h + \Delta R''$$

$$R_f = R_g + \Delta R'$$

the sum of the resistances

$$R_{\text{sum}} = 2R_g + 2R_h + \Delta R' + \Delta R''$$



the sum of the resistances in each output path will be the same

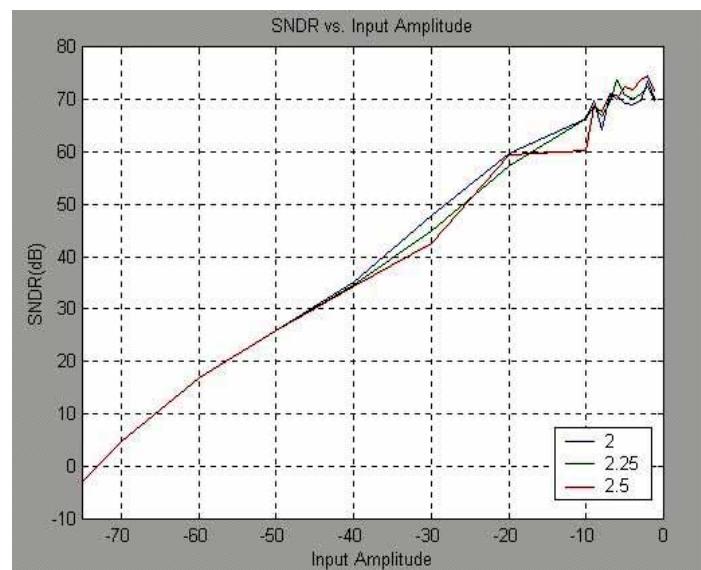
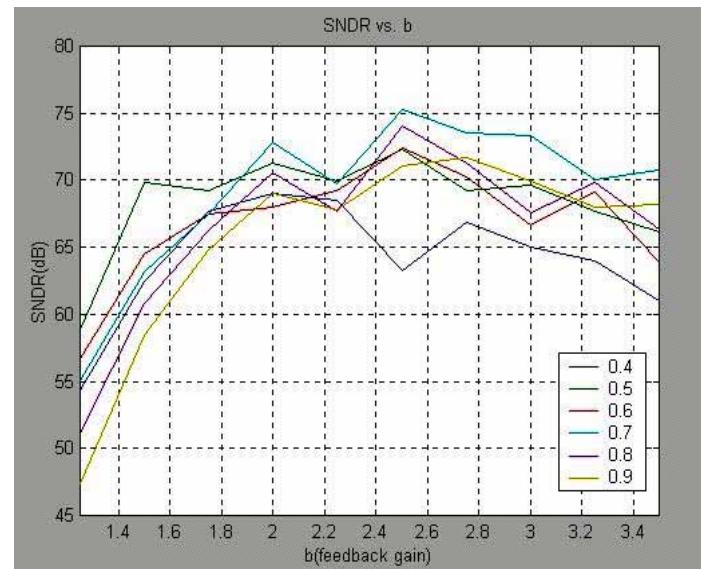
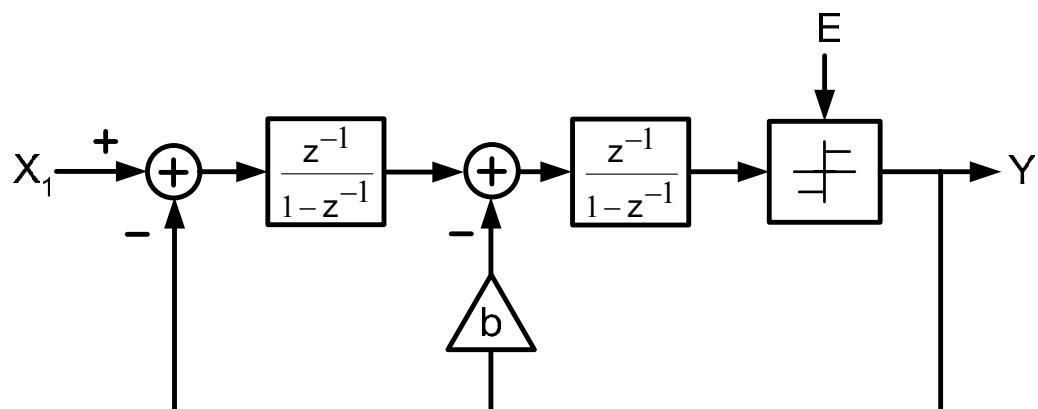
System Consideration

- A Second-Order Lowpass $\Delta\Sigma$ Modulator

- $V_{in} = -6 \text{ dB}$, $f_{in} = 10 \text{ KHz}$
- Sampling frequency $f_s = 2.56 \text{ MHz}$
- Signal BW = 22.05KHz

- Consideration

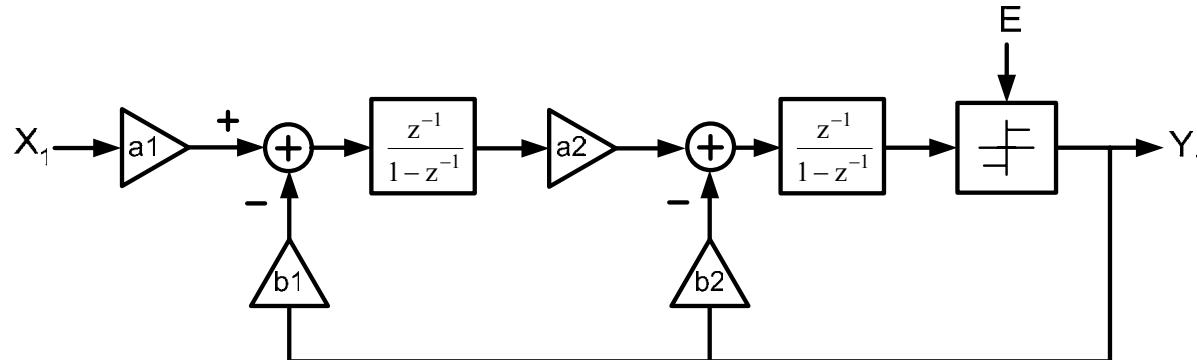
- Overload level
- Noise floor
- Signal dependence
- \Rightarrow Take $b=2.25$



System Consideration

- Coefficients Scaling

- The outputs of the first and the second integrators are ± 2.67 and ± 4 , respectively

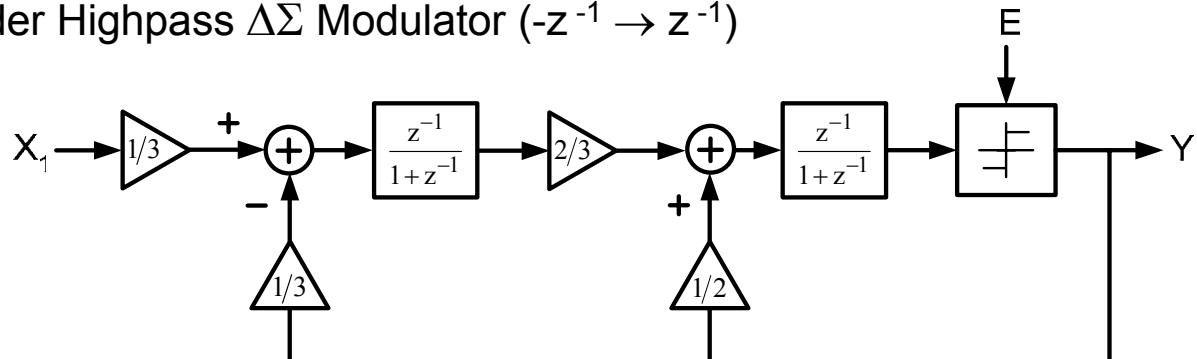


$$a_1 = b_1 < \sigma/2.67 = 0.3745 \quad (\sigma = 1)$$

$$b_2/b < \sigma/4 = 0.25 \quad \text{for } b = 2.25 \quad \Rightarrow \text{take } b_2 = 0.5$$

$$b_2/(b_1 \cdot a_2) = b \quad \Rightarrow \text{take } b_1 = 1/3, a_2 = 2/3$$

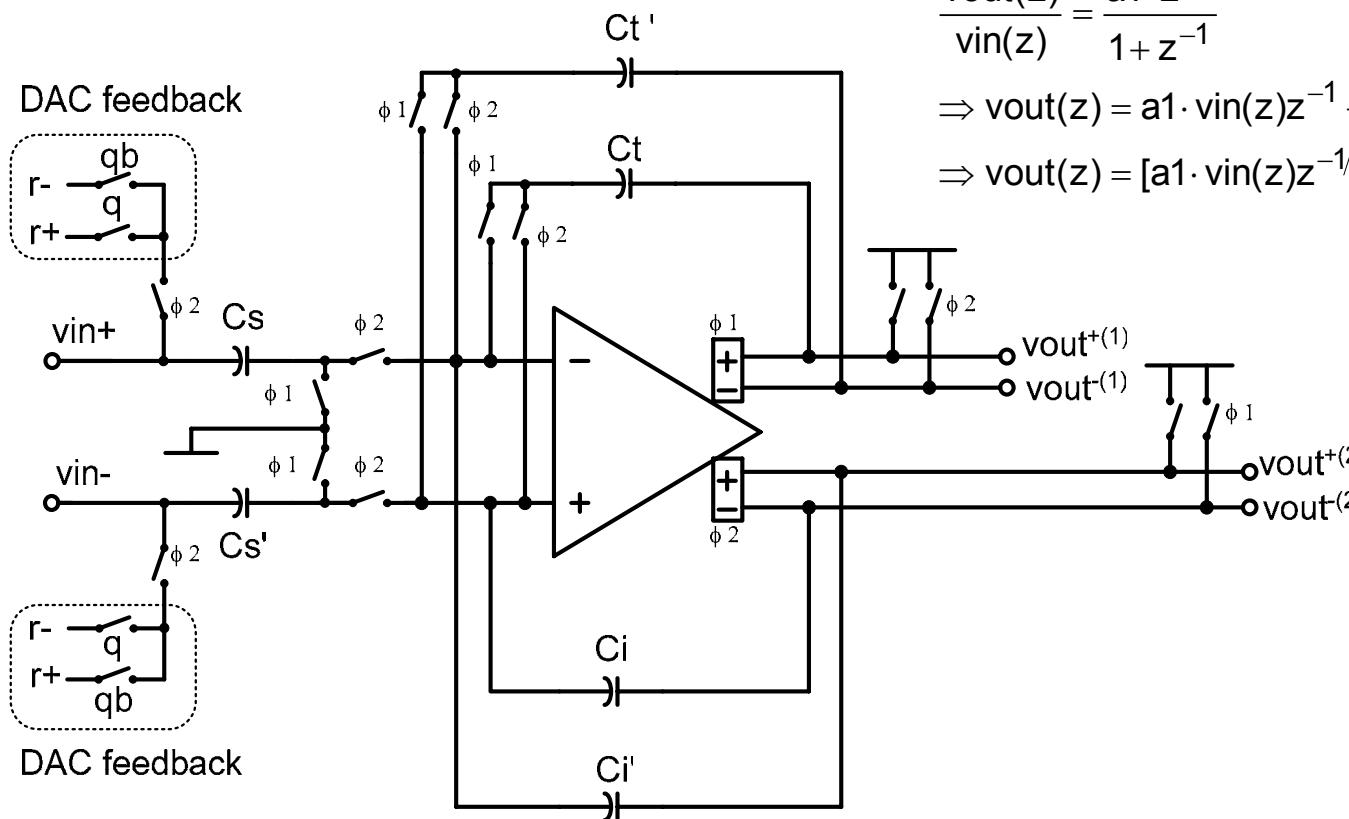
- A Second-Order Highpass $\Delta\Sigma$ Modulator ($-z^{-1} \rightarrow z^{-1}$)



Implementation

- The First Stage

- In phase ϕ_1 , input is sampled and the output is transferred to $v_{out}^{(1)}$
- In phase ϕ_2 , input and the output $v_{out}^{\pm(1)}$ are integrated to $v_{out}^{\mp(2)}$
 - $C_t = C_t' = C_i = C_i'$
 - $C_s'/C_i = C_s/C_i' = 1/3 = a_1$



$$\frac{v_{out}(z)}{vin(z)} = \frac{a_1 \cdot z^{-1}}{1 + z^{-1}}$$

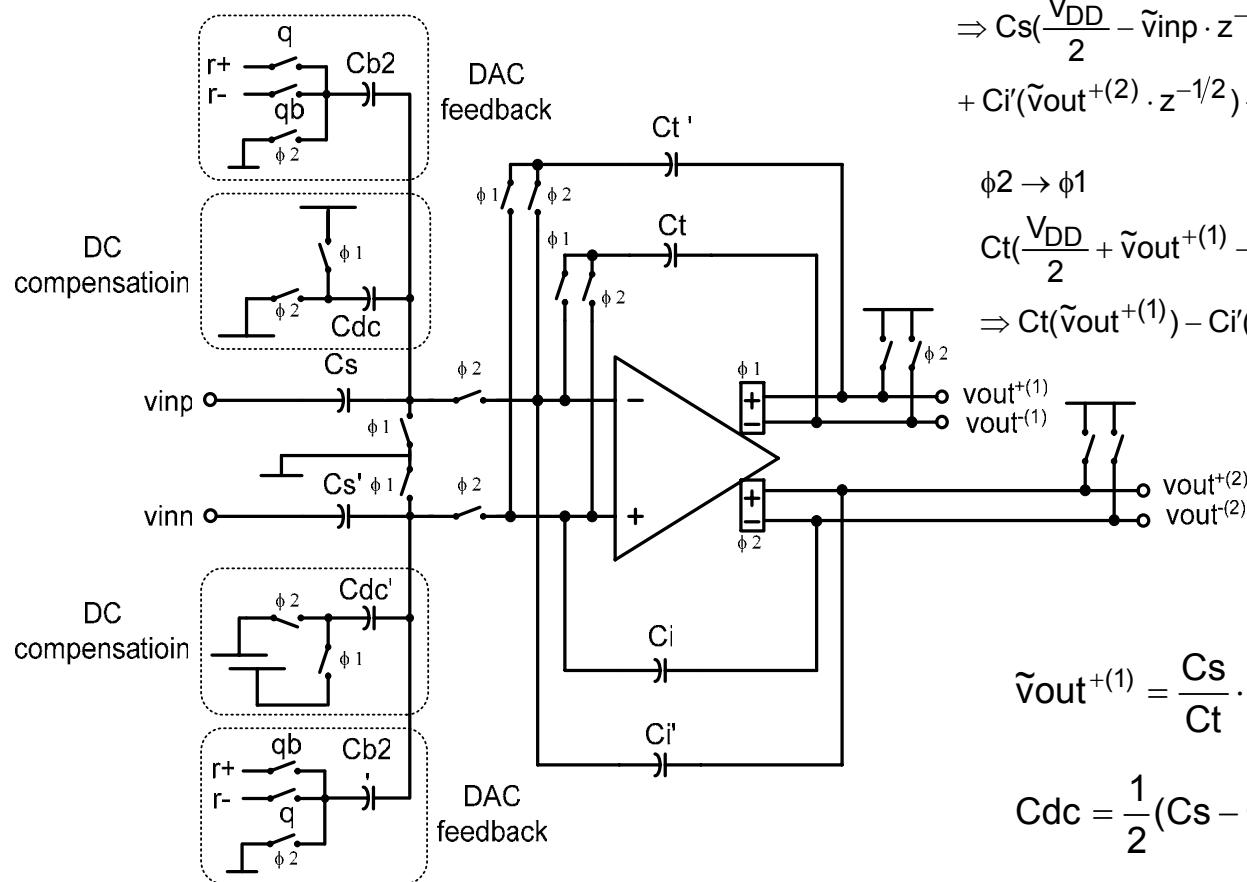
$$\Rightarrow v_{out}(z) = a_1 \cdot vin(z)z^{-1} - v_{out}(z)z^{-1}$$

$$\Rightarrow v_{out}(z) = [a_1 \cdot vin(z)z^{-1/2} - v_{out}(z)z^{-1/2}] \cdot z^{-1/2}$$

Implementation

- The Second Stage

- DAC feedback
- DC compensation circuits



$\phi_1 \rightarrow \phi_2$

$$\begin{aligned} & C_s(V_{DD} - \frac{V_{DD}}{2} - \tilde{v}_{inp} \cdot z^{-1}) + C_{b2}(-\frac{V_{DD}}{2} - \tilde{r} \cdot z^{-1}) + C_{dc}(-V_{DD}) \\ & + C_{i'}(\frac{V_{DD}}{2} + \tilde{v}_{out}^{(2)} \cdot z^{-1/2} - V_{DD}) + C_t'(V_{DD} - \frac{V_{DD}}{2} - \tilde{v}_{out}^{(1)} \cdot z^{-1}) = 0 \\ & \Rightarrow C_s(\frac{V_{DD}}{2} - \tilde{v}_{inp} \cdot z^{-1}) + C_{b2}(-\frac{V_{DD}}{2} - \tilde{r} \cdot z^{-1}) + C_{dc}(-V_{DD}) \\ & + C_{i'}(\tilde{v}_{out}^{(2)} \cdot z^{-1/2}) - C_t'(\tilde{v}_{out}^{(1)} \cdot z^{-1}) = 0 \end{aligned}$$

$\phi_2 \rightarrow \phi_1$

$$\begin{aligned} & C_t(\frac{V_{DD}}{2} + \tilde{v}_{out}^{(1)} - V_{DD}) + C_{i'}(V_{DD} - \frac{V_{DD}}{2} - \tilde{v}_{out}^{(2)} \cdot z^{-1/2}) = 0 \\ & \Rightarrow C_t(\tilde{v}_{out}^{(1)}) - C_{i'}(\tilde{v}_{out}^{(2)} \cdot z^{-1/2}) = 0 \end{aligned}$$

$$\tilde{v}_{out}^{(1)} = \frac{C_s}{C_t} \cdot \tilde{v}_{inp} \cdot \frac{z^{-1}}{1+z^{-1}} - \frac{C_{b2}}{C_t} (-\tilde{r}) \frac{z^{-1}}{1+z^{-1}}$$

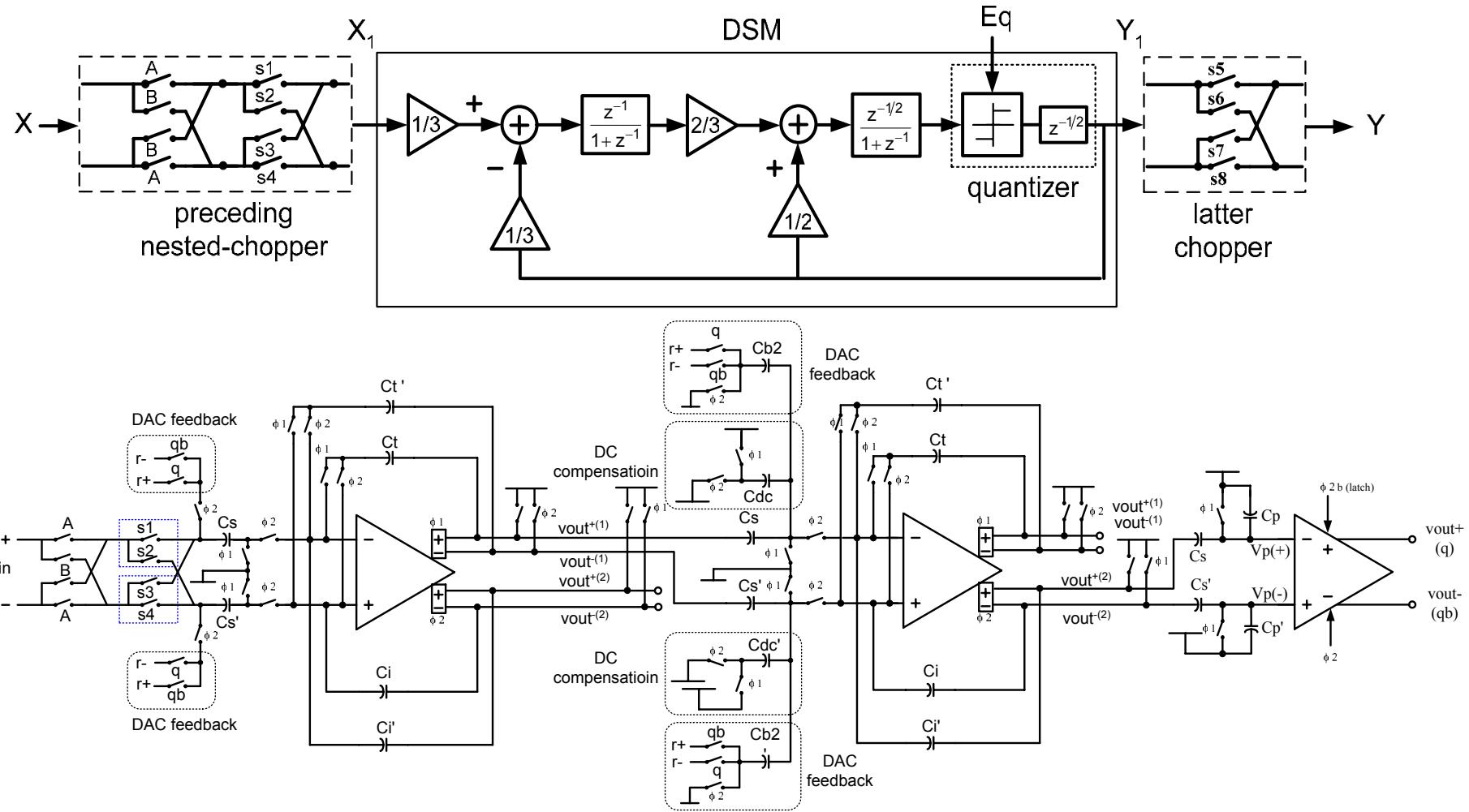
$$C_{dc} = \frac{1}{2}(C_s - C_{b2})$$



Implementation

Linear Model of the Whole Modulator

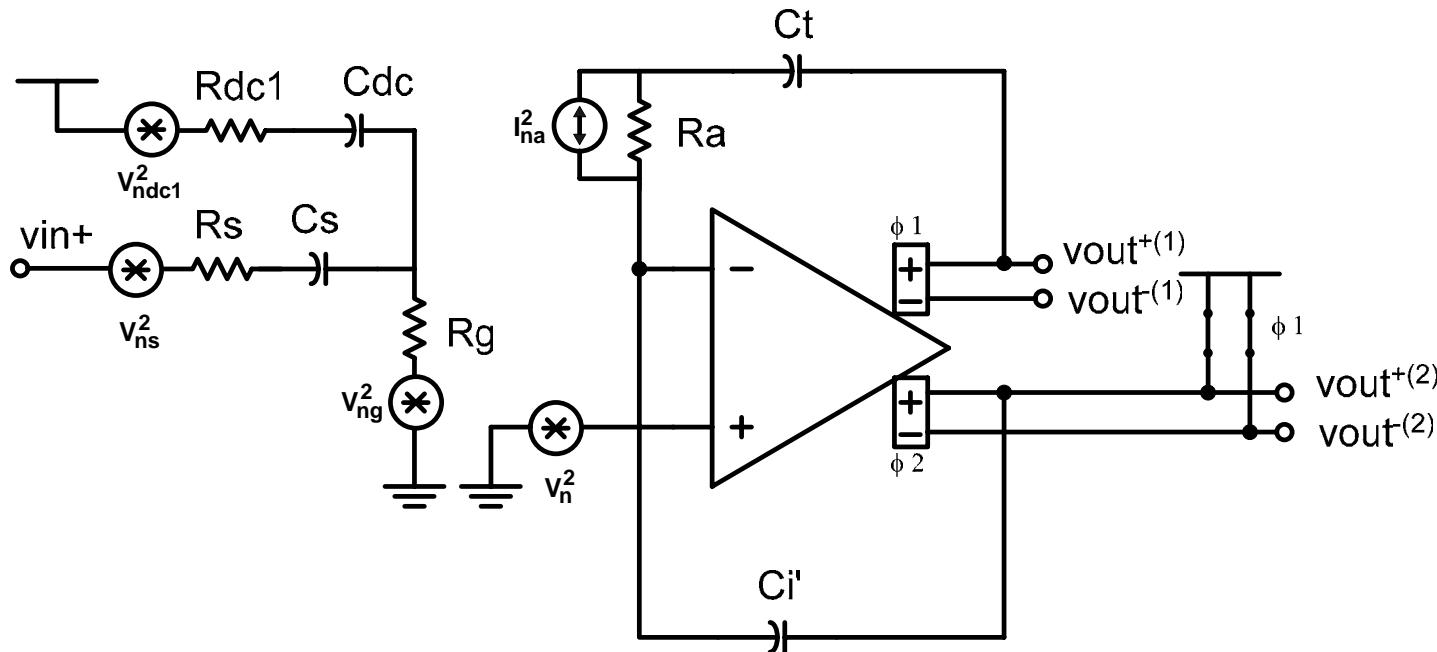
- Comparator introduces half delay, the output of the second stage is sampled at ϕ_2



Noise Analysis

- The First Stage

- In sampling phase $\phi 1$



$$V_{ns1}^2 = (V_{ns}^2 + V_{ng}^2) \cdot \frac{\pi}{2} \cdot \frac{1}{2\pi(R_s + R_g)C_s} = \frac{kT}{C_s}$$

$$V_{noa1}^2 = I_{na}^2 \cdot \left| Ra + \frac{1}{sC_i} \right|^2 = \frac{4kT}{Ra} \cdot \left| \frac{1+sC_iRa}{sC_i} \right|^2$$

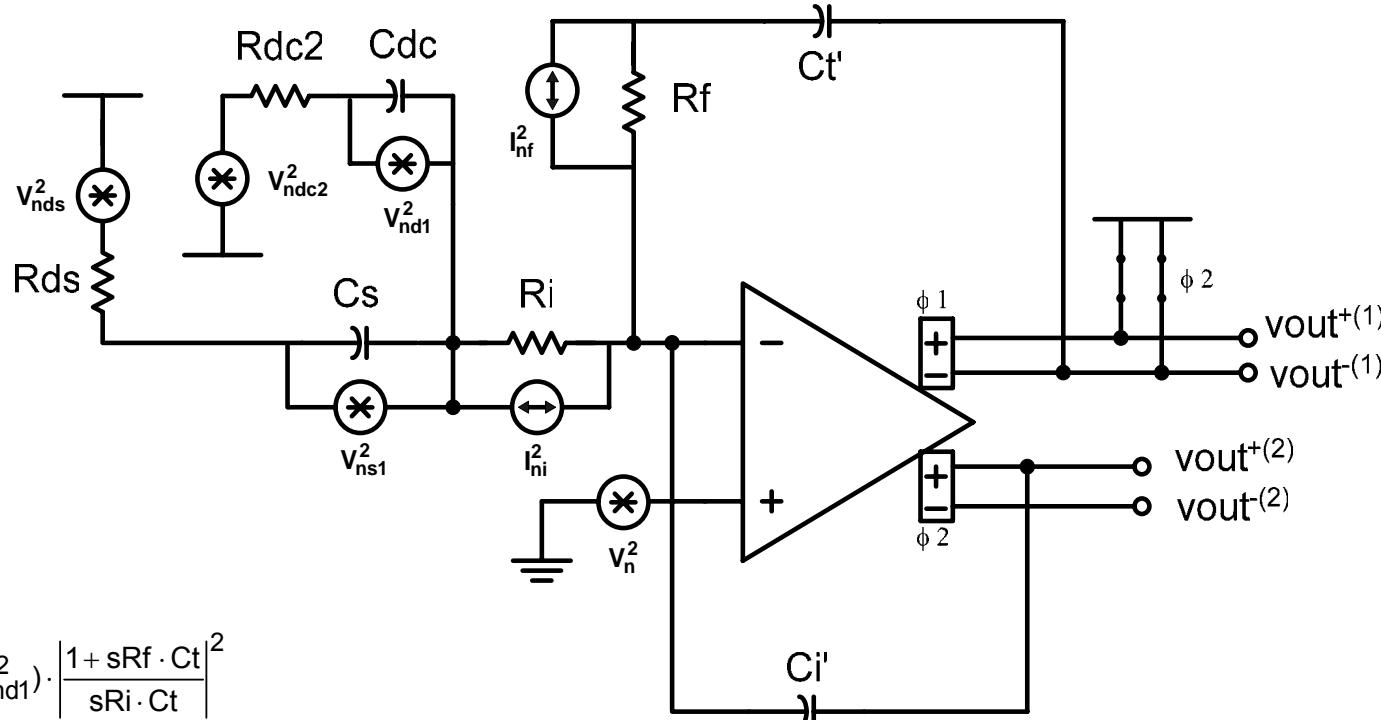
$$V_{nd1}^2 = \frac{kT}{C_{dc}}$$

$$V_{nop1}^2 = V_n^2$$

Noise Analysis

- The First Stage

- In integrating phase $\phi 2$



$$V_{noe}^2 = (V_{ns1}^2 + V_{nd1}^2) \cdot \frac{|1 + sRf \cdot Ct|^2}{sRi \cdot Ct}$$

$$V_{nos2}^2 = V_{ndc2}^2 \cdot \frac{(1 + sRdc2 \cdot Cdc) \cdot Cs}{(1 + sRds \cdot Cs) \cdot Cdc + (1 + sRdc2 \cdot Cdc) \cdot Cs} \cdot \frac{|1 + sRf \cdot Ct|^2}{sRi \cdot Ct}$$

$$V_{nod2}^2 = V_{ndc2}^2 \cdot \frac{(1 + sRds \cdot Cs) \cdot Cdc}{(1 + sRds \cdot Cs) \cdot Cdc + (1 + sRdc2 \cdot Cdc) \cdot Cs} \cdot \frac{|1 + sRf \cdot Ct|^2}{sRi \cdot Ct}$$

$$V_{nof2}^2 = (I_{nf}^2 + I_{ni}^2) \cdot \left| Rf + \frac{1}{sCt} \right|^2 = 4kT \left(\frac{1}{Rf} + \frac{1}{Ri} \right) \cdot \frac{|1 + sCt \cdot Rf|^2}{sCt}$$

$$V_{nop2}^2 = V_n^2 \cdot \left[1 + \frac{\frac{sCt}{sCt}}{\frac{(1 + sRdc2 \cdot Cdc)(1 + sRds \cdot Cs)}{(1 + sRdc2 \cdot Cdc) \cdot sCs + (1 + sRds \cdot Cs) \cdot sCdc} + Ri} \right]$$

Noise Analysis

- Equivalent Input Noises

- Dividing these noises by transfer function

In phase ϕ_1

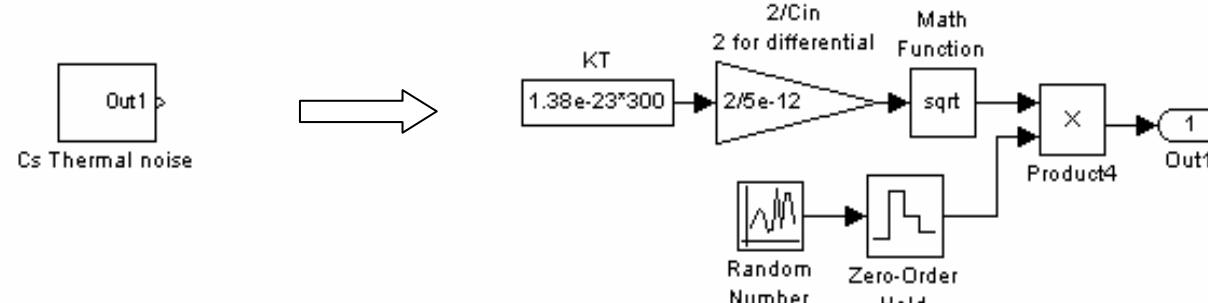
$$V_{ns1}^2 = \frac{kT}{Cs}$$

$$V_{nd1}^2 = \frac{kT}{Cdc}$$

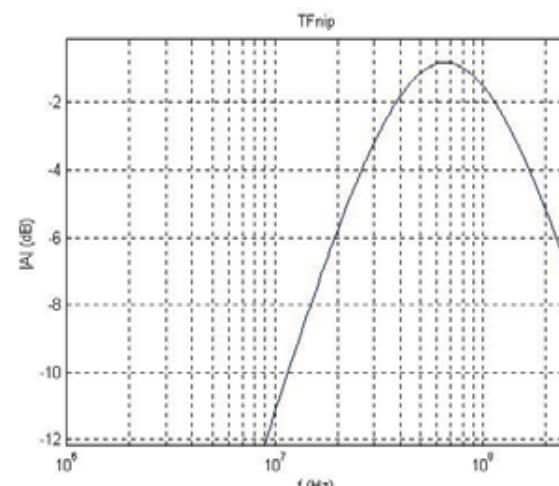
$$V_{nip1}^2 = \frac{V_{nop1}^2}{TF(s)} = V_n^2 \cdot \left| \frac{sRi \cdot Ct}{1 + sRf \cdot Ct} \right|^2$$

$$V_{nia1}^2 = 4kTRa \cdot \left| \frac{1 + sRa \cdot Ct}{1 + sRf \cdot Ct} \cdot \frac{Ri}{Ra} \right|^2$$

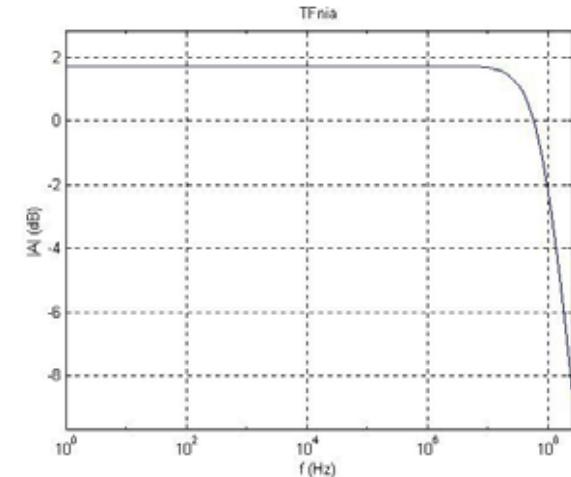
$R=200\Omega$, $C=5pF$, $f_t=100MHz$



Thermal noise model



$$V_{nip1(rms)}^2 = 6.0288 \times 10^{-9} V^2$$



$$V_{nia(rms)}^2 = 4.0896 \times 10^{-10} V^2$$

Noise Analysis

- Equivalent Input Noises

- Dividing these noises by transfer function

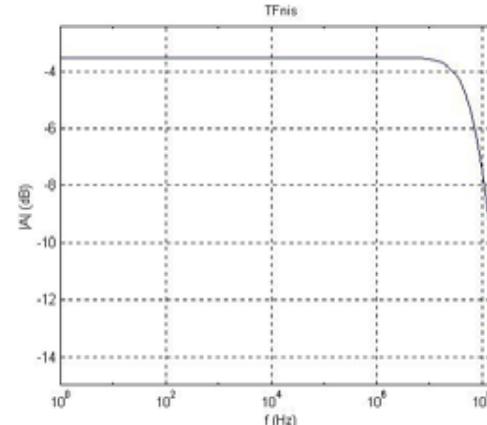
In phase ϕ_2

$$V_{nis2}^2 = \frac{V_{nos2}^2}{TF(s)} = V_{nds}^2 \cdot \left| \frac{(1+sRdc2 \cdot Cdc) \cdot Cs}{(1+sRds \cdot Cs) \cdot Cdc + (1+sRdc2 \cdot Cdc) \cdot Cs} \right|^2$$

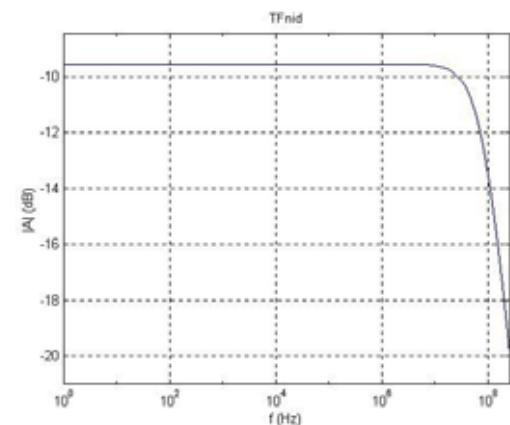
$$V_{nid2}^2 = \frac{V_{nod2}^2}{TF(s)} = V_{ndc2}^2 \cdot \left| \frac{(1+sRds \cdot Cs) \cdot Cdc}{(1+sRds \cdot Cs) \cdot Cdc + (1+sRdc2 \cdot Cdc) \cdot Cs} \right|^2$$

$$V_{nif2}^2 = 4kT \left(\frac{Rf + Ri}{Rf} \right) \cdot Ri \cdot \left| \frac{1+sRf \cdot Ct}{1+sRf \cdot Ct} \right|^2$$

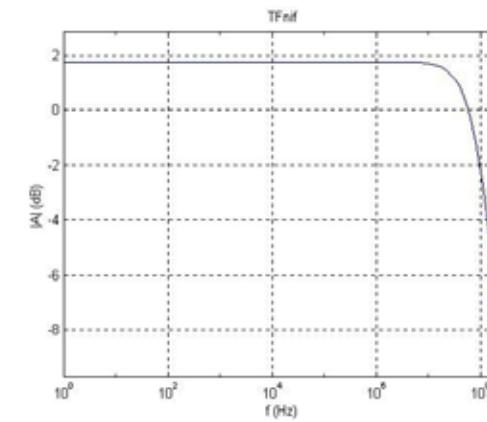
$$V_{nip2}^2 = V_n^2 \cdot \left[1 + \frac{1}{\frac{(1+sRdc2 \cdot Cdc)(1+sRds \cdot Cs)}{(1+sRdc2 \cdot Cdc) \cdot sCsRi + (1+sRds \cdot Cs) \cdot sCdc \cdot Ri}} + 1 \right]$$



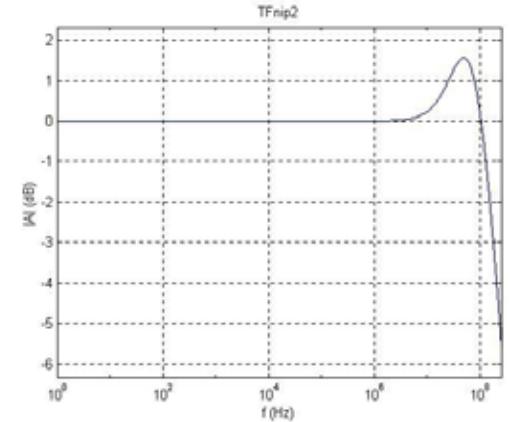
$$V_{nis2}^2 = 1.0906 \times 10^{-10} V^2$$



$$V_{nid2}^2 = 2.7264 \times 10^{-11} V^2$$



$$V_{nif}^2 = 1.0224 \times 10^{-9} V^2$$

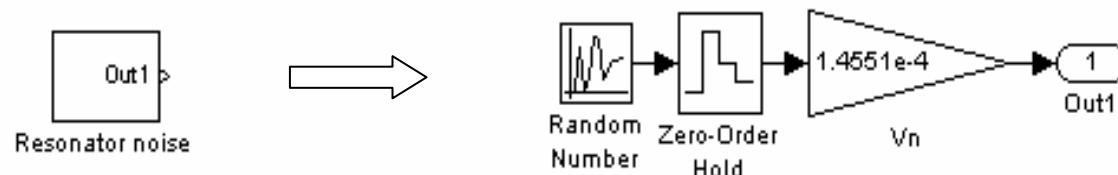


$$V_{nip2}^2 = 1.2010 \times 10^{-8} V^2$$

Noise Analysis

- Total Equivalent Input Noise

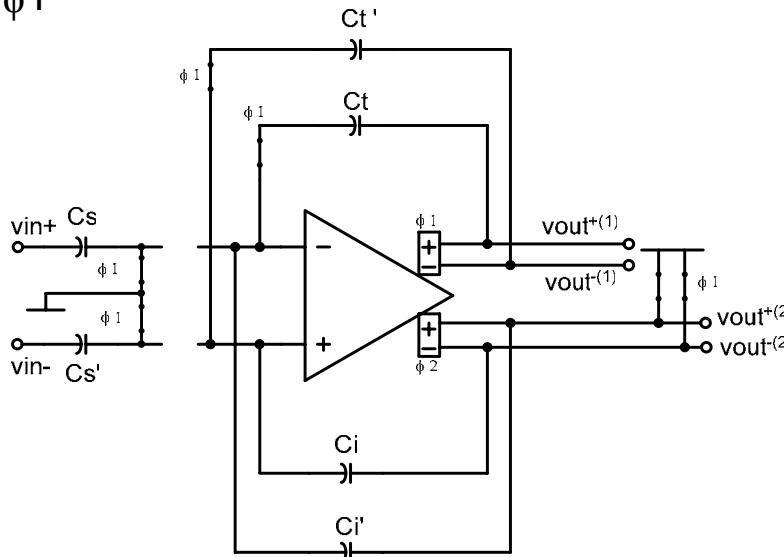
$$V_{in(rms)} = \sqrt{V_{nip1}^2 + 2 \times (V_{nia1}^2 + V_{nis2}^2 + V_{nid2}^2 + V_{nif2}^2) + V_{nip2}^2} = 1.4551 \times 10^{-4} V$$



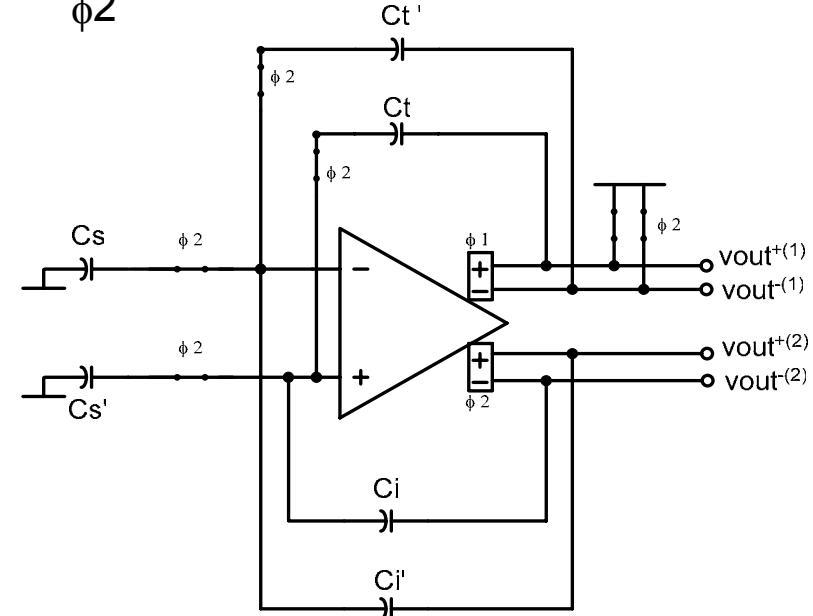
Nonlinear Gain of Opamp

- The Opamp's Gain is a function of Output Level

$\phi 1$



$\phi 2$

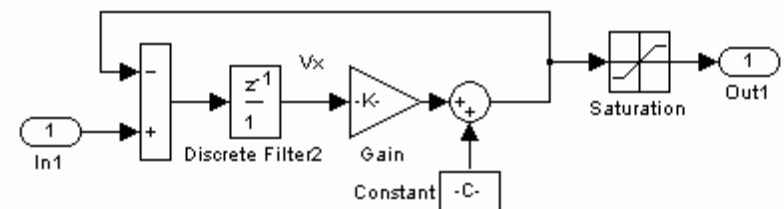


$$\phi 2 \rightarrow \phi 1 \quad v_{out} \cdot \left(1 + \frac{2}{A(n)}\right) = v_{out} \cdot \left(1 + \frac{2}{A(n-1/2)}\right) \cdot z^{-1/2}$$

$$\phi 1 \rightarrow \phi 2 \quad C_s \cdot \left[\frac{v_{out}}{A(n-1/2)} z^{-1/2} - v_{in} \cdot z^{-1} \right] + C_i \cdot [v_{out} \cdot z^{-1/2} + \frac{2 \cdot v_{out}}{A(n-1/2)} z^{-1/2} + v_{out} \cdot z^{-1}] = 0$$

$$v_{out} \approx \frac{C_s}{C_i} \cdot v_{in} \cdot z^{-1} - v_{out} \cdot z^{-1} - \left(2 + \frac{C_s}{C_i}\right) \frac{v_{out}}{A(n)} = v_x - \left(2 + \frac{C_s}{C_i}\right) \frac{v_{out}}{A(n)}$$

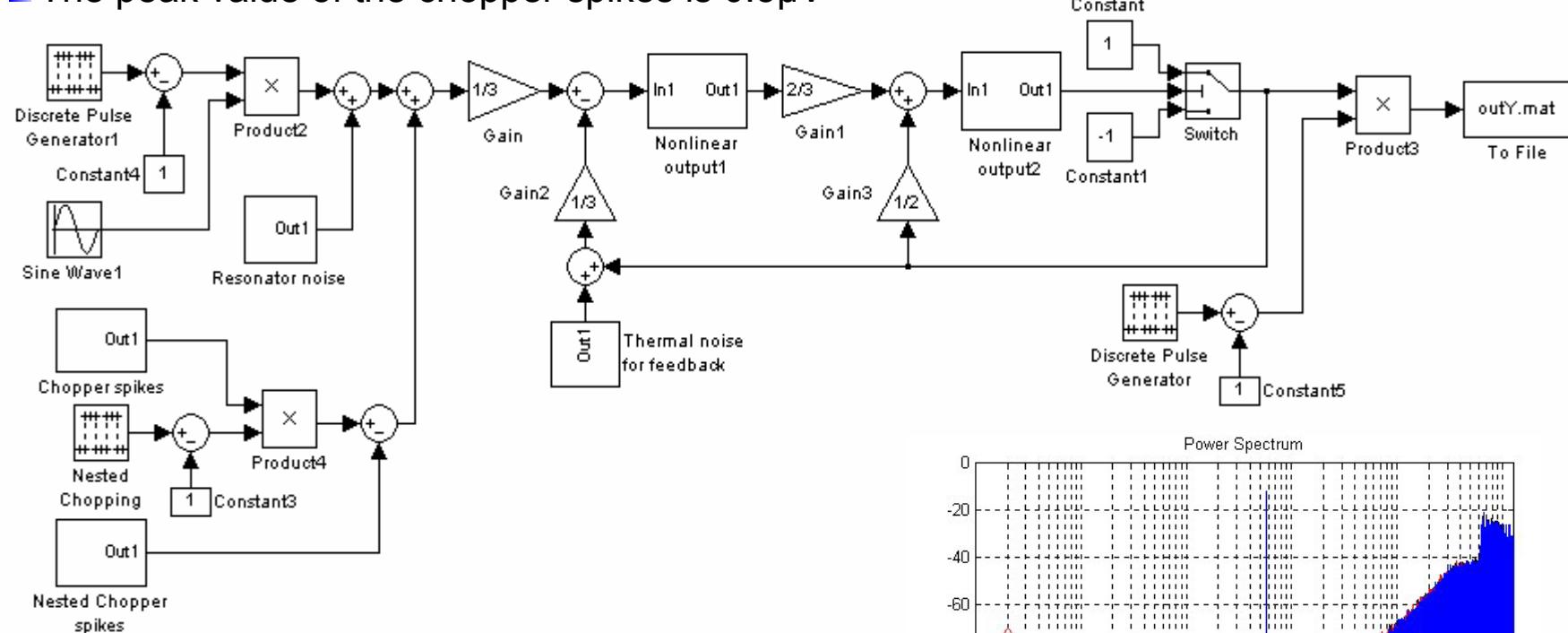
$$v_x = v_{out} + \left(2 + \frac{C_s}{C_i}\right) \frac{v_{out}}{f(v_{out})} = g(v_{out})$$



MATLAB Simulation

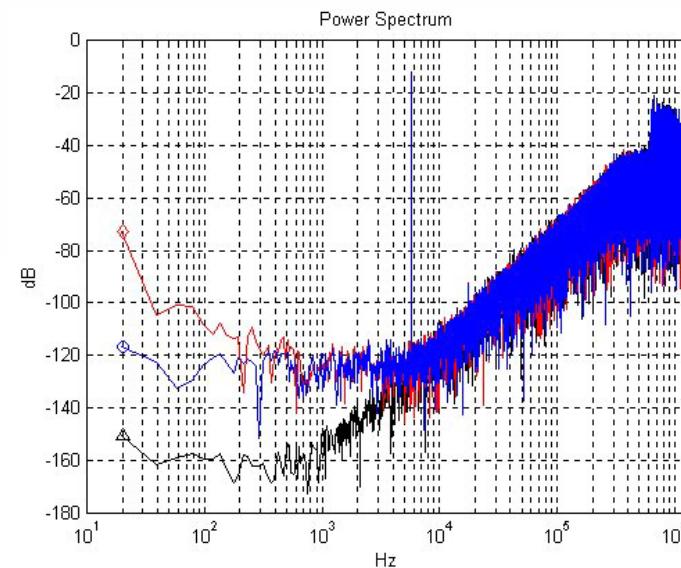
- $A_{in} = 0.5V$, $f_{in} = 5.78125 \text{ kHz}$, $f_s = 2.56\text{MHz}$

- The peak value of the chopper spikes is $0.5\mu\text{V}$



65,535-point FFT

- chopper-stabilized $\Delta\Sigma$ modulator
- nested-chopper $\Delta\Sigma$ modulator
- ideal chopper- stabilized $\Delta\Sigma$ modulator



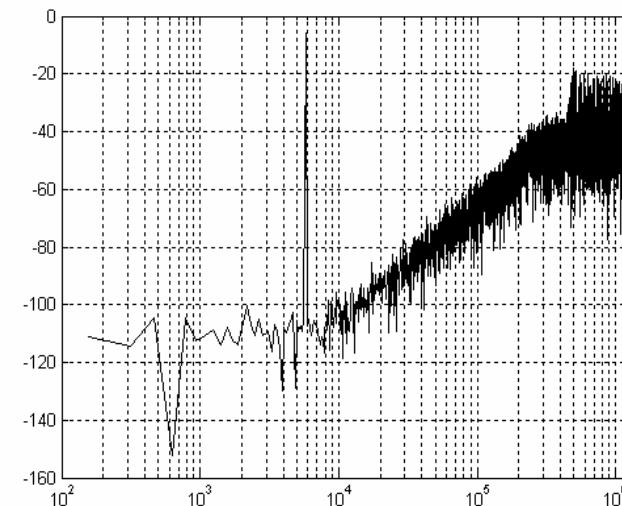
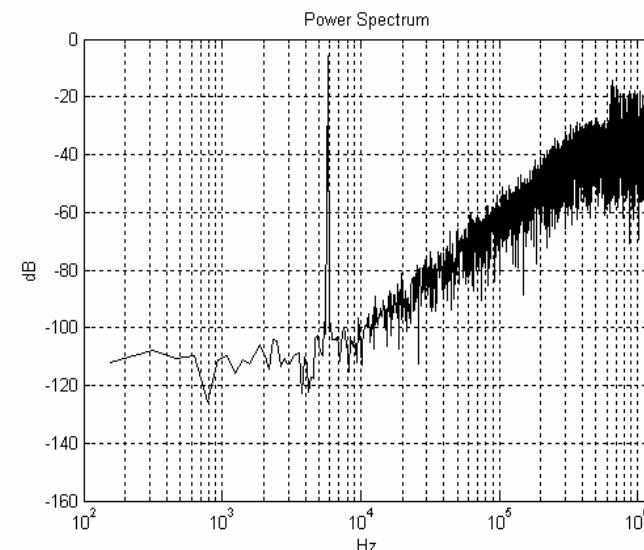
Simulation

- MATLAB (16,384-point FFT)

- $f_s=2.56\text{MHz}$
- Bandwidth = 22.05kHz
- SNDR=70dB

- HSPICE (16,384-point FFT)

- $V_{DD}=1\text{V}$
- $V_{ref+}=0.75\text{V}$
- $V_{ref-}=0.25\text{V}$
- $f_s=2.56\text{MHz}$
- Bandwidth = 22.05kHz
- SNDR=69.9dB



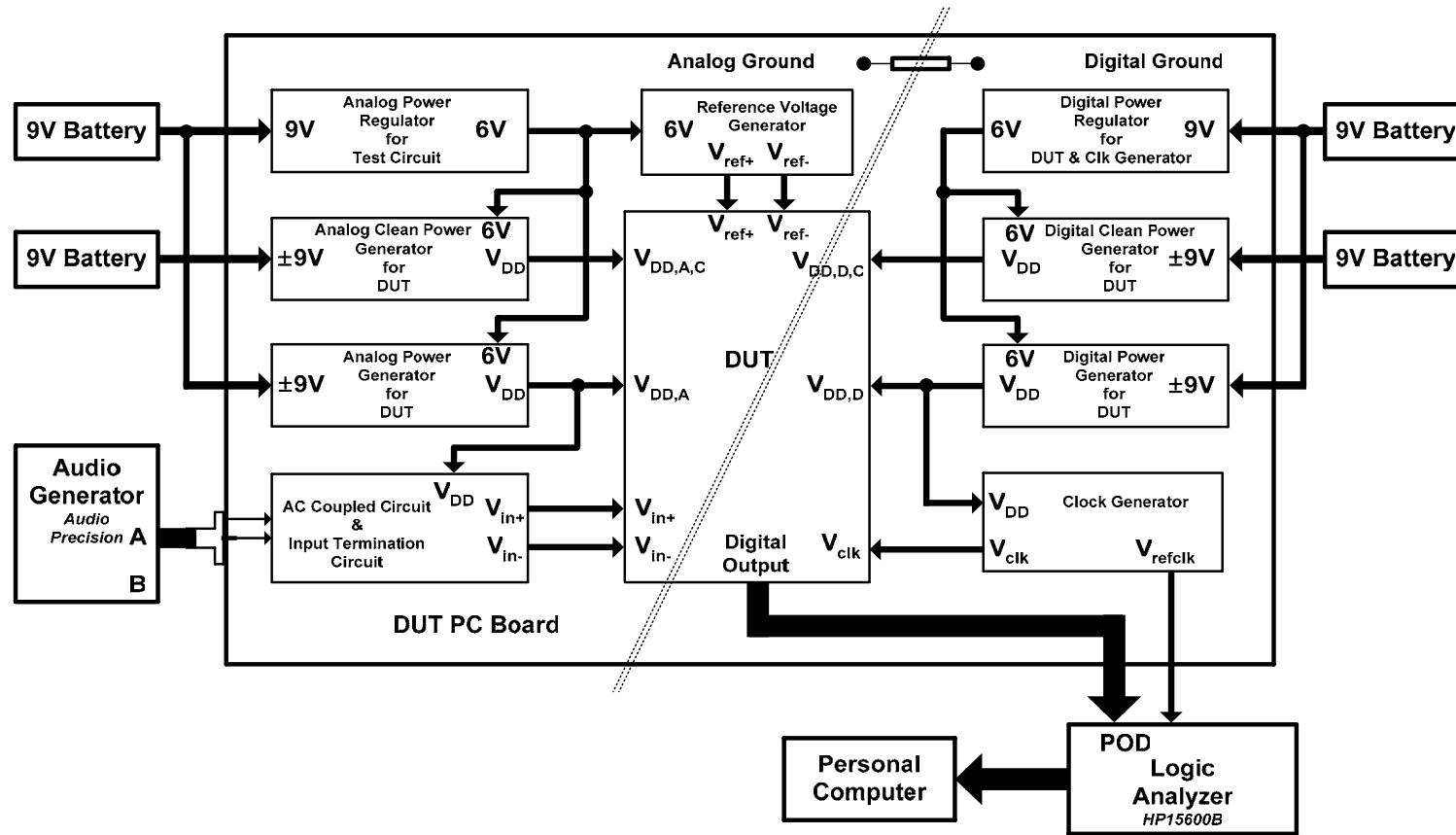
16,384-point FFT



Experimental Setup

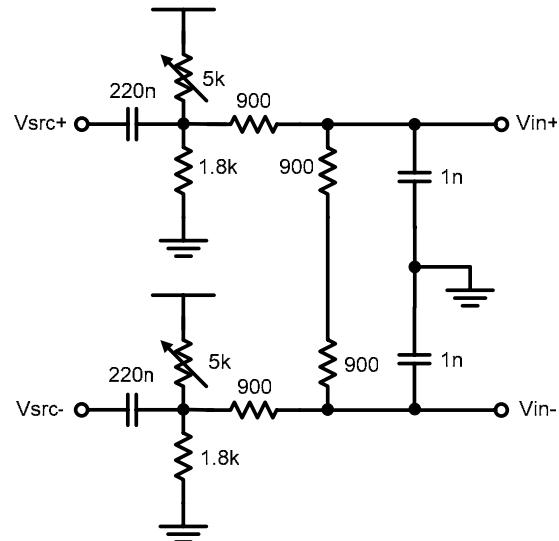
● Experimental Test Setup

- Audio Precision
- Logic Analyzer HP 16702A

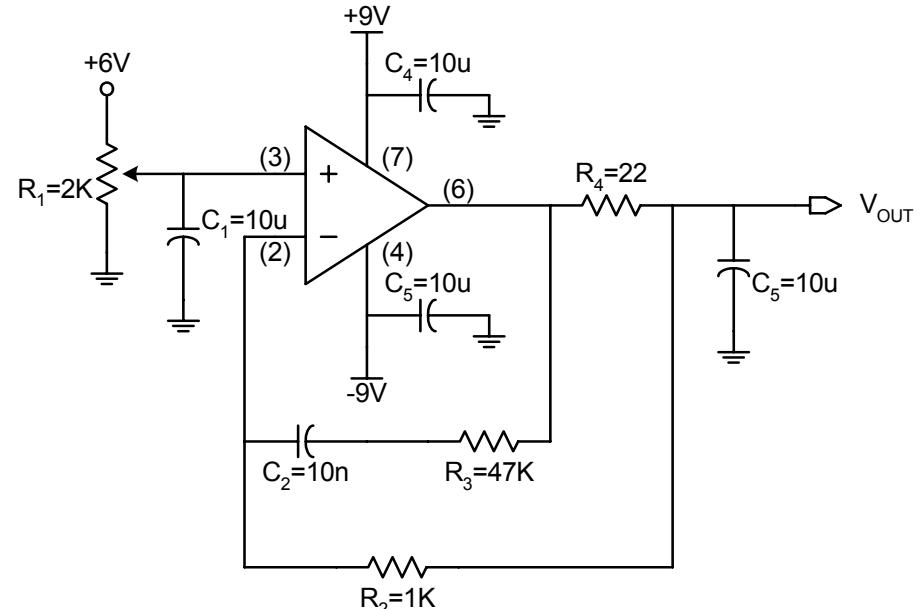


Experimental Setup

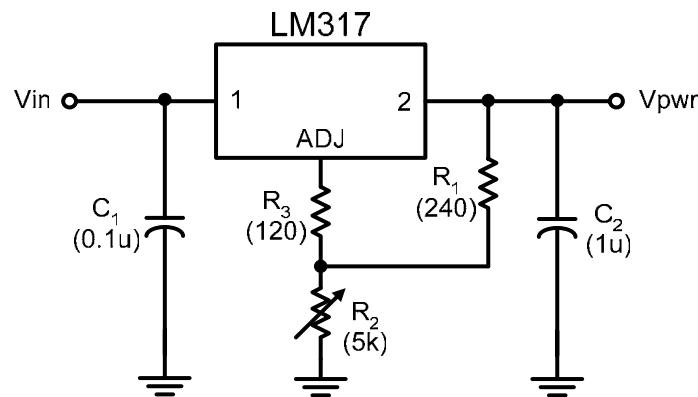
● Input Termination Circuit



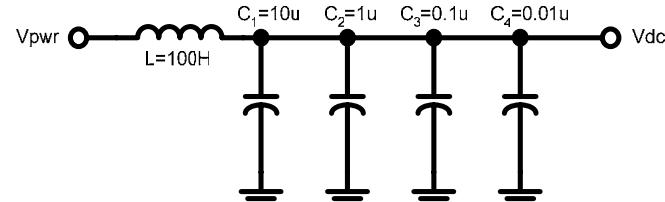
● The Reference Voltage Circuit



● Regulator Circuit



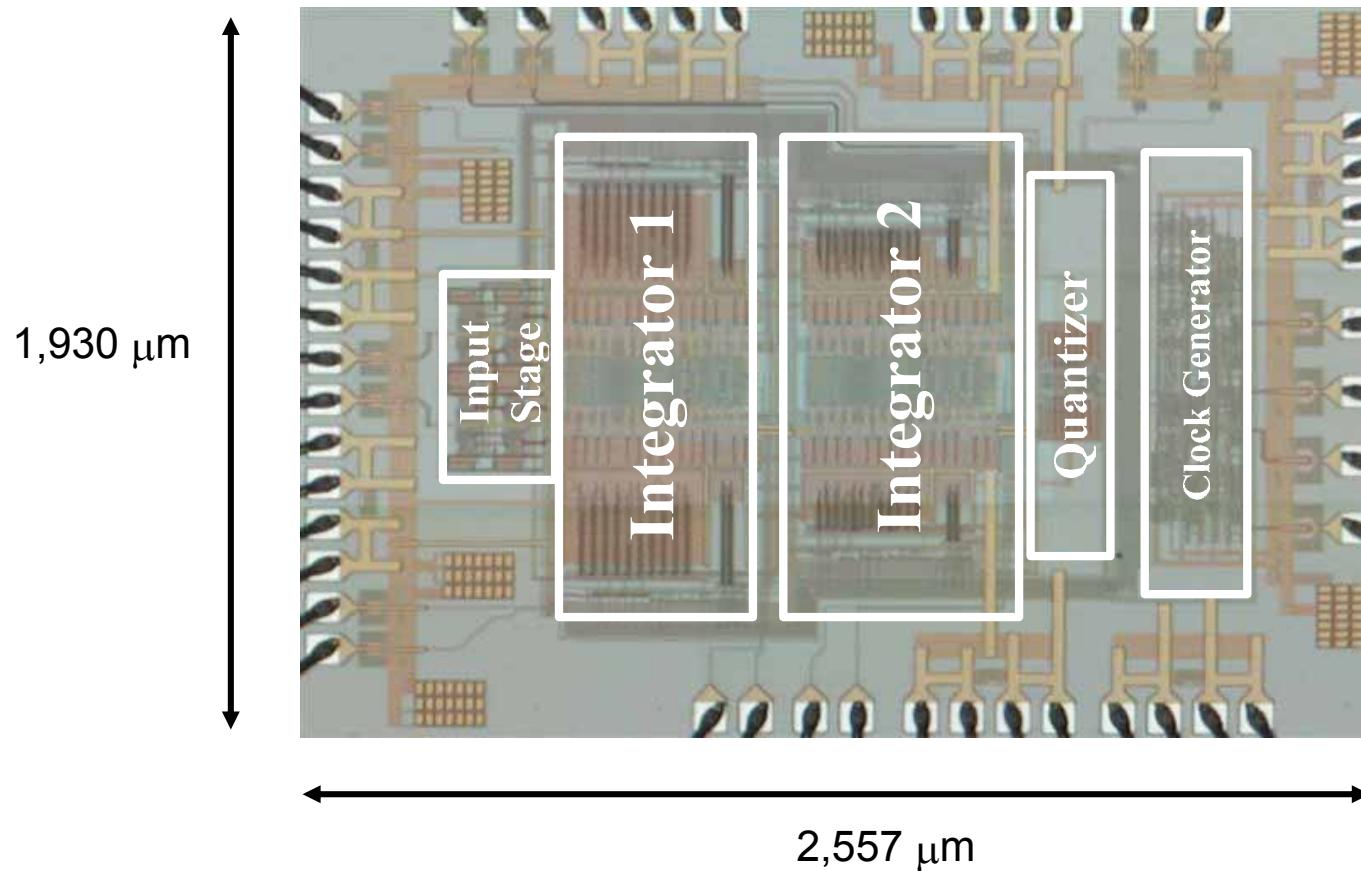
● Filter Tank for the Supply Voltages



S. Rabii and B. A. Wooley, "The Design of Low-Voltage, Low-Power Sigma Delta Modulator," Kluwer academic publisher, 1999

Experimental Setup

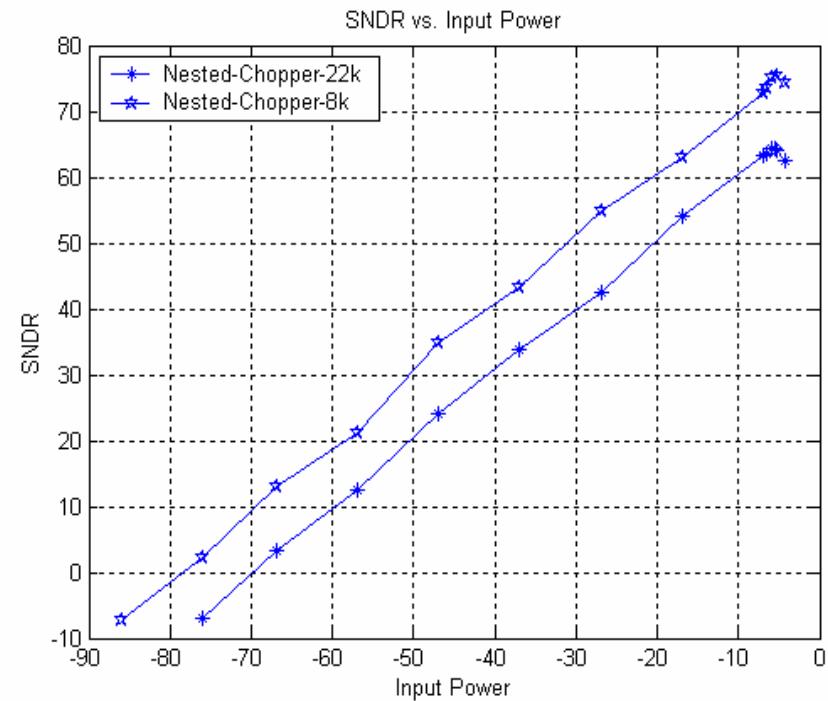
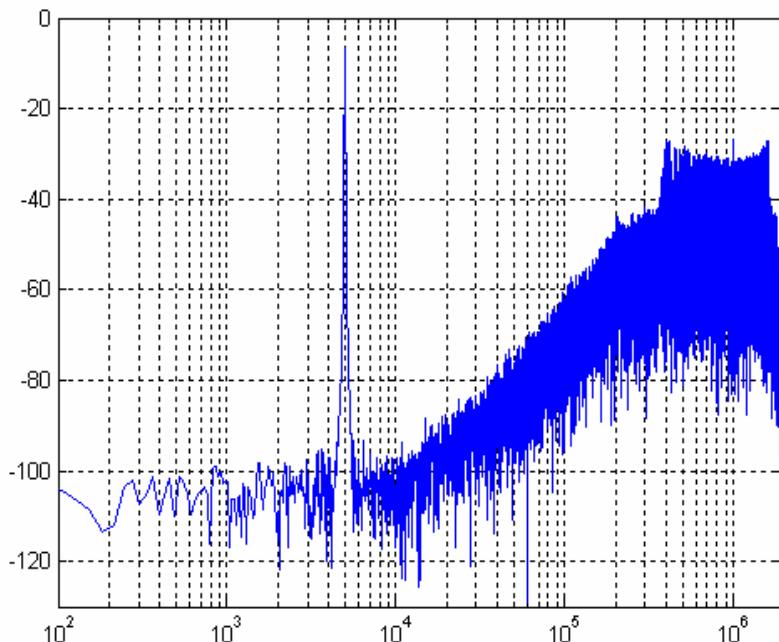
- Chip Photo (0.25μm CMOS MIM process)
 - Clean guard ring
 - Separate V_{DD}, V_{SS}



Experimental Results

- 32,768-Point FFT

- fs=2MHz, fin=5kHz, A=-6dB
- SNDR=65dB, Dynamic Range (DR)=63dB for BW=22.05KHz
- SNDR=74dB, DR=72dB for BW=8KHz

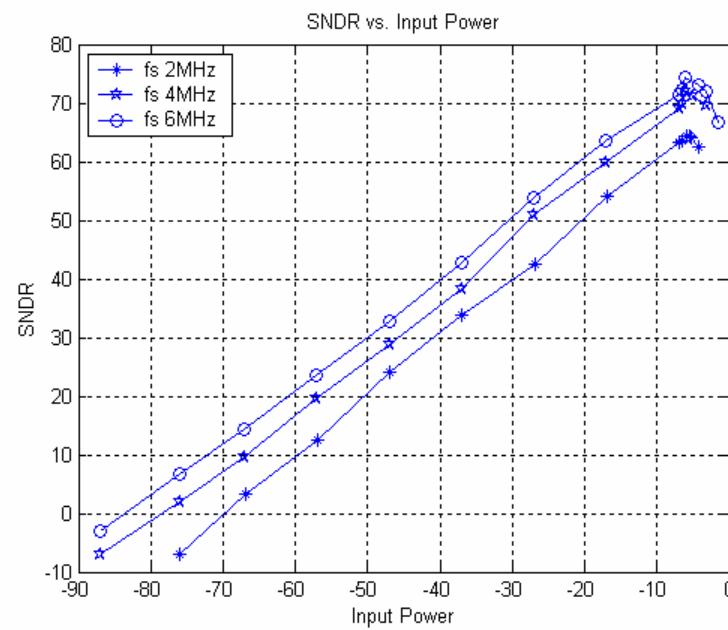


Experimental Results

- 16,384-Point FFT

■ fin=5kHz for BW=22.05kHz

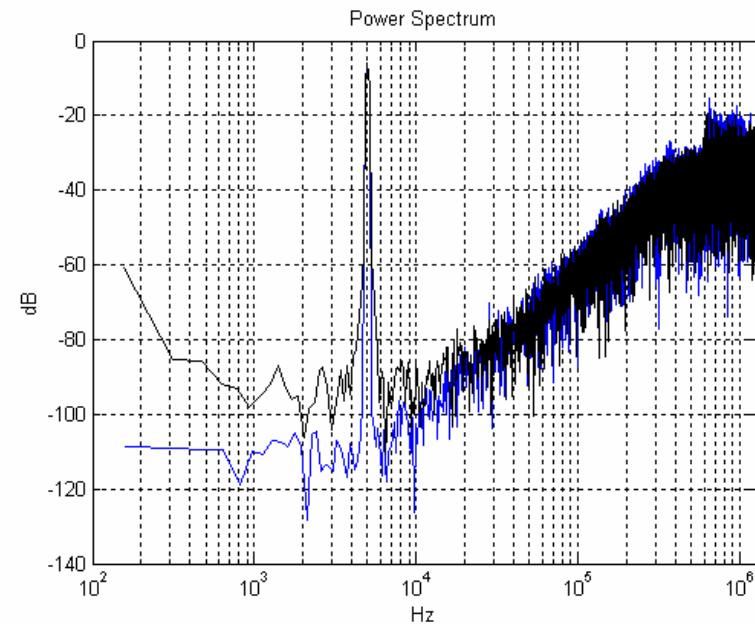
fs	2MHz	4MHz	6MHz
SNDR	65dB	72dB	74dB
DR	63dB	72dB	78dB



- 16,384-Point FFT

■ fs=2.5MHz, fin=5kHz

- SNDR=66.67dB (measurement)
- SNDR=69.9dB (simulation)



Comparison

	This Work	M. Keskin	Qunying Li	J. Sauerbrey	T. Tille	M. Dessouky	V. Peluso
Reference	-	[90]	[94]	[89]	[88]	[87]	[91]
Technology	0.25 μ m CMOS 1P5M	0.35 μ m CMOS	0.35 μ m CMOS	0.18 μ m CMOS 1P3M	0.25 μ m CMOS	0.35 μ m CMOS DPTM	0.5 μ m CMOS
Order	second-order	second-order	second-order	second-order	second-order	third-order	third-order
Sampling frequency	6MHz	10.24MHz	500kHz	1.024MHz	1.024MHz	5MHz	1.538MHz
OSR	136	256	64	64	64	100	48
Signal Swing	0.5Vpp	1.2Vpp	0.9Vpp	-	0.5Vpp	-	0.9Vpp
Bandwidth	22.05kHz	20kHz	50kHz	300-3.4kHz	8kHz	8kHz	25kHz
Peak SNDR	74dB	78dB	70dB	63dB	67dB	71dB	85dB
Dynamic Range	78dB	80dB	74dB	75dB	75dB	-	88dB
Area(mm ²)	2.55x1.93	0.41	0.7	0.51x0.16	0.06	0.9x0.7	0.85
Power(mW)	6.2mW	5.6mW	0.038mW	0.08mW	1mW	0.95 μ W	0.04mW
Power Supply	1V	1V	1.2V	0.7V	1.8V	1V	0.9V

[87] M. Dessouky and A. Kaiser, "Very Low-Voltage Digital-Audio Modulator with 88-dB Dynamic Range Using Local Switch Bootstrapping," IEEE J. Solid-State Circuits, vol.36, pp. 349-355, Mar. 2001.

[88] T. Tille, J. Sauerbrey, and D. Schmitt-Landsiedel, "A Low-Voltage MOSFET-Only Modulator for Speech Band Applications Using Depletion-Mode MOS-Capacitors in Combined Series and Parallel Compensation," in Proc. IEEE ISCAS, vol. 1, no. 3, pp. 376-379, May 2001.

[89] J. Sauerbrey, T. Tille, and D. Schmitt-Landsiedel, "A 0.7-V MOSFET-Only Switched-Opamp modulator in Standard Digital CMOS Technology," IEEE J. Solid-State Circuits, vol. 37, no. 12, pp. 1662-1669, Dec. 2002.

[90] M. Keskin, U. K. Moon, and Gabor. C. Temes, "A 1-V 10-MHz Clock-Rate 13-Bit CMOS modulator using Unity-Gain-Reset Opamps," IEEE J. Solid-State Circuits, vol. 37, no. 7, pp. 817-824, Jul. 2002.

[91] V. Peluso, P. Vancorenland, A. Marques, M. Steyaert, and W. Sansen, "A 900mV 40 μ W Switched Opamp Modulator with 77 dB Dynamic Range," ISSCC Digest of Technical Papers, pp. 68 -69, Feb. 1998.

[94] Li Qunying, J. Van der Spiegel, and K. R. Laker, "A 1.2V, 38 μ W Second-Order Modulator with Signal Adaptive Control Architecture," in Proc. IEEE 2nd Dallas CAS Workshop on Low Power/Low Voltage Mixed-Signal Circuits and Systems, pp. 23-26, 2001.



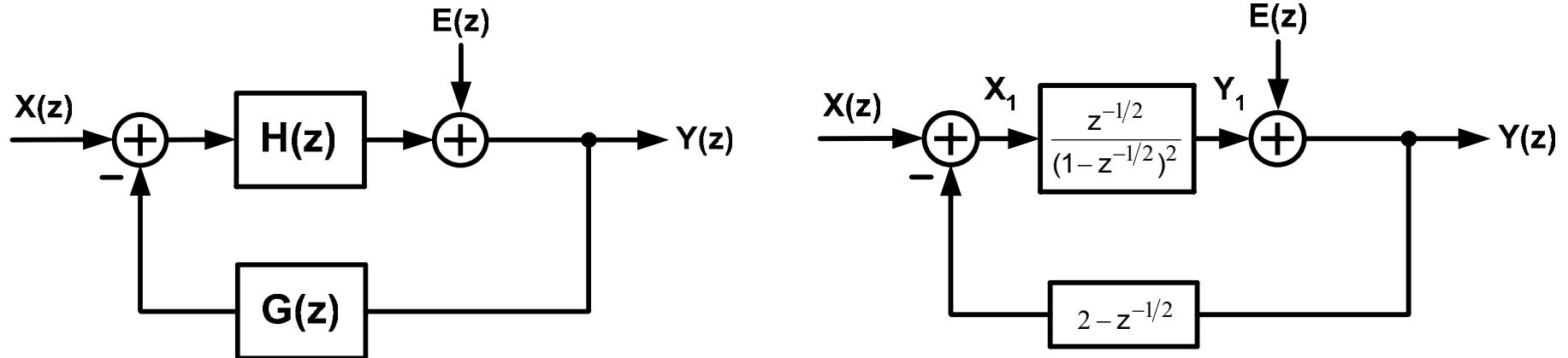
Outline

1. Introduction
2. Low Voltage Circuits for Delta Sigma Modulator
3. Low Voltage Nested-Chopper Delta Sigma Modulator
4. Low Voltage Second-Order Delta Sigma Modulator Using a Single Opamp
 - System Considerations
 - Implementation
 - Simulation & Experimental Results
5. Low Voltage Fourth-Order Bandpass Delta Sigma Modulator



System Considerations

- Block Diagram of a Second-order $\Delta\Sigma$ Modulator



$$Y(Z) = X(z) \frac{H(z)}{1 + G(z)H(z)} + E(z) \frac{1}{1 + G(z)H(z)} = X(Z) \cdot z^{-1} + E(Z) \cdot (1 - z^{-1})^2$$

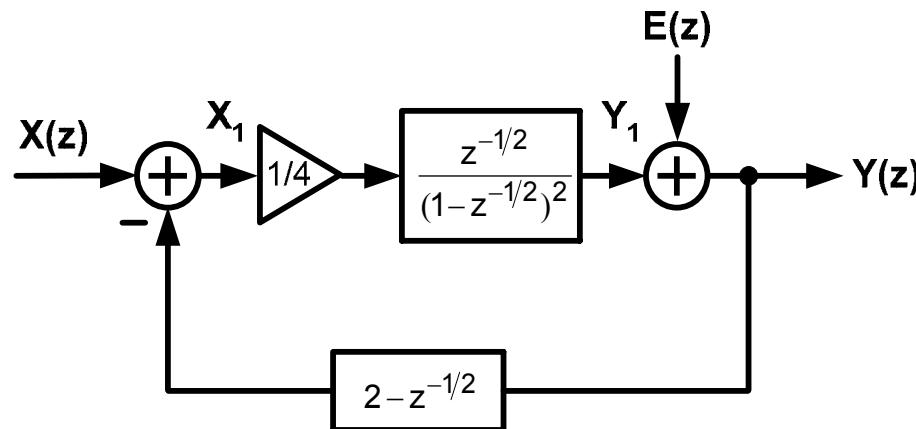
$\rightarrow \begin{cases} H(z) = \frac{z^{-1}}{(1 - z^{-1})^2} \\ G(z) = 2 - z^{-1} \end{cases}$

Double Sampling $\rightarrow \begin{cases} H(z) = \frac{z^{-1/2}}{(1 - z^{-1/2})^2} \\ G(z) = 2 - z^{-1/2} \end{cases}$

z^{-2} is difficult to be implemented

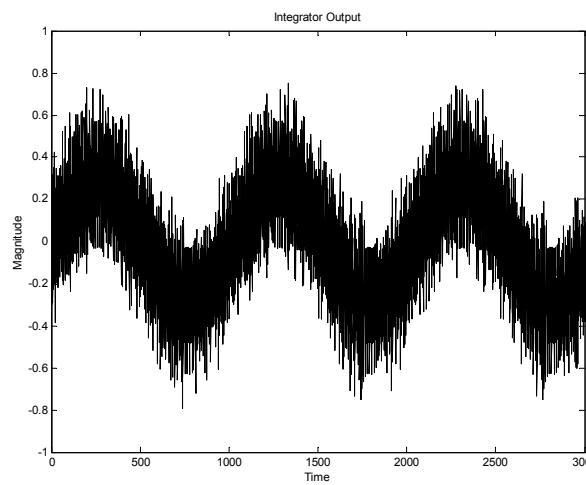
System Considerations

- Coefficients Scaling

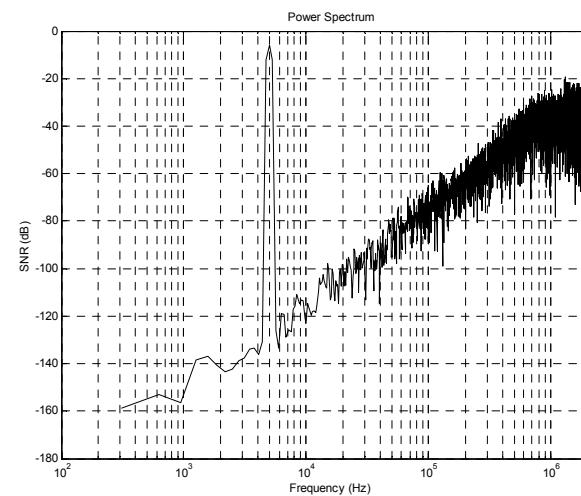


$A = -6\text{dB}$, $f_{in} = 5\text{kHz}$, $f_s = 2.56\text{MHz}$

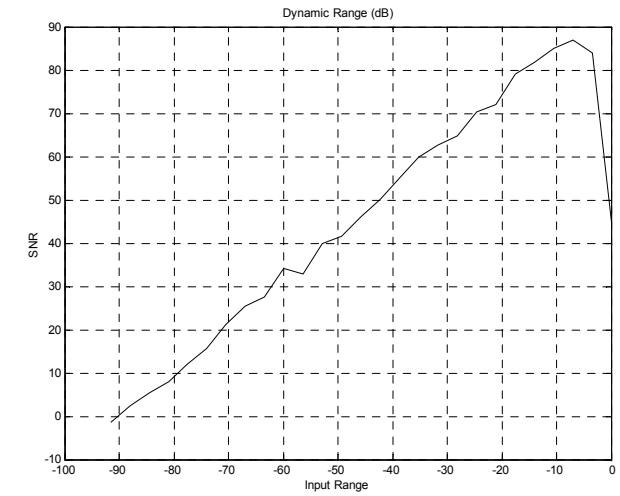
BW = 22.05kHz



Integrator output scaled



SNDR = 87 dB



Dynamic Range = 82 dB

Implementation

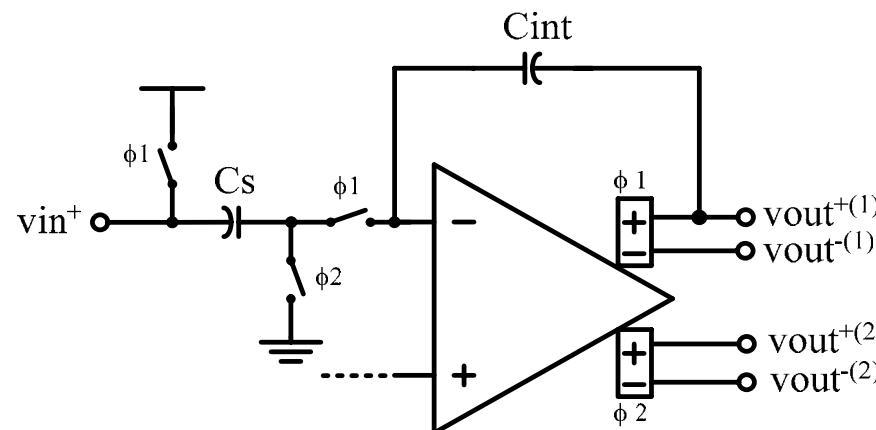
- Integrator

$$H(z) = \frac{Y_1(z)}{X_1(z)} = \frac{1/4 \cdot z^{-1/2}}{(1 - z^{-1/2})^2}$$

$$Y_1(z) = (1/4) \cdot z^{-1/2} X_1(z) + 2z^{-1/2} Y_1(z) - z^{-1} Y_1(z)$$

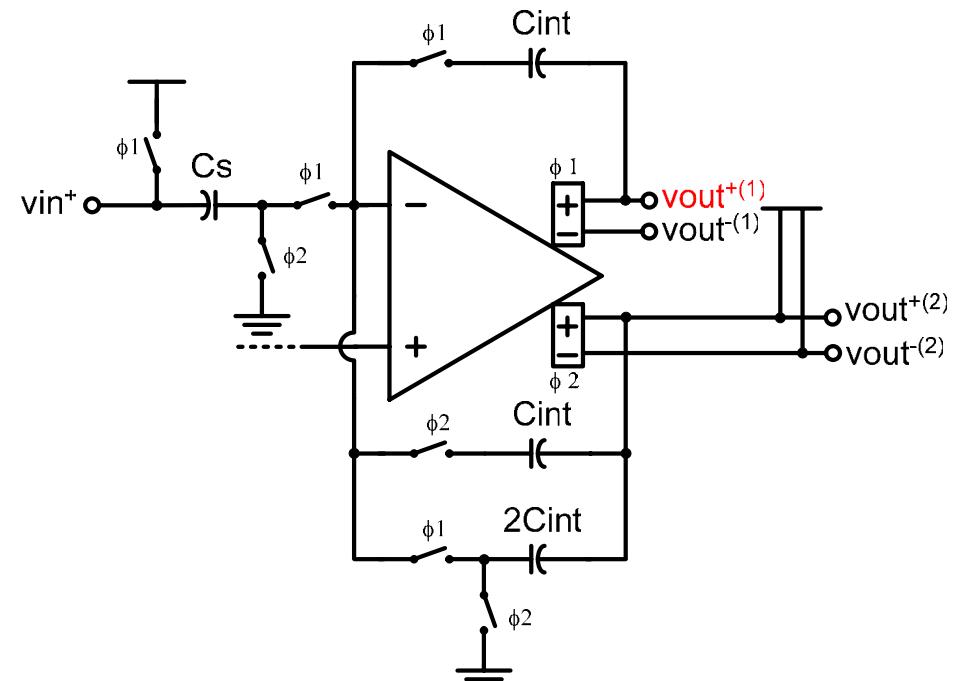
- The first term $+(1/4) \cdot z^{-1/2} X_1(z)$

→ $C_s/C_{int} = 1/4$



- The second term $+2 \cdot z^{-1/2} Y_1(z)$

→ pseudo-n path

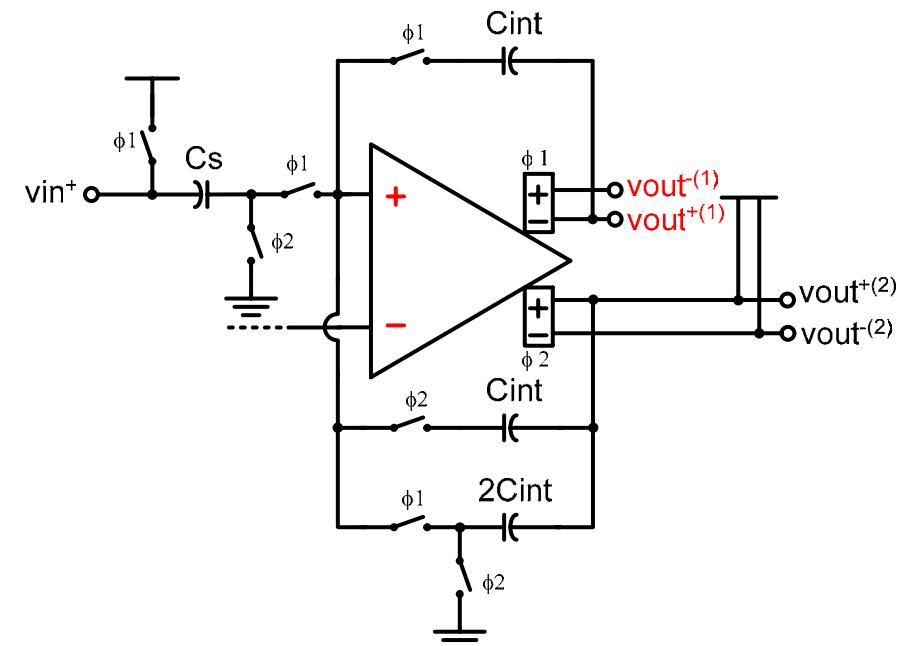
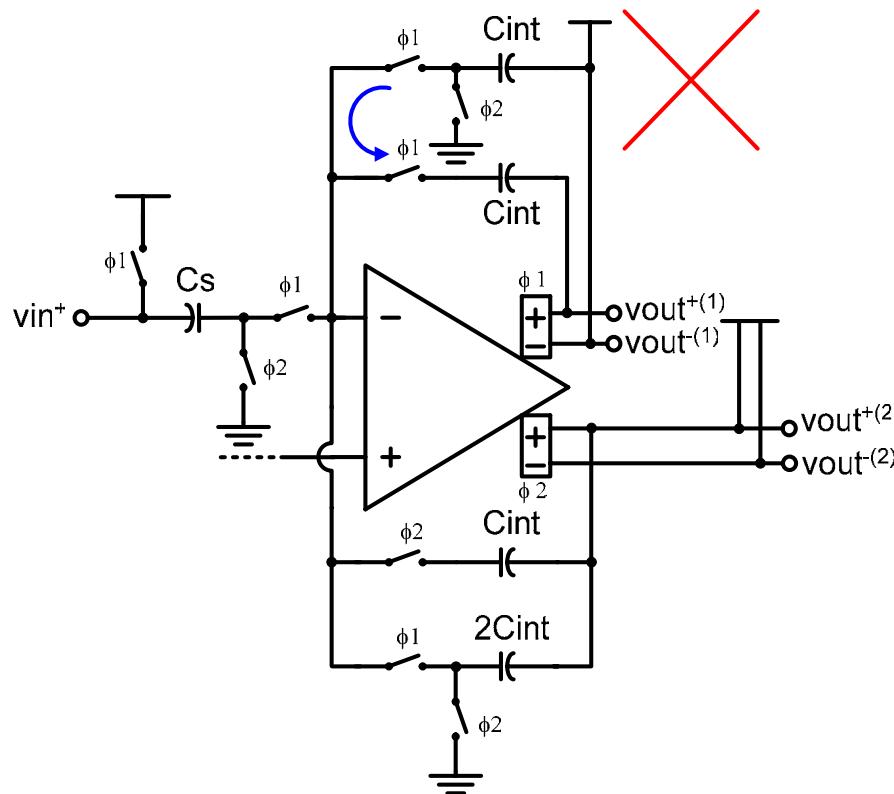


Implementation

- Integrator

- The third term $-z^{-1}Y_1(z)$

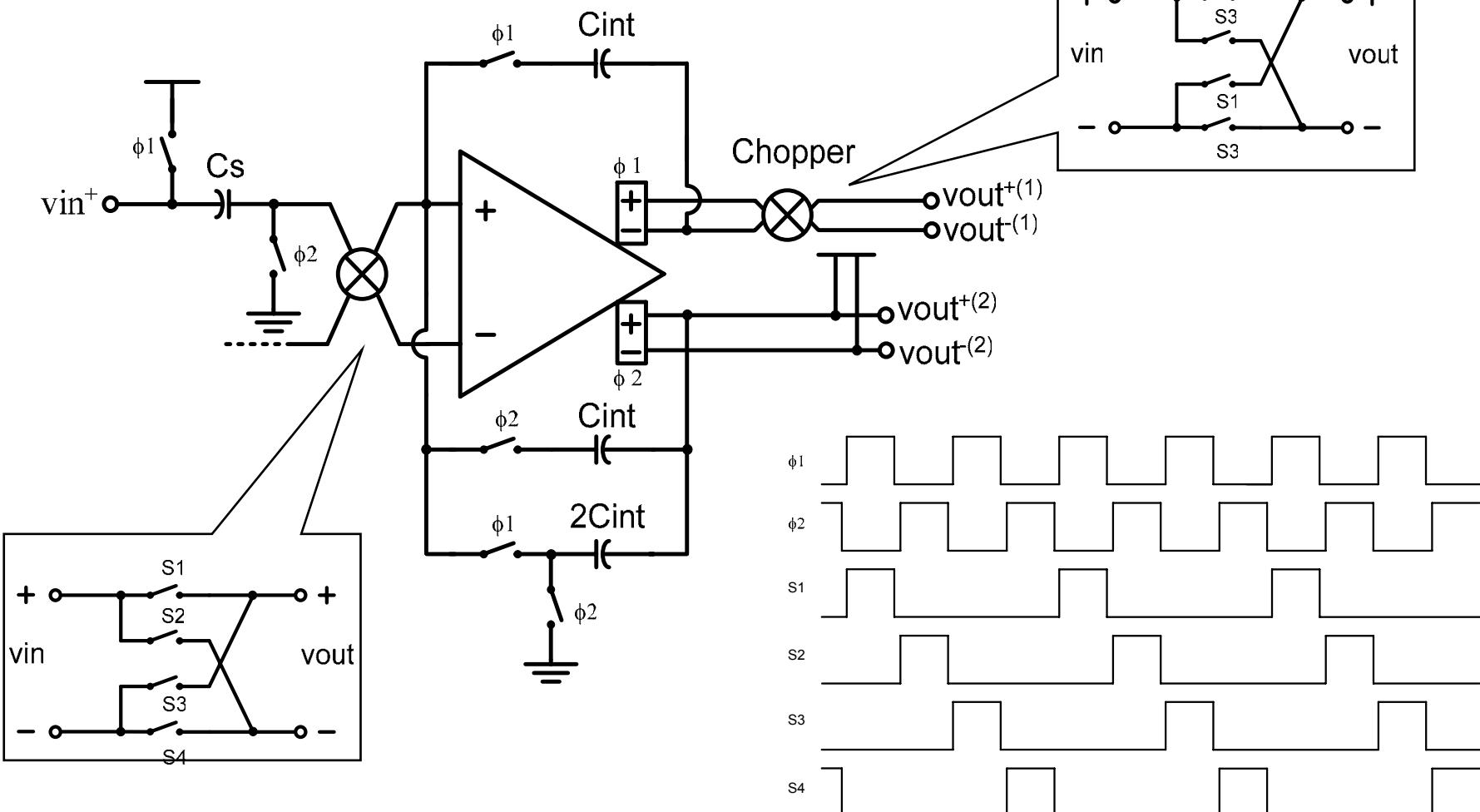
- One capacitor is saved each output node



Implementation

- Integrator

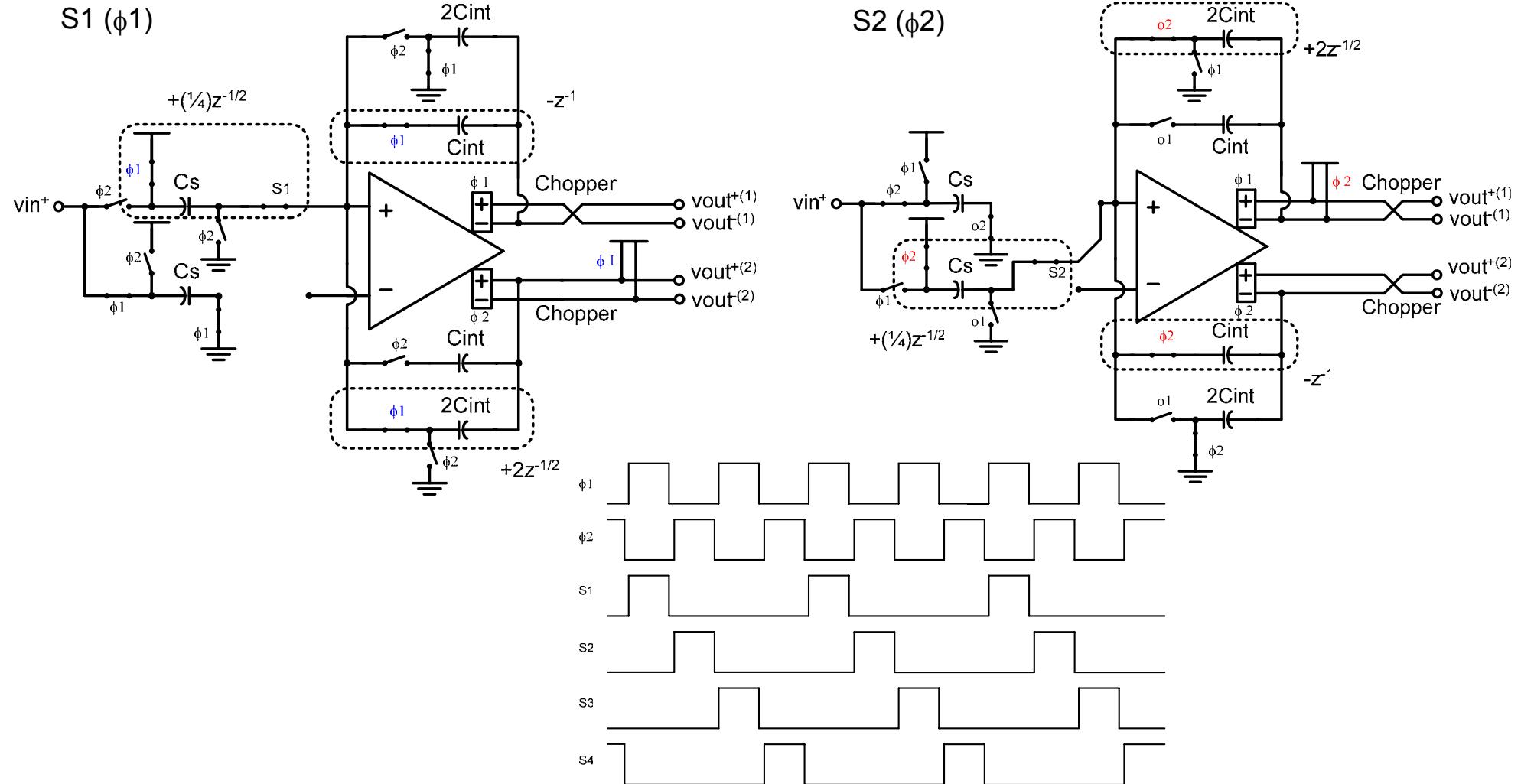
- Choppers at the input and output of the opamp



Implementation

- Four Phases (S1, S2, S3, and S4)

$$v_{out}^{+(1)}(z) = (1/4) \cdot z^{-1/2} v_{in}^+(z) + 2z^{-1/2} v_{out}^{+(1)}(z) - z^{-1} v_{out}^{+(1)}(z)$$

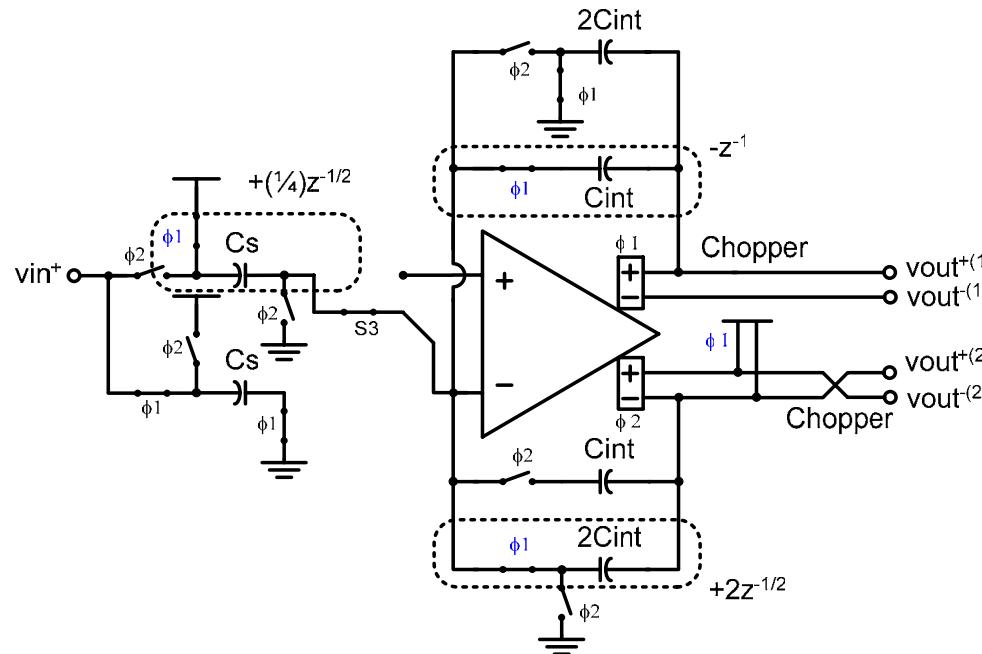


Implementation

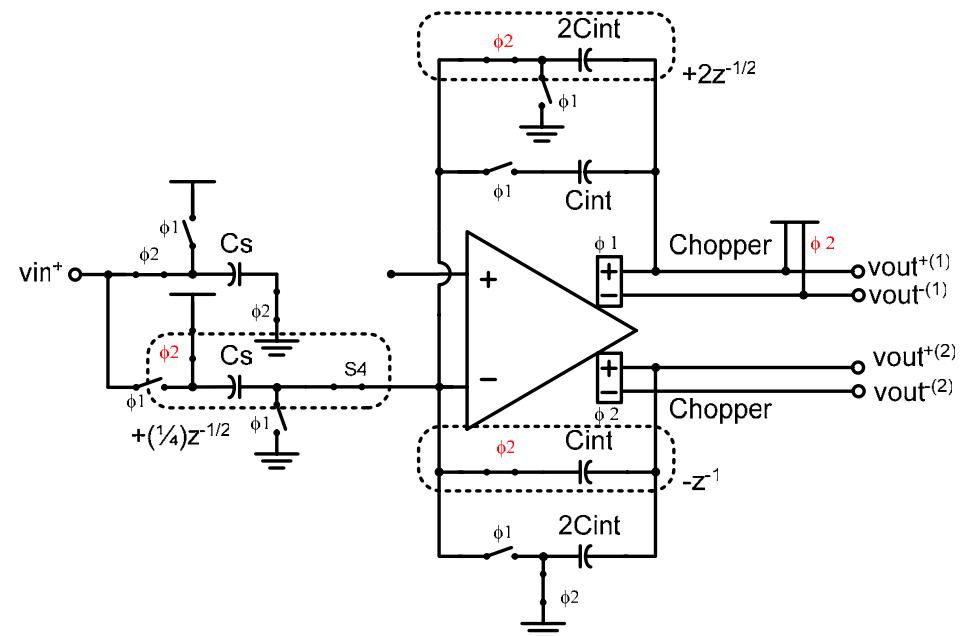
- Four Phases (S1, S2, S3, and S4)

- Remove the chopper at the output of the opamp

S3 (ϕ_1)



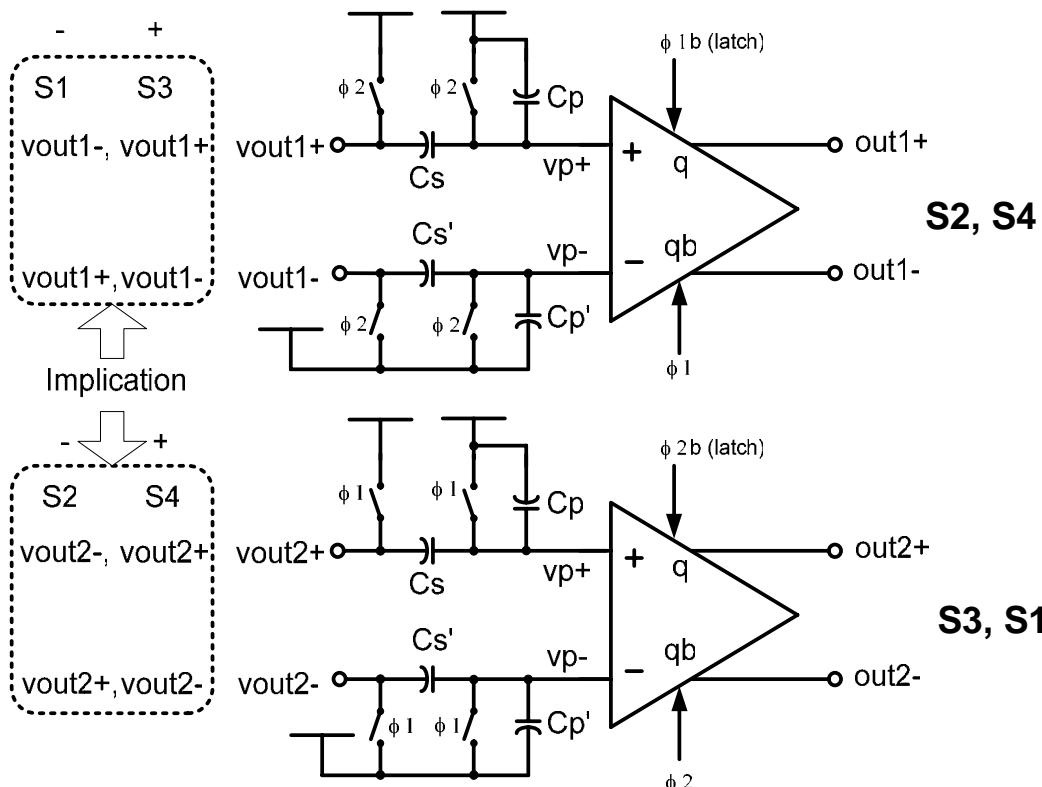
S4 (ϕ_2)



Implementation

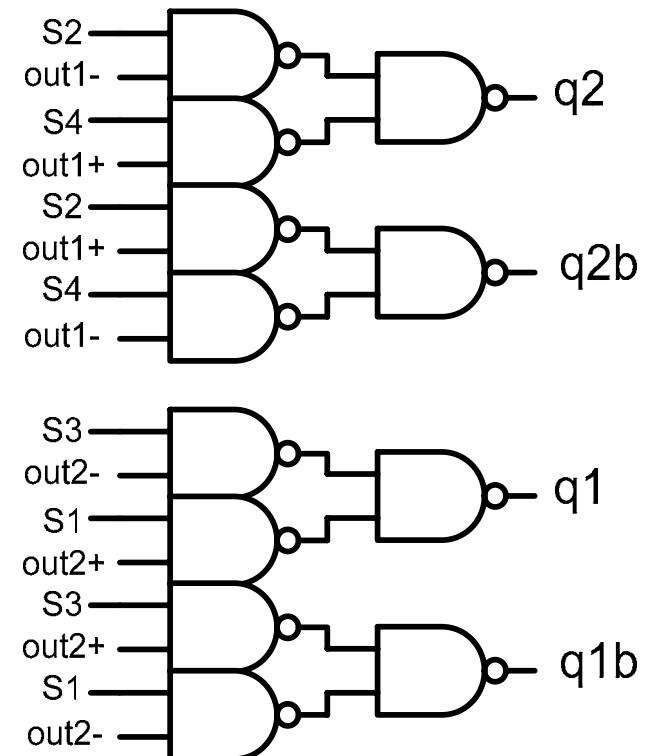
- Two Quantizers

- Connect to the outputs directly



- Multiplexer

- Chopper function is given



$$q_2 = S_2 \cdot (out_{1-}) + S_4 \cdot (out_{1+})$$

$$q_{2b} = S_2 \cdot (out_{1+}) + S_4 \cdot (out_{1-})$$

$$q_1 = S_3 \cdot (out_{2-}) + S_1 \cdot (out_{2+})$$

$$q_{1b} = S_3 \cdot (out_{2+}) + S_1 \cdot (out_{2-})$$

Implementation

- DAC Feedback ($2-z^{-1/2}$)

- The first term $\times 2$

- ➡ $V_{ref+}=0.75V$, $V_{ref-}=0.25V$

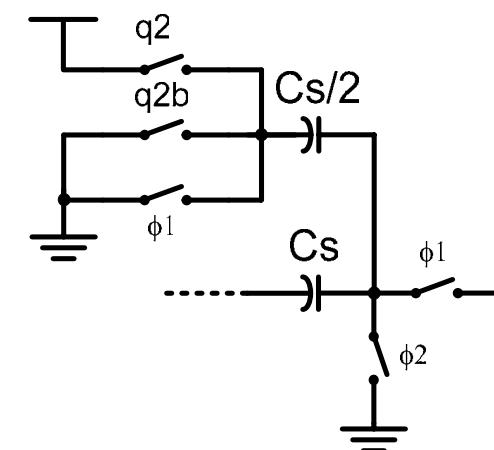
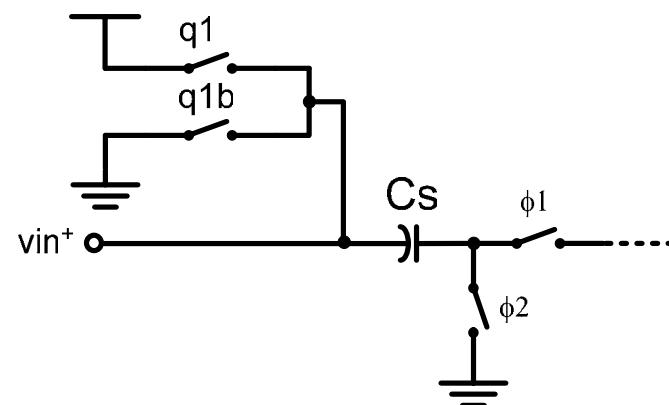
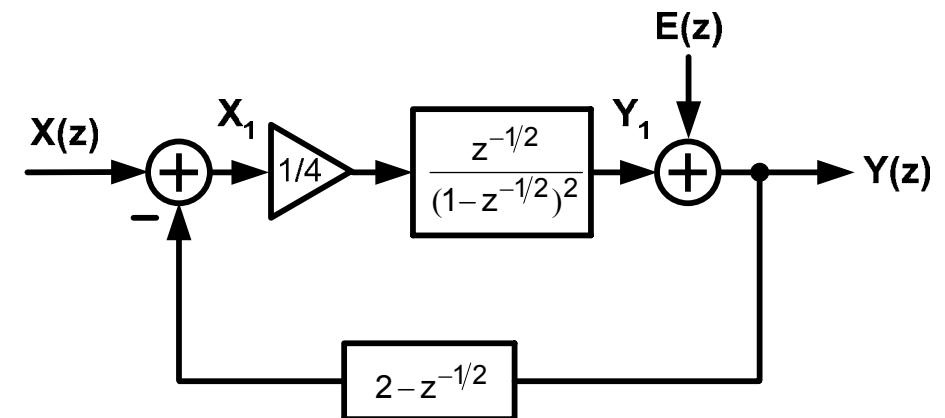
- ➡ $V_{ref+}=1V$ (V_{DD}), $V_{ref-}=0V$ (V_{SS})

- The second term $-z^{-1/2}$

- ➡ $V_{ref+}=1V$ (V_{DD}), $V_{ref-}=0V$ (V_{SS})

- ➡ Capacitor size is half the sampling capacitor

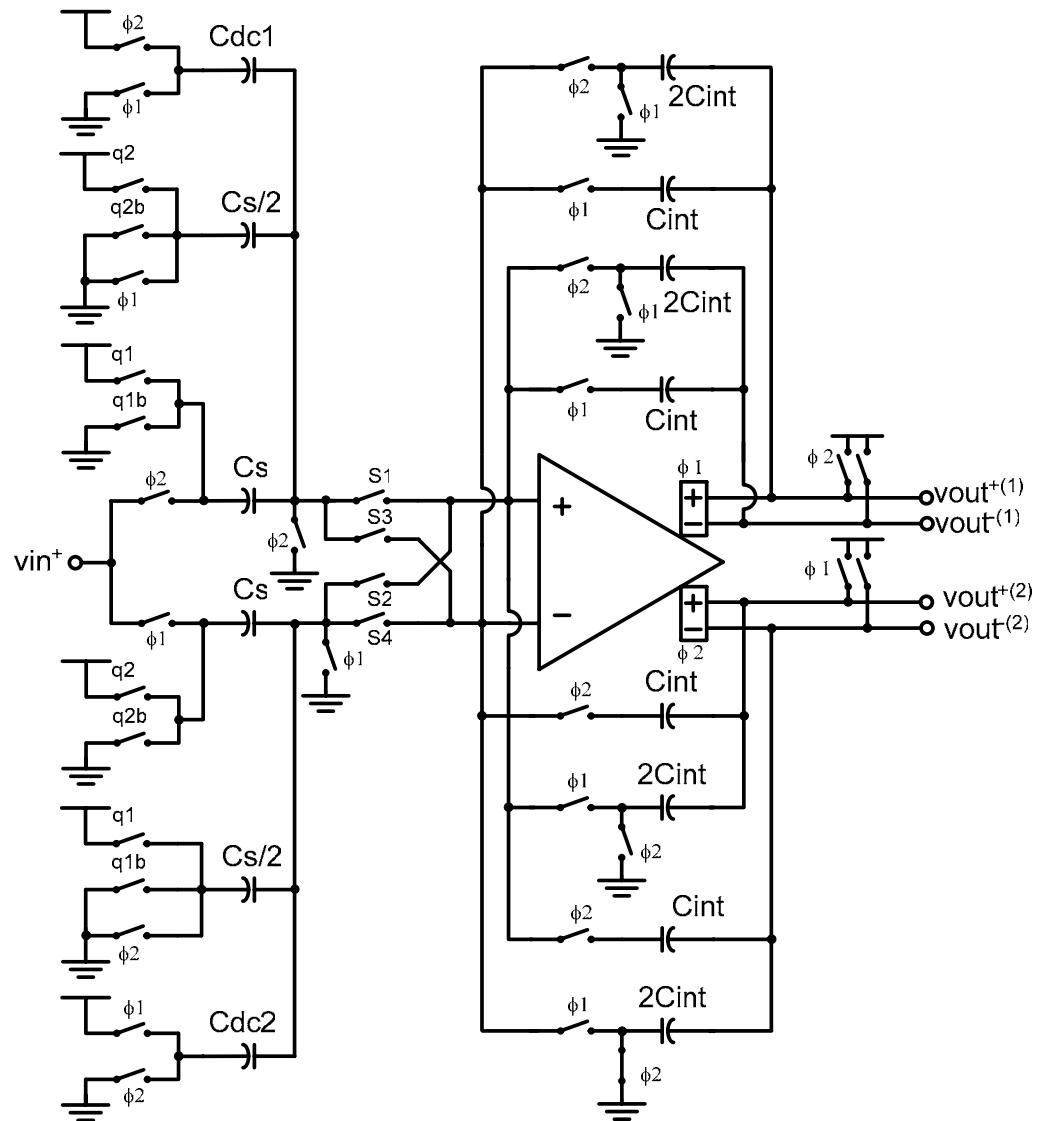
- Reference Voltage Circuits in PC board are saved



Implementation

• Second-Order Integrator with DAC Feedback

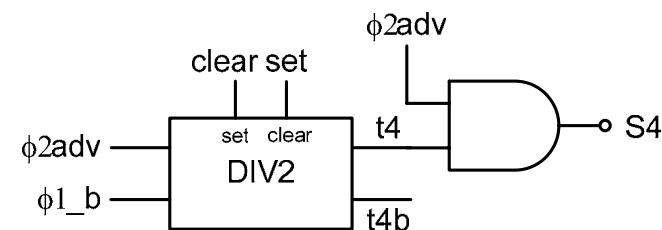
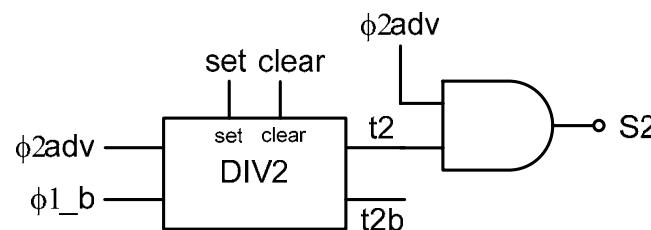
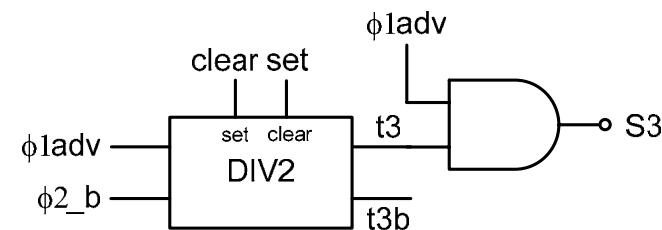
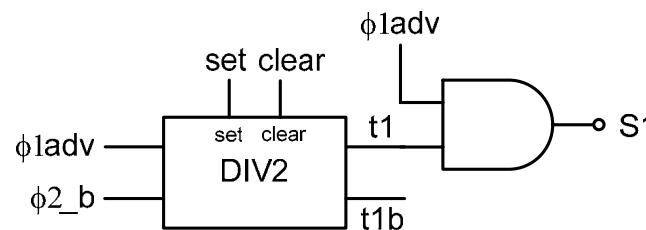
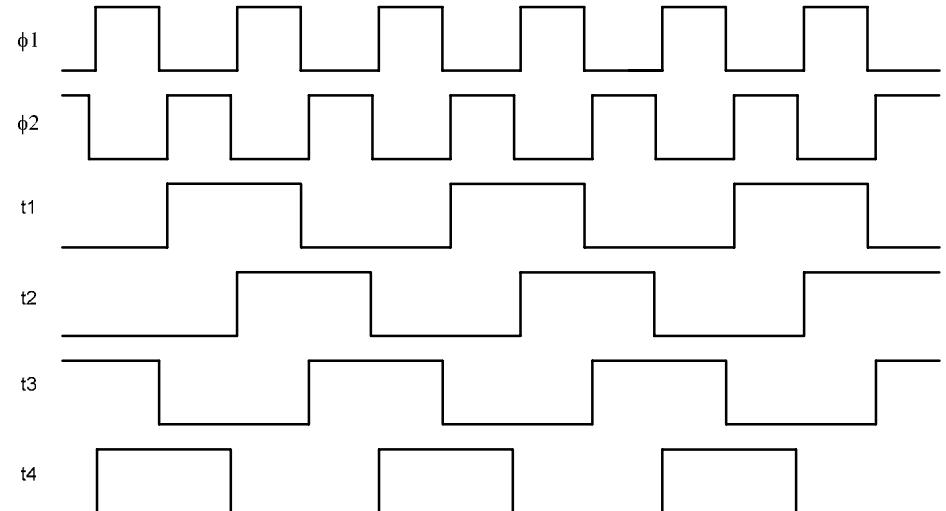
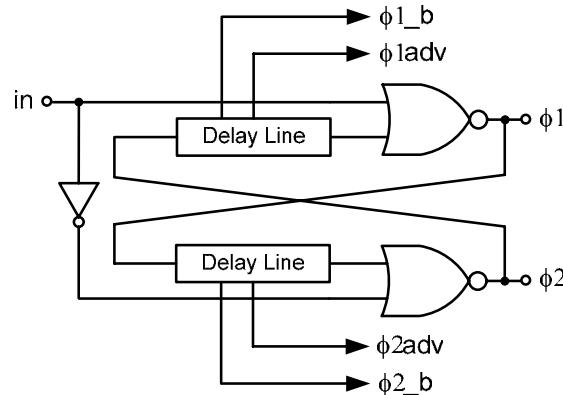
- Only one-ended connection is plotted
 - Compensation capacitors
 - ➡ Cdc1
 - ➡ Cdc2



Implementation

- Clock Generator

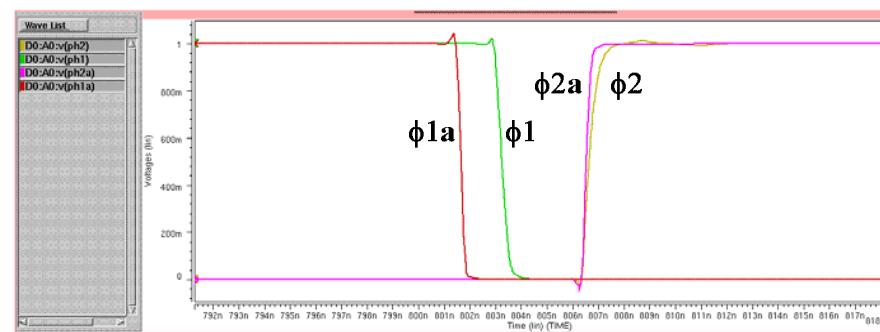
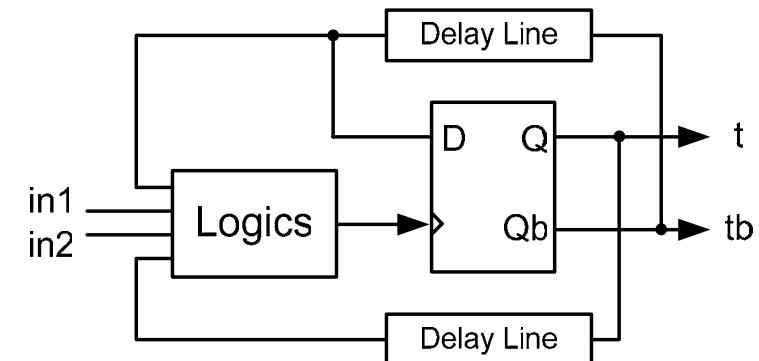
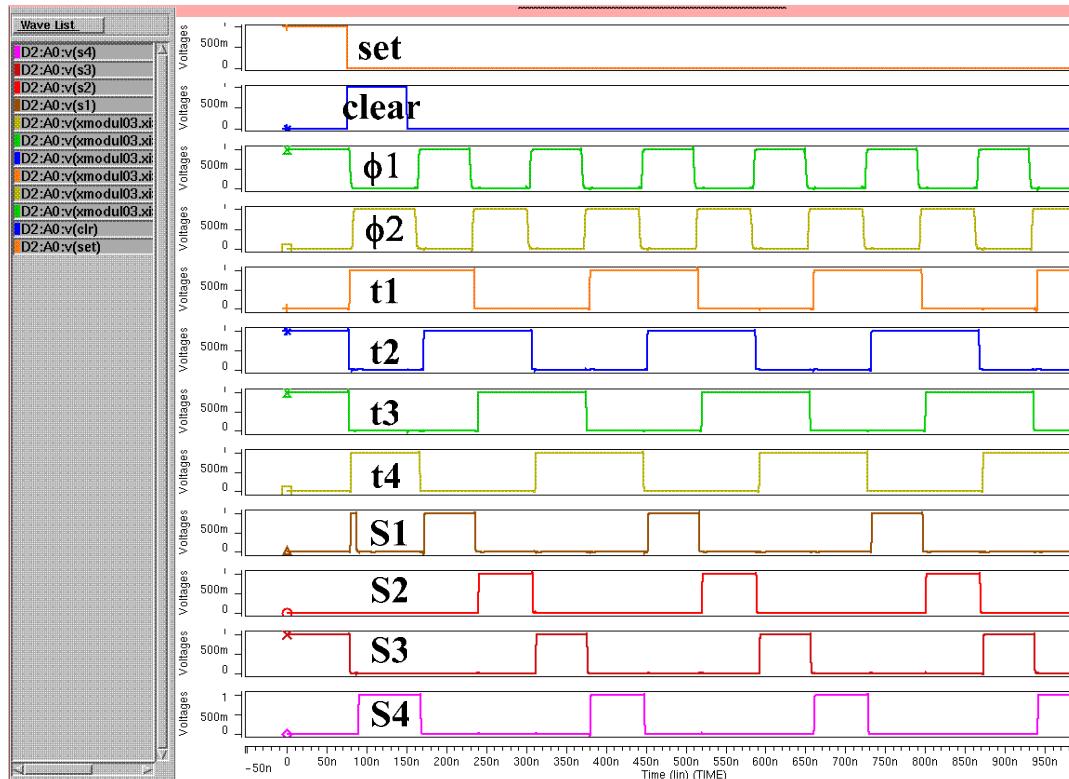
- The nonoverlapping clocks generator
- Dividing-two circuits



Implementation

Clock Generator

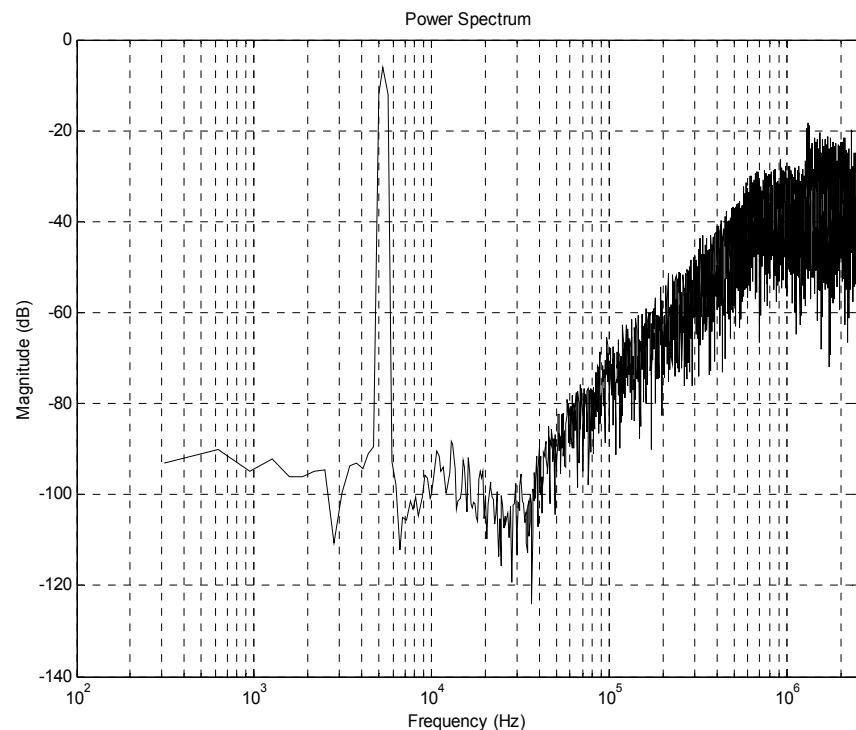
- The nonoverlapping dividing-two circuit
 - Negative-edge triggered logics to avoid spikes



Simulation Results & Chip Photo

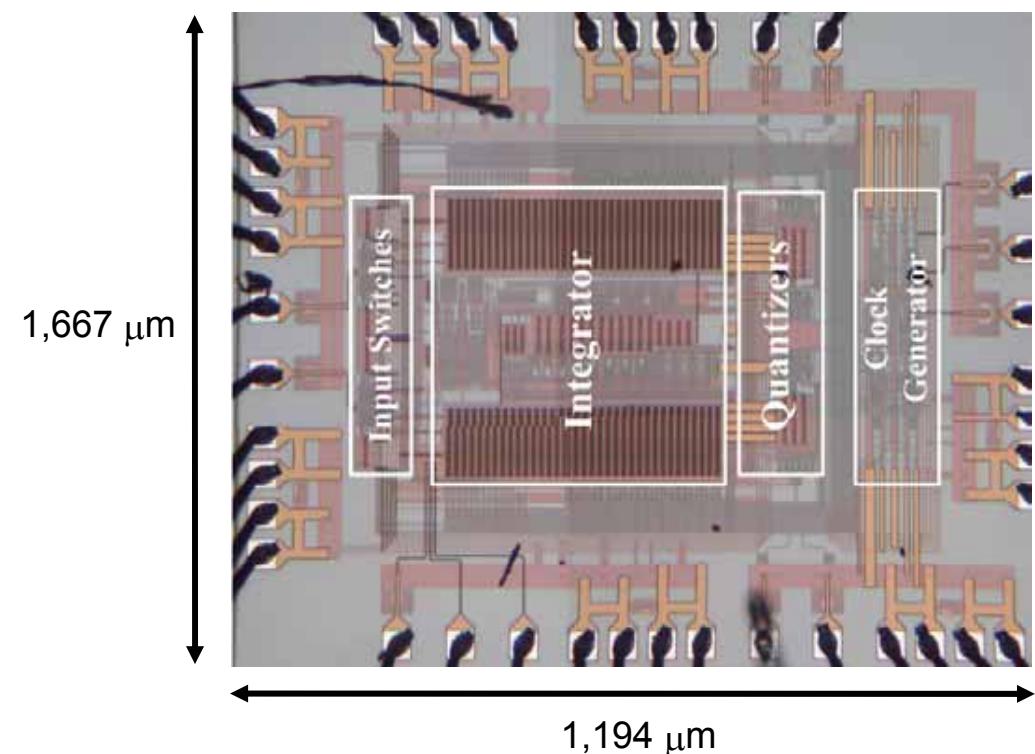
- 16,384-Point FFT

- A = -6dB, fin=5.78125kHz, fs = 2.5MHz
- SNDR = 73 dB for BW=22.05kHz



- 0.25μm CMOS 1P5M MIM process

- Clean guard ring
- Separate V_{DD}, V_{SS}

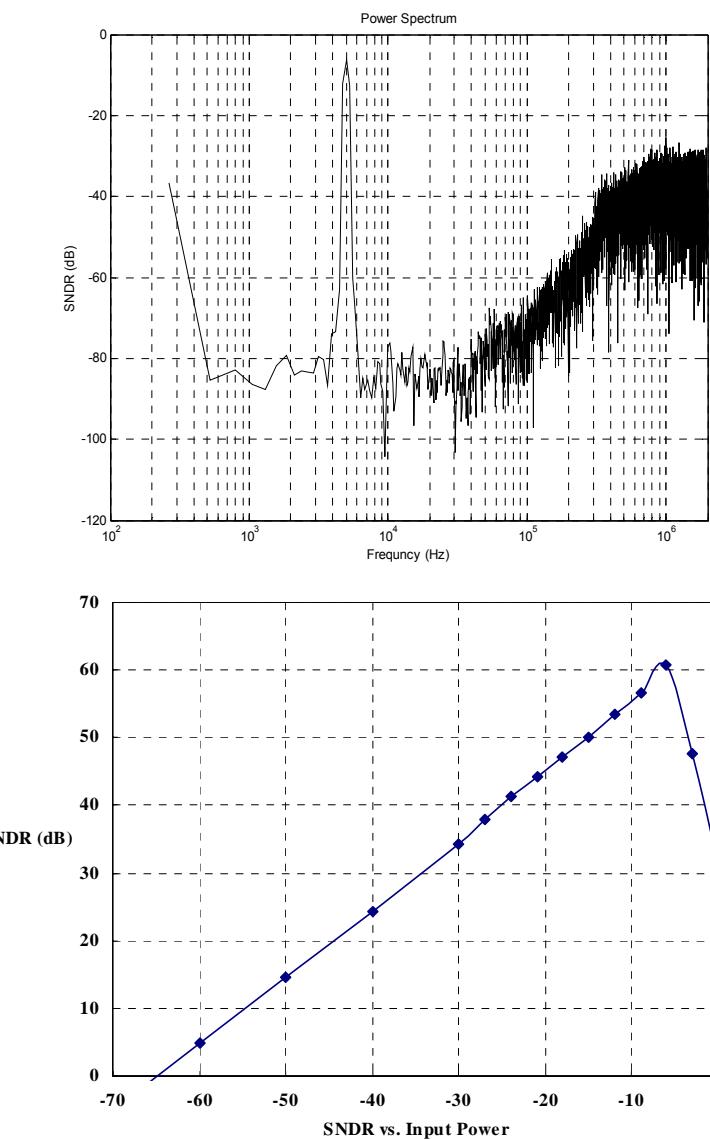


Experimental Results

- 16,384-Point FFT

- A = -6dB, fin = 5kHz, fs = 2.5MHz
- SNDR = 68dB for BW = 22.05kHz
- 7.2mW (V_{DD} = 1V)

Architecture	One-Opamp Second-Order Modulator
Power Supply	1.0V
Input Range	0.5Vp-p
Sampling Rate	2.5MHz
OSR	64
Signal Bandwidth	22.05 kHz
Peak SNDR	60dB
Resolution	10Bits
Dynamic Range	62dB
Power Dissipation	7.2mW
Active Area	1,667×1,194 μm^2
Process	0.25 μm 1P5M MIM standard process



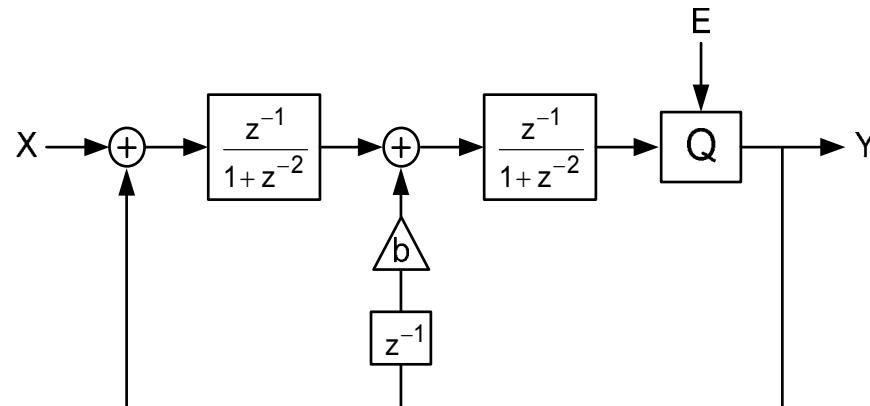
Outline

1. Introduction
2. Low Voltage Circuits for Delta Sigma Modulator
3. Low Voltage Nested-Chopper Delta Sigma Modulator
4. Low Voltage Second-Order Delta Sigma Modulator Using a Single Opamp
5. Low Voltage Fourth-Order Bandpass Delta Sigma Modulator
 - System Considerations
 - Implementation
 - Simulation & Experimental Results



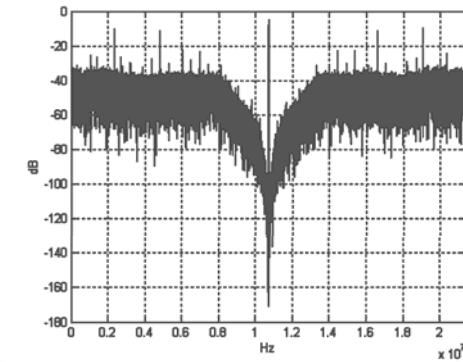
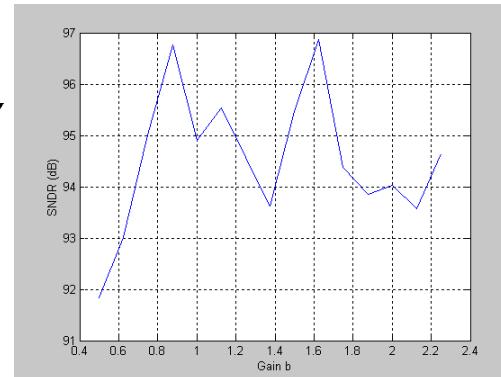
System Considerations

- Block Diagram of a Fourth-Order Bandpass $\Delta\Sigma$ Modulator



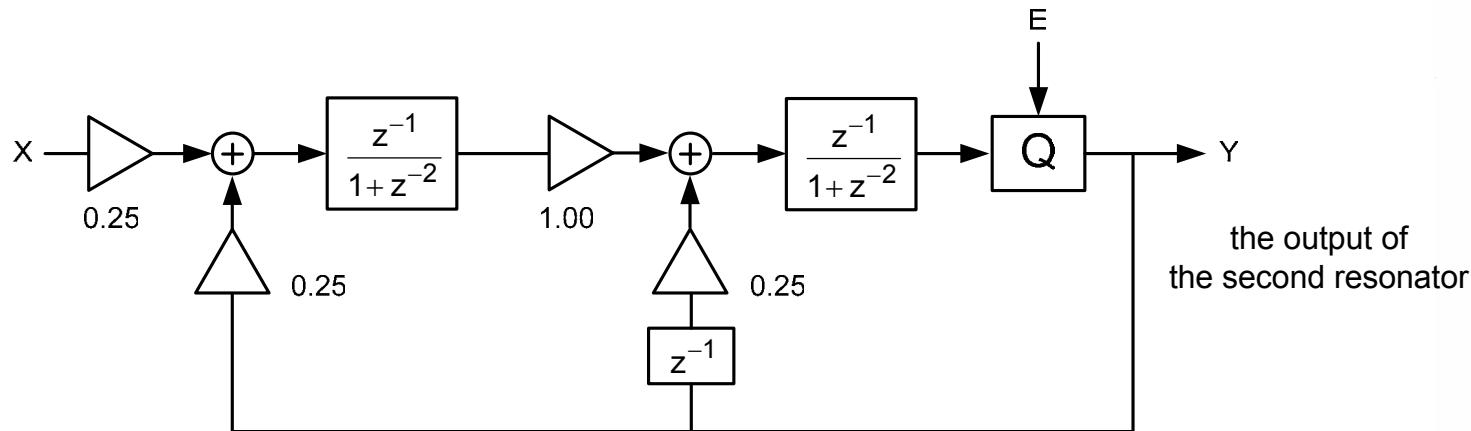
for $b = 1$

$$Y(z) = X(z) \cdot z^{-2} + E(z) \cdot (1 + z^{-2})^2$$

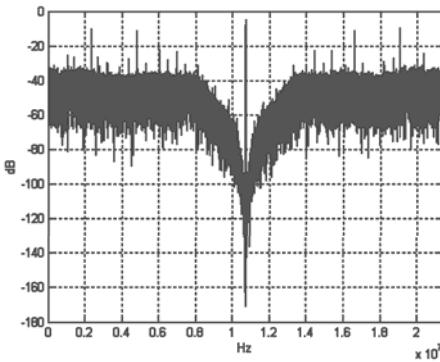
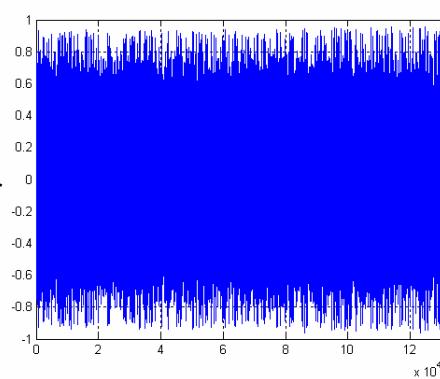


the output of
the first resonator

- Coefficients Scaling



the output of
the second resonator



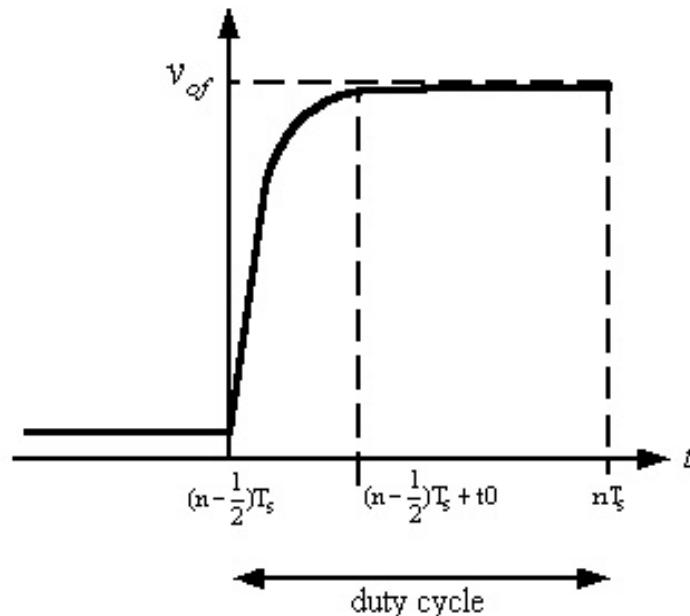
System Considerations

- Sampling Frequency

- $f_s = 42.8\text{MHz}$

- Settling

- 1/3 duty cycle



$$\left\{ \begin{array}{l} f_s = 42.8\text{MHz} \\ t_0 = \frac{T_s/2}{3} = 3.894\text{ns} \\ 1 - e^{-t_0/\tau_{amp}} = 99.9\% \end{array} \right.$$

$$\rightarrow \tau_{amp} = 1.1275\text{ ns}$$

Unit-gain frequency

$$\rightarrow A_0 f_0 = \frac{(1.875)/1.1275\text{ns}}{2\pi} = 529.36\text{MHz}$$

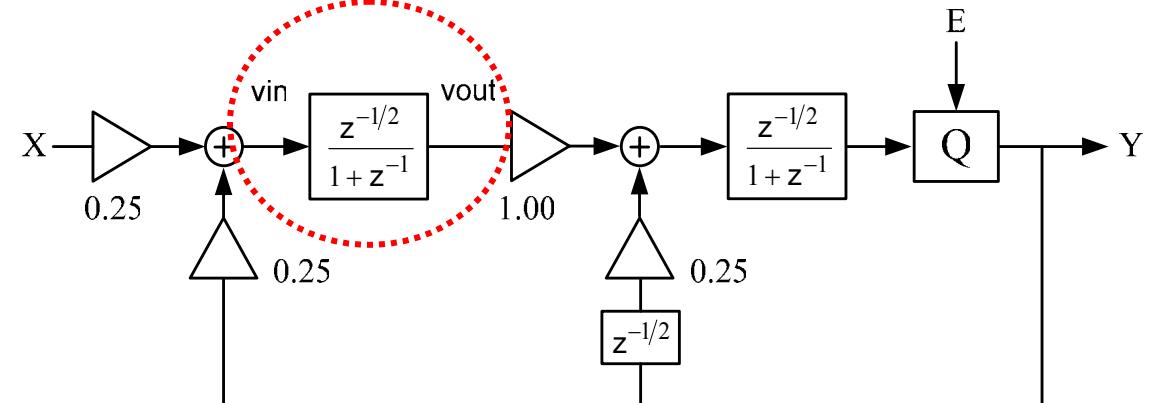
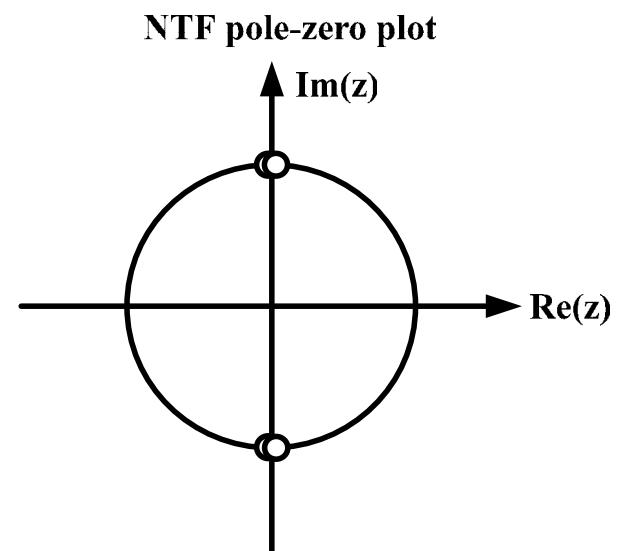
Double Sampling is applied (264.68MHz)

The unit-gain frequency is too high to be accepted

System Considerations

- Sampling Frequency

- Signal frequency = 10.7MHz (fs/4)
- Set 10.7MHz = 3/4 *fs \rightarrow fs = 14.26MHz
- Double sampling \rightarrow fs = 7.13MHz



$$Y = X \cdot z^{-2} + E \cdot (1+z^{-2})^2$$
$$\Rightarrow NTF = \frac{Y}{E} = (1+z^{-2})^2$$

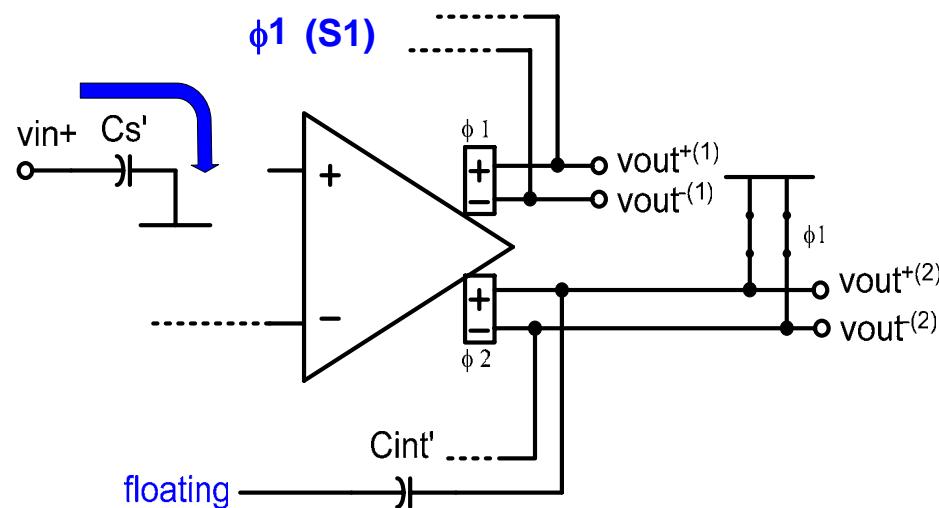
Implementation

- The First Resonator

- Function

$$\frac{v_{out}(z)}{v_{in}(z)} = \frac{z^{-1/2}}{1+z^{-1}} \Rightarrow v_{out}(z) = z^{-1/2} \cdot v_{in}(z) - z^{-1} \cdot v_{out}(z)$$

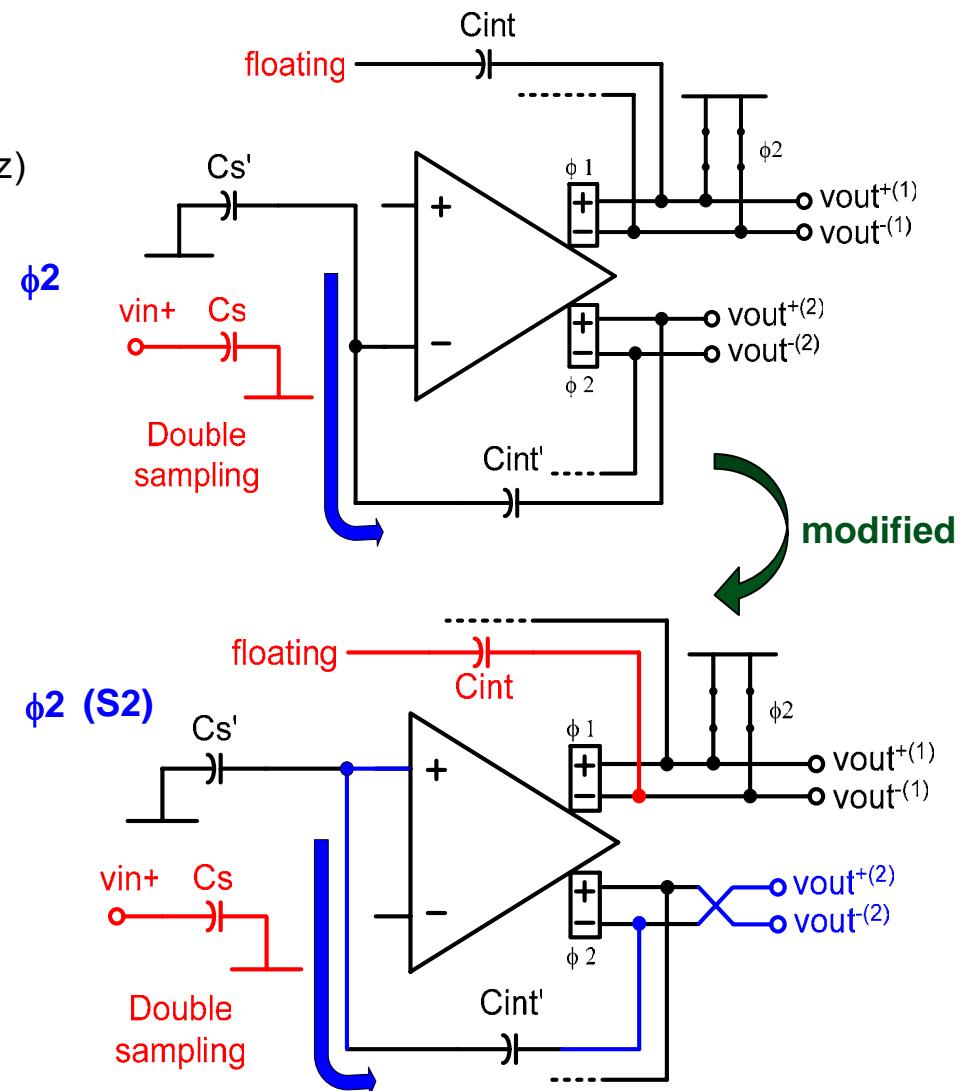
- The first term $z^{-1/2} \cdot v_{in}(z)$



- The second term $-z^{-1} \cdot v_{out}(z)$

$\rightarrow -z^{-1}v_{out}(z) = +z^{-1}v_{out}(z)$

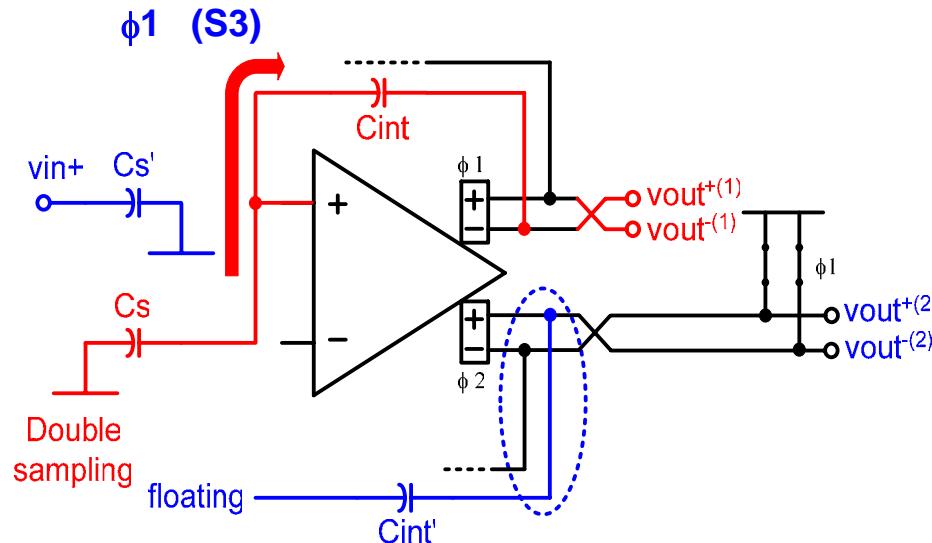
- Positive input sample \Rightarrow the negative output



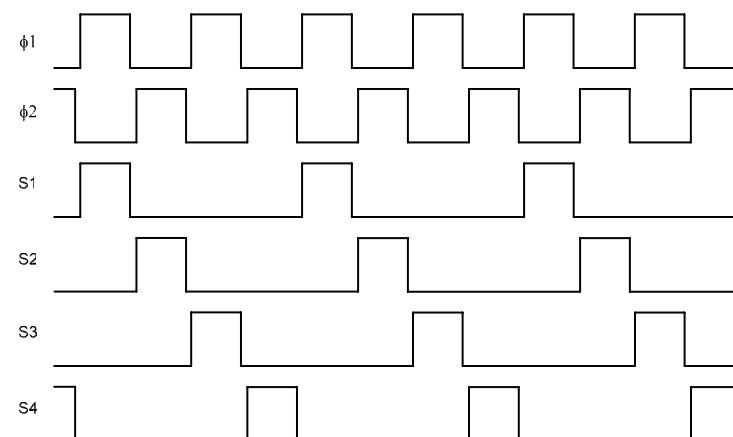
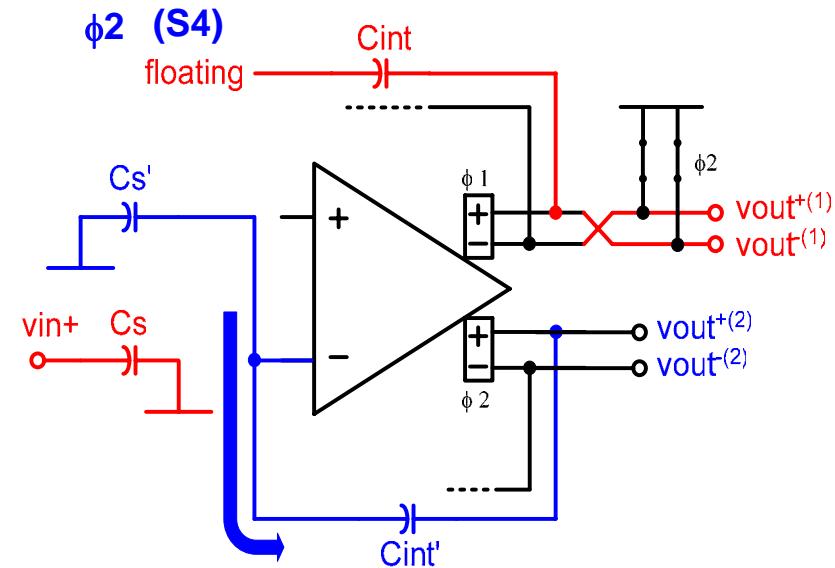
Implementation

- The First Resonator

- The succeeding phases



- four phases (S1, S2, S3, and S4)

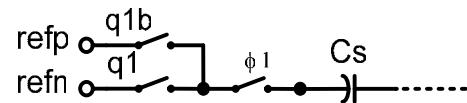
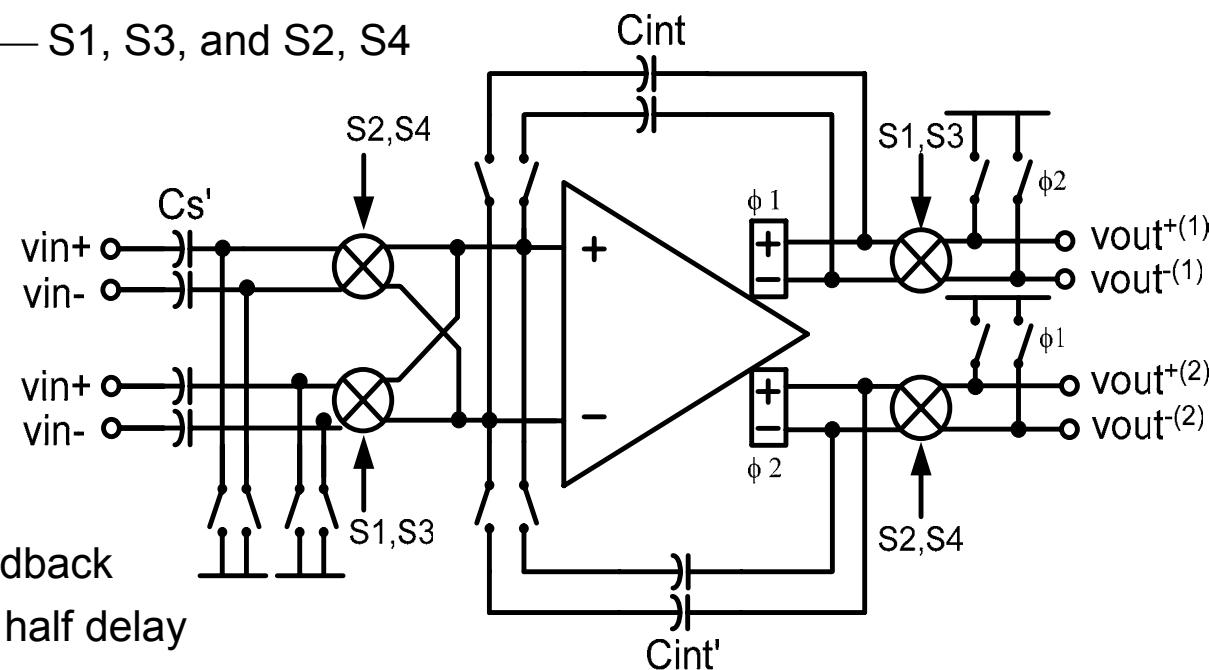


Implementation

- The First Resonator

- Input — positive, negative
- Opamp — negative feedback
- Input Chopper — S2, S4, and S1, S3
- Output Chopper — S1, S3, and S2, S4

- Positive DAC feedback
 - Quantizer — half delay
 - no DC compensation circuit

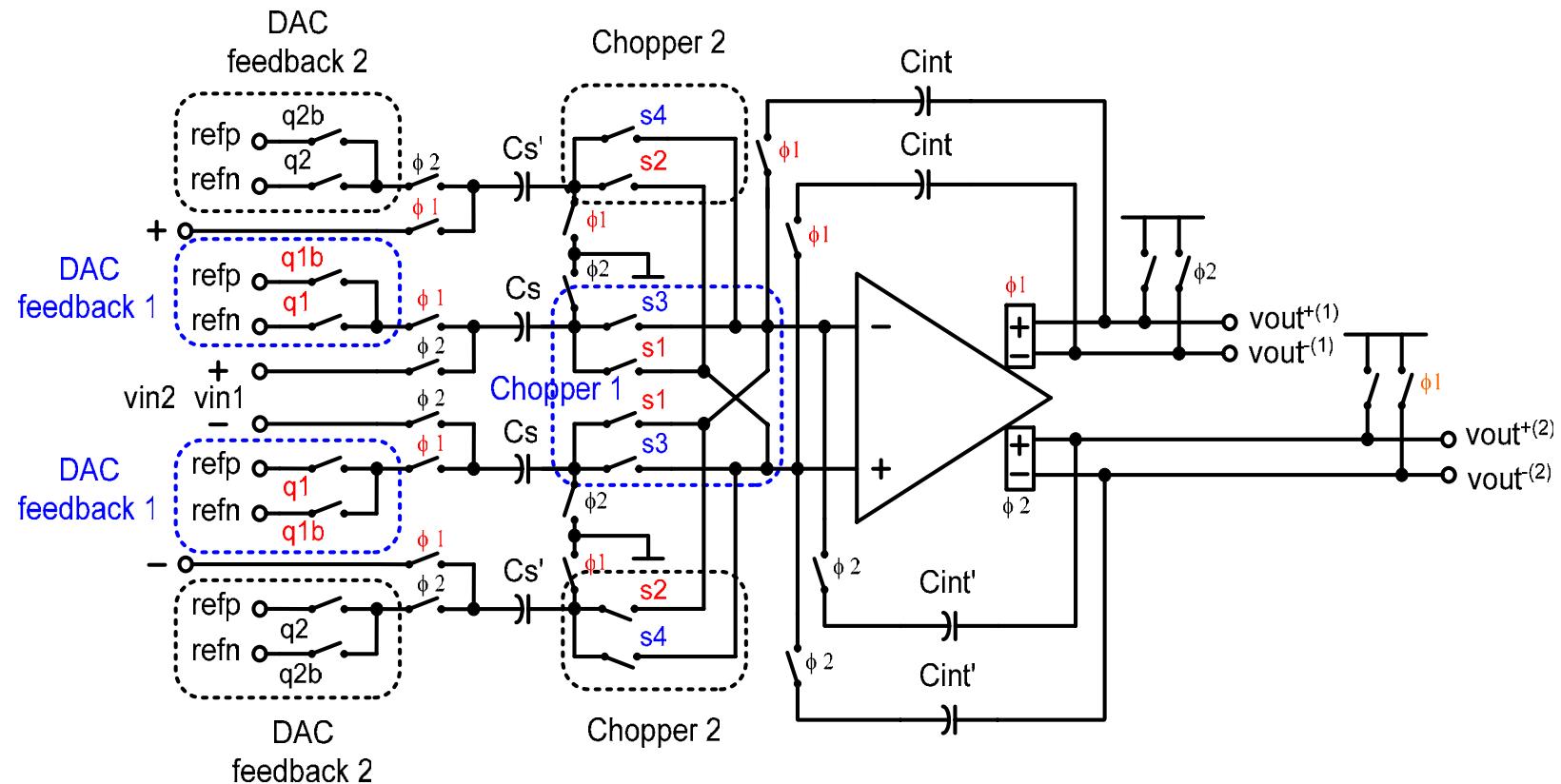


Integration phase

Implementation

The First Resonator

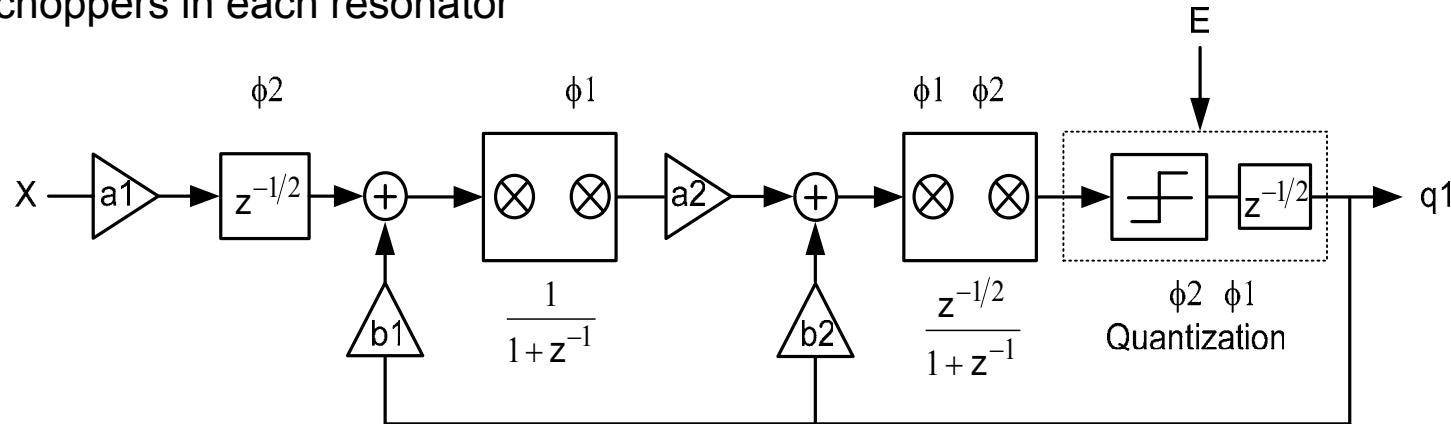
- The chopper at the output of the opamp is omitted



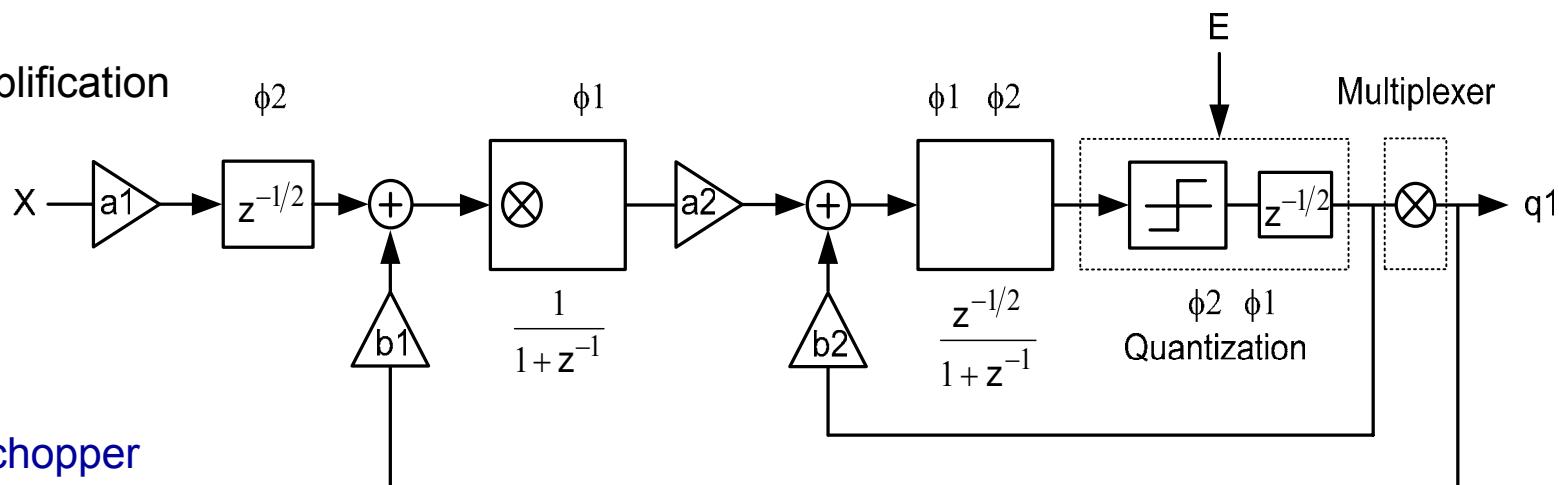
Implementation

- The Combination of the Choppers

- Two choppers in each resonator



- Simplification



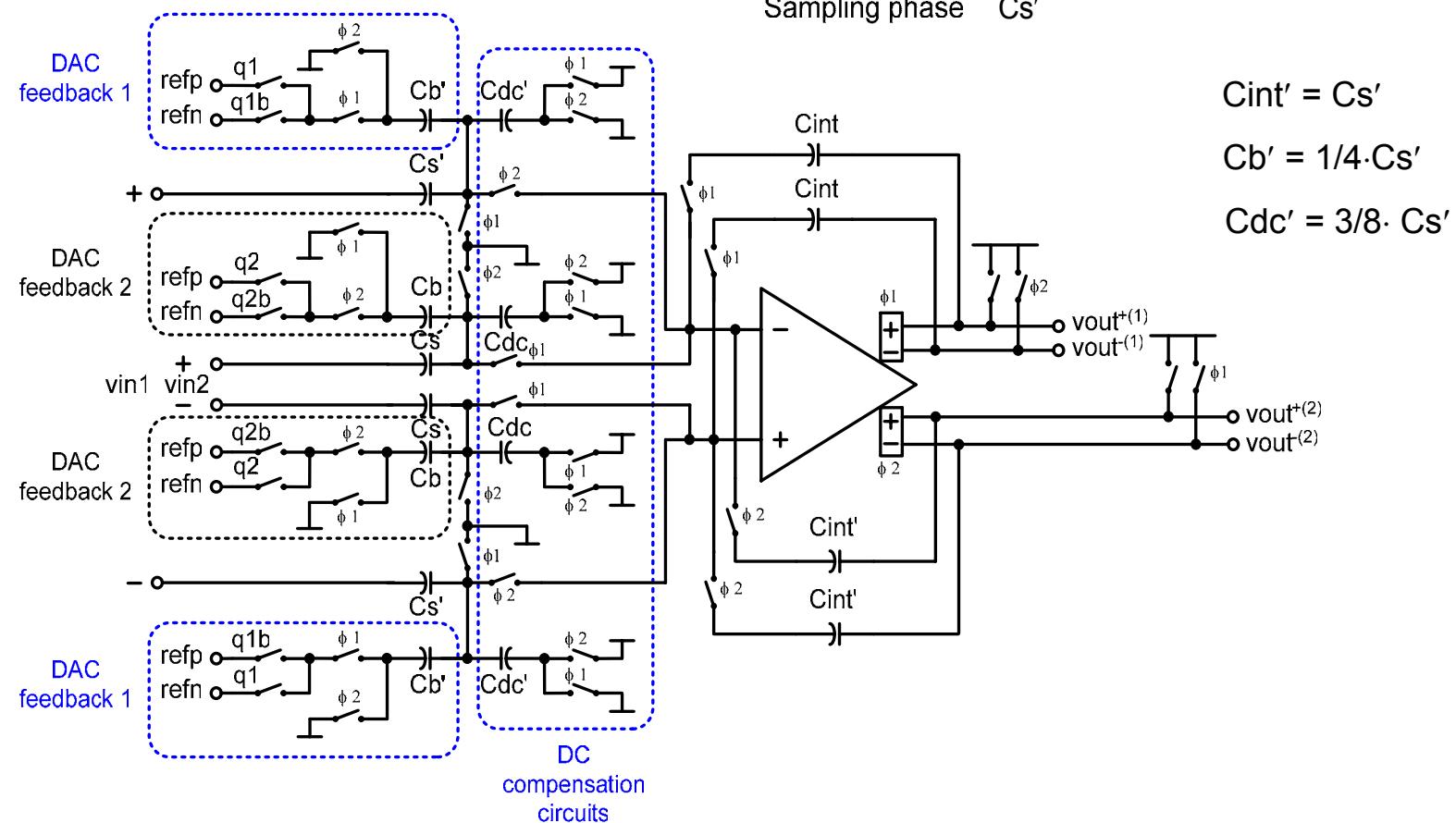
- No chopper

- DAC feedback

► The outputs of the first resonator will be pulled high in the integrating phase

Implementation

- The Second Resonator
 - Positive DAC feedback
 - DC compensation circuits



Implementation

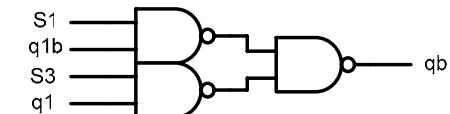
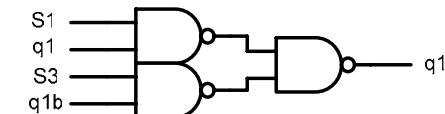
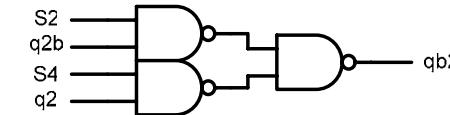
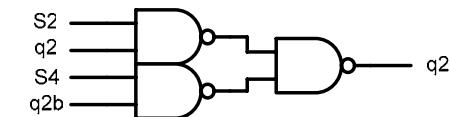
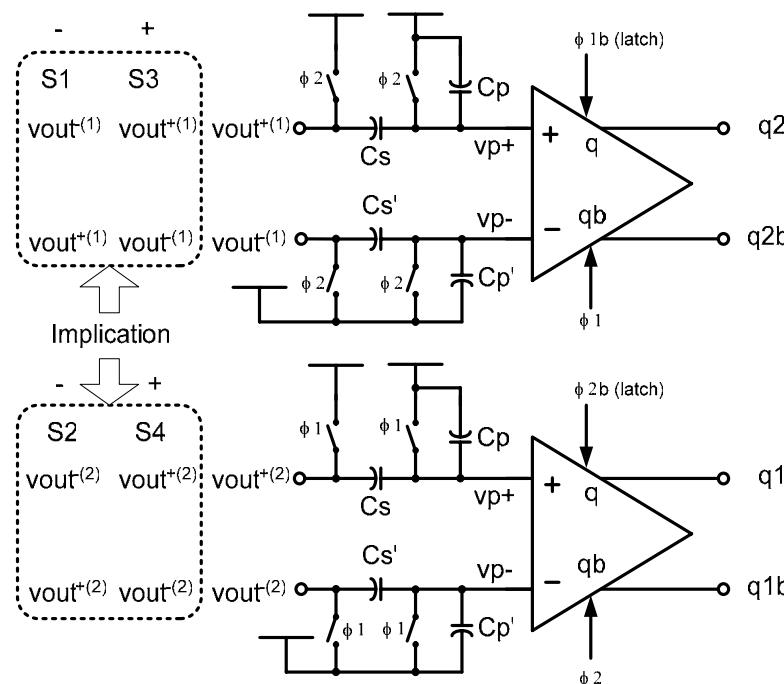
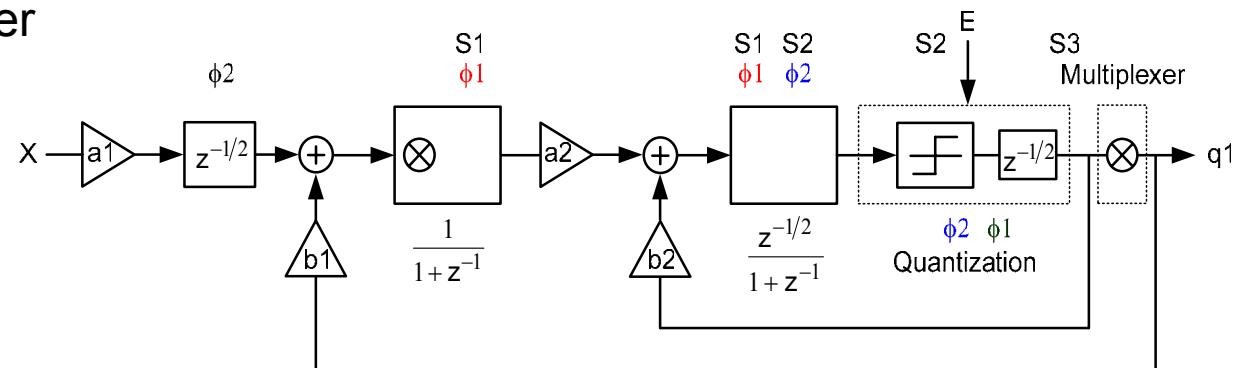
- The Quantizers and Multiplexer

- Chopper

Integrated & sampled

- Integrated & Compared

- Latched



$$q1' = S3 \cdot q1b + S1 \cdot q1$$

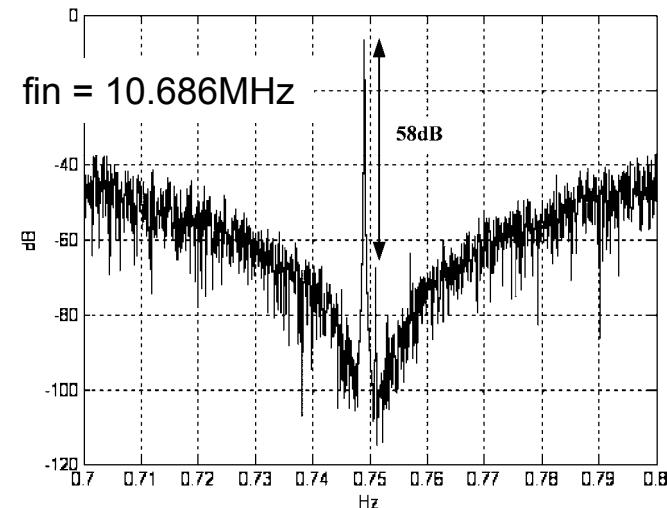
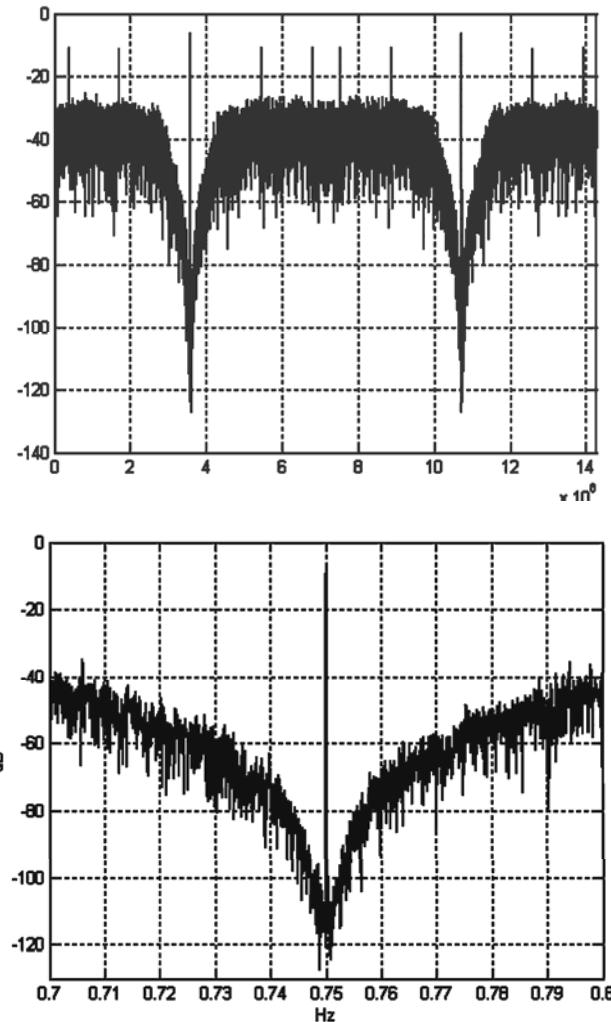
$$q1b' = S3 \cdot q1 + S1 \cdot q1b$$

$$q2' = S2 \cdot q2 + S4 \cdot q2b$$

$$q2b' = S2 \cdot q2b + S4 \cdot q2$$

Simulation Results

- 32,768-Point FFT ($v_{in}=0.125V$)

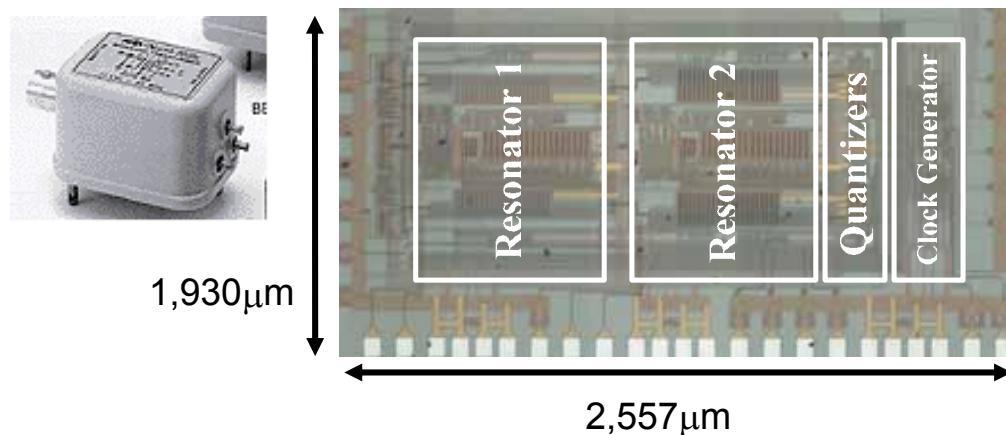


fin = 10.7MHz		
Supply Voltage V_{DD}	1V	
Reference Vref+	0.75V	
Reference Vref-	0.25V	
Sampling frequency f_s	7.13 MHz	
$\text{SNDR}_{\text{peak}}$	200kHz	60.33 dB
	100kHz	76.40dB
	30kHz	90.42dB
Image tone		58 dBc

Experimental Results

● Experimental Test Setup

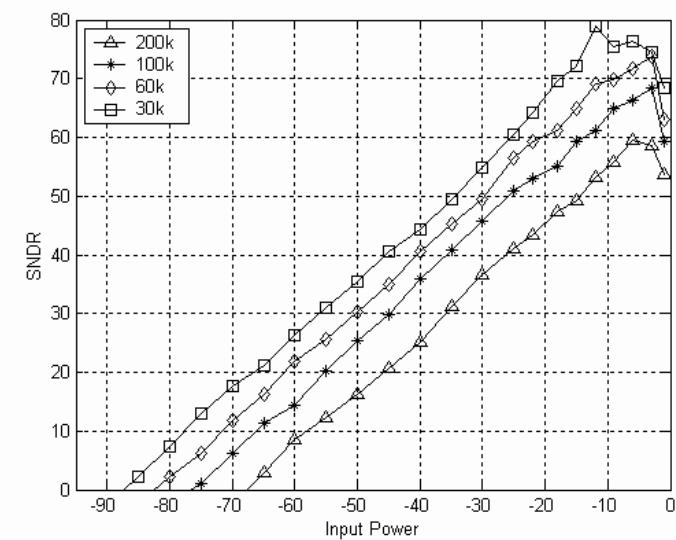
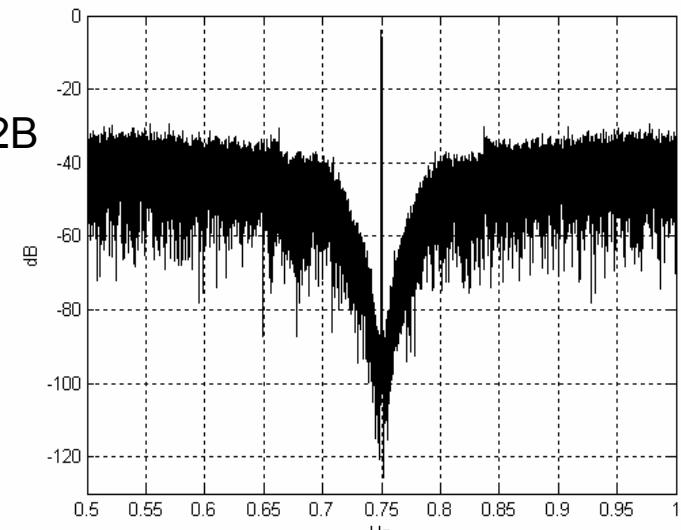
- Power — Isolation
- Signal generator — ESG Series Signal Generator E4422B
 - balun (Single \Rightarrow Differential)



● 65,535-Point FFT

- $A = -6\text{dB}$
- $f_{in} = (3/2) \times fs$ ($f_{in} = 10.7\text{MHz}$, $fs = 7.13\text{MHz}$)
- Power = 8.45mW ($V_{DD} = 1\text{V}$)

BW	200kHz	100kHz	60kHz	30kHz
SNDR	58.52dB	68.39dB	73.73dB	76.47dB
DR	62dB	74dB	79dB	82dB



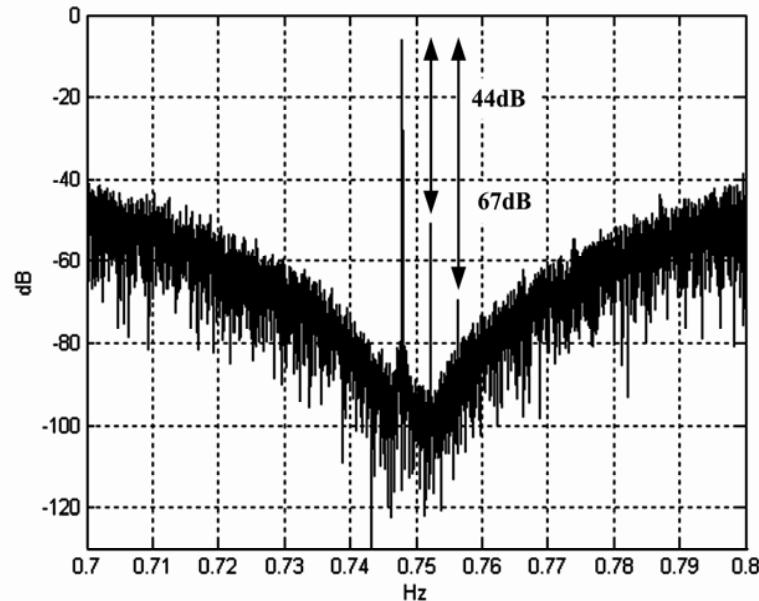
Experimental Results

- Image Tone Test

 - 0.748fs

 - ➡ Image -44dB

 - ➡ The third harmonic -67dB

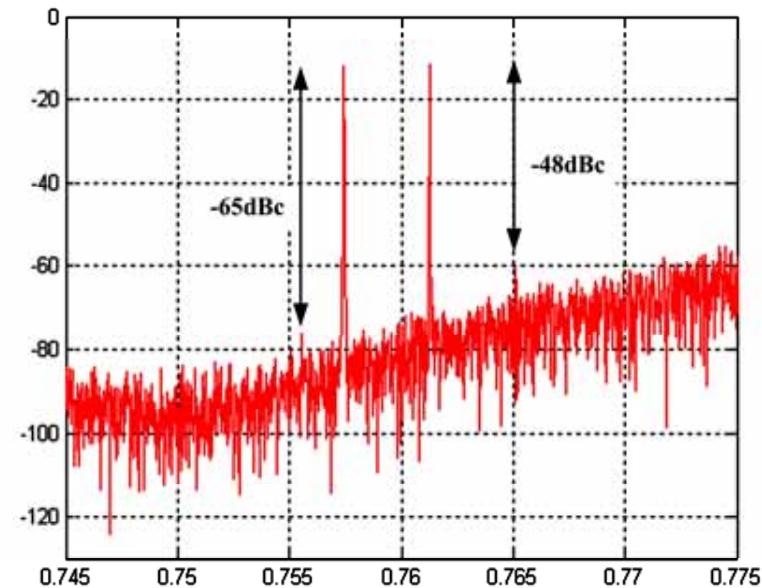


- Two-Tone Test

 - Two signals — 0.7578fs and 0.7615fs

 - Two tones — 0.7541fs and 0.7652fs

 - ➡ -65dBc in band



Summary

	This circuit	Vincent [67]	A. Baschirotto [53]	P. Cusinato [68]	J.A. E.P.van Engelen [69]	L. Louis [70]
Technology	CMOS 0.25um	CMOS 0.35um	CMOS 0.5um	CMOS 0.35um	CMOS 0.5um	BiCMOS0.8um
Power Supply	1V	1V	1V	3.3V	5V(A) 3.3V(D)	± 2.5V
Order	Fourth	Fourth	Fourth	sixth	sixth	eighth
Sampling frequency	7.13 MHz	42.8 MHz	1.8 MHz	42.8 MHz 14.27MHz	40 MHz	14.3 MHz
Center frequency	10.7 MHz	10.7 MHz	400 kHz	10.7 MHz	10.7MHz	10.7MHz
Band Width	200kHz	200kHz	20kHz	200kHz 9 kHz	200kHz 9 kHz	200kHz
Signal Swing	0.5 Vp-p	-	2 Vp-p	4.4 V(diff.)	0.2 Vp-p	± 1.5 V
Peak SNDR	59.52dB	42.3 dB	42 dB	61 dB 65 dB	63.5 dB 76 dB	59 dB
Dynamic Range	68 dB	-	45 dB	74 dB 76 dB	67 dB 81 dB	67 dB
IP3	60 dBc	-	-	-	75 dBc	-
Area (mm²)	3.233	1.3	0.18	1	-	2.89
Power (mW)	8.45	12	0.24	76	66	60
						157

[67] Vincent S. L. Cheung, Howard C. Luong, and Wing-Hung Ki, “A 1-V 10.7-MHz switched-opamp bandpass Sigma Delta modulator using double-sampling finite-gain-compensation technique”, IEEE J. Solid-State Circuits, vol. 37 No. 10, Oct. 2002.

[53] A. Baschirotto, and R. Castello, “Low-voltage fully differential switched-opamp bandpass Sigma Delta modulator”, IEE Pro. Circuits Devices System, vol. 146, No. 5, Oct. 1999.

[68] P. Cusinato, D. Tonietto, F. Stefani, and A. Baschirotto, “A 3.3-V CMOS 10.7-MHz sixth-order bandpass Sigma Delta modulator with 74-dB dynamic range”, IEEE J. SSC, vol. 36, No. 4, Apr. 2001

[69] J.A. E. P. van Engelen, R. J. van de Plassche, E. Stikvoort, and A. G. Venes, “A sixth-order continuous-time bandpass sigma-delta modulator for digital radio IF”, IEEE J. SSC, vol. 34, No. 12, Dec. 1999.

[70] L. Louis, J. Abcarian, and G. W. Roberts, “An eighth-order bandpass spl Delta spl Sigma modulator for AD conversion in digital radio”, IEEE J. Solid-State Circuits, vol. 34 No. 4, April 1999.

