Jiajun ZHOU (Thomas)

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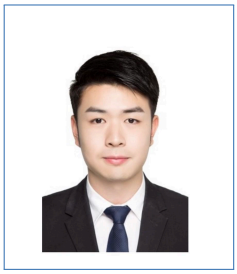

Education

2022–2025 **The University of Hong Kong**, *Ph.D.*, EEE, Supervisor: Prof. Ngai Wong

2018–2019 **The Hong Kong University of Science and Technology**, *M.Sc.*, IC Design Engineering,

2017 **Yuan Ze University**, *B.Sc.*, Electrical Engineering, *EE Exchange Student*

2014–2018 **National Huaqiao University**, *B.Sc.*, Integrated Circuit Design and Integrated System, *B.E.*

Experience

2021.04-12 **Research Assistant**, *Aiot Lab, CUHK*, Research Focusing on NFC-Wireless Charging System design and FPGA prototyping,

2021.09–12 **Research Principal Engineer**, *ThingX Technologies Limited Company*, The development and design of embedded software/hardware systems, *HKSTP*

2019–2021 **Mixed-signal IC Engineer**, *Technology Co-Design Group, Hong Kong Applied Science and Technology Research Institute*, Participated in industry projects and Hong Kong government-fund projects, and the delivery of high performance, high quality, on-time IP spanning all aspects of silicon design. Mixed-signal architecture selection for optimum performance and ADC architecture selection for optimum system performance,

RESEARCH EXPERIENCE

Hardware Acceleration for AI at the Edge, *Jan 2021 - Now*, HKU EEE

Focus on hardware-aware algorithmic techniques for high-performance machine learning and edge AI accelerators, such as FPGA. Research topics: 1). Sparse and fast linear transform DNNs. A distinct ingredient in my research work is the strong presence of analytical components and their translation into a practical realization of compact hardware-friendly DNNs by the blooming era of edge AI. A revamped design of the linear transform and a regularized hardware architecture. This task targets a field-programmable gate array (FPGA) realization of dedicated NN chains. Vivado high-level synthesis (HLS) tools to compile algorithmic descriptions (e.g., C/C++, Python) to RTL designs for quick ASIC or FPGA implementation of hardware accelerators. Furthermore, an ASIC can be designed to achieve this research goal. 2). Heterogeneous distributed platform: research on an FPGA/ASIC-accelerated heterogeneous architecture provides resource management and programming support for computing-intensive applications. We need to further find a way to the interdependence among these different customization techniques on several hardware architectures(CPU/GPU/ASIC/FPGA), allowing designers to balance various performance/area/accuracy trade-offs.

FPGA-GPU-CPU Embedded Heterogeneous Platform, *Aug 2021 - Dec 2022*, CUHK Aiot Lab

Research on a hybrid FPGA-GPU/CPU DL acceleration method and demonstrate that heterogeneous acceleration outperforms GPU/CPU acceleration. This platform through joint optimization of DNN model scaling and real-time scheduling.

NFC Wireless Charging System, *Apr 2021 - Present*, CUHK Aiot Lab

The system enables devices to communicate with neighboring devices and to transfer power from WLC-P to WLC-L. Antenna and Frontend Design: Antenna design working at a frequency of 13.56 MHz. (ISO/IEC 14443, ISO/IEC 15693, ISO/IEC 18092, ISO/IEC 21481, ISO/IEC 18000-3, NFC Forum standards) and used in different form factors like smartcards, tags, fobs, wearables, earbuds, and gaming devices. Additionally, it needs to cover antenna design for NFC readers and wireless charging.

2MHz 10 bits Vcm-based SAR ADC Design, *Oct 2019 - Mar 2021*, ASTRI Project

Work with chip leads to develop detailed and prioritized chip-level design and layout workflow, and we use a Vcm-based bottom-plate sampling and reference scaling method to reduce the effect of mismatch. Design and develop complex CMOS analog circuits such as reference generators, clocks, comparators, amplifiers, and data converters. Built an ADC evaluation platform to test the performance of ADC. The fabricated ADC chip runs at a sampling frequency of 2.024 MHz and reaches an ENOB of 9.07 and SNR = 56.3dB. INL = +-0.93LSB/ DNL=-0.73/+0.82 LSB. The project is utilizing 110nm CSMC.(Tape-out)

Analog Front-end design for IR sensor, *Aug 2020 - Mar 2021*, ASTRI Project

Research on PGA, SDM ADC, and PMU. Mainly focus on 16bits 2-order CT Sigma-Delta ADC design and high PSRR LDO.

High speed interface platform : MIPI D-PHY, *Feb 2020 - Sep 2020*, ASTRI Project

Core design: built Verilog model including differential HS functions (HS-TX and HS-RX), single-ended LP functions (LP-TXs and LP-RXs), and LP contention detectors (LP-CD), serializer, deserializer. This project presented a MIPI D-PHY analog part that meets the MIPI standard and supports HS and LP modes. PMU: implemented a fast response LDO with 10pF output capacitance and the load regulation is 15.4mV/mA at 500mV output voltage with 1.2V supply. The LDO is simulated with TSMC 130nm process and used to supply the drive of HS TX.

HONORS AND AWARDS

IBM Data Science - non-credit Professional Certificate (Code:XPX7R62L4DCS)), *April 2020*

Excellent Prize of Course Implement Competition in Yuan Ze University, Design and Implementation of IPv6 SOHO Network Gateway for Internet of Things, *Jun 2017*

1nd Scholarship of College of Information Science and Engineering in HQU, *Sep 2017*

2nd Scholarship of College of Information Science and Engineering in HQU, *Dec 2016*

Computer Skills

MATLAB

Simulink

Vivado

Python, C/C++

Cadence

Linux