FPGA Countdown Timer

Functionality

Countdown timer takes in a 6 bit input as decimal and decrements the time

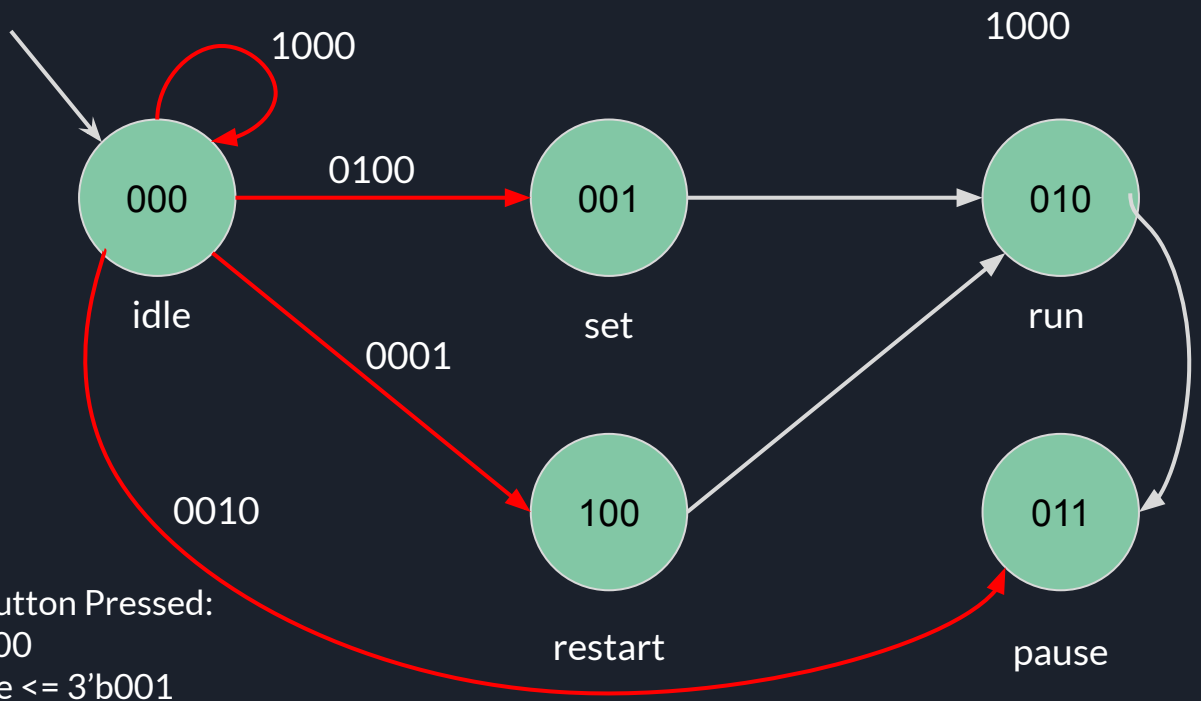
Reset: stops all timers and takes in input from switches and displays on SSD

Start/Continue: starts or continues the timer based on the initial input

Pause: pauses or stops the input and if timer is reached, blinks LED

Restart: restarts timer and continues the countdown until reaches zero.

State Diagram



NS Dependent On Button Pressed:

- Reset <= 3'b000
- Start/Continue <= 3'b001
- Pause <= 3'b011
- Restart <= 3'b100

*Note : [3:0] Inputs = {reset, start, pause, restart}

*Not Shown: Each state has 4 connections dependent on button pressed

States and what they do

Idle: Takes in input and displays on SSD but does nothing else. (Reset input)

Set: Takes current input ONLY and initializes it to register (Start_con input)

Run: Decrements value by one every posedge of a clock (set and restart state)

Pause: Blinks LED if register is empty, if not does nothing (Pause input)

Restart: Sets register to initial value (Restart input)

*Note: To start a timer for a new input, state must be set to Idle first

Problems & How We Fixed Them

- Toggling Between Restart and Run State
- Setting value of next_state in two always blocks
- SSD implementation
- Binary to BCD conversion
- Clock cycle of the SSD was too fast
- Code working in Vivado but not on the FPGA


Thank you for
listening!