# CNT-TFT Compact Model User Manual

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## Model Setup

- Environment and File Required: Linux Cadence 6.15 or New, CNT_Sim.tar
- Import the Library:
  - 1. Extract the file: *tar –xvf CNT_TFT_Verilog_A.tar*
  - 2. Add to your Library Path: *vim cds.lib* add the lib to your path as shown in Fig 1. After importing, you should be able to access the *CNT_Sim* and some Example Cells

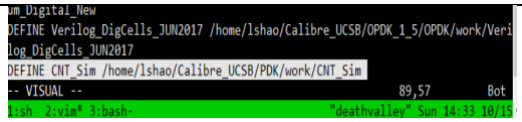


*Figure 1 Add the CNT_Sim to your Library Path. Change the "/home/lshao.." to your work dir*


*Figure 2 CNT_Sim Lib and SubCells*

- Cell : Test_InvD (This is a test cell of Pseudo-D Inverter)
  - Open Test_InvD as shown in Fig 3 and 4.

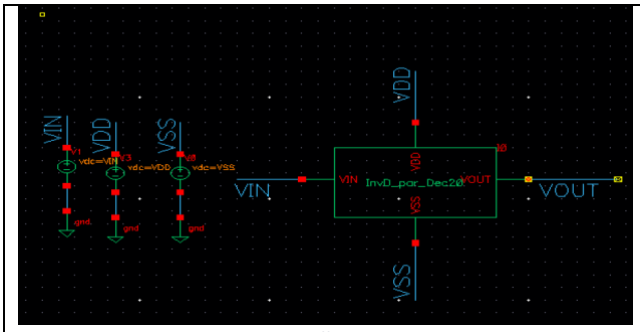


*Figure 3 Cell--Test_InvD*

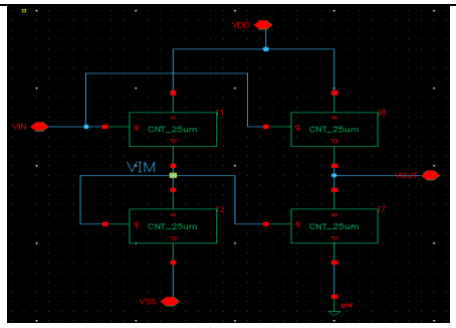


*Figure 4 Decedent into the InvD_par_Dec20*

  - Open ADE and Load the default simulation setting by *Session—Load State*
    - Load the state from the "/your word dir/CNT_Sim/Test_InvD/", and you will see the default simulation setting as shown in Fig 5 and 6.

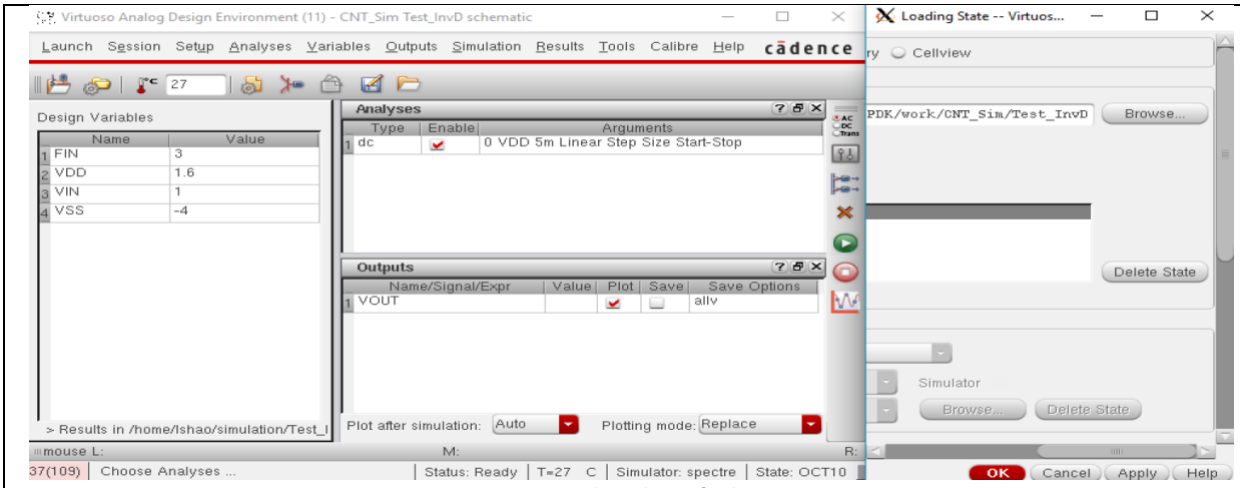


*Figure 5 Loading the Default State*

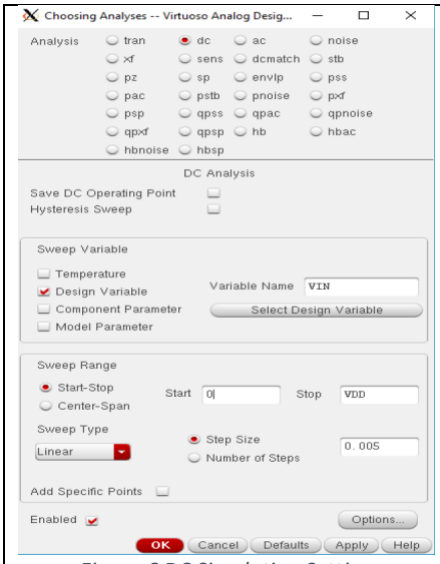


*Figure 6 DC Simulation Setting*

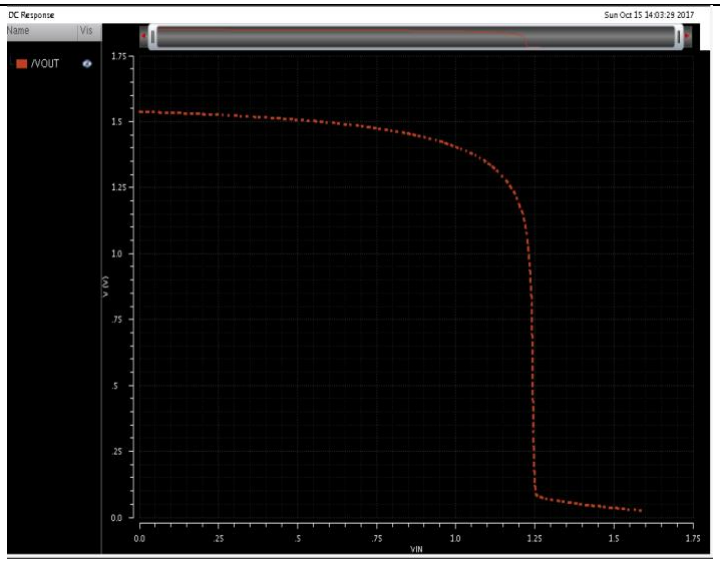


*Figure 7 Expected Simulation Results*

- Cell: Test_RING5 (Test cell of 5 stage ring oscillator)

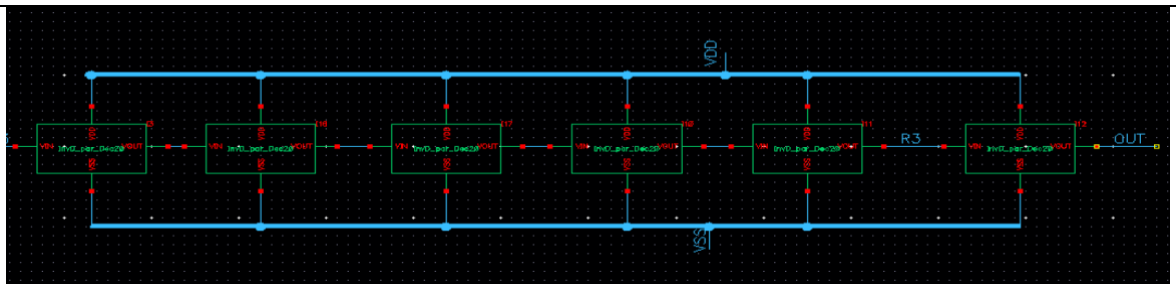


*Figure 8 Schematic of RING5*

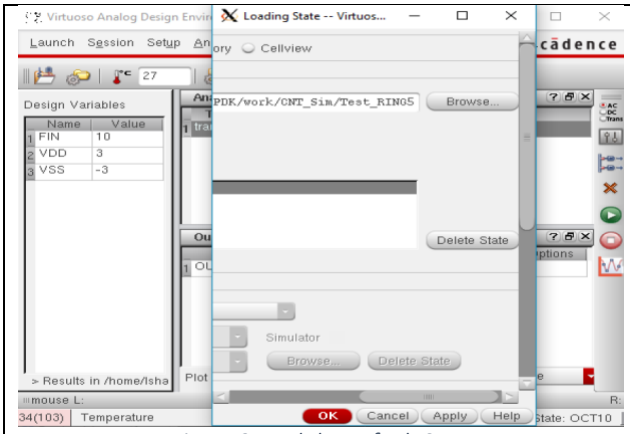


*Figure 9 Load the Default State*

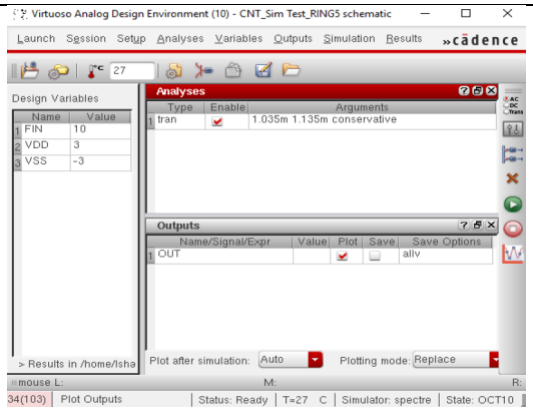


*Figure 10 Default tran simlation*

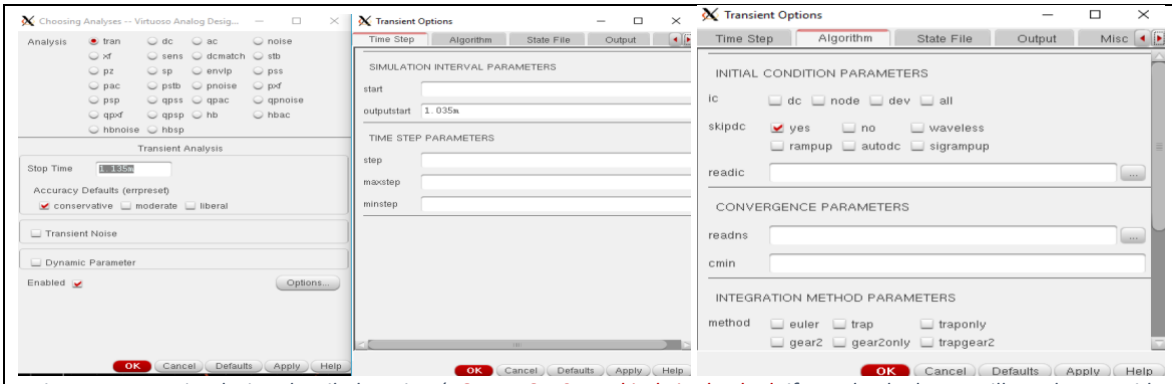


*Figure 11 tran simulation detailed setting (TO BE NOTICED: skipdc is checked, if not checked, you will need to provide a appropriate initial state of the RING5.)*

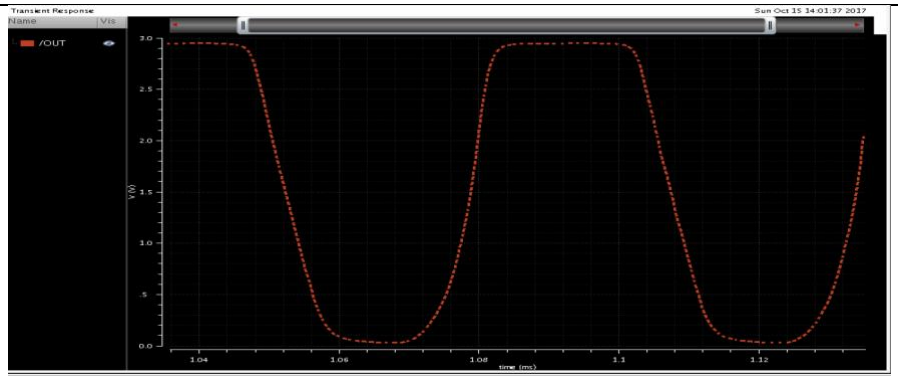


*Figure 12 Expected Waveform*

## Summary

Current model may exist some convergence problems especially for transient simulations. The gate capacitor model is based on Mayer's Cap Model, so may exist discrepancies with real devices

Ref: L. Shao, Huang, T. - C., Lei, T., Bao, Z., Beausoleil, R., and Cheng, K. - T., "Compact Modeling of Carbon Nanotube Thin Film Transistors for Flexible Circuit Design", in *Design, Automation and Test in Europe (DATE)*, Dresden, Germany, 2018.