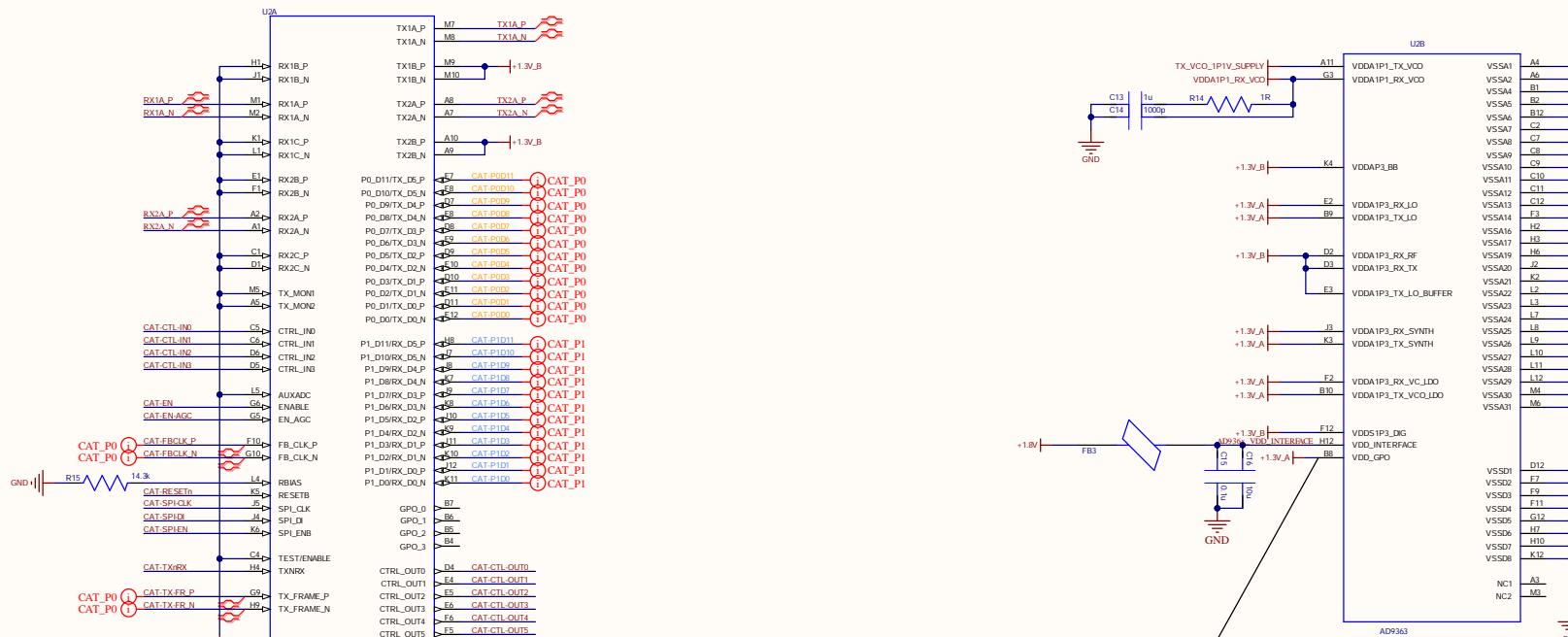
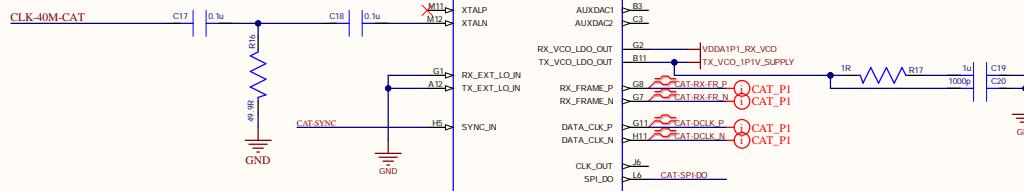


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Size A4	Number
Date:	7/09/2024
File:	C:\Users\..\ACCESSORIESPARTSSchD\DashBv:

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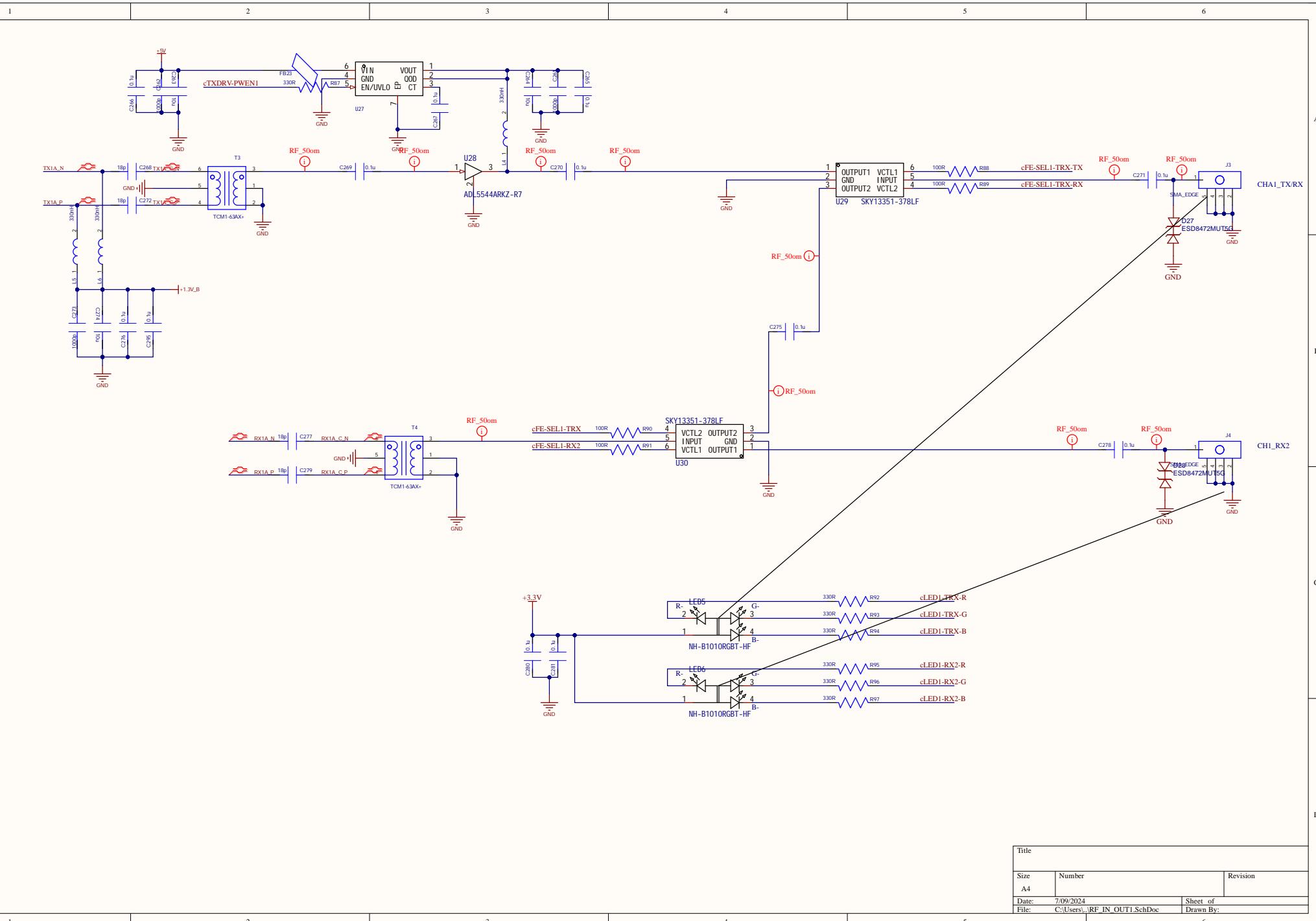


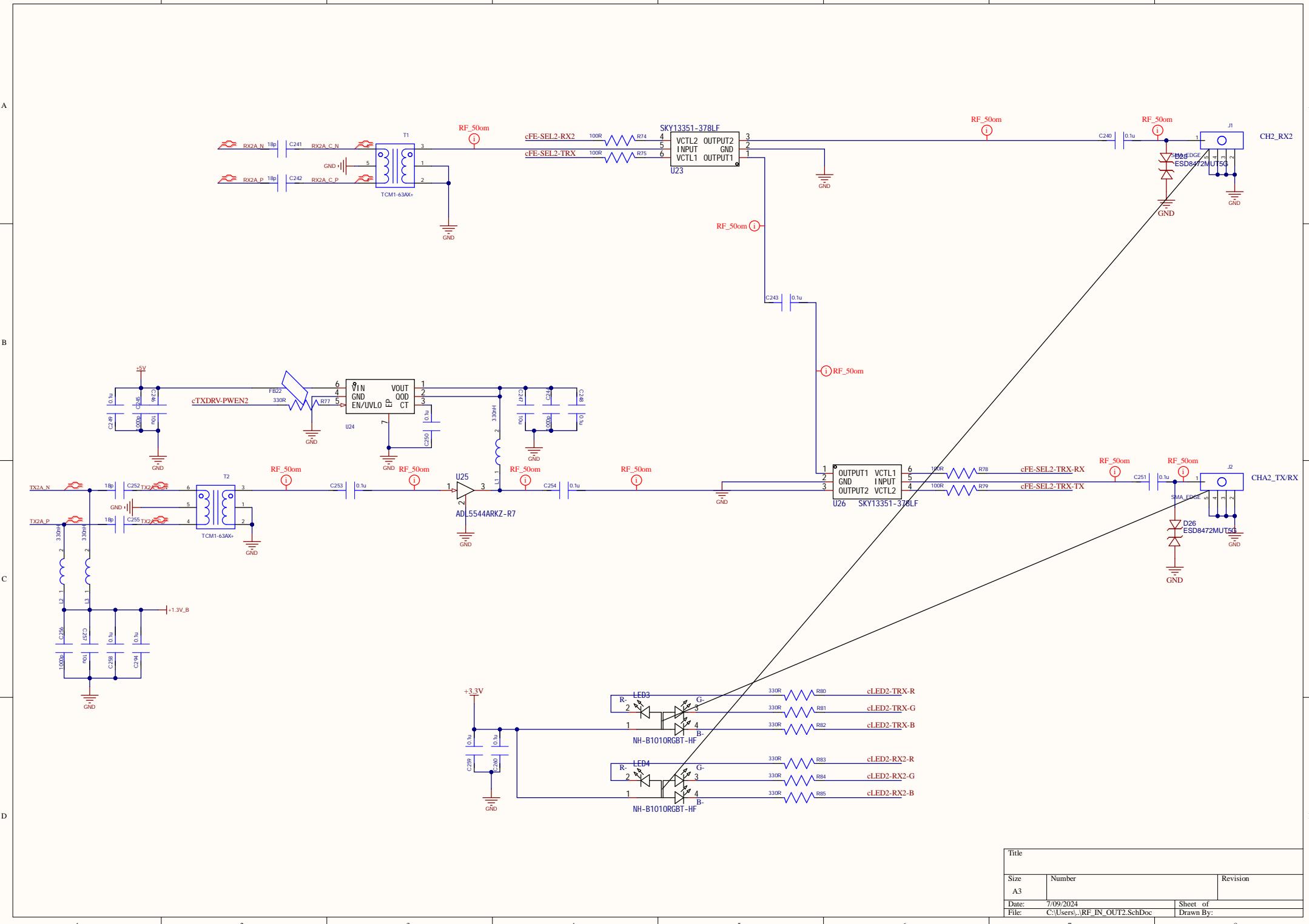
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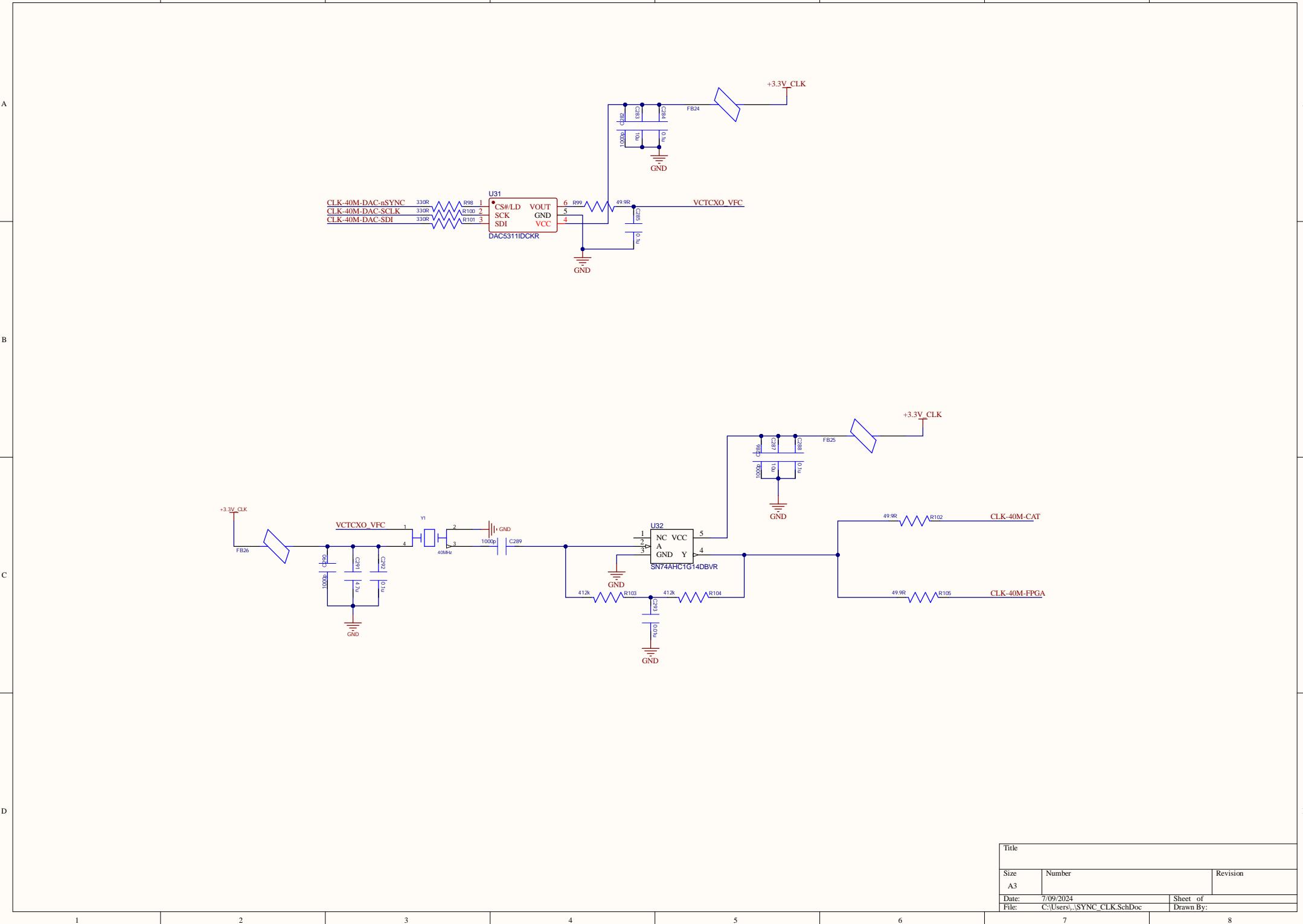


C

Title		
Size	Number	Revision
A4		
Date: 7/09/2024	Sheet of	
File: C:\Users\...\AD9363.SchDoc	Drawn By:	







Title		
Size	Number	Revision
A3		
Date: 7/09/2024	Sheet of	
File: C:\Users\...\SYNC_CLK.SchDoc	Drawn By:	

A

A

B

B

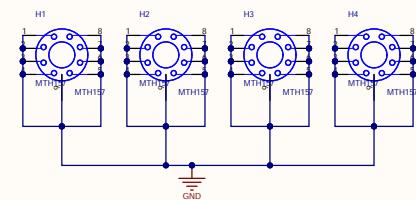
C

C

D

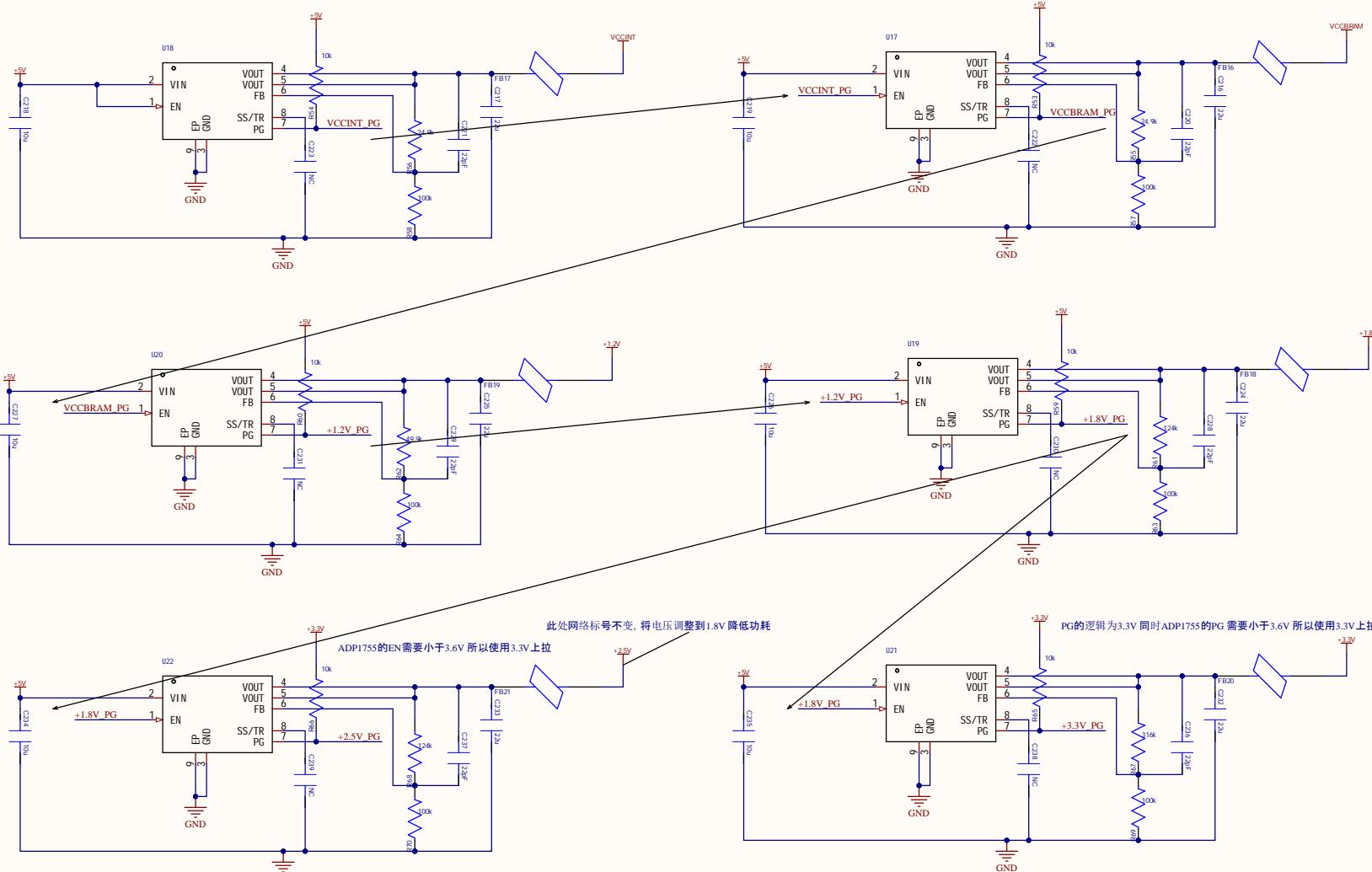
D

- MARK1
- MARK2
- MARK3
- MARK4
- MARK5

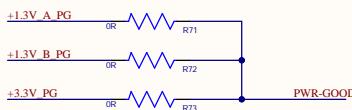


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Size	Number	Revision
A4		
Date: 7/09/2024	Sheet of	
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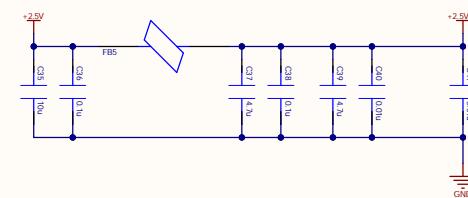
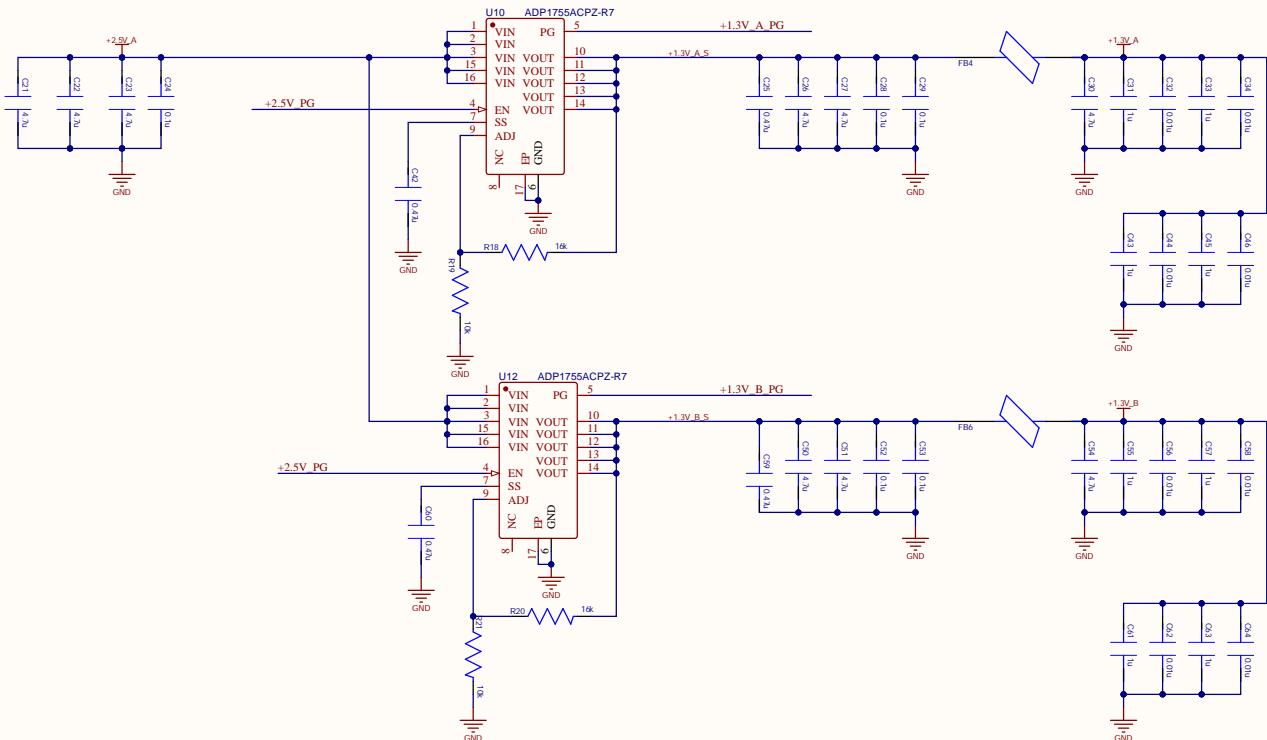
上电顺序1.0V(VCCINT) -> 1.0V(VCCBRAM) -> 1.2V(FX3 INT) -> 1.8V ->(2.5V,3.3V)



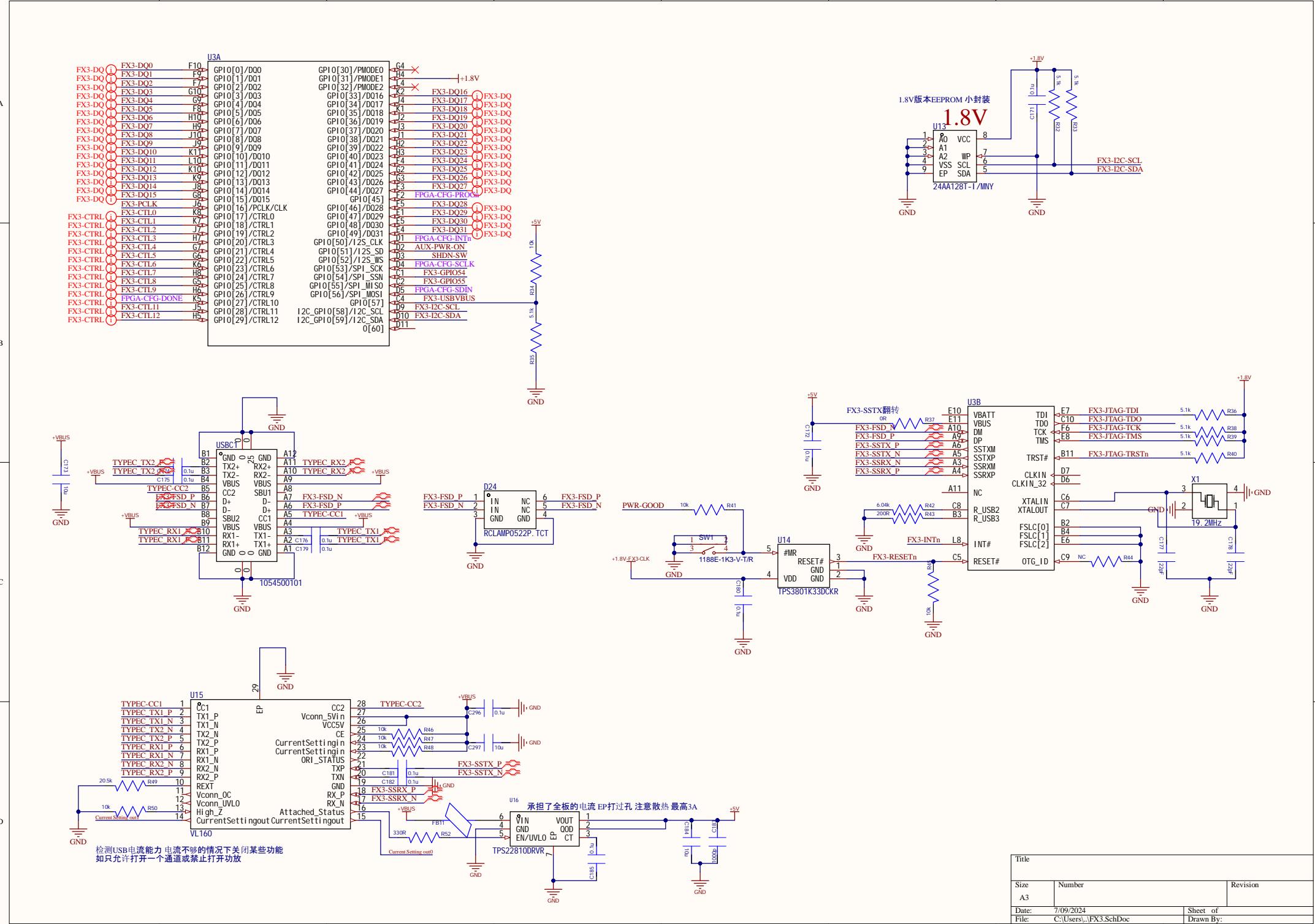
$$V_{OUT} = V_{FB} \times \left(1 + \frac{R1}{R2}\right) = 0.8V \times \left(1 + \frac{R1}{R2}\right)$$



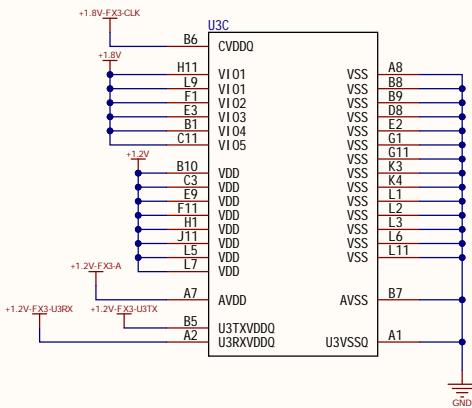
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Size	Number	Revision
A4		
Date:	7/09/2024	Sheet of
File:	C:/Users/.../POWER.SchDoc	Drawn By:



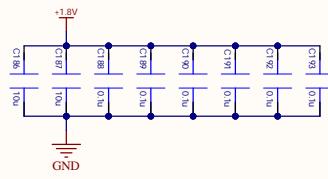
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Size	Number	Revision
A4		
Date: 7/09/2024	Sheet of	
File: C:\Users\...\ANALOG_PWR.SchDoc		Drawn By:



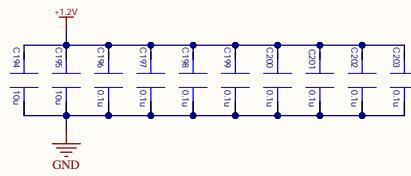
A



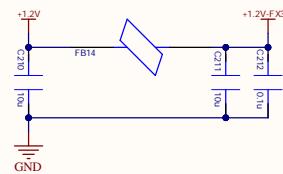
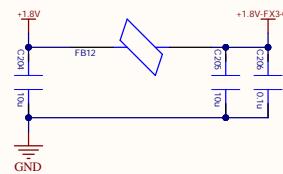
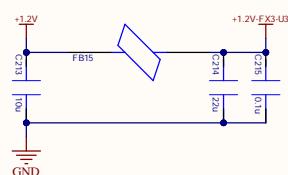
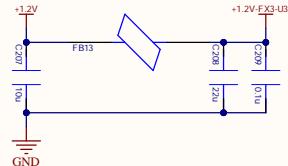
B



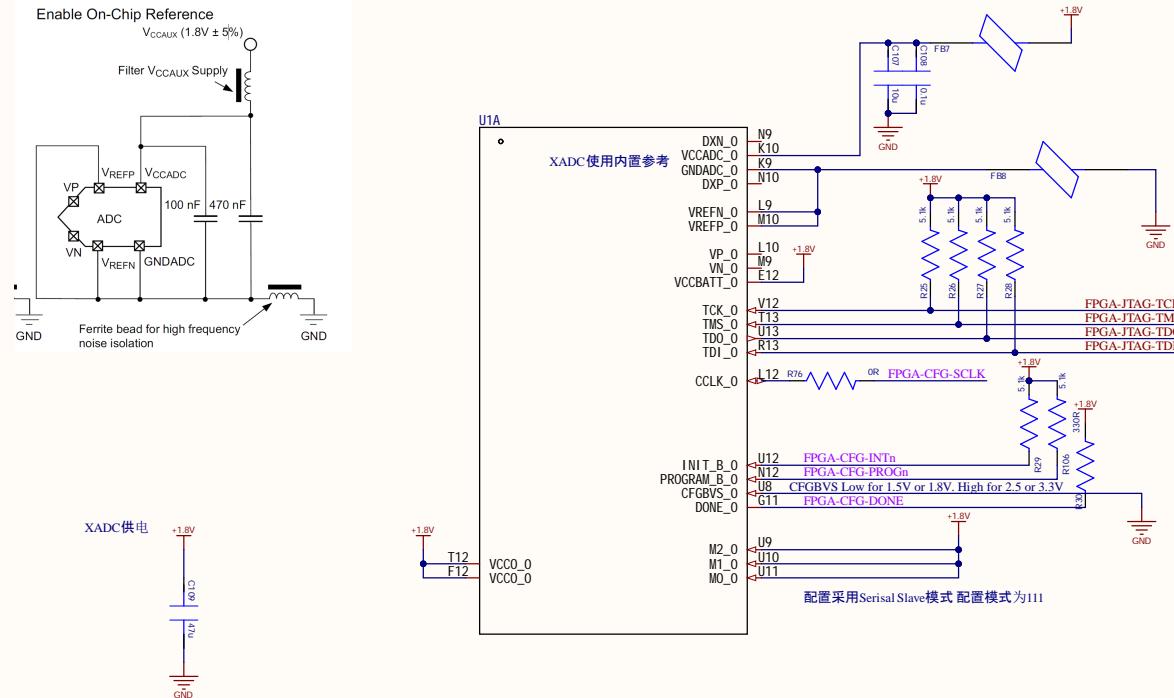
C



D



Title		
Size	Number	Revision
A3		
Date: 7/09/2024	Sheet of	
File: C:\Users\...\FX3_POWER.SchDoc	Drawn By:	



Title		
Size	Number	Revision
A3		
Date: 7/09/2024	Sheet of	
File: C:\Users...\FPGA_CONFIG.SchDoc	Drawn By:	

A

A

B

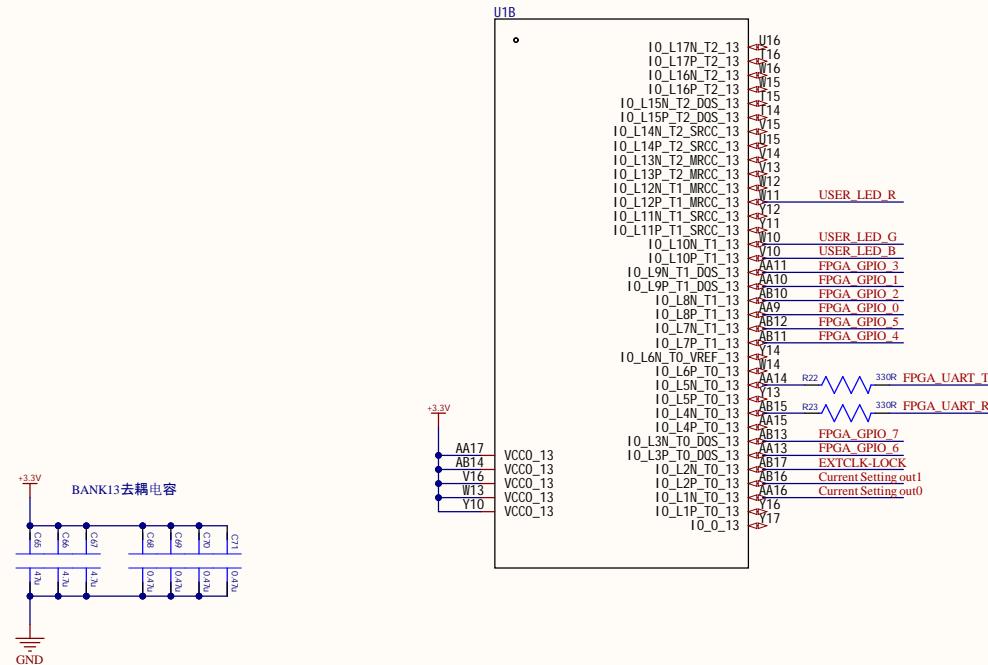
B

C

C

D

D



Title		
Size	Number	Revision
A3		
Date: 7/09/2024	Sheet of	
File: C:\Users\.\FPGA_BANK13.SchDoc	Drawn By:	

A

1

F

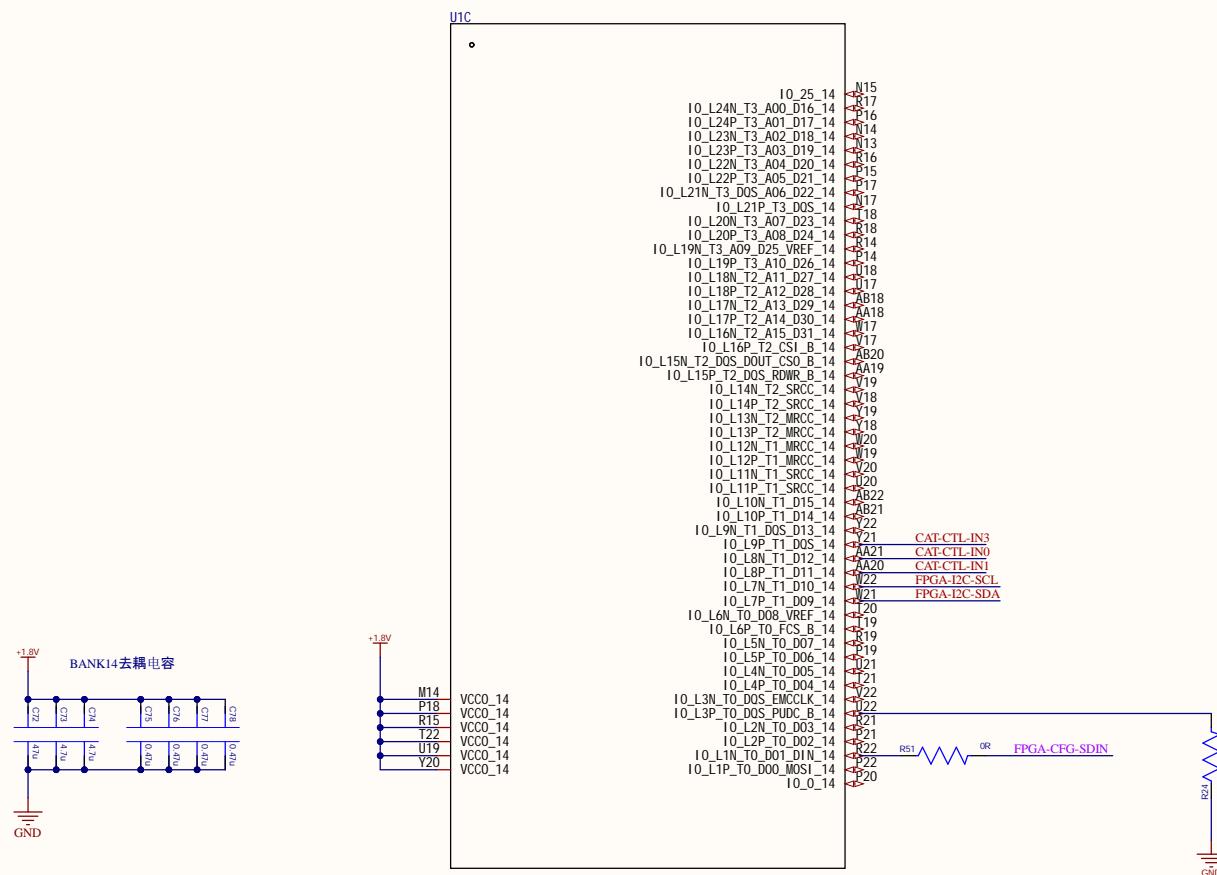
I

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Title			
Size	Number	Revision	
A3			
Date:	7/09/2024	Sheet	of
File:	C:\Users\.\FPGA_BANK14.SchDoc	Drawn By:	

A

A

B

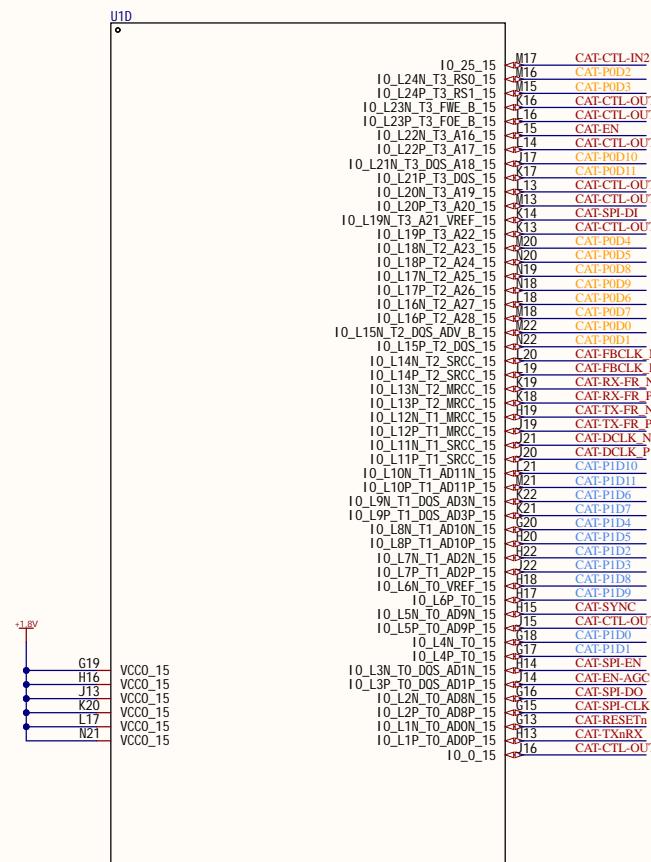
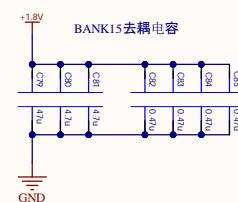
B

C

C

D

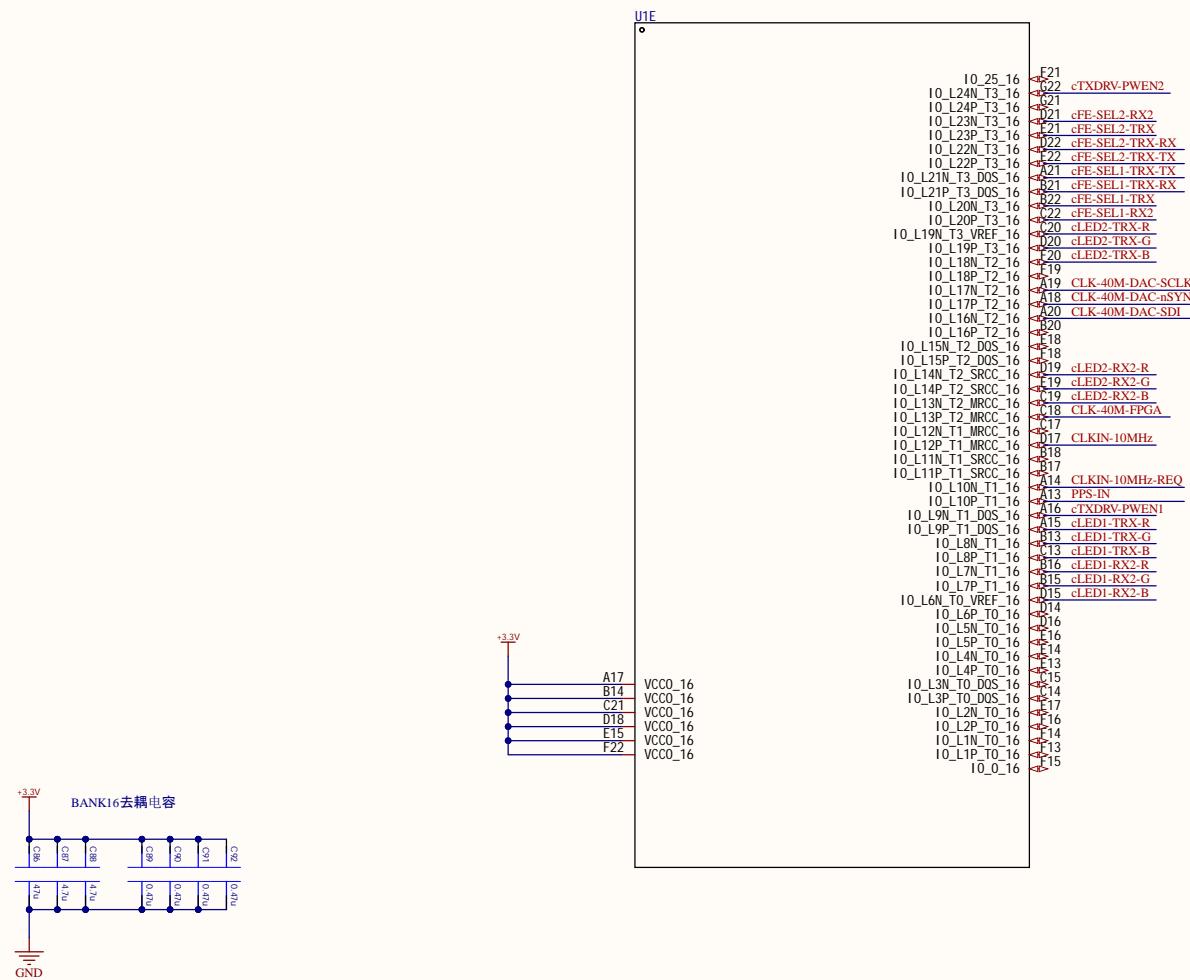
D



Title		
Size	Number	Revision
A3		
Date: 7/09/2024	Sheet of	
File: C:\Users\...\FPGA_BANK15.SchDoc	Drawn By:	

A

A



时钟信号 连接到时钟专用管脚

时钟信号 连接到时钟专用管脚

B

B

C

C

D

D

Title		
Size	Number	Revision
A3		
Date: 7/09/2024	Sheet of	
File: C:\Users\.\FPGA_BANK16.SchDoc	Drawn By:	

A

A

THIS BANK LEAVE FOR DDR3

Mini版此处用1.8V io电平替代 完整版更换为1.5V电平

B

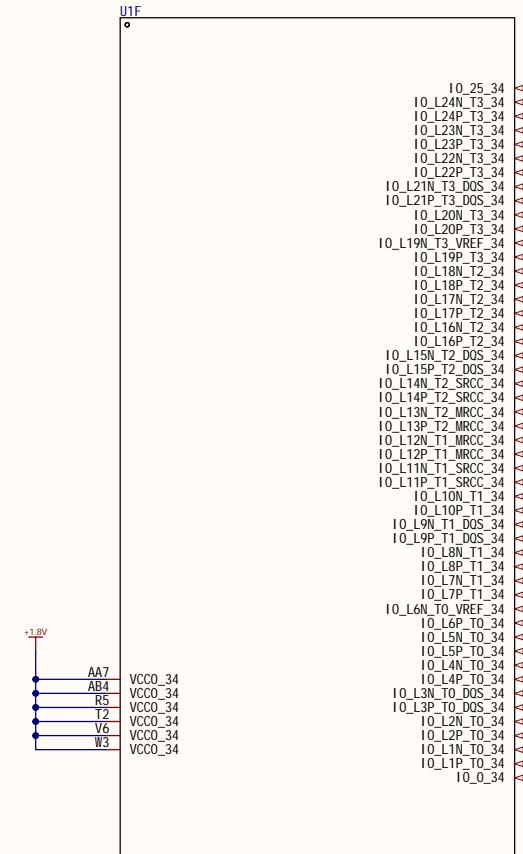
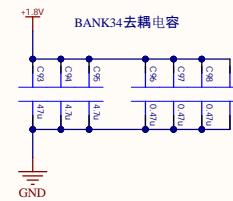
B

C

C

D

D



A

A

B

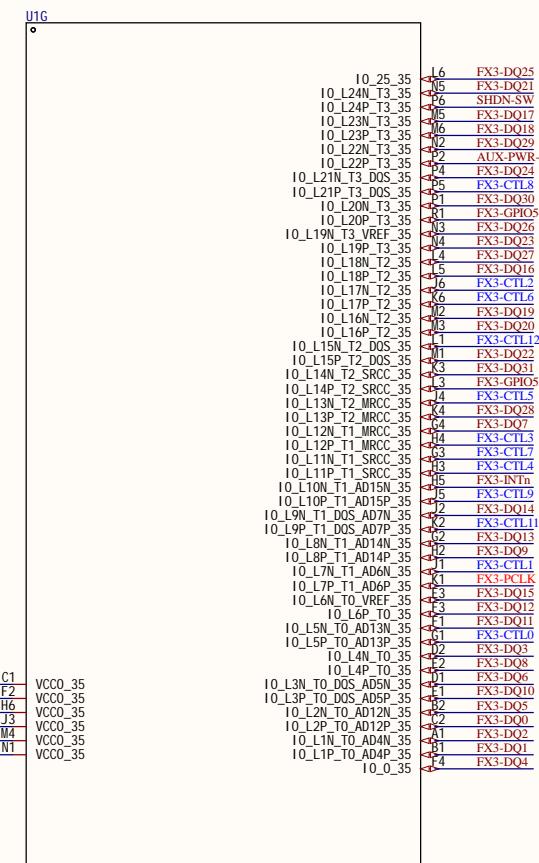
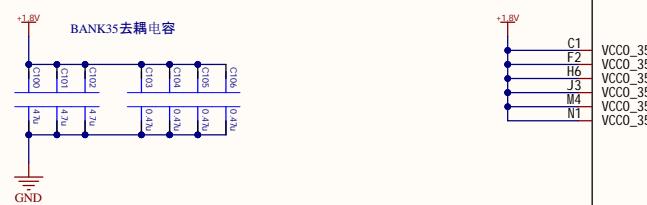
B

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C

D

D



Title		
Size	Number	Revision
A3		
Date: 7/09/2024	Sheet of	
File: C:\Users\...\FPGA_BANK35.SchDoc	Drawn By:	

A

A

B

B

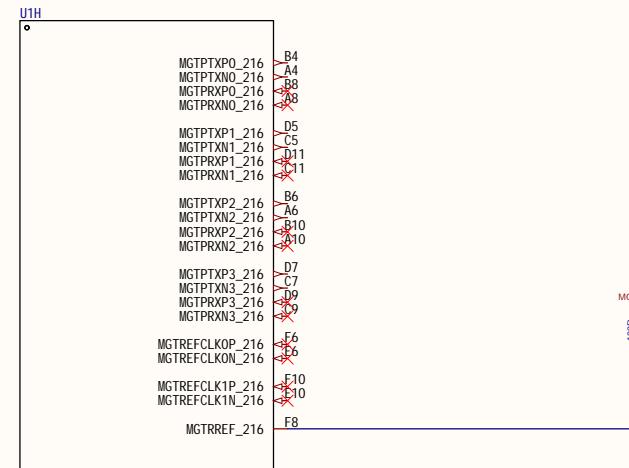
C

C

D

D

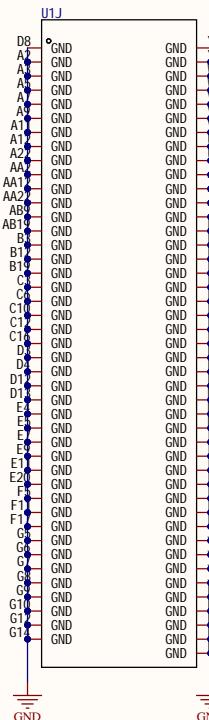
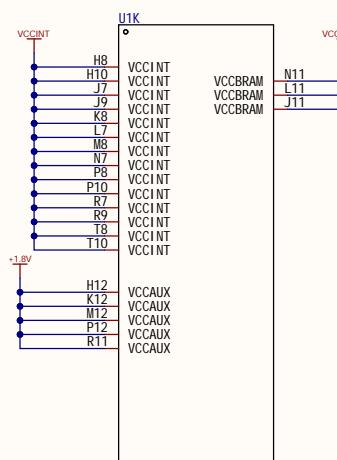
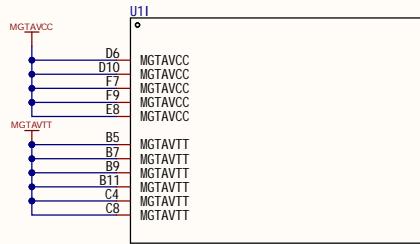
BANK NOT USED



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Size	Number	Revision
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Date: File:	7/09/2024 C:\Users\.\FPGA_GTSchDoc	Sheet of Drawn By:

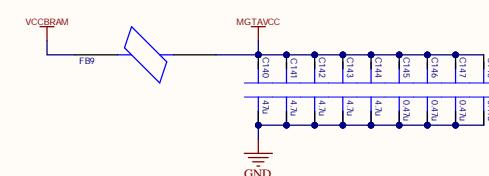
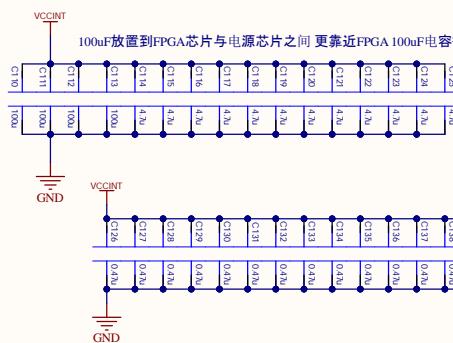
A

1



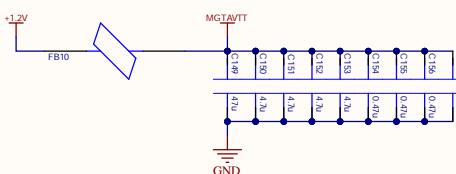
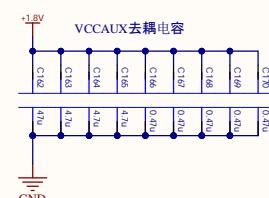
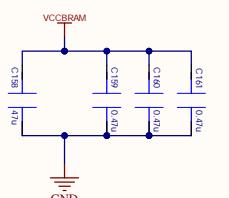
B

I



C

1

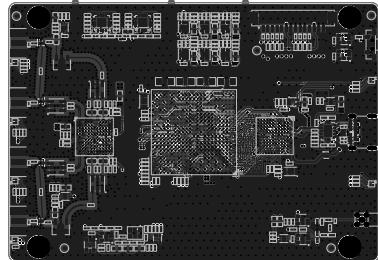


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1

Title		
Size A3	Number	Revision
Date: 7/09/2024	Sheet of	
File: C:\Users\.\FPGA_POWER.SchDoc	Drawn By:	

Erl	10层			单线50				顶层隔层参考单线50			差分100			顶层隔层参考差分100			差分90				
	板厚	叠层结构		层次	阻抗	线宽	参考层	铜厚	阻抗	线宽	参考层	阻抗	线宽	间距	阻抗	线宽	间距	参考层	阻抗	线宽	间距
1.6				TOP	50	5mil	L2	1OZ	50	13mil	L3	100	4.1mil	7.5mil	100	9.2mil	7.5mil	L3	90	4.7mil	6mil
	4.2	3.2mil						0.5OZ													
	4.2	4mil		L3	50	5mil	L2/L5	0.5OZ	/	/	/	100	4mil	7mil	/	/	/	/	90	4.8mil	6mil
	4.2	12.6mil		L4	50	5mil	L2/L5	0.5OZ	/	/	/	100	4mil	7mil	/	/	/	/	90	4.8mil	6mil
	4.2	4mil						0.5OZ													
	4.2	5.5mil						0.5OZ													
	4.2	4mil		L7	50	5mil	L6/L9	0.5OZ	/	/	/	100	4mil	7mil	/	/	/	/	90	4.8mil	6mil
	4.2	12.6mil		L8	50	5mil	L6/L9	0.5OZ	/	/	/	100	4mil	7mil	/	/	/	/	90	4.8mil	6mil
	4.2	4mil						0.5OZ													
	4.2	3.2mil		BOT	50	5mil	L2	1OZ	/	/	/	100	4.1mil	7.5mil	/	/	/	/	90	4.7mil	6mil



TOP01 SIG03 SIG04 SIG07 SIG08 BOT110