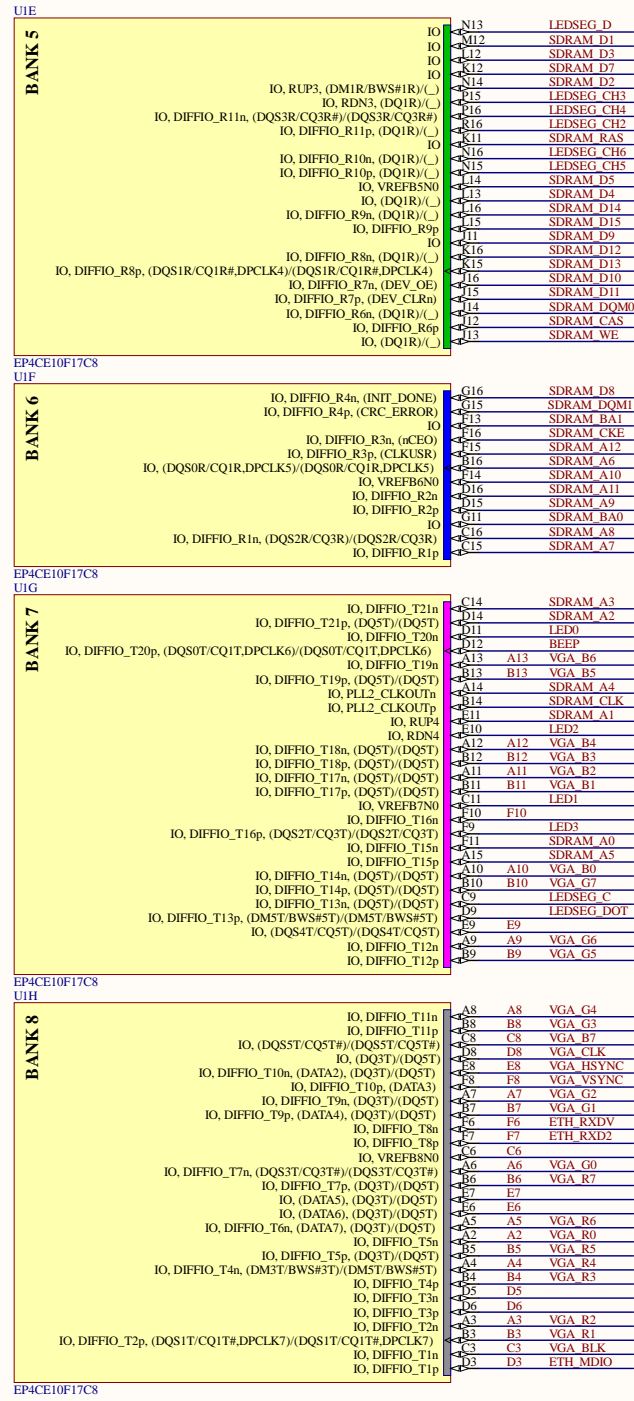


BANK 1	UIB		IO, (DQ52L/CQ3L)/(DQ52L/CQ3L)	D4	D4
			IO, DIFFIO_L1p, (DATA1,ASDO)	E5	ETH MDC
			IO, VREFB1N0	F5	ETH RXD0
			IO, DIFFIO_L2p, (FLASH_nCE,nCS0)	B1	SDIO D2
			IO, DIFFIO_L2n	C2	SDIO D3
			IO, DIFFIO_L3p	F1	EPCS ASD0
			IO, DIFFIO_L3n	F3	F3
			IO, DIFFIO_L4p, (DQ50L/CQ1L,DPCLK0)/(DQ50L/CQ1L,DPCLK0)	D2	EPCS CS
			IO, DIFFIO_L4n	D1	SDIO CMD
			IO, (DATA0)	G5	ETH RXD1
				F2	LCD XL
				F1	LCD YU
				G2	LCD XR
				G1	LCD YD
				F2	EPCS DATA0
EP4CE10F17C8					
BANK 2	UIB		IO, DIFFIO_L5p, (DQ1L)/( )	P2	SDIO SCK
			IO, DIFFIO_L5n, (DQ1L)/( )	J1	LCD DEN
			IO, DIFFIO_L6p	J6	ETH TXC
			IO, DIFFIO_L6n	K6	ETH TXD0
			IO, DIFFIO_L7p	L6	ETH RESET
			IO, DIFFIO_L7n, (DQ1L)/( )	C1	SDIO D1
			IO, DIFFIO_L8p, (DQ51L/CQ1L#,DPCLK1)/(DQ51L/CQ1L#,DPCLK1)	L2	LCD HSYNC
			IO, DIFFIO_L8n, (DQ1L)/( )	L1	LCD VSYNC
			IO, VREFB2N0	L3	ETH TXD3
			IO, DIFFIO_L9p, (DQ1L)/( )	N2	LCD CLK
			IO, DIFFIO_L9n, (DQ1L)/( )	N1	LCD DISP
			IO, RUP1, (DQ1L)/( )	K5	ETH TXD1
			IO, RDN1, (DQ1L)/( )	L4	ETH TXEN
			IO, (DQ53L/CQ3L#)/(DQ53L/CQ3L#)	R1	LCD B5
			IO, DIFFIO_L10p, (DQ1L)/( )	P2	LCD B6
			IO, DIFFIO_L10n, (DM1L BWS#1L)/( )	P1	LCD B7
EP4CE10F17C8					
BANK 3	UIC		IO, DIFFIO_B1p	N3	LCD B3
			IO, DIFFIO_B1n, (DM3B/BWS#3B)/(DM5B/BWS#5B)	P3	LCD B2
			IO, DIFFIO_B2p, (DQ3B)/(DQ5B)	R3	LCD B1
			IO, DIFFIO_B2n	T3	LCD B0
			IO, (DQ51B/CQ1B#,DPCLK2)/(DQ51B/CQ1B#,DPCLK2)	L2	LCD B4
			IO, PLL1_CLKOutP	R4	LCD G7
			IO, PLL1_CLKOutN	T4	LCD G6
			IO, DIFFIO_B4p, (DQ3B)/(DQ5B)	S5	UART_RX
			IO, DIFFIO_B4n, (DQ3B)/(DQ5B)	M6	CMOS_D5
			IO, (DQ3B)/(DQ5B)	M6	M6
			IO, VREFB3N0	M6	CMOS_D4
			IO, DIFFIO_B5p, (DQ53B/CQ3B#)/(DQ53B/CQ3B#)	M7	UART_TX
			IO, DIFFIO_B5n	K8	ETH RXD3
			IO, DIFFIO_B6p, (DQ3B)/(DQ5B)	R5	LCD G5
			IO, DIFFIO_B6n	T5	LCD G4
			IO, DIFFIO_B7p, (DQ3B)/(DQ5B)	M6	LCD G3
			IO, DIFFIO_B7n	T6	LCD G2
			IO, DIFFIO_B8p, (DQ3B)/(DQ5B)	L7	ETH TXD2
			IO, DIFFIO_B8n, (DQ55B/CQ5B#)/(DQ55B/CQ5B#)	R7	LCD G1
			IO, DIFFIO_B9p, (DQ3B)/(DQ5B)	T7	LCD G0
			IO, DIFFIO_B9n, (DM5B/BWS#5B)/(DM5B/BWS#5B)	L8	ETH RXC
			IO, DIFFIO_B10p, (DQ5B)/(DQ5B)	M8	CMOS_D3
			IO, DIFFIO_B10n, (DQ5B)/(DQ5B)	M8	CMOS_D2
			IO, DIFFIO_B11p	R8	CMOS_D1
			IO, DIFFIO_B11n	R8	LCD R7
				T8	LCD R6
EP4CE10F17C8					
BANK 4	UID		IO, DIFFIO_B12p	R9	LCD R5
			IO, DIFFIO_B12n	T9	LCD R4
			IO, DIFFIO_B13p	M9	CMOS_D0
			IO, DIFFIO_B13n	M9	CMOS RESET
			IO, DIFFIO_B14p	M9	CMOS HREF
			IO, DIFFIO_B14n, (DQ5B)/(DQ5B)	M9	CMOS_SCL
			IO, DIFFIO_B15p, (DQ5B)/(DQ5B)	R10	LCD R3
			IO, DIFFIO_B15n, (DQ54B/CQ5B)/(DQ5		



The schematic diagram illustrates the hardware circuit for the proposed system. It features three main microcontroller units: U1K, U1L, and U1J. U1K is an EP4CE10K10F7C8 FPGA, U1L is an EP4CE10K10F7C8 FPGA, and U1J is an EP4CE10K10F7C8 FPGA. The circuit includes various power supply connections for VCC3.3, VCC1.2, and VCC2.5, and signal connections for TDI, TDO, TCK, TMS, DCLK, CONF\_DONE, and nSTATUS. The diagram also shows the connection of various peripheral components like resistors, capacitors, and connectors.

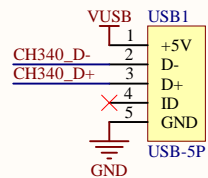
The schematic diagram shows the EPCS configuration. The EPCS device (U2) is connected to the EPIC device. The EPCS device has pins for EPICS\_CLK (6), EPICS\_ASDO (5), EPICS\_DATA0 (2), VCC3.3 (8), and HOLD (4). The EPIC device has pins for EPCS\_CS (1), VCC3.3 (3), and GND (4). A capacitor C2 (M25P16, 104) is connected between the VCC3.3 pins and GND.

U11

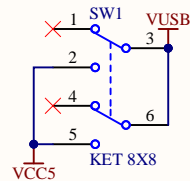
Input Signal	Output Signal
FPGA_CLK	CLK1, DIFFCLK_0n
KEY2	CLK2, DIFFCLK_1p
RESET	CLK3, DIFFCLK_1n
KEY1	CLK4, DIFFCLK_2p
KEY0	CLK5, DIFFCLK_2n
M15	CLK6, DIFFCLK_3p
KEY3	CLK7, DIFFCLK_3n

EP4CE10F17C8

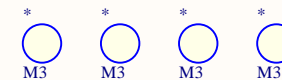
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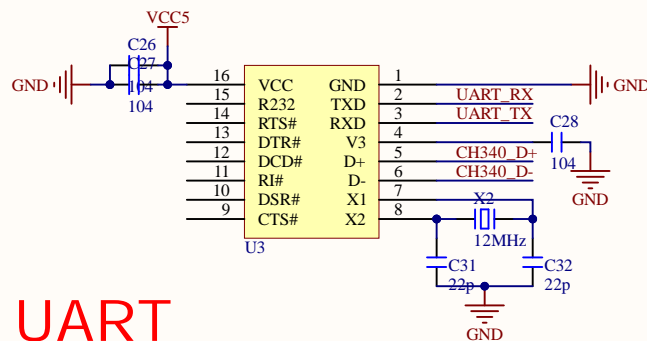
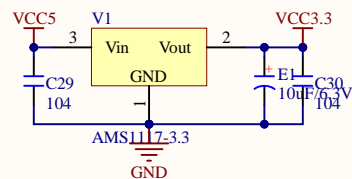
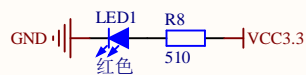
USB



电源开关

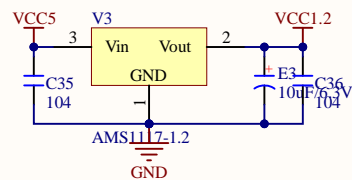
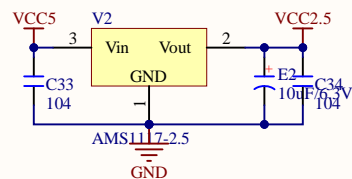
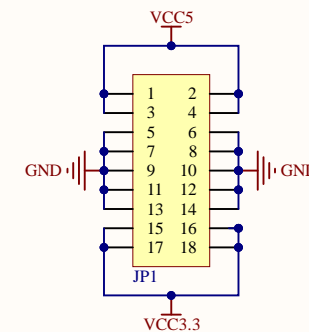


POWER

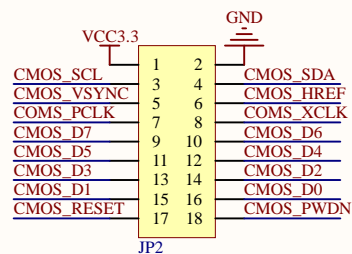


UART

电源扩展



摄像头



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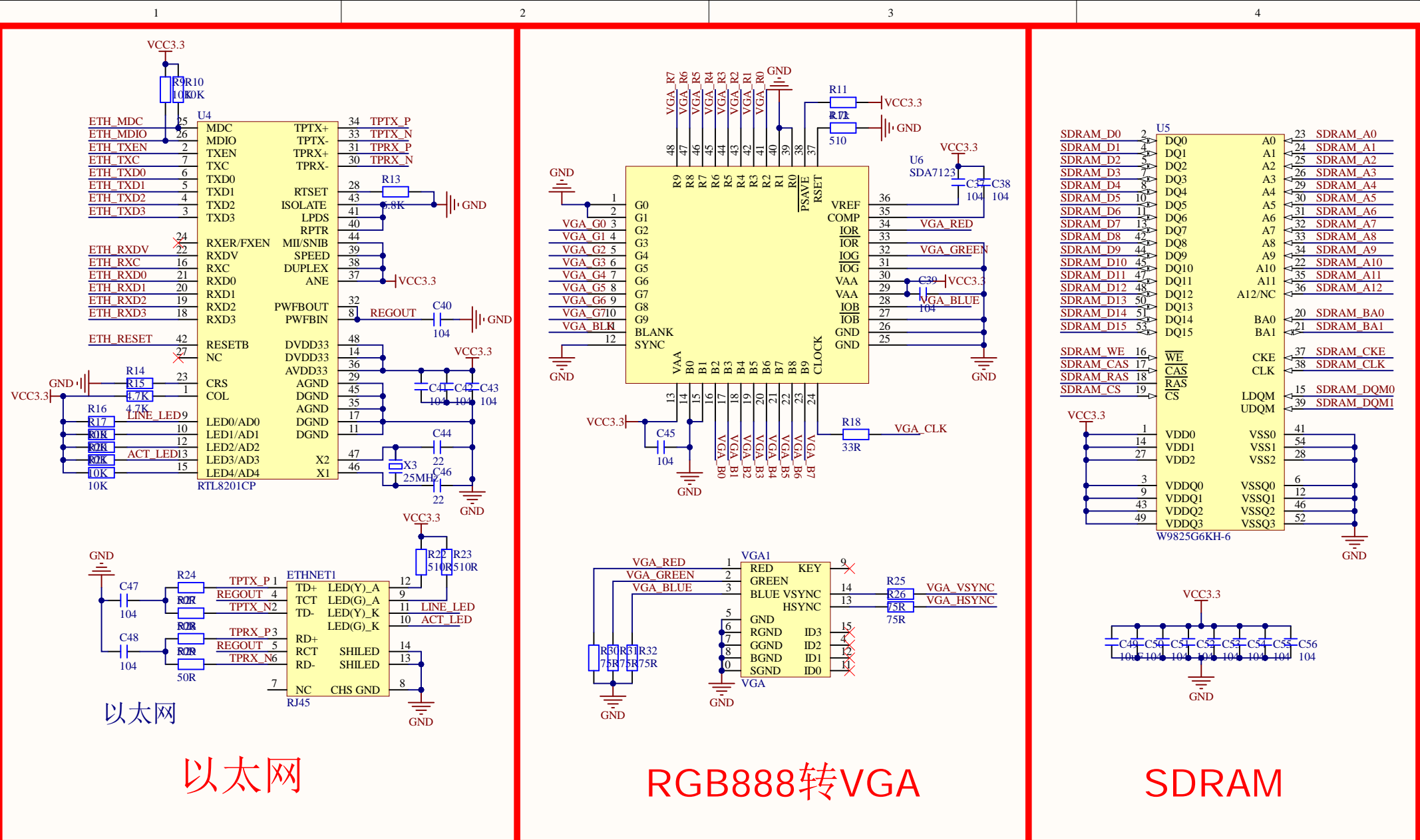
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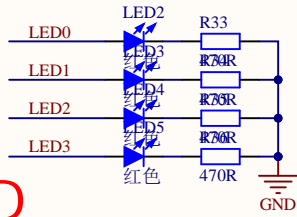
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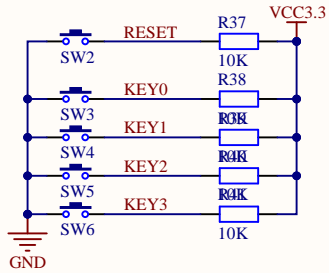


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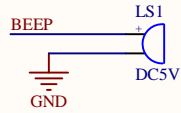
# LED



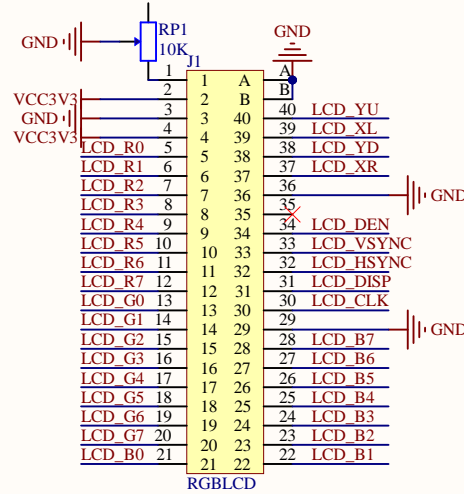
# KEY



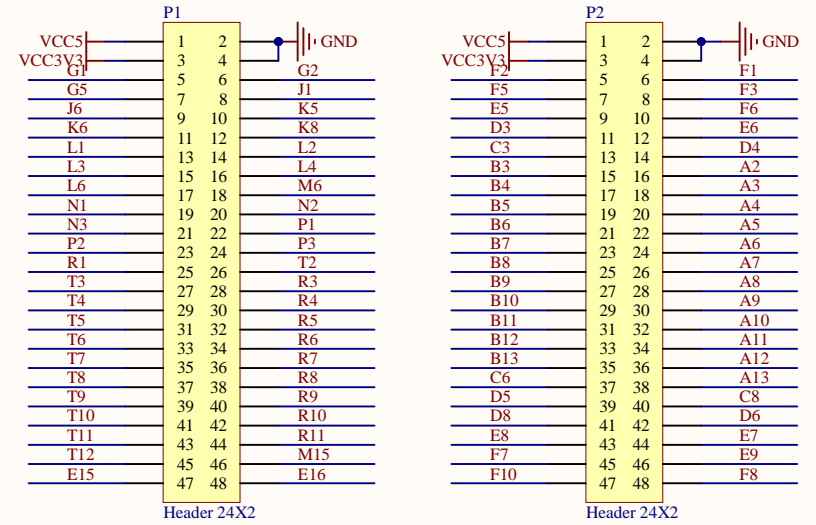
# BEEP



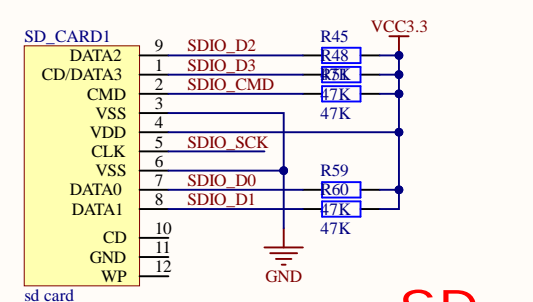
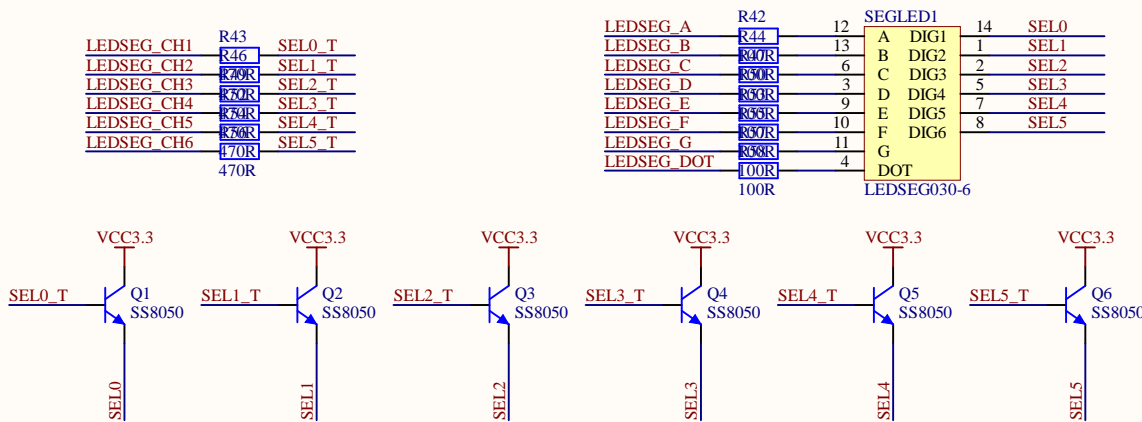
# RGB\_LCD



# 扩展IO



# LED DIGITAL TUBE



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