The basics of decoupling capacitors

How to stabilize digital supply voltages - and why most of the online advice on th
topic is suspect.

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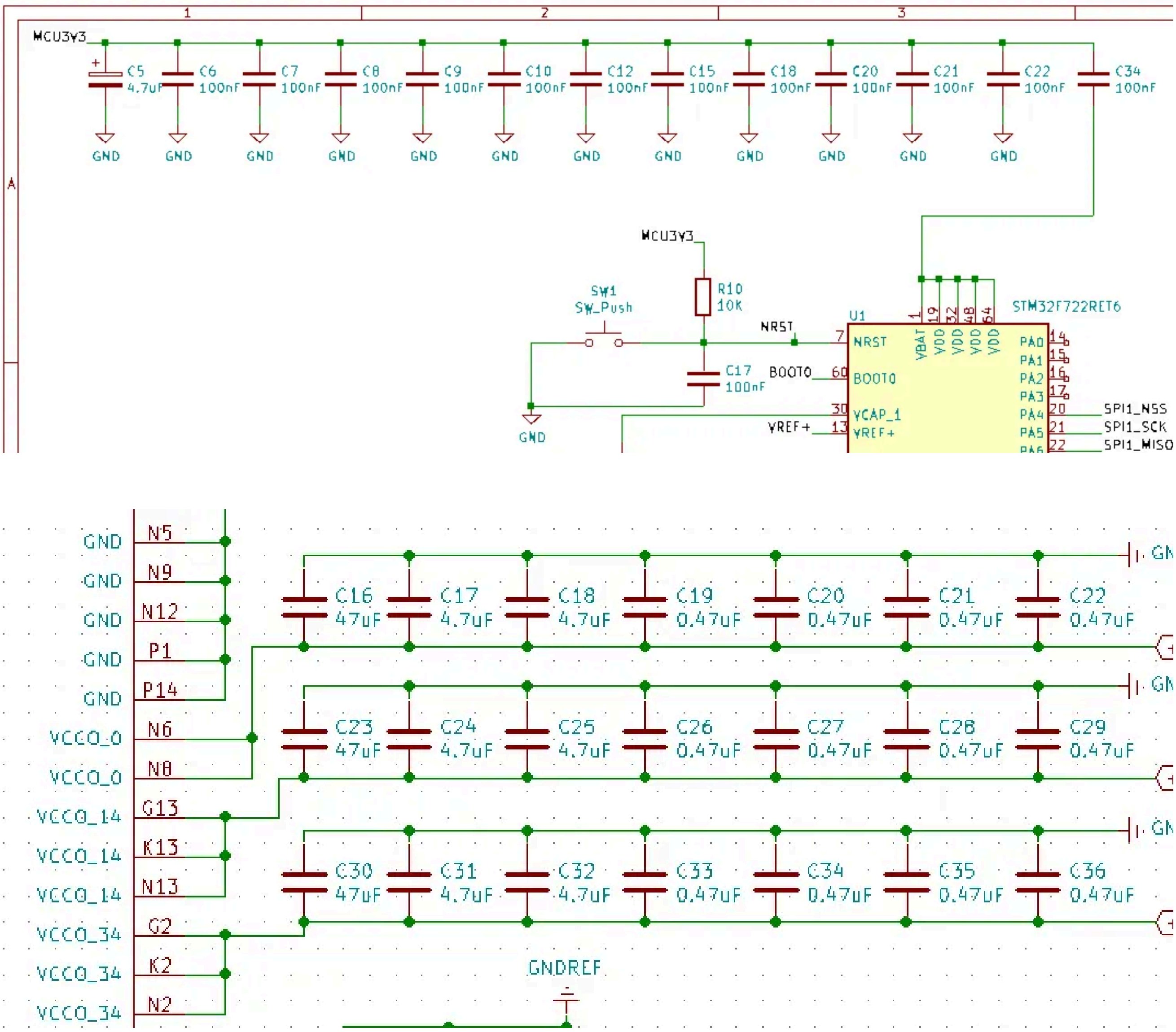
Two decades ago, to build a portable music player, you had to clobber together several hundred electronic components. Today, you can accompl the same with a single chip and a dozen passives. Heck, you might even ge Wi-Fi and Bluetooth for free.

One of the few discrete components that survive and thrive in the face of growing integration is the humble decoupling capacitor. It's not just that t device is hard to manufacture on the die of an integrated circuit; in the wo high data speeds and low supply voltages, it has an increasingly important role to play in keeping the circuits humming along.

Among hobbyists, the understanding of decoupling caps continues to be h and-miss. Some folks skip them altogether and live to tell; others follow ancient lore of uncertain origins, producing monstrosities such as this:



Decoupling capacitor galore. Found on the internet.

In this article, I'm hoping to cast some light on the actual role of decouplin capacitors in digital circuits — and to offer advice on how to integrate the into your designs without going overboard.

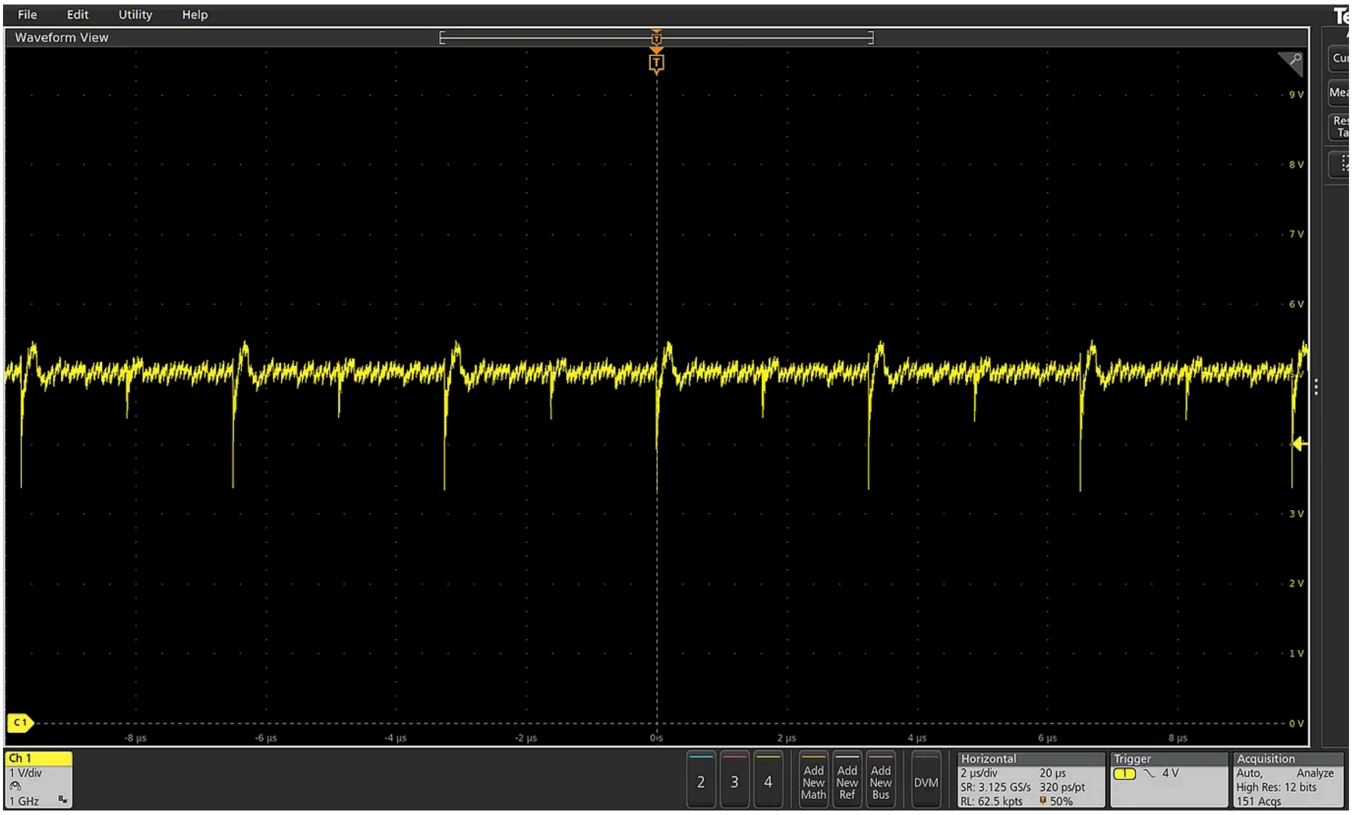
What does a decoupling capacitor do, anyway?

In a steady state, a typical CMOS integrated circuit needs very little powe The chip's energy consumption is associated predominantly with state transitions — that is, toggling between "zero" and "one". That's because the process requires moving electrons back and forth to charge or discharge t gates of field effect transistors inside the chip.

Some internal state transitions require relatively little current, but others more demanding; this is particularly true for the operation of larger transistors that drive output lines. To toggle them at megahertz speeds — task that demands rapid rise and fall times — the chip must momentarily source significant currents. In a typical microcontroller, the transition usu takes no more than several nanoseconds, but may involve hundreds of milliamps.

This poses a challenge. At high and rapidly varying currents, PCB traces exhibit resistive losses and non-trivial [inductive reactance](). The imperfect demand response characteristics of the power supply also get in the way. the end, even seemingly minor digital switching can cause significant volt fluctuations and electrical noise across the entire circuit.

The following oscilloscope plot shows the effects of a popular ATmega microcontroller repeatedly toggling a couple of unconnected output pins. MCU clock speed is 8 MHz; square wave rise time is somewhere in the ballpark of 5 ns:



Observed supply voltage noise for a simple MCU application.

The peak-to-peak amplitude of this noise, as sampled at the MCU supply p is almost 2 volts — about 40% of the nominal supply voltage. This in itself c be enough to destabilize the MCU. Just as important, because the chip no longer has a stable Vdd and GND reference shared with other parts of the circuit, interfacing it to other devices might prove difficult. It's not that th setup is *bound* to malfunction, but unexplained and hard-to-diagnose issu can creep up with ease.

This brings us to the purpose of decoupling capacitors: they are placed ac the voltage supply lines and physically close to the offending chip to handl switching transients while preventing high currents and minimizing voltag fluctuations in other parts of the circuitry.

To do this, the capacitors must have low equivalent series resistance (i.e., able to charge and discharge quickly); for this reason, multilayer ceramics (MLCCs) should be used instead of the comparatively sluggish electrolytic caps. But above all, to work effectively, the capacitors must be as close as practical to the chip's supply pins. The following oscilloscope trace captur for another mildly noisy 8-bit MCU illustrates the point:

The effect of capacitor distance on the switching noise of an AVR Dx MCU.

One could analyze the setup in terms of an [RC or LC lowpass filter] formed tandem with upstream and downstream impedances, but these parameter are hard to faithfully estimate. Most of the time, we go by rules of thumb: a single 100 nF to 1 µF MLCC per supply domain, operated well clear of its maximum voltage, is typically enough to deal with all intrinsic switching currents of PIC, AVR, or mid-range ARM microcontrollers.

Beyond this, additional "bulk" capacitance might be appropriate if the MC driving substantial loads. This can be accomplished with a single larger Ml (e.g., 10 µF); with several smaller MLCCs in parallel; or with a small fast-act MLCC coupled with a larger but slower aluminum-polymer cap (10-100 µF the latter configuration, the larger capacitor can be safely placed some distance away.

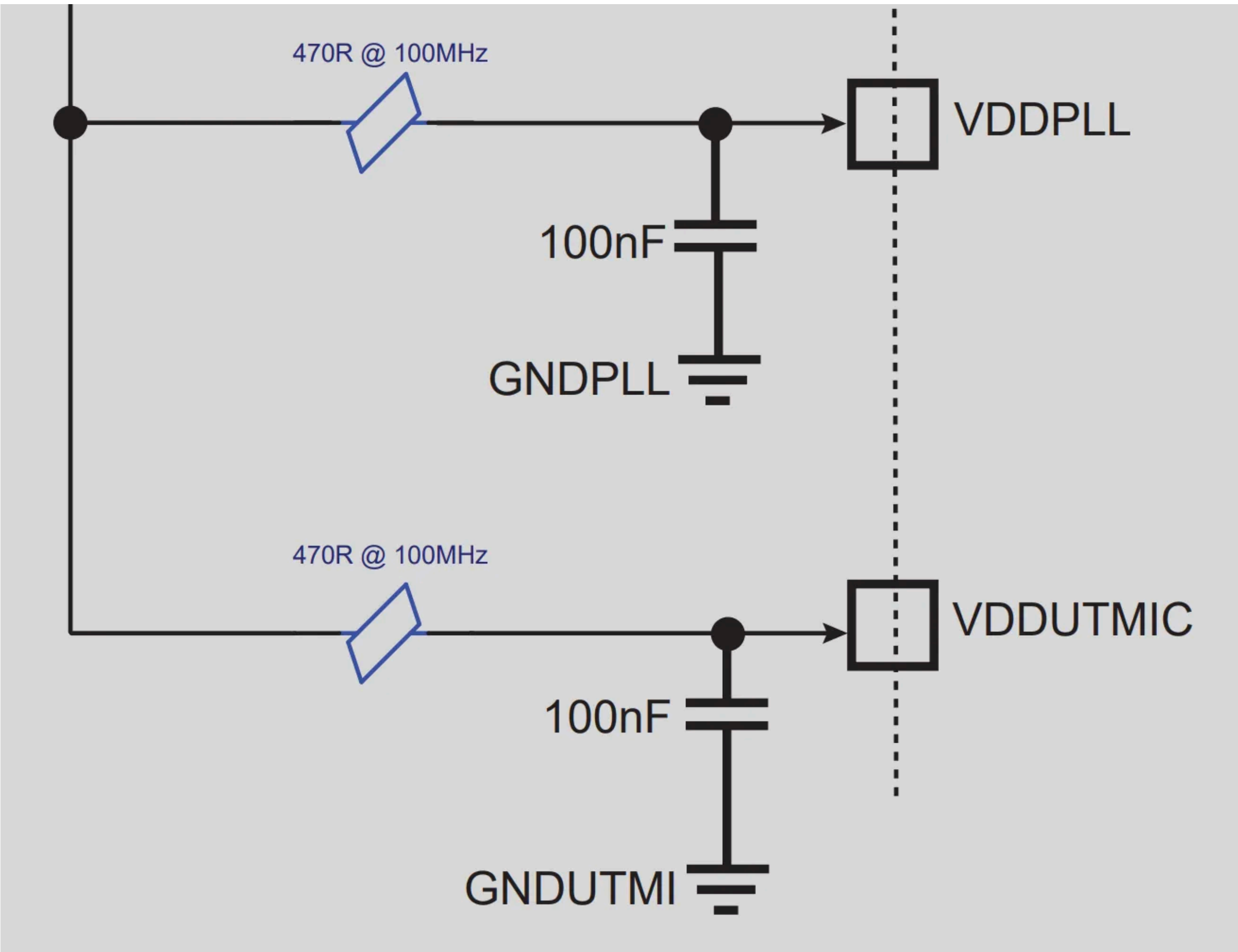
Is a capacitor always enough?

A well-chosen decoupling capacitor can greatly reduce switching noise, b the component has a finite capacitance and a non-zero impedance. The capacitor's impedance increases not only toward DC, but also toward very high frequencies; this is because of the fairly large, conductive surface are inside the device that forms a small inductor and limits the capacitor's response speed. The end result is that a typical MLCC can't supply high currents at (sine wave) frequencies above 100 MHz or so.

In other words, some attenuated high-frequency noise will inevitably get through — and while adding extra capacitors can offer some modest improvement, the strategy has diminishing returns.

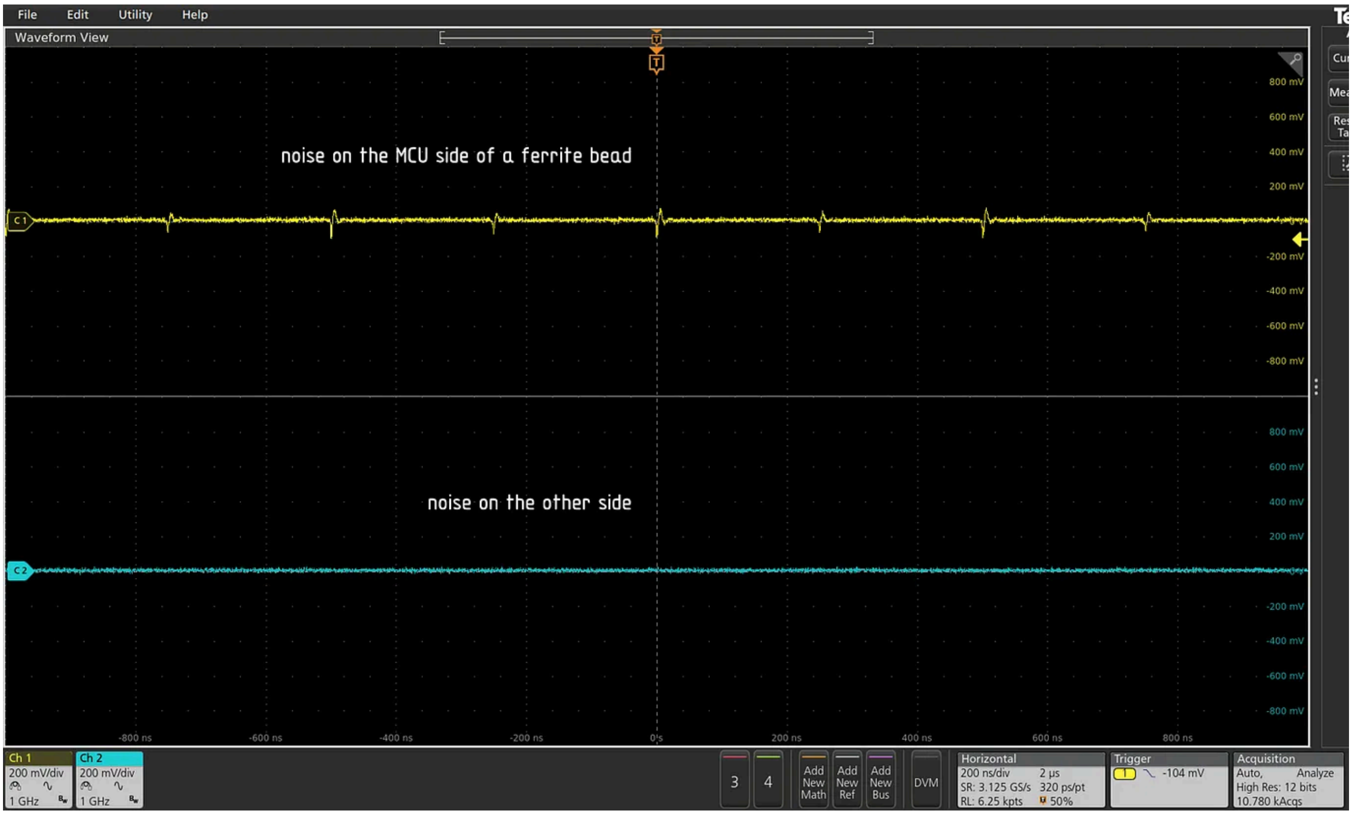
In sensitive circuits, the problem of this residual high-frequency noise car further mitigated by placing a small ferrite bead in series with the supply a ahead of the decoupling caps. The inductor provides a low impedance pat (few milliohms) for DC signals while impeding megahertz-range AC much better than a shunt capacitor to the ground can — usually performing wel GHz or so, at which point parasitics once again get in the way.

The following example from the spec for SAM S70 MCUs, recommending t use of two beads with an impedance of 470 Ω at 100 MHz on the supply lir for the USB transceiver and the phase-locked loop (PLL) clock multiplier:



Noise-filtering beads on MCU supply lines.

Combined with decoupling capacitors, the setup works remarkably well:



Noise containment afforded by a ferrite bead.

That said, it must be underscored that a ferrite bead doesn't eliminate noi it merely contains it to the side it originated from. It can shield analog circuitry from digital switching artifacts, or it can protect the MCU from r originating elsewhere; in all cases, it must be followed by a decoupling capacitor to provide some power reserve for downstream circuitry. An upstream (supply-side) capacitor is wise, too.

A related trick is to put small ferrite beads on MCU output lines; this takes edge off fast-rising square wave signals, and can reduce needless currents spurious radio frequency emissions when operating slower buses such as or SPI. In a pinch, small resistors might also do, although they will typicall perform worse.

With this out of the way, most other noise mitigation techniques tend to revolve around board design. For example, keeping sensitive analog circui at an arm's length from digital signals is a good PCB layout strategy; so is placing an unbroken ground plane immediately under high-speed data lin to avoid forming large current loops that radiate wideband noise into the open space. (For a separate article on this topic, click here.)

What if the manufacturer says…

The datasheets for some digital chips will outline a suggested way of decoupling them. These recommendations should not be ignored, but are to be taken as gospel. The manufacturer is trying to cover a variety of extremes, including:

- Circuits operated at the lowest permissible supply voltage,
- Devices running at the maximum supported clock speed,
- Peak utilization of on-chip peripherals,
- The customer using the worst decoupling capacitors money can buy (the "Y5V" variety that loses ~80% of rated capacitance when operated elevated temperatures or near the cap's maximum voltage).

Further, the manufacturer is making assumptions about customers' desigr preferences. A typical 100 nF MLCC costs about $0.005 a piece; in contras 10 μF aluminum-polymer cap is about $0.25. A customer doing robotic assembly might favor a dozen MLCCs in lieu of a single MLCC paired with polymer capacitor. A hobbyist soldering by hand might not.

Instead of blindly following the spec — a practice that still doesn't guarant success — it can more useful to validate your design in three ways:

- Examine circuit supply noise under normal operating conditions. If th peaks exceed maximum permissible supply ripple, minimum supply voltage, or maximum supply voltage for the digital components, or if switching noise propagates to sensitive analog circuitry, you should improve the design.

- If relevant in your project, confirm that signals on any high-speed outp busses (e.g., USB) look correct, especially in terms of expected rise anc times, noise, and any periodic glitches. Oscilloscope "eye diagrams" ca help.
- As a final test, observe the circuit with IC supply voltage reduced 10-2 from the design goal. If the digital circuitry continues to operate corre you likely have a good safety margin when it comes to switching noise

What about the "1 nF / 10 nF / 100 nF" rule?

There is this old adage that for optimal decoupling, you must combine at l three capacitors, one or two decades (orders of magnitude) apart. The exa progression of recommended values changes from one oral account to another, but the bottom line is that if you don't heed the warning, some terrible fate awaits.

The advice made some sense back when each of these capacitors would b made in a different technology. The lowest capacitance would be ceramic, offering low impedance but not packing enough punch to smooth out long lasting flukes; the middle cap could be tantalum, offering balanced performance but not excelling in any dimension; and the last one would b aluminum electrolytic, delivering poor high-frequency response but storin quite a bit of juice.

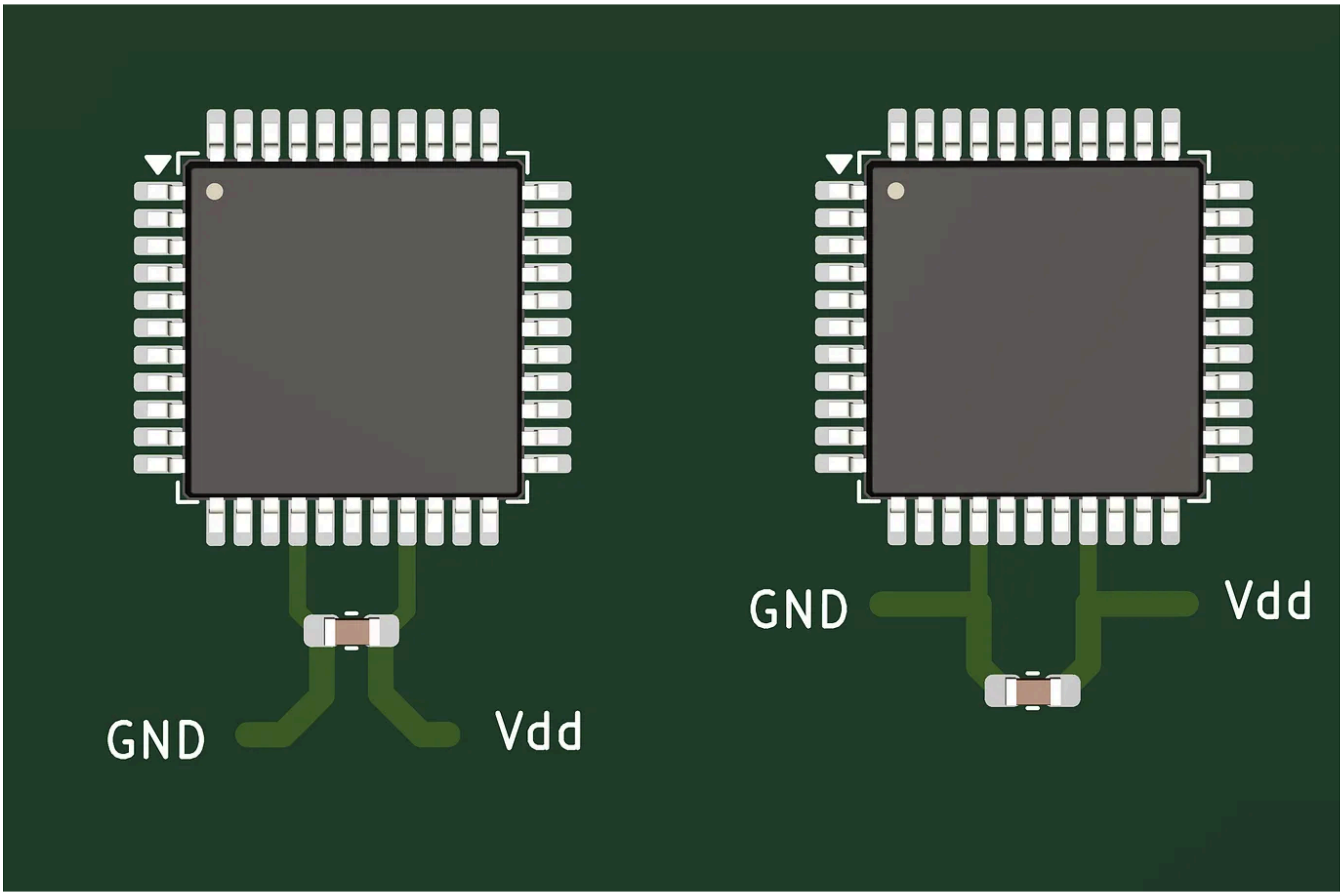
Today, low-cost MLCCs combine high capacitance and low impedance acr a wide range of frequencies, so there's usually little to be gained by playing such tricks — at least not for circuits operating at "hobby" speeds. A single nF or 1 µF MLCC per each functionally distinct digital voltage supply line is almost always enough.

It is true that at very high frequencies — hundreds of megahertz — the capacitor's residual inductance becomes a limiting factor. At that point, combining multiple different capacitors can offer somewhat better wideba noise suppression at the expense of potentially creating undesirable anti-resonance peaks in the system (rendering it ineffective at dealing with a handful of specific frequencies). That said, a simpler solution with fewer si effects is to use a specialized low-inductance ("low-ESL") MLCC.

What about PCB layout?

As discussed earlier on, it's important to keep decoupling capacitors reasonably close to integrated circuits; the resistance and inductance of lo traces prevents the caps from doing their job. As a rule of thumb, keep the distance under 1-2 cm whenever practical.

On the flip side, it's best not to get sidetracked with more exotic advice fo on the internet. One persistent claim is that the layout on the left is dramatically better than the one on the right:



Capacitor placement, taken to the extreme.

As the story goes, in the first circuit, voltage spikes reach the capacitor fir allowing it to kick in before the noise "spills over" onto the supply lines. In second layout, the capacitor is supposedly reached too late. Don't get me wrong: signal propagation speeds sometimes need to be taken into accour PCB design. That said, across such tiny distances, it doesn't matter unless you're working with multi-gigahertz signals — and in that frequency range your standard MLCC isn't of much help.

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