## High-aspect-ratio silicon dioxide pillars

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This paper presents a technique for fabricating high-aspect-ratio silicon dioxide pillars by electrochemical etching of n-type silicon in hydrofluoric acid (HF) solutions. Basic process flow and etching conditions are described, which make it possible to obtain high-aspect-ratio pillar arrays with good uniformity. Pillar arrays of different dimensions (i.e. diameter and separation) and of different arrangements can be produced in a single etch step on the same wafer. The large surface area makes these pillar arrays possible candidates for applications in biological sensing.

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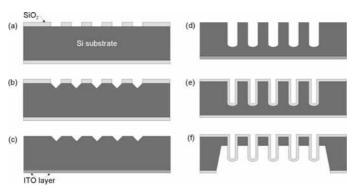
Macroporous silicon, also called coherent porous silicon (CPS), produced by masked electrochemical etching of silicon has proved to be a promising material for a wide variety of electronic and optical devices. Ordered macropore arrays with pore diameters below 1 µm and depth up to the wafer thickness are achievable and are good candidates for applications as IR photonic crystals [1,2]. Taking profit of its geometrical structure, applications in the field of sensors and microsystems have been suggested: membranes [3], cooling devices [4], high-aspect-ratio interconnections [5], etc. Macroporous silicon has been used as a starting material to obtain silicon needles by successive oxidation and oxide etching [6]. Very recently, small silicon dioxide pillars, fabricated on the front side of a silicon wafer have been proposed for DNA separation [7]. Here, starting from macroporous silicon fabrication we show a technique that makes it possible to obtain high-aspect-ratio silicon dioxide (SiO<sub>2</sub>) pillars on the backside of a silicon wafer. The uniformity and the dimensions of these pillar arrays depend only on the etching conditions that ensure a stable growth of high-aspect-ratio macropores.

The key technique in silicon dioxide pillar fabrication is the macropore formation by electrochemical etching of n-type silicon in HF solution [8]. The wafer is mounted in an electrochemical cell with the front side in contact with the electrolyte. Then, a positive voltage is applied to the silicon against the platinum counter electrode. The pore formation mechanism is ruled by the reverse-biased space-charge region (SCR) [8-11] at silicon-electrolyte interface. The positive carriers (holes), required for anodic dissolution of silicon, are focused by the SCR mainly at the pore tips. Consequently, the pores grow in perpendicular to the surface direction and pore walls become passivated against dissolution. In n-type silicon, holes are minority carriers and must be photogenerated from the backside of the wafer. A 100 W halogen lamp was used, coupled to an IR cut-off filter to prevent hole generation near the surface.

Stable pore growth and well-ordered macropore arrays are only achievable if etching parameters, such as HF concentration, doping level, applied voltage and photogenerated current, are properly adjusted. HF

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electrolytes of various concentrations were tested in order to achieve stable pore growth and aspect ratios (pore depth/pore diameter) over 100. Diffusional limitations are known to be a source of degeneration for the uniform formation of deep (high-aspect-ratio) pores [10]. Low HF concentrations (between 2 and 6%) must be used in order to obtain uniform pores of depth up to the wafer thickness. Bubbles caused by hydrogen gas evolution are another source of degeneration. Bubbles stick to the sample surface and prevent the fresh electrolyte from reaching the hole tips. This problem is commonly avoided by adding ethanol or surfactants to reduce the surface tension at silicon-electrolyte interface. We used a small amount (few drops per liter) of the non-ionic surfactant Triton X-100. The applied voltage and the generated photocurrent need to be controlled during the etching in order to obtain a constant pore diameter in depth. Values between 2 and 10 mA/cm² for the current density and between 1 and 2 V for the applied voltage were found to be the optimal conditions for obtaining uniform pores with diameters between 2 and 4 µm.

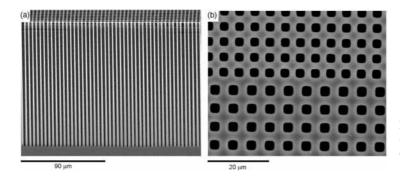


**Fig. 1** Basic process sequence for micropillar fabrication: (a) thermal oxidation and photolithography of the oxide layer; (b) formation of the initial pits by TMAH etching; (c) ITO sputtering for the backside electrode; (d) formation of the macropores by electrochemical etching; (e) thermal oxidation along the macropores and (f) TMAH etching of backside silicon.

The basic process flow for pillar fabrication is given in Fig. 1. The starting material was n-type (100) silicon wafers with a resistivity of 2-6  $\Omega$ .cm. First, a silicon dioxide layer (1000 Å) was grown on the wafers by thermal oxidation. Next, the oxide layer on the front side of the wafer was patterned by a standard photolithographic process and subsequent wet etching in a buffered hydrofluoric acid (BHF) (Fig. 1a). Pyramidal notches which serve as nucleation centers for pore growth were then created by tetramethyl ammonium hydroxide (TMAH) 25 wt.% etching at 80°C for few minutes (Fig. 1b). After removing the SiO<sub>2</sub> layer, a transparent ohmic contact was made on the backside of the wafer by indium thin oxide (ITO) sputtering (Fig. 1c). Then, macropores were formed by electrochemical etching in 2.5 wt.% aqueous HF electrolyte with Triton-X surfactant at room temperature (Fig. 1d). The applied voltage was in the range 1.5-2 V. The current density was 4 mA/cm² and was kept constant during the etching by adjusting backside illumination. Etching times of 240 min led to a depth of about 135  $\mu$ m. This results in a mean etch rate of about 0.56  $\mu$ m/min. After etching, the backside ITO contact was removed by short HF 5% dip.

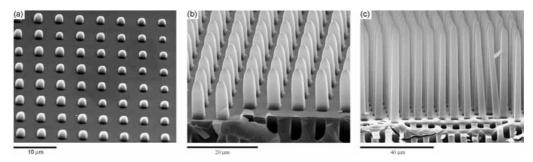
Next, wafers were thermally oxidized in dry oxygen at 1100°C for 190 minutes to obtain an oxide thickness of about 2100 Å (Fig. 1e). Pore diameter and separation can be finely tuned by successive oxidation/etching steps. Electrochemical etching produces macropores with rounded square shapes [8]. Performing successive oxidation/etching steps provides circular holes with very good uniformity in both diameter and spacing. Care should be taken with oxidation induced stress. Thinner oxide layers, lower temperatures and shallower pores minimize this problem.

Finally, the oxide layer on the backside of the wafer was patterned to open the windows where silicon should be removed. The last step is etching of silicon in TMAH solution to release the pillars (Fig. 1f). This is done at 85°C in 25% TMAH solution. The oxide within the pores is resistant to the TMAH etch. Consequently, when the membrane is thin enough silicon dioxide tips begin to appear on the backside of the wafer.



**Fig. 2** Cross-sectional (a) and plain (b) views of macropores before the oxidation.

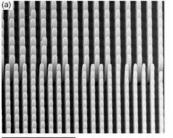
In the experimental conditions described, macropore arrays up to 135  $\mu$ m depth were obtained in 240 minutes. Pores with a diameter of 2.5  $\mu$ m and a pitch of 4  $\mu$ m are shown in Fig. 2a. It can be observed that the pores exhibit a conical shape with decreasing of their diameter in depth. This effect cannot be ascribed to diffusional limitations because the diffusion-related phenomenon usually yields pores with increasing of their diameter in depth for constant current density. Our experiments have shown that when the current density is kept constant during the etching this always leads to conical pores with decreased diameter. The results suggest that pore walls are not completely passivated against the dissolution and this pore-wall dissolution, even it is low, should not be neglected. We found that the present conicity of pores depends on the temperature and on the added surfactants. This effect will be discussed in further publications. Fig. 2b shows two regions with different patterning, which can be simultaneously etched on the same sample. In fact, the pitch of the patterns across the sample surface can be scaled by a maximum factor of about three [11].



**Fig. 3** SEM micrographs of silicon dioxide pillars after TMAH etching of silicon: (a) silicon dioxide tips; (b) and (c) longer silicon dioxide pillars

In Fig. 3 we show examples of  $SiO_2$  pillars released after the silicon has been etched back. Samples were etched for different times, thus revealing pillars of different heights. In Fig. 3a etching was stopped just when the pillars were reached. The geometry of the pillar tips is almost hemispherical. Figures 3b and 3c show higher pillar arrays which were obtained through longer silicon etch. Some pillars were broken when the wafer was cleaved for SEM inspection. The samples have been tilted for better observation. In Fig. 3b the pillars have a diameter of about 3  $\mu$ m and height of about 14  $\mu$ m. In Fig. 3c the pillars are 48  $\mu$ m high. The silicon can be completely removed and the pillar height is then equal to the macropore depth. Even in this case the structural characteristics of the pillars are still good.

The pillar arrangement is determined by the pre-etching pattern. By adjusting such etching conditions as wafer resistivity and photogenerated current, a wide variety of pores and, thus, pillar arrangements can be achieved. In Fig. 4a are shown two square patterns of pillars arrays with different dimensions, which were obtained in a single etch step. Fig. 4b shows silicon dioxide pillars ordered in a triangular lattice.



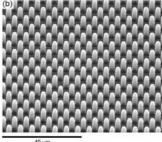


Fig. 4 SEM micrographs showing silicon dioxide pillars of different patterning: (a) two square patterns of pillar arrays with different dimensions; (b) pillar arrays in a triangular arrangement.

In conclusion, we have presented a technique for fabrication of silicon dioxide micro-pillars, based on the electrochemical etching of silicon. High-aspect-ratio pillars are achievable, the only limiting factor being the etching conditions that ensure stable pore growth. The pillar arrays show good structural characteristics and mechanical stability. The proposed technology enlarges the designer toolbox in different fields. New applications can be envisaged. For instance, in Fig. 5a we show SiO<sub>2</sub> pillar arrays inside of a set of truncated pyramids. Figure 5b shows closer view to one pyramid and, Fig. 5c and 5d show pyramids with different pillar arrangements inside. The fabrication procedure is just the same as described above, selecting smaller mask for the back silicon etch. As the etching is anisotropic, the size of the mask together with the etching time determine the dimensions of the pyramid. A large number of these structures can be fabricated on a single wafer. Each one of those truncated pyramids can be used for detection of different molecular binding events [12, 13] increasing at the same time the contact area between probes and target molecules due to the presence of the pillars. The probe molecules can be immobilized on the pillar surface. In this way the third dimension (pillar height) is exploited which can improve the intermixing between the molecules because of the closer contact, provided between the analyte and probe. The contact area can be further increased by downscaling of the pillar dimensions (diameter and separation) in the submicrometer range. Pore arrays with pitch as low as 0.5 µm have been reported so far [14].

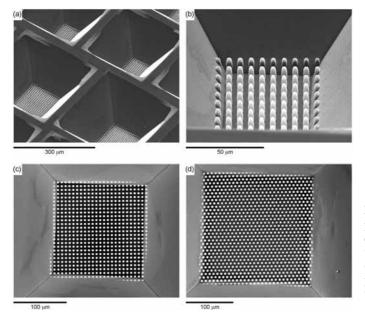


Fig. 5 Micro-pillars inside of truncated pyramids which could be used as three dimensional sensor platforms: (a) general view of a set of pyramids with micro-pillar; (b) closer view of one pyramid; (c) and (d) pyramids with micro-pillars in square and triangular arrangements.

In another field of applications the pillars can be filled from the front side and the silicon dioxide easily eliminated resulting in pillar arrays of different materials. Alternatively, pillars can be used as a mold and after etching high aspect ratio macropores in unusual materials could be obtained.

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