SRIO VIP RELEASE NOTES

Revision	Author	Date	Change Description
1.0	MV	04/26/2013	Initial Release.
1.1	MV	06/04/2013	More logics related to 1.x and 2.x.
1.2	MV	07/26/2013	GEN3 Support.
1.3	MV	09/20/2013	TXRX model support, more GEN3 features.
1.3.1	MV	10/07/2013	Fix for Bug#249 and randomizing idle2 sequence length.
1.3.2	MV	11/08/2013	Fix for Bug#250 and multiple Ack id support.
1.3.3	MV	12/02/2013	Fix for transmit flow control.
1.3.4	MV	12/16/2013	Control symbol enhancement in GEN3.
1.3.5	MV	12/30/2013	Fix for Link CRC32
1.3.6	MV	01/29/2014	Fix for Tracker,Bug#251

1.3.7	MV	02/11/2014	Fix for Bug#252, CRF option Included
1.3.8	MV	02/28/2014	Fixed CRC24 calculation in control symbol
1.3.9	MV	03/20/2014	Update for Gen3 Link response , xamsbs, deskewing
1.3.10	MV	04/11/2014	Update for link request timeout
1.3.11	MV	04/23/2014	Update for Packet and Control symbol transmission
1.3.12	MV	05/14/2014	Update for retry clearing on link request
1.3.13	MV	05/26/2014	Update for Asym State Machine Display
1.3.14	MV	06/10/2014	Added "UVM_DISABLE_AUTO_ITEM_RECORDING"
1.3.15	MV	06/30/2014	Added code to avoid VCS associative array issue for versions lesser than 2014.03
1.3.16	MV	07/30/2014	Fixed AET code to transmit commands continuosly
1.3.17	MV	08/28/2014	Fixed entering IES before link is initialized
1.3.18	MV	09/05/2014	Fix - Bug#253 not entering IRS when Stomp is received
1.3.19	MV	09/10/2014	Fix - Not entering IRS when Stomp is received-Gen3
1.3.20	MV	09/25/2014	Fixes for KRRR in Idle2 and skip, packet check in Idle3
1.3.21	MV	10/07/2014	Update – Slip alignment for DME in parallel mode
1.3.22	MV	10/15/2014	Fix - Slip alignment for DME in parallel mode
1.3.23	MV	11/3/2014	Update – Option to control max pkt size err cause filed
1.3.24	MV	11/11/2014	Fix- Ackid status in Link response, PNAC CS in PD Err, CW Alignment in Parallel mode
1.3.25	MV	11/24/2014	Fix – Error during unexpected stomp/restart from retry CS
1.3.26	MV	12/01/2014	Fix- Errors during 2x to 1x transition
1.3.27	MV	12/12/2014	Update – CW Slip alignment in parallel mode; Fix- Unexpected Packet Accepted Control symbol
1.3.28	MV	12/24/2014	Fix – State Machine Transition request, reset clock compensation in silent ,update ackid status in link response
1.3.29	MV	01/30/2015	Updated Testcases
1.3.30	MV	02/24/2015	Gen3 DME fixes
1.3.31	MV	03/25/2015	Updated Testcases, Parallel mode fix, Gen3 update
1.3.32	MV	05/05/2015	Fixes to clear warnings on tx_monitor
1.3.33	MV	05/07/2015	Reg model fixes / updates in testcases
1.3.34	MV	05/21/2015	Reg model updates
1.3.35	MV	06/09/2015	Env config to reset ackids/ VCS error fixes
1.3.36	MV	06/19/2015	Fix-Reorder for priority on retry

Table of Contents

1. Introduction

This document contains details about the SRIO VIP release.

2. Purpose

This document is for RTA members, for using SRIO VIP. It also serves the purpose of reference for Mobiveil about the fixes/patches/modifications/enhancements done at each SRIO VIP release for RTA.

3. SRIO VIP Release Database

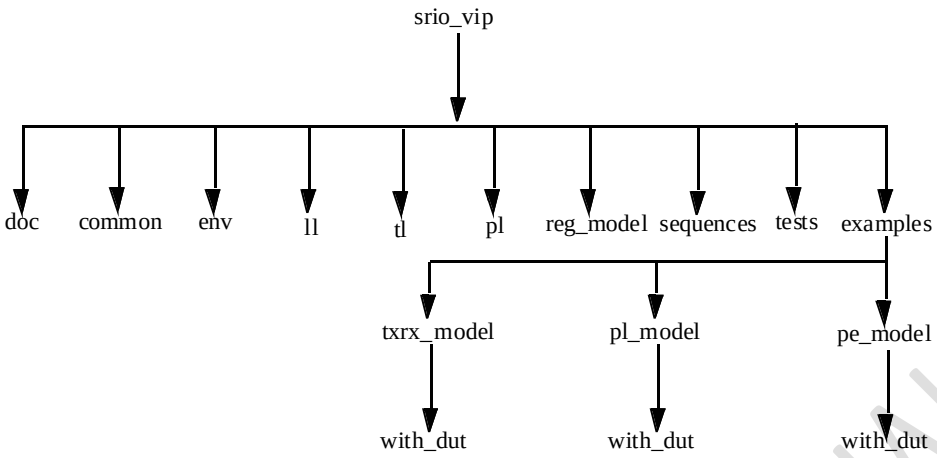
The release database is uploaded to RTA's CVS repository and tagged with RELEASE_SRIO_VIP_V_1_3_P36.

To check out the release, follow the below instructions –

1. setenv CVSROOT :pserver:<user name>@workspace.rapidio.org:/home/rapidio/var/cvs
2. cvs login
3. cvs co –r RELEASE_SRIO_VIP_V_1_3_P36 srio-vip

3.1 Release Database Structure

srio-vip	: the complete data base
doc	: contains the documents
ll	: contains logical layer agent's files
tl	: contains transport layer agent's files
pl	: contains the physical layers agent's files
common	: contains sequence item and interface files
env	: contains srio env files
reg_model	: contains register model files
sequences	: contains sequences for PL,TL and LL
tests	: contains test cases for PL,TL and LL
examples	: contains PE/PL/TXRX model back to back setup



3.2 Running Simulation

To run any simulation follow the below procedure.

Set the SRIO VIP Path.

setenv SRIO_VIP_PATH <Path of the srio-vip directory>

Set the UVM library path.

setenv UVM_PATH <Path of the UVM library>

VCS users need to also set the following variable.

setenv VCS_UVM_HOME $UVM_PATH/src

PE Model.

Run the simulation from srio-vip/examples/pe_model directory.

Example RUN command:

./RUN -test srio_ll_nread_req_test

PL Model.

Run the simulation from srio-vip/examples/pl_model directory.

Example RUN command:

./RUN -test srio_pl_nwrite_swrite_req_test

TXRX Model.

Run the simulation from srio-vip/examples/txrx_model directory.

Example RUN command:

./RUN -test srio_txrx_model_test

4. Features / Enhancements / Patches

Release 1.3.36:

Features Included:

- Fix – "Out of Bound Access" Errors in VCS
- Fix – Packets are reordered based on priority on receiving retry

Release 1.3.35:

Features Included:

- Fix – "Out of Bound Access" Errors in VCS
- Update - Added env config variable "reset ackid" to reset BFM ackid

Release 1.3.34:

Features Included:

- Updates – Reg Model

Release 1.3.33:

Features Included:

- Fix/Updates – Reg Model/testcases

Release 1.3.32:

Features Included:

- Fix – Gen3 tx_monitor warnings - IDLE3_SEQUENCE_DIFFERENT_SC_CW_IN_SC_OS_CHECK

Release 1.3.31:

Features Included:

- Fix – Gen3 transmission controlled during silent
- Fix – Gen2 errors fixed for vcs in parallel mode
- Update - Testcases

Release 1.3.30:

Features Included:

- Fix – Gen3 DME Manchester encoding, pattern generation and transmission control
- Fix – Gen3 Packet byte count with embedded control symbol

Release 1.3.29:

Features Included:

- Updated Testcases

Release 1.3.28:

Features Included:

- Fix – State Machine Transition request fix for X1 modes
- Fix – Update expected ackid status on link response
- Fix – Reset Clock Compensation counter in Silent state

Release 1.3.27:

Features Included:

- Update – CW Slip Alignment in parallel mode for Gen3
- Fix – Unexpected Packet Accepted control Symbol when errors are detected and link request is generated from the sequence.

Release 1.3.26:

Features Included:

- Fix – Errors during 2x to 1x transition on 1x mode detection

Release 1.3.25:

Features Included:

- Fix – Error state for Unexpected Stomp and Restart from Retry Control Symbol
- Update – If IES , mark as error state even if link request is transmitted without PNAC CS

Release 1.3.24:

Features Included:

- Fix – AckId Status in Link Response Control Symbol
- Fix – Generation of Packet Not Accepted Control Symbol for Control Symbol delimiter error

- Update – CodeWord Alignment in Parallel mode for Gen3

Release 1.3.23:

Features Included:

- Update – Option to control the cause field for max packet size error

Release 1.3.22:

Features Included:

- Fix – Slip Alignment for DME in parallel mode for Gen3

Release 1.3.21:

Features Included:

- Update – Slip Alignment for DME in parallel mode for Gen3

Release 1.3.20:

Features Included:

- Fix – Idle2 termination for transmitting KRRR has been fixed
- Fix - For tx monitor, data needs to collected on tx_clk. This was done on rx_clk earlier
- Fix - For Idle3, descrambling is fixed for skip control word
- Fix – For Idle3, packet checker when control symbol was embedded before EOP control symbol was fixed

Release 1.3.19:

Features Included:

Fix – Updated to enter IES state when packet is cancelled with Stomp when not in error or retry state for Gen3

Release 1.3.18:

Features Included:

Fix – Updated to enter IES state when packet is cancelled with Stomp when not in error or retry state for Bug #253

Release 1.3.17:

Features Included:

- Fix – Updated to prevent BFM from entering into IES state before link is initialized

Release 1.3.16:

Features Included:

- Fix – AET to transmit configured number of commands continuously

Release 1.3.15:

Features Included:

- Update – Added code to avoid VCS associative array issues for versions lower than mx-vI-2014.03. Define to be used for this is VCS_ASS_ARR_FIX

Release 1.3.14:

Features Included:

- Update – Added UVM_DISABLE_AUTO_ITEM_RECORDING for pipelined operations

Release 1.3.13:

Features Included:

- Update – Asymmetric State Machine display

Release 1.3.12:

Features Included:

- Fix – Control Symbol CRC error detection in error/retry state
- Fix – Status Control Symbol rate for Link Request
- Fix – Link Response param1 in Gen3
- Fix – Packet Ackid issues when in both error and retry state
- Fix – Stomp CS transmission in other control symbols during retry/error state
- Fix – Control symbol ackid error in retry/error state
- Fix – Idle2 Termination for Link Request
- Fix – Clear retry state on Link Request Control Symbol

Release 1.3.11:

Features Included:

- Update – Packet Transmission in IES/IRS state
- Update – Control Symbol Transmission,Idle2 Check, Error state on Link timeout

- Fix - Stop lane transmission during silent

Release 1.3.10:

Features Included:

- Update – 'scramble_dis' variable moved to srio_env_config.svh to allow control from callback
- Update – Events to indicate timeout added in srio_env_config.svh
- Update – Random cause insertion for Packet Not Accepted Control Symbol
- Update – Exiting Retry state upon receiving link request
- Update – Packet Not Accepted Control Symbol for Errors detected
- Update – Detection of error free BIP
- Fix – Error in Packet Ackid in IRS/ORS state
- Fix – AET error for ack after command goes low

Release 1.3.9:

Features Included:

- GEN3 – Update in Link Response check
- Updates in deskewing logic, Error detection
- Fix in extended address formation

Release 1.3.8:

Features Included:

- GEN3 – Fixed CRC24 for Control Symbol
- Updates in Lane BIP Calculation

Release 1.3.7:

Features Included:

- CRF Support Option has been included
- Fix for Bug#252
- Fix for Gen3 Packet Termination with Descrambler Seed Sequence

Release 1.3.6:

Features Included:

- Fix for Bug#251
- Fix for Gen3 Tracker Display
- Idle Detection after sync

Release 1.3.5:

Features Included:

• Link CRC32 Fix

Release 1.3.4:

Features Included:

- Packet termination with Restart_From_Retry/LinkRequest Control Symbol
- Control Symbol enhancements in Gen3

Release 1.3.3:

Features Included:

- Fix for Transmit Flow Control

Release 1.3.2:

Features Included:

- Multiple AckID support feature enhancement
- Fast Recovery Option
- Packet Termination with SOP
- Fix for Bug# 250

Release 1.3.1:

Features Included:

- Randomizing Idle2 sequence length
- Modifications on Idle2 termination
- Fix for Bug #249

Release 1.3:

Features Included:

- Asymmetric mode
- Timing Synchronization
- TxRx Model support
- More comments included in the code
- More compliance test cases
- More functional coverage

Release 1.2:

Features Included:

- Initial version of GEN3 logic
- PL Model Support
- Feedback from member companies incorporated
- More comments included in the code
- More compliance test cases
- More functional Coverage

Features Not Supported:

- Asymmetric Mode
- Timing Synchronization
- TxRx Model

Release 1.1:

Features Included:

- Advanced Equalization Training
- Error injection, detection and handling
- Multi VC Support
- More compliance test cases
- More functional Coverage
- Multiple VC Support
- GSM packet type
- Tracker Files

Features Not Supported:

- Specification Version 3.0

Release 1.0:

Features Supported:

- Specification Versions 1.3,2.1 and 2.2
- Number of lanes 1,2,4,8 and 16
- All Baud rates applicable for 1.x and 2.x
- Compliance test cases
- Functional Coverage

Features Not Supported:

- Specification Version 3.0
- Advanced Equalization Training

- Error injection, detection and handling
- Multiple VC support
- GSM packet type
- Tracker Files

5. Sequences

Following table lists the sequences available in this release.

S.No	Sequence Name	Description
Logical Layer		
1.	srio_ll_nread_req_seq	Creates random nread request transactions
2.	srio_ll_nwrite_req_seq	Creates random nwrite request transactions
3.	srio_ll_nwrite_r_req_seq	Creates random nwrite_r request transactions
4.	srio_ll_swrite_req_seq	Creates random swrite request transactions
5.	srio_ll_atomic_inc_seq	Creates random Atomic Increment transactions
6.	srio_ll_atomic_dec_seq	Creates random Atomic Decrement transactions
7.	srio_ll_atomic_set_seq	Creates random Atomic Set transactions
8.	srio_ll_atomic_clr_seq	Creates random Atomic Clear transactions
9.	srio_ll_atomic_swap_seq	Creates random Atomic swap transactions
10.	srio_ll_atomic_test_and_swap_seq	Creates random Atomic Test-and-Swap transactions
11.	srio_ll_compare_and_swap_seq	Creates random Atomic Compare-and- Swap transactions
12.	srio_ll_maintenance_rd_req_seq	Creates random Maintenance Read Request transactions
13.	srio_ll_maintenance_wr_req_seq	Creates random Maintenance Write Request transactions
14.	srio_ll_maintenance_port_wr_req_seq	Creates random Maintenance Port Write Request transactions
15.	srio_ll_maintenance_rd_resp_seq	Creates random Maintenance Read Response transactions
16.	srio_ll_message_req_seq	Creates random Data Message Request transaction (includes both single segment and multi segment)
17.	srio_ll_msg_sseg_req_seq	Creates Data Message - Single Segment i.e. Message size should be equal to segment size.
18.	srio_ll_msg_mseg_req_seq	Creates Data Message - Multi Segment i.e. Message size should be greater than segment Size.
19.	srio_ll_doorbell_req_seq	Creates random Doorbell Request transaction
20.	srio_ll_ds_pdu_seq	Creates random Data Streaming transaction (includes both single and multi-segment stream transaction)
21.	srio_ll_ds_sseg_req_seq	Creates Data Streaming -- Single Segment stream. ie., pdulength should be less than or equal to mtu size. Maximum payload is 256B
22.	srio_ll_ds_mseg_req_seq	Creates Data Streaming -- Multi Segment stream. ie., pdulength should be greater than mtu size

		maximum payload is 64K
23.	srio_ll_lfc_flow_arb_spdu_seq	Creates LFC - Flow arbitration with single PDU
24.	srio_ll_lfc_flow_arb_mpdu_seq	Creates LFC - Flow arbitration with Multiple PDU
25.	srio_ll_lfc_orphaned_xoff_seq	Creates LFC - without XON
26.	srio_ll_lfc_multi_xoff_xon_same_flowid_seq	Creates LFC - Same FlowID with Multiple XOFF and XON Count
27.	srio_ll_lfc_multi_xoff_xon_diff_flowid_seq	Creates LFC - Different FlowID with Multiple XOFF and XON Count
28.	srio_ll_lfc_xoff_xon_seq	Creates LFC - Normal XOFF and XON Sequence
29.	srio_ll_lfc_xon_without_xoff_seq	Creates LFC - Without XOFF Only XON
30.	srio_ll_lfc_timeout_check_seq	Creates LFC - XOFF Count > XON, XON Count > XOFF
31.	srio_ll_lfc_with_diff_id_seq	Creates LFC - XOFF with different SrcID and TargetID transaction
32.	srio_ll_lfc_with_diff_flowid_seq	Creates LFC - XOFF with different flowID - Priority and CRF transaction
33.	srio_ll_lfc_multi_orphaned_xoff_seq	Creates LFC - Multiple Orphaned XOFF transaction
34.	srio_ll_gsm_rd_owner_seq	Creates random GSM Read Owner transaction
35.	srio_ll_gsm_rd_to_own_owner_seq_seq	Creates random GSM Read to Own Owner transaction
36.	srio_ll_gsm_io_rd_owner_seq	Creates random GSM IO Read Owner transaction
37.	srio_ll_gsm_rd_home_seq	Creates random GSM Read Home transaction
38.	srio_ll_gsm_rd_to_own_home_seq	Creates random GSM Read to Own Home transaction
39.	srio_ll_gsm_io_rd_home_seq	Creates random GSM IO Read Home transaction
40.	srio_ll_gsm_dkill_home_seq	Creates random GSM DKill Home transaction
41.	srio_ll_gsm_ikill_home_seq	Creates random GSM IKill Home transaction
42.	srio_ll_gsm_tlbie_seq	Creates random GSM TLBIE transaction
43.	srio_ll_gsm_tlbsync_seq	Creates random GSM TLBSYNC transaction
44.	srio_ll_gsm_iread_home_seq	Creates random GSM IRead Home transaction
45.	srio_ll_gsm_ikill_sharer_seq	Creates random GSM IKill Sharer transaction
46.	srio_ll_gsm_dkill_sharer_seq	Creates random GSM DKill Sharer transaction
47.	srio_ll_gsm_castout_seq	Creates random GSM CASTOUT transaction
48.	srio_ll_gsm_flush_with_data_seq	Creates random GSM FLUSH with Data transaction
49.	srio_ll_gsm_flush_without_data_seq	Creates random GSM FLUSH without Data transaction
50.	srio_ll_invalid_ftype_seq	Creates transactions with invalid ftype
51.	srio_ll_io_rdsize_wdptr_err_seq	Creates SRIO IO Operations with rdsize_wdptr Error
52.	srio_ll_io_wrsize_wdptr_err_seq	Creates SRIO IO Operations with wrsize_wdptr Error transaction
53.	srio_ll_atomic_payload_err_seq	
54.	srio_ll_swrite_payload_error_seq	Creates Unsupported payload bytes such as 3,5,6,7 Bytes of transaction
55.	srio_ll_resp_with_payload_seq	Creates random Logical Response with payload

		transaction and covers possible sta-tus values.
56.	srio_ll_resp_without_payload_seq	Creates random Logical Response without payload transaction and covers possible sta-tus values.
57.	srio_ll_ds_pdu_error_seq	Creates Data Streaming packets with invalid PDU
58.	srio_ll_ds_mtu_error_seq	Creates Data Streaming packets with invalid MTU size
59.	srio_ll_ds_sop_error_seq	Creates Data Streaming packets with SOP error transaction
60.	srio_ll_ds_eop_error_seq	Creates Data Streaming packets with EOP error transaction
61.	srio_ll_ds_odd_error_seq	Creates Data Streaming packets with ODD error transaction
62.	srio_ll_ds_pad_error_seq	Creates Data Streaming packets with PAD error transaction
63.	srio_ll_ttype_error_seq	Creates random TTYPE error transaction
64.	srio_ll_resp_pri_error_seq	Creates random illegal response priority transaction
65.	srio_ll_size_error_seq	Creates random packet with size exceed error transaction
66.	srio_ll_payload_exist_error_seq	Creates random packet with payload exist error transaction
67.	srio_ll_doubleword_align_error_seq	Creates random packet with double word alignment error transaction
68.	srio_ll_lfc_pri_error_seq	Creates random LFC – illegal priority sequence
69.	srio_ll_msg_size_error_seq	Creates random Message packet with illegal size error sequence
70.	srio_ll_msgseg_error_seq	Creates random message packet with invalid segment size error sequence.
71.	srio_ll_lfc_user_gen_xoff_seq	Creates LFC user generated xoff sequence
72.	srio_ll_lfc_user_gen_xon_seq	Creates LFC user generated xon sequence
73.	srio_ll_io_random_seq	Creates IO random sequence
74.	srio_ll_ds_mseg_single_mtu_seq	Creates multi segment DS packet with single MTU value sequence
75.	srio_ll_port_resp_timeout_reg_seq	Creates transaction to configure Port Response Timeout Register
76.	srio_ll_all_atomic_req_seq	Creates Maintenance read-write packet to configure Port Response Timeout Register
77.	srio_ll_ds_concurrent_seq	Creates DS packet with valid MTU and PDU length value
78.	srio_ll_ds_max_seg_support_seq	Creates DS packets to support maximum segment sequence
79.	srio_ll_ds_mtu_reserved_seq	Creates DS packet with invalid MTU value sequence
80.	srio_ll_ds_s_e_err_seq	Creates DS packet with invalid Start and End bit sequence
81.	srio_ll_ds_traffic_seq	Creates DS packet with user defined COS and StreamID value sequence
82.	srio_ll_ds_traffic_mgmt_basic_stream_xoff_seq	Creates Traffic Management basic stream xoff packet sequence

83.	srio_ll_ds_traffic_mgmt_basic_stream_xon_seq	Creates Traffic Management basic stream xon packet sequence
84.	srio_ll_normal_ds_payload_size_err_seq	Creates DS payload size Error packet sequence
85.	srio_ll_ds_traffic_mgmt_xtype_err_seq	Creates Traffic Management packet with invalid xtype sequence
86.	srio_ll_ds_traffic_mgmt_user_rate_xoff_seq	Creates user generated Traffic Management xoff packet for rate mode sequence
87.	srio_ll_ds_traffic_mgmt_user_rate_xon_seq	Creates user generated Traffic Management xon packet for rate mode sequence
88.	srio_ll_ds_traffic_mgmt_user_credit_xon_seq	Creates user generated Traffic Management xon packet for credit mode sequence
89.	srio_ll_ds_traffic_mgmt_user_credit_xoff_seq	Creates user generated Traffic Management xoff packet for credit mode sequence
90.	srio_ll_ds_traffic_mgmt_tmop_err_seq	Creates Traffic Management packet with invalid TMOP value sequence
91.	srio_ll_ds_traffic_mgmt_parameter1_err_seq	Creates Traffic Management packet with invalid parameter1 value sequence
92.	srio_ll_ftype_default_seq	Creates packets with random ftype values sequence
93.	srio_ll_lfc_unsupport_flowid_seq	Creates LFC packet with unsupportedflowID value sequence
94.	srio_ll_maintenance_wr_rd_seq	Create maintenance read-write packets to configure all registers sequence
95.	srio_ll_lfc_xon_arb_0_seq	Creates LFC flow arbitration XON sequence number 0
96.	srio_ll_lfc_xon_arb_1_seq	Create LFC flow arbitration XON sequence number 1
97.	srio_ll_lfc_ds_single_pdu_arb_seq	Creates FAM DS single PDU sequence
98.	srio_ll_lfc_ds_multi_pdu_arb_seq	Creates FAM DS multi PDU sequence
99.	srio_ll_lfc_request_flow_spdu_1_seq	Creates FAM request for single PDU sequence number 0
100.	srio_ll_lfc_request_flow_spdu_0_seq	Creates FAM request for single PDU sequence number 0
101.	srio_ll_lfc_release_0_seq	Creates FAM release for sequence number 0
102.	srio_ll_lfc_release_1_seq	Creates FAM release for sequence for 1
103.	srio_ll_flow_arb_support_reg_seq	Creates FAM support enable sequence
104.	srio_ll_lfc_request_flow_mpdu_1_seq	Creates FAM request for multi PDU sequence number 1
105.	srio_ll_lfc_request_flow_mpdu_0_seq	Creates FAM request for multi PDU sequence number 0
106.	srio_ll_traffic_mgmt_tm_type_mode_err_seq	Creates Traffic Management packet with invalid TM_Mode value sequence
107.	srio_ll_ds_traffic_mgmt_mask_err_seq	Creates Traffic Management packet with invalid mask value sequence
108.	srio_ll_ds_traffic_mgmt_diff_operation_seq	Creates Traffic Management packet for different operation sequence
109.	srio_ll_ds_traffic_mgmt_user_credit_err_seq	Creates user generated Traffic Management packet with credit support and invalid parameter values sequence

110.	srio_ll_ds_traffic_mgmt_specific_stream_xoff_seq	Creates Traffic Management packet for specific Stream xoff sequence
111.	srio_ll_ds_traffic_mgmt_specific_stream_xon_seq	Creates Traffic Management packet for specific Stream xon sequence
112.	srio_ll_ds_traffic_mgmt_specific_cos_xoff_seq	Creates Traffic Management packet for specific COS xoff sequence
113.	srio_ll_ds_traffic_mgmt_specific_cos_xon_seq	Creates Traffic Management packet for specific COS xon sequence
114.	srio_ll_ds_traffic_mgmt_group_of_cos_xoff_seq	Creates Traffic Management packet for Group of COS xoff sequence
115.	srio_ll_ds_traffic_mgmt_group_of_cos_xon_seq	Creates Traffic Management packet for Group of COS xon sequence
116.	srio_ll_ds_traffic_mgmt_random_cos_xoff_seq	Creates Traffic Management packet for random of COS xoff sequence
117.	srio_ll_ds_traffic_mgmt_random_cos_xon_seq	Creates Traffic Management packet for random of COS xon sequence
118.	srio_ll_lfc_ds_seq	Creates DS packet with valid Priority and Crf value sequence
119.	srio_ll_ds_all_traffic_xoff_seq	Creates Traffic Management packet for all traffic xoff sequence
120.	srio_ll_ds_all_traffic_xon_seq	Creates Traffic Management packet for all traffic xon sequence
121.	srio_ll_nwrite_nread_34_addr_seq	Creates NWRITE and NREAD with 34 bits addressing bit packets sequence
122.	srio_ll_nwrite_nread_50_addr_seq	Creates NWRITE and NREAD with 50 bits addressing bit packets sequence
123.	srio_ll_nwrite_nread_66_addr_seq	Creates NWRITE and NREAD with 66 bits addressing bit packets sequence
124.	srio_ll_lfc_ds_random_prio_seq	Creates DS packet with random priority sequence
125.	srio_ll_nwrite_nread_mem_access_seq	Creates nwrite and nread packets to access memory block sequence
126.	srio_ll_user_gen_random_prio_seq	Creates user generated random priority sequence
127.	srio_ll_maintenance_ds_support_reg_seq	Creates Maintenance read-write packet to configure for DS packet sequence
128.	srio_ll_ds_traffic_random_streamid_seq	Creates DS packet with random StreamID sequence
129.	srio_ll_ds_traffic_random_streamid_cos_seq	Creates DS packet with random StreamID and COS sequence
130.	srio_ll_ds_all_traffic_seq	Creates Traffic Management packed with wild card 3'b111 sequence
131.	srio_ll_ds_all_traffic_mgmt_credit_control_seq	Creates Traffic Management packet with credit control sequence
132.	srio_ll_illegal_io_seq	Creates IO packets with illegal ttype,rd_size and wr_size sequence
133.	srio_ll_illegal_gsm_seq	Creates GSM packets with illegal ttype,rd_size and wr_size sequence
134.	srio_ll_illegal_msg_seq	Creates MSG packets with illegal ttype and segments sequence
135.	srio_ll_vc_lfc_xon_seq	Creates LFC xon packet with multi VC support

		sequence
136.	srio_ll_vc_lfc_xoff_seq	Creates LFC xon packet with multi VC support sequence
137.	srio_ll_vc_ds_mseg_req_seq	Creates DS multi segments packet with multi VC support sequence
138.	srio_ll_multi_vc_nwrite_swrite_seq	Creates nwrite and swrite packet with multi VC support sequence
139.	srio_ll_msg_mseg_req_with_err_seq	Creates message packets with invalid length sequence
140.	srio_ll_msg_mseg_max_req_seq	Creates message packets with maximum length sequence
141.	srio_ll_ds_traffic_mgmt_random_basic_stream_seq	Creates DS Traffic Management Basic packet with random parameter and specific stream values sequence
142.	srio_ll_ds_traffic_mgmt_random_rate_stream_seq	Creates DS Traffic Management Rate packets with random parameter and specific stream values sequence
143.	srio_ll_ds_traffic_mgmt_random_credit_stream_seq	Creates DS Traffic Management Credit packets with random parameter and specific stream values sequence
144.	srio_ll_atomic_invalid_size_seq	Creates Atomic packets with illegal size sequence
145.	srio_ll_ds_mseg_req_err_seq	Creates DS multi segment packets with invalid size sequence
146.	srio_ll_ds_max_streamid_seq	Creates DS packets with maximum Stream_ID sequence
147.	srio_ll_msg_unsupported_seq	Creates message packets for unsupported message transition sequence
148.	srio_ll_db_unsupported_seq	Creates message packets for unsupported doorbell transition sequence
149.	srio_ll_outstanding_unack_req_seq	Creates random packets request with maximum unacknowledged request sequence
150.	srio_ll_unexp_msg_resp_req_seq	Creates unexpected message response packets without message request packet sequence
151.	srio_ll_msg_mseg_max_mbox_letter_req_seq	Creates message packets with maximum letter and fixed mbox values sequence
Transport Layer		
152.	srio_tl_pkt_seq	Transport Layer Packet Sequence
153.	srio_tl_pkt_err_seq	Transport Layer Packet Sequence with error (eg., corrupt tt field)
154.	srio_tl_rand_all_packets_seq	Generates all types of packets.
155.	srio_tl_rand_all_packets_err_seq	Generates all types of packets with errors injected.
156.	srio_tl_pkt_tt_seq	Generated TL packet with TT sequence
Physical Layer		
157.	srio_pl_pkt_acc_cs_seq	Packet Accepted CS Sequence
158.	srio_pl_pkt_rty_cs_seq	Packet Retry CS Sequence
159.	srio_pl_pkt_na_cs_seq	Packet Not Accepted CS Sequence
160.	srio_pl_status_cs_seq	Status CS Sequence
161.	srio_pl_vc_st_cs_seq	VC Status CS Sequence
162.	srio_pl_link_res_cs_seq	Link Request CS Sequence

163.	srio_pl_dis_nxmode_sm_seq	Discovery to Nxmode state transition sequence
164.	srio_pl_dis_2xmode_sm_seq	Discovery to 2xmode state transition sequence
165.	srio_pl_dis_1xmode_ln0_sm_seq	Discovery to 1xmode_lane0 state transition sequence
166.	srio_pl_dis_1xmode_ln1_sm_seq	Discovery to 1xmode_lane1 state transition sequence
167.	srio_pl_dis_1xmode_ln2_sm_seq	Discovery to 1xmode_lane2 state transition sequence
168.	srio_pl_dis_sl_sm_seq	Discovery to Silent state transition sequence
169.	srio_pl_nxmode_sl_sm_seq	Nxmode to Silent state transition sequence
170.	srio_pl_nxmode_dis_sm_seq	Nxmode to Discovery state transition sequence
171.	srio_pl_2xmode_sl_sm_seq	2xmode to Silent state transition sequence
172.	srio_pl_2xmode_2x_rec_sm_seq	2xmode to 2x recovery state transition sequence
173.	srio_pl_1xmode_ln0_sl_sm_seq	1xmode lane0 to Silent state transition sequence
174.	srio_pl_1xmode_ln0_1x_rec_sm_seq	1xmode lane0 to 1x recovery state transition sequence
175.	srio_pl_1xmode_ln1_sl_sm_seq	1xmode lane1 to Silent state transition sequence
176.	srio_pl_1xmode_ln1_1x_rec_sm_seq	1xmode lane1 to 1x recovery state transition sequence
177.	srio_pl_1xmode_ln2_sl_sm_seq	1xmode lane2 to Silent state transition sequence
178.	srio_pl_1xmode_ln2_1x_rec_sm_seq	1xmode lane2 to 1x recovery state transition sequence
179.	srio_pl_2x_rec_2xmode_sm_seq	2x Recovery to 2xmode state transition sequence
180.	srio_pl_2x_rec_1xmode_ln0_sm_seq	2x Recovery to 1xmode lane0 state transition sequence
181.	srio_pl_2x_rec_1xmode_ln1_sm_seq	2x Recovery to 1xmode lane1 state transition sequence
182.	srio_pl_2x_rec_sl_sm_seq	2x Recovery to silent state transition sequence
183.	srio_pl_1x_rec_sl_sm_seq	1x Recovery to Silent state transition sequence
184.	srio_pl_1x_rec_1xmode_ln0_sm_seq	1x Recovery to 1xmode lane0 state transition sequence
185.	srio_pl_1x_rec_1xmode_ln1_sm_seq	1x Recovery to 1xmode lane1 state transition sequence
186.	srio_pl_1x_rec_1xmode_ln2_sm_seq	1x Recovery to 1xmode lane2 state transition sequence
187.	srio_pl_pkt_ackid_error_seq	Creates ackid error sequence transaction
188.	srio_pl_pkt_early_crc_error_seq	Creates random early crc error sequence transaction
189.	srio_pl_pkt_final_crc_error_seq	Creates random final CRC error sequence transaction
190.	srio_pl_pkt_illegal_prio_err_seq	Creates illegal priority error sequence transaction

191.	srio_pl_pkt_illegal_crf_error_seq	Creates illegal CRF error sequence transaction
192.	srio_pl_idle2_csfield_corruption_seq	Idle2 csfield corruption sequence
193.	srio_pl_idle2_psr_corruption_seq	Idle2 pseudo random field corruption sequence
194.	srio_pl_idle2_csmarker_corruption_seq	Idle2 cs field marker corruption sequence
195.	srio_pl_idle2_descr_sync_break_seq	Idle2 descrambler sync break sequence
196.	srio_pl_idle2_csfield_truncation_seq	Idle2 cs field truncation sequence
197.	srio_pl_idle2_psr_truncation_seq	Idle2 pseudo random truncation sequence
198.	srio_pl_idle2_csmarker_truncation_seq	Idle2 cs marker truncation sequence
199.	srio_pl_idle2_csfield_update_seq	Idle2 cs field update sequence
200.	srio_pl_force1x_mode_portwidth_override_seq	Force 1x mode port width override sequence
201.	srio_pl_force1x_mode_laner_portwidth_override_seq	Force 1x mode lane R port width override sequence
202.	srio_pl_nxmode_enabled_2x_disabled_portwidth_override_seq	Force Nx mode enabled 2x mode disabled port width override sequence
203.	srio_pl_2xmode_enabled_nx_disabled_portwidth_override_seq	Force 2x mode enabled Nx disabled port width override sequence
204.	srio_pl_force_reinit_seq	Force re-initialization sequence
205.	srio_pl_nx_mode_support_disable_seq	Creates NX mode support disable sequence
206.	srio_pl_x2_mode_support_disable_seq	Creates 2X mode support disable sequence
207.	srio_pl_pkt_na_ackid_err_cs_seq	Creates packet not accepted ackID error sequence
208.	srio_pl_pkt_na_crc_err_cs_seq	Creates packet not accepted CRC error sequence
209.	srio_pl_pkt_na_non_maintenace_rep_stop_cs_seq	Creates packet not accepted non maintenance error sequence
210.	srio_pl_pkt_na_invalid_char_cs_seq	Creates packet not accepted invalid character error sequence
211.	srio_pl_pkt_na_lack_buf_res_cs_seq	Creates packet not accepted lack of buffer error sequence
212.	srio_pl_pkt_na_loss_descr_sync_cs_seq	Creates packet not accepted loss of desr error sequence
213.	srio_pl_nwrite_swrite_req_seq	Creates nwrite and swrite sequence and force it directly to pl sequencer
214.	srio_pl_ll_io_random_seq	Creates IO packets with randomized pl variables sequence
215.	srio_txrx_seq	Creates packets with TxRx status control symbols sequence
216.	srio_pl_sop_nwrite_eop_seq	Creates packet with sop ,nwrite packets and eop control symbol sequence
217.	srio_pl_gen3_sop_padded_seq	Creates GEN3 packets with padded start of packet (sop) sequence
218.	srio_pl_gen3_eop_padded_seq	Creates GEN3 packets with padded end of packets (eop) sequence

6. Test Cases

Following table lists the test cases available in this release.

S.NO	Test Case Name	Description
Logical Layer		
1.	srio_ll_nread_req_test.sv	Creates random nread request transactions
2.	srio_ll_atomic_dec_test.sv	Creates random Atomic Decrement transactions
3.	srio_ll_atomic_set_test.sv	Creates random Atomic Set transactions
4.	srio_ll_atomic_clear_test.sv	Creates random Atomic Clear transactions
5.	srio_ll_nwrite_req_test.sv	Creates random nwrite request transactions
6.	srio_ll_nwrite_r_req_test.sv	Creates random nwrite_r request transactions
7.	srio_ll_atomic_swap_test.sv	Creates random Atomic swap transactions
8.	srio_ll_atomic_compare_and_swap_test.sv	Creates random Atomic Compare-and- Swap transactions
9.	srio_ll_atomic_test_and_swap_test.sv	Creates random Atomic Test-and-Swap transactions
10.	srio_ll_swrite_req_test.sv	Creates random swrite request transactions
11.	srio_ll_lfc_xoff_test.sv	Creates random XOFF sequence
12.	srio_ll_lfc_xon_test.sv	Creates random XON sequence
13.	srio_ll_lfc_xon_xoff_test.sv	Creates LFC - Normal XOFF and XON Sequence
14.	srio_ll_lfc_multi_xon_xoff_same_flowid_test.sv	Creates LFC - Same FlowID with Multiple XOFF and XON Count
15.	srio_ll_lfc_multi_xoff_orphaned_test.sv	Creates LFC - Multiple Orphaned XOFF transaction
16.	srio_ll_lfc_xoff_arb_0_test.sv	Creates LFC flow arbitration xoff arb_0 packet
17.	srio_ll_lfc_xoff_arb_1_test.sv	Creates LFC flow arbitration xoff arb_1 packet
18.	srio_ll_lfc_xoff_release_0_test.sv	Creates LFC flow arbitration xoff release_0 packet
19.	srio_ll_lfc_xoff_release_1_test.sv	Creates LFC flow arbitration xoff release 1 packet
20.	srio_ll_lfc_xoff_request_flow_spdu_1_test.sv	Creates LFC xoff request flow single PDU for sequence 1
21.	srio_ll_lfc_xoff_request_flow_mpdu_1_test.sv	Creates LFC xoff request flow multi PDU for sequence1
22.	srio_ll_lfc_xoff_request_flow_mpdu_0_test.sv	Creates LFC xoff request flow multi PDU for sequence0
23.	srio_ll_lfc_xoff_request_flow_grnt_0_test.sv	Creates LFC xoff request flow granted for sequence 0
24.	srio_ll_lfc_xoff_request_flow_grnt_1_test.sv	Creates LFC xoff request flow granted for sequence 1
25.	srio_ll_maintenance_rd_req_test.sv	Creates random Maintenance Read Request transactions
26.	srio_ll_maintenance_wr_req_test.sv	Creates random Maintenance Write Request transactions
27.	srio_ll_maintenance_rd_resp_req_test.sv	Creates random Maintenance Read Response transactions
28.	srio_ll_maintenance_wr_resp_req_test.sv	Creates random Maintenance Write Request transactions
29.	srio_ll_maintenance_port_wr_req_test.sv	Creates random Maintenance Port Write Request transactions
30.	srio_ll_ds_sseg_req_test.sv	Creates Data Streaming -- Single Segment stream. i.e., pdulength should be less than or equal to mtu size.

		Maximum payload is 256B
31.	srio_ll_ds_mseg_req_test.sv	Creates Data Streaming -- Multi Segment stream. i.e., pdulength should be greater than mtu size maximum payload is 64K
32.	srio_ll_ds_traffic_mgmt_basic_stream_test.sv	Creates random Data Streaming basic Traffic Management transaction
33.	srio_ll_ds_traffic_mgmt_rate_control_test.sv	Creates random Data Streaming rate based control Management transaction
34.	srio_ll_ds_traffic_mgmt_credit_control_test.sv	Creates random Data Streaming credit based control Management transaction
35.	srio_ll_ds_traffic_mgmt_appln_stream_control_test.sv	Creates random Data Streaming traffic management application Stream control Transaction
36.	srio_ll_doorbell_req_test.sv	Creates random Doorbell Request transaction
37.	srio_ll_msg_ssize_8byte_req_test.sv	Creates Data Message Request transaction with seg size as 8 bytes
38.	srio_ll_msg_ssize_16byte_req_test.sv	Creates Data Message Request transaction with seg size as 16 bytes
39.	srio_ll_msg_ssize_32byte_req_test.sv	Creates Data Message Request transaction with seg size as 32 bytes
40.	srio_ll_msg_ssize_64byte_req_test.sv	Creates Data Message Request transaction with seg size as 64 bytes
41.	srio_ll_msg_ssize_128byte_req_test.sv	Creates Data Message Request transaction with seg size as 128 bytes
42.	srio_ll_msg_ssize_256byte_req_test.sv	Creates Data Message Request transaction with seg size as 256 bytes
43.	srio_ll_maintenance_rd_req_base_test.sv	Creates random Maintenance Read Request transactions
44.	srio_ll_msg_mseg_req_test.sv	Creates Data Message - Multi Segment i.e. Message size should be greater than segment size.
45.	srio_ll_msg_sseg_req_test.sv	Creates Data Message - Single Segment i.e. Message size should be equal to segment size.
46.	srio_ll_default_test.sv	Creates random transaction.
47.	srio_ll_message_random_test.sv	Creates random message transaction.
48.	srio_ll_ds_random_req_test.sv	Creates random data streaming transaction
49.	srio_ll_gsm_rd_owner_test.sv	Creates GSM Read Owner transaction
50.	srio_ll_gsm_rd_owner_test.sv	Creates random GSM Read Owner transaction
51.	srio_ll_gsm_rd_to_own_owner_seq _test.sv	Creates random GSM Read to Own Owner transaction
52.	srio_ll_gsm_io_rd_owner_test.sv	Creates random GSM IO Read Owner transaction
53.	srio_ll_gsm_rd_home_test.sv	Creates random GSM Read Home transaction
54.	srio_ll_gsm_rd_to_own_home_test.sv	Creates random GSM Read to Own Home transaction
55.	srio_ll_gsm_io_rd_home_test.sv	Creates random GSM IO Read Home transaction
56.	srio_ll_gsm_dkill_home_test.sv	Creates random GSM DKill Home transaction
57.	srio_ll_gsm_ikill_home_test.sv	Creates random GSM IKill Home transaction
58.	srio_ll_gsm_tlbie_test.sv	Creates random GSM TLBIE transaction
59.	srio_ll_gsm_tlbsync_test.sv	Creates random GSM TLBSYNC transaction
60.	srio_ll_gsm_iread_home_test.sv	Creates random GSM IRead Home transaction
61.	srio_ll_gsm_ikill_sharer_test.sv	Creates random GSM IKill Sharer transaction

62.	srio_ll_gsm_dkill_sharer_test.sv	Creates random GSM DKill Sharer transaction
63.	srio_ll_gsm_castout_test.sv	Creates random GSM CASTOUT transaction
64.	srio_ll_gsm_flush_with_data_test.sv	Creates random GSM FLUSH with Data transaction
65.	srio_ll_gsm_flush_without_data_test.sv	Creates random GSM FLUSH without Data transaction
66.	srio_ll_invalid_ftype_test.sv	Creates transactions with invalid ftype
67.	srio_ll_io_rdsize_wdptr_err_test.sv	Creates SRIO IO Operations with rdsize_wdptr Error
68.	srio_ll_io_wrsize_wdptr_err_test.sv	Creates SRIO IO Operations with wrsize_wdptr Error transaction
69.	srio_ll_atomic_payload_err_test.sv	Creates atomic packet with payload error
70.	srio_ll_swrite_payload_error_test.sv	Creates Unsupported payload bytes such as 3,5,6,7 Bytes of transaction
71.	srio_ll_resp_with_payload_test.sv	Creates random Logical Response with payload transaction and covers possible sta-tus values.
72.	srio_ll_resp_without_payload_test.sv	Creates random Logical Response without payload transaction and covers possible sta-tus values.
73.	srio_ll_ds_pdu_error_test.sv	Creates Data Streaming packets with invalid PDU
74.	srio_ll_ds_mtu_error_test.sv	Creates Data Streaming packets with invalid MTU size
75.	srio_ll_ds_sop_error_test.sv	Creates Data Streaming packets with SOP error transaction
76.	srio_ll_ds_eop_error_test.sv	Creates Data Streaming packets with EOP error transaction
77.	srio_ll_ds_odd_error_test.sv	Creates Data Streaming packets with ODD error transaction
78.	srio_ll_ds_pad_error_test.sv	Creates Data Streaming packets with PAD error transaction
79.	srio_ll_ttype_error_test.sv	Creates random TTYPE error transaction
80.	srio_ll_resp_pri_error_test.sv	Creates random illegal response priority transaction
81.	srio_ll_size_error_test.sv	Creates random packet with size exceed error transaction
82.	srio_ll_payload_exist_error_test.sv	Creates random packet with payload exist error transaction
83.	srio_ll_doubleword_align_error_test.sv	Creates random packet with double word alignment error transaction
84.	srio_ll_lfc_pri_error_test.sv	Creates random LFC – illegal priority sequence
85.	srio_ll_msg_size_error_test.sv	Creates random Message packet with illegal size error sequence
86.	srio_ll_msgseg_error_test.sv	Creates random message packet with invalid segment size error sequence.
87.	srio_ll_callback_test.sv	Creates call back sequences for logical layer packets
88.	srio_ll_ds_interleaved_test.sv	Creates Data Streaming Interleaved packets
89.	rio_ll_msg_interleaved_req_test.sv	Creates Message Interleaved request packets
90.	srio_ll_msg_outoforder_resp_test.sv	Creates out of order responses for message packets
91.	srio_ll_lfc_user_gen_xon_xoff_test.sv	Creates LFC user generated xoff and xon packets w.r.t. priority
92.	srio_ll_io_random_test.sv	Creates IO random packets transaction
93.	srio_ll_ds_mseg_single_mtu_test.s	Creates Data Streaming multi segment packet with

	v	single MTU value
94.	srio_ll_random_interleaved_test.sv	Creates random interleaved packet for DS
95.	srio_ll_random_interleaved_weight_round_robin_test.sv	Creates random interleaved packet for DS by placing weighted round robin method
96.	srio_ll_resp_error_ratio_test.sv	Creates transactions with configured response ratio
97.	srio_ll_resp_no_response_ratio_test.sv	Creates transactions without response with configured no response ratio
98.	srio_ll_resp_gen_mode_test.sv	Creates response gen mode disabled and random mode
99.	srio_ll_port_resp_timeout_reg_test.sv	Creates transactions to configure Port Response Timeout register for Port Response timeout
100.	srio_ll_ds_pkt_ratio_test.sv	Creates DS packets to configure DS packet ratio values
101.	srio_ll_db_pkt_ratio_test.sv	Creates DB packets to configure DB packet ratio values
102.	srio_ll_io_pkt_ratio_test.sv	Creates IO packets to configure IO packet ratio values
103.	srio_ll_gsm_pkt_ratio_test.sv	Creates GSM packets to configure GSM packet ratio values
104.	srio_ll_msg_pkt_ratio_test.sv	Creates Message packets to configure MSG packet ratio values
105.	srio_ll_all_atomic_req_test.sv	Creates all atomic transaction
106.	srio_ll_ds_concurrent_test.sv	Creates transactions of concurrent DS packets
107.	srio_ll_ds_max_seg_support_test.sv	Creates DS packet with Maximum Segment Support error
108.	srio_ll_ds_mtu_reserved_test.sv	Creates DS packet with reserved MTU values
109.	srio_ll_ds_s_e_err_test.sv	Creates DS packets with Start and End bit error
110.	srio_ll_read_write_test.sv	Creates NREAD and NWRITE packets transactions
111.	srio_ll_io_concurrent_trans.sv	Creates transactions of concurrent IO packets
112.	srio_ll_msg_concurrent_req_test.sv	Creates transactions of concurrent Message packets
113.	srio_ll_io_msg_gsm_ds_random_test.sv	Creates random IO,MSG,DS,GSM packets transactions
114.	srio_ll_io_ds_test.sv	Creates random IO,DS packets transactions
115.	srio_ll_io_message_req_test.sv	Creates random IO,MSG request packets transactions
116.	srio_ll_io_message_doorbell_req_test.sv	Creates random IO, MSG, Door Bell packets transactions
117.	srio_ll_ds_traffic_mgmt_basic_stream_xoff_test.sv	Creates transaction of Basic Traffic Management packets to block DS packet w.r.t StreamID
118.	srio_ll_lfc_orphaned_xoff_test.sv	Creates LFC xoff without XON
119.	srio_ll_nread_req_env1_env2_test.sv	Creates transaction of back to back NREAD packets
120.	srio_ll_ds_pdu_length_err_test.sv	Creates DS packet with PDU length error
121.	srio_ll_ds_env1_env2_test.sv	Creates DS packets with back to back transactions
122.	srio_ll_lfc_xon_without_xoff_test.sv	Creates LFC xon packets without LFC xoff packets transaction
123.	srio_ll_lfc_test.sv	Creates random LFC tests
124.	srio_ll_ds_normal_error_test.sv	Creates error DS packets followed by normal DS packets

125.	srio_ll_ds_traffic_mgmt_xtype_err_test.sv	Creates DS Traffic Management packets with invalid xtype values
126.	srio_ll_lfc_multi_xon_xoff_diff_flowid_test.sv	Creates LFC with multiple XOFF and XON
127.	srio_ll_lfc_timeout_check_test.sv	Creates LFC XOFF greater than XON
128.	srio_ll_maintenance_wr_rd_test.sv	Creates Packets of Maintenance Read-Write to configure all the registers values of the register model
129.	srio_ll_ds_traffic_mgmt_xoff_test.sv	Creates DS Traffic Management Xoff packet without Xon packets transaction
130.	srio_ll_lfc_timeout_check1_test.sv	Creates LFC XOFF lesser than XON
131.	srio_ll_lfc_random_test.sv	Creates LFC with random priority packets
132.	srio_ll_lfc_with_diff_id_test.sv	Creates LFC with different target destination ID
133.	srio_ll_ds_traffic_mgmt_user_credit_xoff_xon_test.sv	Creates user generated Traffic Management Xoff and Xon packets to block and release DS packets in credit mode
134.	srio_ll_ds_traffic_mgmt_user_rate_xoff_xon_test.sv	Creates user generated Traffic Management Xoff and Xon packets to block and release DS packets in rate mode
135.	srio_ll_ds_traffic_mgmt_xon_test.sv	Creates DS Traffic Management Xon packet without Xoff packets transaction
136.	srio_ll_ds_traffic_mgmt_tmop_err_test.sv	Creates Traffic Management packets with invalid TMOP values
137.	srio_ll_ds_traffic_mgmt_parameter1_err_test.sv	Creates Traffic Management packets with invalid parameter1 values
138.	srio_ll_unsupported_scr_dest_err_test.sv	Creates unsupported Ftype error by configuring CAR registers
139.	srio_ll_lfc_unsupported_flowid_test.sv	Creates LFC packets with unsupported flowID values
140.	srio_ll_fam_req_xon_ds_release_multi_pdu_0_test.sv	Creates FAM request with xon sequence number 0 and DS with mutli PDU with release 0
141.	srio_ll_fam_req_xon_ds_single_pdu_0_test.sv	Creates FAM request with xon sequence number 0 and DS with single PDU
142.	srio_ll_fam_req_xon_ds_release_multi_pdu_1_test.sv	Creates FAM request with xon sequence number 1 and DS with mutli PDU with release 1
143.	srio_ll_fam_req_xon_ds_single_pdu_1_test.sv	Creates FAM request with xon sequence number 1 and DS with single PDU
144.	srio_ll_fam_req_no_xon_ds_single_pdu_1_test.sv	Creates FAM request with no xon sequence number 1 and DS with single PDU
145.	srio_ll_fam_req_no_xon_ds_single_pdu_0_test.sv	Creates FAM request with no xon sequence number 0 and DS with single PDU
146.	srio_ll_fam_req_xon_ds_release_single_pdu_1_test.sv	Creates FAM request with xon sequence number 1 with release and DS with single PDU
147.	srio_ll_fam_req_xon_ds_release_single_pdu_0_test.sv	Creates FAM request with xon sequence number 0 with release and DS with single PDU
148.	srio_ll_fam_req_xoff_ds_single_pdu_0_test.sv	Creates FAM request with xoff sequence number 0 and DS with single PDU
149.	srio_ll_fam_req_xoff_ds_single_pdu_1_test.sv	Creates FAM request with no xoff sequence number 1 and DS with single PDU
150.	srio_ll_fam_req_xon_ds_single_pd	Creates FAM request with xon sequence number 0

	u_0_flowid_error_test.sv	and DS with single PDU flow ID error
151.	srio_ll_fam_req_xon_ds_single_pdu_1_flowid_error_test.sv	Creates FAM request with xon sequence number 0 and DS with single PDU flow ID error
152.	srio_ll_traffic_mgmt_tm_type_mode_err_test.sv	Creates Traffic Management packets with invalid tm_mode values
153.	srio_ll_ds_traffic_mgmt_mask_err_test.sv	Creates Traffic Management packet with invalid mask values
154.	srio_ll_ds_traffic_mgmt_diff_operation_test.sv	Creates Traffic Management packets with different modes of operations
155.	srio_ll_ds_traffic_mgmt_user_credit_err_test.sv	Creates DS and user generated Traffic Management packets with invalid credit allocate values
156.	srio_ll_ds_traffic_mgmt_basic_specific_stream_xoff_xon_test.sv	Creates DS and Traffic Management Xoff and Xon packet with basic mode for specific streamID value
157.	srio_ll_ds_traffic_mgmt_rate_specific_stream_xoff_xon_test.sv	Creates DS and Traffic Management Xoff and Xon packet with rate mode for specific streamID value
158.	srio_ll_ds_traffic_mgmt_credit_specific_stream_xoff_xon_test.sv	Creates DS and Traffic Management Xoff and Xon packet with basic mode for specific streamID value
159.	srio_ll_ds_traffic_mgmt_basic_specific_cos_xoff_xon_test.sv	Creates DS and Traffic Management Xoff and Xon packet with basic mode for specific COS value
160.	srio_ll_fam_req_no_xon_ds_release_multi_pdu_0_test.sv	Creates FAM request with no xon and ds multi PDU with release 0
161.	srio_ll_fam_req_no_xon_ds_release_multi_pdu_1_test.sv	Creates FAM request with no xon and ds multi PDU with release 1
162.	srio_ll_fam_req_xoff_ds_release_multi_pdu_1_test.sv	Creates FAM request with xoff and ds multi PDU with release 1
163.	srio_ll_fam_req_xoff_ds_release_multi_pdu_0_test.sv	Creates FAM request with xoff and ds multi PDU with release 0
164.	srio_ll_fam_req_xon_ds_without_release_multi_pdu_1_test.sv	Creates FAM request with xoff and ds multi PDU without release 1
165.	srio_ll_fam_req_xon_ds_without_release_multi_pdu_0_test.sv	Creates FAM request with xoff and ds multi PDU without release 0
166.	srio_ll_fam_req_spdu_xon_ds_multi_pdu_1_test.sv	Creates FAM request single pdu with xon and ds multi PDU with release 1
167.	srio_ll_fam_req_spdu_xon_ds_multi_pdu_0_test.sv	Creates FAM request single pdu with xon and ds multi PDU with release 0
168.	srio_ll_ds_traffic_mgmt_rate_specific_cos_xoff_xon_test.sv	Creates DS and Traffic Management Xoff and Xon packets with rate mode for specific COS value
169.	srio_ll_ds_traffic_mgmt_credit_specific_cos_xoff_xon_test.sv	Creates DS and Traffic Management Xoff and Xon packets with credit mode for specific COS value
170.	srio_ll_ds_traffic_mgmt_basic_group_of_cos_xoff_xon_test.sv	Creates DS and Traffic Management Xoff and Xon packets with basic mode for group of COS value
171.	srio_ll_ds_traffic_mgmt_rate_group_of_cos_xoff_xon_test.sv	Creates DS and Traffic Management Xoff and Xon packets with rate mode for group of COS value
172.	srio_ll_ds_traffic_mgmt_credit_group_of_cos_xoff_xon_test.sv	Creates DS and Traffic Management Xoff and Xon packets with credit mode for group of COS value
173.	srio_ll_ds_traffic_mgmt_basic_random_cos_xoff_xon_test.sv	Creates DS and Traffic Management Xoff and Xon packets with basic mode for random COS value
174.	srio_ll_ds_traffic_mgmt_rate_random_cos_xoff_xon_test.sv	Creates DS and Traffic Management Xoff and Xon packets with rate mode for random COS value
175.	srio_ll_ds_traffic_mgmt_credit_ran	Creates DS and Traffic Management Xoff and Xon

	dom_cos_xoff_xon_test.sv	packets with credit mode for random COS value
176.	srio_ll_ds_all_traffic_basic_xoff_xon_test.sv	Creates DS and Traffic Management Xoff and Xon packets with basic mode for all traffic
177.	srio_ll_ds_all_traffic_rate_xoff_xon_test.sv	Creates DS and Traffic Management Xoff and Xon packets with rate mode for all traffic
178.	srio_ll_ds_all_traffic_credit_xoff_xon_test.sv	Creates DS and Traffic Management Xoff and Xon packets with credit mode for all traffic
179.	srio_ll_lfc_prio_greater_ds_xon_xoff_test.sv	Creates LFC priority packets greater than DS priority packets
180.	srio_ll_fam_req_0_spdu_xon_0_req_1_spdu_ds_spdu_xon_1_ds_spdu_test.sv	Creates FAM request 0 single pdu xon 0 request 1 single PDU with DS single PDU xon 1 ds single PDU
181.	srio_ll_fam_req_0_mpdu_xon_0_ds_mpdu_xoff_0_release_0_test.sv	Creates FAM request 0 multi pdu xon 0 DS multi PDU xoff 0 release 0
182.	srio_ll_fam_req_1_mpdu_xon_1_ds_mpdu_xoff_1_release_1_test.sv	Creates FAM request 1 multi pdu xon 1 DS multi PDU xoff 1 release 1
183.	srio_ll_fam_no_req_xon_1_ds_mpdu_test.sv	Creates FAM no request multi pdu xon 1 DS Multi PDU
184.	srio_ll_fam_no_req_xon_0_ds_mpdu_test.sv	Creates FAM no request multi pdu xon 0 DS multi PDU
185.	srio_ll_fam_no_req_xon_1_ds_spdu_test.sv	Creates FAM no request multi pdu xon 1 DS single PDU
186.	srio_ll_fam_no_req_xon_0_ds_spdu_test.sv	Creates FAM no request multi pdu xon 0 DS single PDU
187.	srio_ll_fam_no_req_no_xon_ds_mpdu_test.sv	Creates FAM no request multi pdu xon 0 DS multi PDU
188.	srio_ll_fam_no_req_no_xon_ds_spdu_test.sv	Creates FAM no request multi pdu no xon 0 DS single PDU
189.	srio_ll_fam_no_req_no_xon_no_ds_release_1_test.sv	Creates FAM no request multi pdu no xon 0 no DS multi PDU release 1
190.	srio_ll_fam_no_req_no_xon_no_ds_release_0_test.sv	Creates FAM no request multi pdu xon 0 no DS multi PDU release 0
191.	srio_ll_fam_req_mpdu_no_xon_no_ds_mpdu_release_1_test.sv	Creates FAM request 1 multi pdu no xon 1 no DS multi PDU release 1
192.	srio_ll_fam_req_mpdu_no_xon_no_ds_mpdu_release_0_test.sv	Creates FAM request 0 multi pdu no xon 0 no DS multi PDU release 0
193.	srio_ll_fam_req_mpdu_xon_0_no_ds_mpdu_release_1_test.sv	Creates FAM request multi pdu xon 0 no DS multi PDU release 1
194.	srio_ll_fam_req_mpdu_xon_1_no_ds_mpdu_release_1_test.sv	Creates FAM request multi pdu xon 0 no DS multi PDU release 1
195.	srio_ll_fam_req_mpdu_xon_0_no_ds_mpdu_release_0_test.sv	Creates FAM request multi pdu xon 0 no DS multi PDU release 0
196.	srio_ll_fam_req_mpdu_xon_1_no_ds_mpdu_release_0_test.sv	Creates FAM request multi pdu xon 1 no DS multi PDU release 0
197.	srio_ll_fam_req_mpdu_xon_0_xon_0_ds_mpdu_release_0_test.sv	Creates FAM request multi PDU xon 0 DS multi PDU release 0
198.	srio_ll_fam_req_spdu_xon_1_xon_1_ds_spdu_test.sv	Creates FAM request single PDU xon 1 xon1 ds single PDU
199.	srio_ll_fam_req_mpdu_xon_1_xon_1_ds_mpdu_release_1_test.sv	Creates FAM request multi PDU xon 1 xon 1 DS multi PDU release 1

200.	srio_ll_fam_req_spdu_xon_0_xon_0_ds_spdu_test.sv	Creates FAM request single PDU xon 0 xon0 ds single PDU
201.	srio_ll_fam_req_spdu_xon_1_xoff_1_ds_spdu_test.sv	Creates FAM request single PDU xon 1 xoff 1 ds single PDU
202.	srio_ll_fam_req_spdu_xon_0_xoff_0_ds_spdu_test.sv	Creates FAM request single PDU xon 0 xoff 0 ds single PDU
203.	srio_ll_fam_req_spdu_xon_1_ds_spdu_xoff_1_xon_1_test.sv	Creates FAM request single PDU xon 1 ds single PDU Xoff 1 xon 1
204.	srio_ll_fam_req_spdu_xon_0_ds_spdu_xoff_0_xon_0_test.sv	Creates FAM request single PDU xon 0 ds single PDU Xoff 0 xon 0
205.	srio_ll_nwrite_nread_34_addr_test.sv	Creates NWRITE and NREAD packets with configured addressing mode value of 34bits
206.	srio_ll_nwrite_nread_50_addr_test.sv	Creates NWRITE and NREAD packets with configured addressing mode value of 50 bits
207.	srio_ll_nwrite_nread_66_addr_test.sv	Creates NWRITE and NREAD packets with configured addressing mode value of 66 bits
208.	srio_ll_fam_req_mpdu_xon_1_ds_mpdu_1_release_1_flowid_error_test.sv	Creates FAM request multi PDU xon 1 DS multi PDU release 1 flowid error
209.	srio_ll_fam_req_mpdu_xon_0_ds_mpdu_0_release_0_flowid_error_test.sv	Creates FAM request multi PDU xon 0 DS multi PDU release 0 flowid error
210.	srio_ll_fam_req_spdu_xon_1_ds_spdu_lesser_flowid_test.sv	Creates FAM request multi PDU xon 1 DS single PDU lesser flowid error
211.	srio_ll_fam_req_spdu_xon_0_ds_spdu_lesser_flowid_test.sv	Creates FAM request multi PDU xon 0 DS single PDU lesser flowid error
212.	srio_ll_fam_req_spdu_xon_1_ds_spdu_greater_flowid_test.sv	Creates FAM request multi PDU xon 1 DS single PDU greater flowid error
213.	srio_ll_fam_req_spdu_xon_0_ds_spdu_greater_flowid_test.sv	Creates FAM request multi PDU xon 0 DS single PDU greater flowid error
214.	srio_ll_fam_mpdu_xon_1_ds_mpdu_release_1_flowid_error_test.sv	Creates FAM multi PDU xon 1 DS multi PDU release 1 flowid error
215.	srio_ll_fam_mpdu_xon_0_ds_mpdu_release_0_flowid_error_test.sv	Creates FAM multi PDU xon 0 DS multi PDU release 0 flowid error
216.	srio_ll_parallel_mode_test.sv	Creates parallel mode running test
217.	srio_ll_lfc_prio_lesser_ds_xon_xoff_test.sv	Creates LFC priority packets lesser than DS priority packets
218.	srio_ll_lfc_prio_ds_block_release_xon_xoff_test.sv	Creates LFC packets with decremented priority values and DS packets with random priority values
219.	srio_ll_lfc_ds_random_prio_xon_xoff_test.sv	Creates LFC packets with random priority values and DS packets with random priority values
220.	srio_ll_nwrite_nread_mem_access_test.sv	Creates NWRITE and NREAD packets to access the memory block
221.	srio_ll_traffic_mgmt_lfc_xoff_xon_test.sv	Creates Traffic Management ,LFC Xoff and Xon packets to block and release IO and DS packets
222.	srio_ll_fam_req_mpdu_xon_1_ds_mpdu_xoff_1_ds_mpdu_release_1_test.sv	Creates FAM request multi PDU xon 1 DS multi PDU xoff 1 DS multi PDU release 1
223.	srio_ll_fam_req_mpdu_xon_0_ds_mpdu_xoff_0_ds_mpdu_release_0	Creates FAM request multi PDU xon 0 DS multi PDU xoff 0 DS multi PDU release 0

	_test.sv	
224.	srio_ll_gsm_resp_retry_ratio_test.sv	Creates GSM packets with retry response
225.	srio_ll_msg_db_resp_retry_ratio_test.sv	Creates MSG and Door Bell packets with retry response
226.	srio_ll_illegal_io_trans_dec_test.sv	Creates IO packets with illegal ttype,rd_size and wr_size values
227.	srio_ll_illegal_msg_trans_dec_test.sv	Creates MSG packets with illegal ttype and segment values
228.	srio_ll_vc_ds_mseg_req_test.sv	Creates multi segments Ds packets with multi VC support
229.	srio_ll_vc_ds_lfc_xoff_xon_test.sv	Creates LFC Xoff and Xon packets ,DS packets with multi VC support
230.	srio_ll_multi_vc_nwrite_swrite_test.sv	Creates NWRITE and SWRITE packets with multi VC support
231.	srio_ll_msg_interleaved_out_of_order_test.sv	Creates Message packets with interleaved in out of order
232.	srio_ll_vc_support_2_lfc_xoff_xon_test.sv	Creates test with VC enabled for 2 support with DS across LFC xoff and XON
233.	srio_ll_vc_support_4_lfc_xoff_xon_test.sv	Creates test with VC enabled for 4 support with DS across LFC xoff and XON
234.	srio_ll_msg_mseg_req_with_msgseg_err_test.sv	Creates Message packets with multi segment error using callback
235.	srio_ll_msg_mseg_req_with_msglen_err_test.sv	Creates multi segment Message packets with multi segment length error using callback
236.	srio_ll_msg_mseg_req_max_pld_test.sv	Creates multi segment Message packets with maximum payload size value
237.	srio_ll_msg_mseg_req_with_sseg_neqt_ssize_err_test.sv	Creates multi segment Message packet with start segment not equal to segment size value
238.	srio_ll_msg_mseg_req_with_cseg_neqt_ssize_err_test.sv	Creates multi segment Message packets with continuous segment not equal to segment size value
239.	srio_ll_msg_mseg_req_with_eseg_gt_ssize_err_test.sv	Creates multi segment Message packet with end segment greater than segment size value
240.	srio_ll_msg_mseg_req_without_payload_err_test.sv	Creates multi segment Message packets without payload
241.	srio_ll_vc_support_8_lfc_xoff_xon_test.sv	Creates test with VC enabled for 8 support with DS across LFC xoff and XON
242.	srio_ll_vc_unsupport_flowid_ds_lfc_xoff_xon_test.sv	Creates VC with unsupported flowID for LFC
243.	srio_ll_vc_support_swrite_nwrite_lfc_xoff_xon_test.sv	Creates VC support random nwrite and swrite lfc XOFF and XON
244.	srio_ll_vc_support_random_ds_lfc_xoff_xon_test.sv	Creates VC support random DS lfc XOFF and XON
245.	srio_ll_ds_traffic_mgmt_random_basic_stream_test.sv	Creates DS TM random basic stream test
246.	srio_ll_ds_traffic_mgmt_random_rate_stream_test.sv	Creates DS TM random rate stream test
247.	srio_ll_ds_traffic_mgmt_random_credit_stream_test.sv	Creates DS TM random credit stream test
248.	srio_ll_msg_mseg_resp_with_paylo	Creates Message with multi segment response with

	ad_err_test.sv	payload error
249.	srio_ll_msg_mseg_resp_with_invalid_status_err_test.sv	Creates Message with multi segment response with invalid status error
250.	srio_ll_msg_mseg_resp_with_invalid_tgtinfo_err_test.sv	Creates Message with multi segment response with invalid target info error
251.	srio_ll_msg_db_resp_rand_test.sv	Creates Message with multi segment response with random value
252.	srio_ll_io_resp_rand_test.sv	Creates IO response random value
253.	srio_ll_gsm_resp_rand_test.sv	Creates GSM response random value
254.	srio_ll_atomic_invalid_size.sv	Creates ATOMIC invalid size test
255.	srio_ll_msg_mseg_resp_retry_ratio_test.sv	Creates Message with multi segment response with retry ratio
256.	srio_ll_no_payload_error_demote_test	Example Test case to demote the no payload error
257.	srio_ll_atomic_inc_test.sv	Creates atomic Increment packets test
258.	srio_ll_ds_traffic_mgmt_test.sv	Creates DS Traffic Management test
259.	srio_ll_fam_pipeline_req_multi_pdu_test.sv	Test case with parallel pipeline FAM request packets with multiple PDU values
260.	srio_ll_invalid_tt_test .sv	Creates packets with invalid TT values test
261.	srio_ll_outstanding_unack_req_test.sv	Creates maximum request packets with unacknowledged request test
262.	srio_ll_ds_corner_case_total_pkt_80byte_test.sv	Creates DS packets with 80 bytes test
263.	srio_ll_ds_mseg_req_with_sseg_neqt_mtu_err_test.sv	Creates Multi segment DS packet with start segment not equal to MTU size test
264.	srio_ll_ds_mseg_req_with_cseg_neqt_mtu_err_test.sv	Creates Multi segment DS packet with continuous segment not equal to MTU size test
265.	srio_ll_ds_mseg_req_without_payload_err_test.sv	Creates Multi segment DS packet without payload test
266.	srio_ll_ds_mseg_req_with_invalid_pdulen_err_test.sv	Creates Multi segment DS packets with invalid PDU length test
267.	srio_ll_ds_max_pdu_streamid_test.sv	Creates DS packets with maximum PDU and and Stream_ID test
268.	srio_ll_ds_cov_test.sv	Creates DS packets with different PDU and MTU values test
269.	srio_ll_ds_traffic_mgmt_tmop_err_test .sv	Creates DS and TM packets with invalid TMOP values test
270.	srio_ll_traffic_mgmt_random_test.sv	Creates random Traffic Management packet test
271.	srio_ll_ds_mtu_error_test .sv	Creates DS packets with invalid MTU configured test
272.	srio_ll_ds_max_min_pdu_mtu_test .sv	Creates DS packets with maximum and minimum PDU and MTU values test
273.	srio_ll_ds_traffic_mgmt_credit_rate_control_test.sv	Creates Traffic Management packet with credit and rate control
274.	srio_ll_gsm_resp_err_ratio_test.sv	Creates GSM packets with response status as error test
275.	srio_ll_msg_resp_err_ratio_test.sv	Creates Message packets with response status as error test
276.	srio_ll_msg_max_resp_delay_test.sv	Creates Message packets with maximum response delay test

277.	srio_ll_gsm_address_collision_test.sv	Creates GSM packets with address collision test
278.	srio_ll_msg_consecutive_resp_err_test.sv	Creates Message packets with consecutive error response test
279.	srio_ll_default_illegal_resp_status_err_test.sv	Creates packets with illegal response status test
280.	srio_ll_nwrite_r_gsm_illegal_resp_err_test.sv	Creates NWRITE _R and GSM packets with illegal response test
281.	srio_ll_gsm_io_read_home_test.sv	Creates IO and GSM Read Home packets test
282.	srio_ll_gsm_rd_to_own_owner_test.sv	Creates GSM Read to Own Owner packets test
283.	srio_ll_gsm_random_test.sv	Creates random GSM packets test
284.	srio_ll_ftype_error_test.sv	Creates packets with illegal Ftype test
285.	srio_ll_max_size_error_test.sv	Creates packets with maximum size test
286.	srio_ll_payload_error_test.sv	Creates packets with invalid payload test
287.	srio_ll_no_payload_error_test.sv	Creates packets with no payload test
288.	srio_ll_atomic_compare_and_swap_error_test.sv	Creates Atomic Swap and compare packets with corrupted payload test
289.	srio_ll_atomic_swap_error_test.sv	Creates Atomic Swap packets with corrupted payload test
290.	srio_ll_atomic_test_and_swap_payload_error_test.sv	Creates Atomic Test and Swap packets with corrupted payload test
291.	srio_ll_msg_ssize_error_test.sv	Creates Message packets with invalid ssize value test
292.	srio_ll_resp_rsvd_sts_error_test.sv	Creates Response packet with reserved status test
293.	srio_ll_resp_payload_error_test.sv	Creates Response packets with corrupted payload test
294.	srio_ll_msg_interleaved_req_test.sv	Creates Interleaved Message packets test
295.	srio_ll_vc4_nwrite_swrite_test.sv	Creates NWRITE and SWRITE packets with Vcs4 support test
296.	srio_ll_vc2_nwrite_swrite_test.sv	Creates NWRITE and SWRITE packets with Vcs2 support test
Transport Layer		
297.	srio_tl_callback_test.sv	Creates callback test for Transport layer sequences
298.	srio_tl_destid_corrupt_callback_test.sv	Creates callback test to corrupt the Destid of the packet
299.	srio_tl_ds_scrid_err_cb_test.sv	Creates DS source ID error
300.	srio_tl_pkt_tt_test.sv	Creates random TL packet with changed in TT value forced into tl sequencer
Physical Layer		
301.	srio_pl_dis_nxmode_test.sv	Discovery to Nxmode state transition sequence
302.	srio_pl_dis_2xmode_test.sv	Discovery to 2xmode state transition sequence
303.	srio_pl_dis_1xmode_ln0_test.sv	Discovery to 1xmode_lane0 state transition sequence
304.	srio_pl_dis_1xmode_ln1_test.sv	Discovery to 1xmode_lane1 state transition sequence
305.	srio_pl_dis_1xmode_ln2_test.sv	Discovery to 1xmode_lane2 state transition sequence
306.	srio_pl_dis_sl_test.sv	Discovery to Silent state transition sequence
307.	srio_pl_nxmode_dis_test.sv	Nxmode to Discovery state transition sequence
308.	srio_pl_2xmode_sl_test.sv	2xmode to Silent state transition sequence

309.	srio_pl_2xmode_2x_rec_test.sv	2xmode to 2x recovery state transition sequence
310.	srio_pl_1xmode_ln0_sl_test.sv	1xmode lane0 to Silent state transition sequence
311.	srio_pl_1xmode_ln1_sl_test.sv	1xmode lane1 to Silent state transition sequence
312.	srio_pl_1xmode_ln2_sl_test.sv	1xmode lane2 to Silent state transition sequence
313.	srio_pl_1xmode_ln0_1x_rec_test.sv	1xmode lane0 to 1x recovery state transition sequence
314.	srio_pl_1xmode_ln1_1x_rec_test.sv	1xmode lane1 to 1x recovery state transition sequence
315.	srio_pl_1xmode_ln2_1x_rec_test.sv	1xmode lane2 to 1x recovery state transition sequence
316.	srio_pl_2x_rec_2xmode_test.sv	2x Recovery to 2xmode state transition sequence
317.	srio_pl_2x_rec_1xmode_ln0_test.sv	2x Recovery to 1xmode lane0 state transition sequence
318.	srio_pl_2x_rec_1xmode_ln1_test.sv	2x Recovery to 1xmode lane1 state transition sequence
319.	srio_pl_1x_rec_1xmode_ln0_test.sv	1x Recovery to 1xmode lane0 state transition sequence
320.	srio_pl_1x_rec_1xmode_ln1_test.sv	1x Recovery to 1xmode lane1 state transition sequence
321.	srio_pl_1x_rec_1xmode_ln2_test.sv	1x Recovery to 1xmode lane2 state transition sequence
322.	srio_pl_pkt_acc_cs_test.sv	Packet Accepted CS Sequence
323.	srio_pl_pkt_na_cs_test.sv	Packet not Accepted CS Sequence
324.	srio_pl_pkt_rty_cs_test.sv	Packet Retry CS sequence
325.	srio_pl_pkt_ackid_error_test.sv	Creates ackid error sequence transaction
326.	srio_pl_pkt_early_crc_error_test.sv	Creates random early crc error sequence transaction
327.	srio_pl_pkt_final_crc_error_test.sv	Creates random final CRC error sequence transaction
328.	srio_pl_pkt_illegal_prio_err_test.sv	Creates illegal priority error sequence transaction
329.	srio_pl_pkt_illegal_crf_error_test.sv	Creates illegal CRF error sequence transaction
330.	srio_pl_callback_test.sv	Creates callback sequences for all physical layer sequences
331.	srio_pl_aet_test.sv	Creates random AET test
332.	Srio_pl_aet_tplus_hold_test.sv	Creates AET test for Tap plus status with hold command
333.	srio_pl_aet_tplus_tincr_test.sv	Creates AET test for Tap plus status with increment command
334.	srio_pl_aet_tplus_tdecr_test.sv	Creates AET test for Tap plus status with decrement command
335.	srio_pl_aet_tminus_hold_incr_test.sv	Creates AET test for Tap minus status with hold command --increment
336.	srio_pl_aet_ tminus_ hold_decr_test.sv	Creates AET test for Tap minus status with hold command –decrement
337.	srio_pl_aet_ tminus_incr_ incr_test.sv	Creates AET test for Tap minus status with increment command-- increment
338.	srio_pl_aet_ tminus_ incr_decr_test.sv	Creates AET test for Tap minus status with increment command -- decrement
339.	srio_pl_nop_cs_test.sv	Creates No operation control symbols

340.	srio_pl_multicast_cs_test.sv	Creates Multicast control symbols
341.	srio_pl_sop_cs_test.sv	Creates Start of packet control symbols
342.	srio_pl_eop_cs_test.sv	Creates end of packet control symbols
343.	srio_pl_link_req_input_dev_cs_test.sv	Creates link request with input device control symbols
344.	srio_pl_link_req_rst_dev_cs_test.sv	Creates link request reset device control symbols
345.	srio_pl_restart_rty_cs_test.sv	Creates restart from retry control symbols
346.	srio_pl_stomp_cs_test.sv	Creates stomp control symbols
347.	srio_pl_idle2_csfield_truncation_test.sv	Creates IDLE 2 cs field truncation
348.	srio_pl_idle2_psr_truncation_test.sv	Creates IDLE 2 psr truncation
349.	srio_pl_idle2_csmarker_truncation_test.sv	Creates IDLE 2 cs marker truncation
350.	srio_pl_idle2_csfield_update_truncation_test.sv	Creates IDLE 2 cs field update truncation
351.	srio_pl_idle2_csfield_corruption_test.sv	Creates IDLE 2 cs field corruption
352.	srio_pl_idle2_psr_corruption_test.sv	Creates IDLE 2 psr corruption
353.	srio_pl_idle2_csmarker_corruption_test.sv	Creates IDLE 2 cs marker corruption
354.	srio_pl_idle2_desc_sync_break_corruption_test.sv	Creates IDLE 2 desc sync break corruption
355.	srio_pl_force_reinit_test.sv	Creates force re initialization
356.	srio_pl_nx_mode_support_disable_test.sv	Creates NX mode support disable
357.	srio_pl_2x_mode_support_disable_test.sv	Creates 2X mode support disable
358.	srio_pl_aet_tminus_test.sv	Creates AET tap minus
359.	srio_pl_aet_tplus_random_test.sv	Creates AET tap plus random
360.	srio_pl_aet_tminus_random_test.sv	Creates AET tap minus random
361.	srio_pl_aet_preset_test.sv	Creates AET preset
362.	srio_pl_aet_rst_test.sv	Creates AET reset
363.	srio_pl_force1x_mode_portwidth_override_test.sv	Creates force 1x mode port width override
364.	srio_pl_force1x_mode_laner_portwidth_override_test.sv	Creates force 1x mode laner port width override
365.	srio_pl_nxmode_enabled_2x_disabled_portwidth_override_test.sv	Creates NX mode enabled 2x disabled portwidth override
366.	srio_pl_2xmode_enabled_nx_disabled_portwidth_override_test.sv	Creates 2x mode enabled 2x disabled portwidth override
367.	srio_pl_pkt_na_ackid_err_cs_test.sv	Creates packet not accepted with ackID error control symbols
368.	srio_pl_pkt_na_crc_err_cs_test.sv	Creates packet not accepted with crc error control symbols
369.	srio_pl_pkt_na_non_maintenace_rep_stop_cs_test.sv	Creates packet not accepted with non-maintenance response stop error control symbols
370.	srio_pl_pkt_na_invalid_char_cs_tes	Creates packet not accepted with invalid character

	t.sv	error control symbols
371.	srio_pl_pkt_na_lack_buf_res_cs_test.sv	Creates packet not accepted with lack of buffer response error control symbols
372.	srio_pl_pkt_na_loss_descr_sync_cs_test.sv	Creates packet not accepted with loss descry sync error control symbols
373.	srio_pl_sync_break_test.sv	Creates sync break test
374.	srio_pl_pkt_flow_control_mode_transmit_test.sv	Creates flow control mode transmit
375.	srio_pl_nwrite_swrite_req_test.sv	Creates nwrite swrite request in PL sequncer
376.	srio_pl_skew_max_min_test.sv	Creates max and min skew for all lanes
377.	srio_pl_diff_mode_13_21_test.sv	Creates different mode ie for 1_3 and 2_1
378.	srio_pl_diff_mode_13_22_test.sv	Creates different mode ie for 1_3 and 2_2
379.	srio_pl_diff_mode_22_21_test.sv	Creates different mode ie for 2_2 and 2_1
380.	srio_pl_clck_comp_code_group_cs_test.sv	Creates clock compensation value changed and code group value changed
381.	srio_pl_trans_scramble_enable_test.sv	Creates scrambling enabled
382.	srio_pl_diff_idle_sel_test.sv	Creates different IDLE selection tests.
383.	srio_pl_sync_reset_ns3_to_ns_test.sv	Reset Test case for NO_SYNC_3 state in sync state machine
384.	srio_pl_sync_reset_ns1_to_ns_test.sv	Reset Test case for NO_SYNC_1 state in sync state machine
385.	srio_pl_sync_reset_s_to_ns_test.sv	Reset Test case for SYNC state in sync state machine
386.	srio_pl_sync_reset_s1_to_ns_test.sv	Reset Test case for SYNC_1 state in sync state machine
387.	srio_pl_sync_reset_s3_to_ns_test.sv	Reset Test case for SYNC_3 state in sync state machine
388.	srio_pl_sync_reset_s4_to_ns_test.sv	Reset Test case for SYNC_4 state in sync state machine
389.	srio_pl_nxm_nxr_nxrn_nxm_test.sv	Test case for state transitions from nx_mode to nx_recovery to nx_retrain to nx_mode state
390.	srio_pl_nxm_nxr_nxrn_2x_test.sv	Test case for State transitions from nx_mode to nx_recovery to nx_retrain to 2x_mode state
391.	srio_pl_nxm_nxr_nxrn_x1m0_test.sv	Test case for State transitions from nx_mode to nx_recovery to nx_retrain to x1_mode ln0 state
392.	srio_pl_nxm_nxr_nxrn_x1m1_test.sv	Test case for State transitions from nx_mode to nx_recovery to nx_retrain to x1_mode ln1 state
393.	srio_pl_nxm_nxr_nxrn_x1m2_test.sv	Test case for State transitions from nx_mode to nx_recovery to nx_retrain to x1_mode ln2 state
394.	srio_pl_x2m_x2r_x2rn_x2r_x2m_test.sv	Test case for State transitions from 2x_mode to 2x_recovery to 2x_retrain to 2x_recovery to 2x_mode
395.	srio_pl_x2m_x2r_x2rn_x2r_x1m0_test.sv	Test case for State transitions from 2x_mode to 2x_recovery to 2x_retrain to x2_recovery to x1_mode_ln0 state
396.	srio_pl_x2m_x2r_x2rn_x2r_x1m1_test.sv	Test case for State transitions from 2x_mode to 2x_recovery to 2x_retrain to x2_recovery to x1_mode_ln1 state
397.	srio_pl_x1m0_x1r_x1rn_x1r_x1m0_test.sv	Test case for State transitions from x1_mode_ln0 to 1x_recovery to 1x_retrain to x1_recovery to

		x1_mode_ln0 state
398.	srio_pl_x1m1_x1r_x1rn_x1r_x1m1_test.sv	Test case for State transitions from x1_mode_ln1 to x1_recovery to x1_retrain to x1_recovery to x1_mode_ln1 state
399.	srio_pl_x1m2_x1r_x1rn_x1r_x1m2_test.sv	Test case for State transitions from x1_mode_ln2 to x1_recovery to x1_retrain to x1_recovery to x1_mode_ln2 state
400.	srio_pl_nxr_nxrn_nxr_sil_test.sv	Test case for State transitions from nx_recovery to nx_retrain to nx_recovery to silent state
401.	srio_pl_x1m0_x1r_x1rn_x1r_sl_test.sv	Test case for State transitions from x1_mode_ln0 to x1_recovery to x1_retrain to x1_recovery to silent state
402.	srio_pl_x1m1_x1r_x1rn_x1r_sl_test.sv	Test case for State transitions from x1_mode_ln1 to x1_recovery to x1_retrain to x1_recovery to silent state
403.	srio_pl_x1m2_x1r_x1rn_x1r_sl_test.sv	Test case for State transitions from x1_mode_ln2 to x1_recovery to x1_retrain to x1_recovery to silent state
404.	srio_pl_x2m_x2r_x2rn_x2r_sil_test.sv	Test case for State transitions from x2_mode to x2_recovery to x2_retrain to x2_recovery to silent state
405.	srio_pl_force_reinit_nxretrain_test.sv	Test to asserts force reinit after Nx_retrain in init state machine
406.	srio_pl_force_reinit_2xretrain_test.sv	Test to asserts force reinit after 2x_retrain in init state machine
407.	srio_pl_force_reinit_1xretrain_test.sv	Test to asserts force reinit after 1x_retrain in init state machine
408.	srio_pl_reset_nxretrain_test.sv	Test to asserts reset after nx_retrain in init state machine
409.	srio_pl_reset_2xretrain_test.sv	Test to asserts reset after 2x_retrain in init state machine
410.	srio_pl_reset_1xretrain_test.sv	Test to asserts reset after 1x_retrain in init state machine
411.	srio_pl_2x_rec_sl_test.sv	Test case for State transitions from 2x_recovery to silent state
412.	srio_pl_1x_rec_sl_test.sv	Test case for State transitions from 1x_recovery to silent state
413.	srio_pl_asymmetry_silent_test.sv	Test case for State transitions from assymmetry to silent state
414.	srio_pl_nxm_nxr_test.sv	Test case for State transitions from nx_mode to nx_recovery state
415.	srio_pl_nxr_nxm_test .sv	Test case for State transitions from nx_recovery to nx_mode state
416.	srio_pl_nxr_1xm0_test .sv	Test case for State transitions from nx_recovery to 1x_mode_ln0 state
417.	srio_pl_nxr_1xm1_test.sv	Test case for State transitions from nx_recovery to 1x_mode_ln1 state
418.	srio_pl_nxr_1xm2_test.sv	Test case for State transitions from nx_recovery to 1x_mode_ln2 state
419.	srio_pl_nxr_sil_test.sv	Test case for State transitions from nx_recovery to

		silent state
420.	srio_pl_nxm_asymetry_test.sv	Test case for State transitions from nx_mode to asymmetry state
421.	srio_pl_2xm_asymmetry_test.sv	Test case for State transitions from 2x_mode to asymmetry state
422.	srio_pl_nxr_2xm_test.sv	Test case for State transitions from nx_recovery to 2xmode state
423.	srio_pl_seek_1xmode_ln0_test .sv	Test case for State transitions from seek to 1x_mode_ln0
424.	srio_pl_seek_1xmode_ln2_test.sv	Test case for State transitions from seek to 1x_mode_ln2
425.	srio_pl_nxm_dis_sl_test.sv	Test case for State transitions from nx_mode to discovery to silent
426.	srio_pl_nxm_dis_1xm0_test.sv	Test case for State transitions from nx_mode to discovery to 1x_mode0 state
427.	srio_pl_nxm_dis_1xm1_test.sv	Test case for State transitions from nx_mode to discovery to 1x_mode1 state
428.	srio_pl_nxm_dis_1xm2_test.sv	Test case for State transitions from nx_mode to discovery to 1x_mode2 state
429.	srio_pl_nxm_dis_2xm_test.sv	Test case for state transition from nx mode to discovery
430.	srio_pl_nxm_dis_nxm_test.sv	Test case for state transition from nx mode to discovery to nx Mode
431.	srio_pl_x1m1_x1r_sl_test.sv	Test case for State transitions from x1_mode_ln1 to x1_recovery to silent state
432.	srio_pl_x1m2_x1r_sl_test.sv	Test case for State transitions from x1_mode_ln2 to x1_recovery to silent state
433.	srio_pl_reset_seek_test.sv	Test case to assert reset after seek state
434.	srio_pl_reset_discovery_test.sv	Test case to assert reset after discovery state
435.	srio_pl_reset_nx_mode_test.sv	Test case to assert reset after nx_mode state
436.	srio_pl_reset_2xmode_test.sv	Test case to assert reset after 2x_mode state
437.	srio_pl_reset_nx_recovery_test.sv	Test case to assert reset after nx_recovery state
438.	srio_pl_reset_2x_recovery_test.sv	Test case to assert reset after 2x_recovery state
439.	srio_pl_reset_1xmode_ln0_test.sv	Test case to assert reset after 1x_mode_ln0 state
440.	srio_pl_reset_1xmode_ln1_test.sv	Test case to assert reset after 1x_mode_ln1 state
441.	srio_pl_reset_1xmode_ln2_test.sv	Test case to assert reset after 1x_mode_ln2 state
442.	srio_pl_reset_1xmode_recovery_test.sv	Test case to assert reset after 1x_mode_recovery state
443.	srio_pl_reset_asymmetry_test .sv	Test case to assert reset after asymmetry state
444.	srio_pl_force_reinit_discovery_test .sv	Test case to assert force_reinit after discovery state
445.	srio_pl_force_reinit_seek_test.sv	Test case to assert force_reinit after seek state
446.	srio_pl_force_reinit_nx_mode_test .sv	Test case to assert force_reinit after nx_mode state
447.	srio_pl_force_reinit_2xmode_test.sv	Test case to assert force_reinit after 2x_mode state
448.	srio_pl_force_reinit_nx_recovery_test.sv	Test case to assert force_reinit after nx_recovery state
449.	srio_pl_force_reinit_2x_recovery_test.sv	Test case to assert force_reinit after 2x_recovery state

450.	srio_pl_force_reinit_1xmode_ln0_test.sv	Test case to assert force_reinit after 1xmode _ln0 state
451.	srio_pl_force_reinit_1xmode_ln1_test.sv	Test case to assert force_reinit after 1xmode _ln1 state
452.	srio_pl_force_reinit_1xmode_ln2_test.sv	Test case to assert force_reinit after 1xmode _ln2 state
453.	srio_pl_force_reinit_asymmetry_test.sv	Test case to assert force_reinit after asymmetry state
454.	srio_pl_force_reinit_1xmode_recovery_test.sv	Test case to assert force_reinit after 1x_mode_recovery state
455.	srio_pl_asymmetry_s1xmx2_axe_test.sv	Test for state transition between seek_x1_mode_xmt2 to axe
456.	srio_pl_asymmetry_s2xmx2_axe_test.sv	Test for state transition between seek_x2_mode_xmt2 to axe
457.	srio_pl_asymmetry_s1xmx_s1xmx3_test.sv	Test for state transition between seek_x1_mode_xmt to seek_x1_mode_xmt3
458.	srio_pl_asymmetry_s2xmx_s2xmx3_test.sv	Test for state transition between seek_x2_mode_xmt to seek_x2_mode_xmt3
459.	srio_pl_asymmetry_xmit_width_cmd1_test.sv	Test for Asymmetry transmit width good command followed with bad command
460.	srio_pl_asymmetry_rcv_width_cmd1_test.sv	Test for Asymmetry receive width good command followed with bad command
461.	srio_pl_asymmetry_sm_test.sv	Test case to cover Asymmetry transmit and receive width normal transition
462.	srio_pl_nxm_2xm_asymmetry_sm_test .sv	Test case for Asymmetry transmit width change between NX_mode to 2X_mode
463.	srio_pl_nxm_2xm_1xm_asymmetry_sm_test.sv	Test case for Asymmetry transmit width change between NX_mode to 2X_mode to 1X_mode
464.	srio_pl_nxm_1xm_asymmetry_sm_test.sv	Test case for Asymmetry transmit width change between NX_mode to 1X_mode
465.	srio_pl_asymmetry_2xm_disable_1xm_test .sv	Test case to check received command of unsupported mode
466.	srio_pl_asymmetry_nxm_disable_1xm_test .sv	Test case to check received command of unsupported mode
467.	srio_pl_asymmetry_nxm_disable_2xm_test.sv	Test case to check received command of unsupported mode
468.	srio_pl_asymmetry_xmt_width_port_cmd_nx_2x_1x_nx_test.sv	Test case for mode change between Nx_mode to 2x_mode to 1x_mode to Nx_mode
469.	srio_pl_cw_train1_untrned_test.sv	Test case for code word training , Code word training 1 to untrained.
470.	srio_pl_timestamp_check_test.sv	Test case for timestamp control symbols
471.	srio_pl_asymmetry_rcv_1x_recovery_test.sv	Test case for Asymmetry State machines state transition between 1x_recovery to 1x_retrain state
472.	srio_pl_asymmetry_rcv_2x_recovery_test.sv	Test case for Asymmetry State machines state transition between 2x_recovery to 2x_retrain state
473.	srio_pl_asymmetry_rcv_s2xmrcv_rwn_test.sv	Test case for Asymmetry State machines state transition between seek_2x_mode_rcv to rwn
474.	srio_pl_aet_tminus_incr_incr_test.sv	Test case for AET, Tap Minus value increment command
475.	srio_pl_aet_tminus_incr_decr_test.	Test case for AET, Tap Minus value increment

	sv	decrement command
476.	srio_pl_aet_tminus_incr_hold_test.sv	Test case for AET, Tap Minus value increment hold command
477.	srio_pl_aet_tminus_hold_decr_test.sv	Test case for AET, Tap Minus value hold with decrement command
478.	srio_pl_link_req_rst_3_b2b_sop_link_req_rst_cs_test.sv	Test case for Link request reset 3 times back to back and SOP and link request reset.
479.	srio_pl_link_req_rst_2_b2b_sop_2_b2b_link_req_rst_cs_test.sv	Test case for Link request reset 2 times back to back and SOP and 2 link request reset
480.	srio_pl_lane_align_sm_test.sv	Test cases for align state machine to break align
481.	srio_pl_aligned_aligned1_notaligned_sm_test.sv	Test case for align state machine, from aligned1 to not aligned.
482.	srio_pl_pkt_prob_test.sv	Test cases for probability of packet accepted, retry and not accepted ratio
483.	srio_pl_sync_sm_test.sv	Test case for sync state machine to corrupt the sync.
484.	srio_pl_gen3_sync_sm_s_s1_s2_test.sv	Test case for sync path transition from sync-sync1-s2
485.	srio_pl_gen3_sync_sm_s_s1_s2_all_lanes_test.sv	Test case for sync path transition from sync-sync1-s2 for all lanes.
486.	srio_pl_cw_retrain_test .sv	Test cases for code word retrain .
487.	srio_pl_sop_with_eop_cs_test.sv	Test case for Control symbols with sop and eop combination.
488.	srio_pl_sop_stomp_cs_test.sv	Test case for Control symbols with sop and stomp
489.	srio_pl_sop_link_req_cs_test.sv	Test case for Control symbols with sop and link request input status
490.	srio_pl_sop_link_req_rst_cs_test.sv	Test case for Control symbols with sop and link request reset.
491.	srio_pl_gen2_a1_a2_a2_sm_test.sv	Test case for align state machine path transitions.
492.	srio_pl_link_response_cs_test.sv	Test case to generate link response
493.	srio_pl_align_error_test.sv	Test case to break the align.
494.	srio_pl_dme_test.sv	Test case for basic DME Long-Run testing
495.	srio_pl_dme_hold_test.sv	Creates DME Long-Run test with Hold command test
496.	srio_pl_dme_decr_test.sv	Creates DME Long-Run test with Decrement command test
497.	srio_pl_dme_incre_test.sv	Creates DME Long-Run test with Increment command test
498.	srio_pl_dme_init_test.sv	Creates DME Long-Run test with Initialize command test
499.	srio_pl_dme_prst_test.sv	Creates DME Long-Run test with Preset command test
500.	srio_pl_dme_max_limit_test.sv	Creates DME Long-Run test with Increment command for maximum limit test
501.	srio_pl_dme1_dmef_test.sv	Test case for state transition between DME_1 to DME_FAIL state
502.	srio_pl_dme1_to_untrk_dmet2_test.sv	Test case for state transition between DME_1 to UNTRAINED to DME_2 state
503.	srio_pl_dme_min_limit_test.sv	Creates DME Long-Run test with Decrement command for minimum limit test
504.	srio_pl_dme_port_initialize_to_sile	Creates DME testing with intermediate force_reinit

	nt_test.sv	for re-initialization test
505.	srio_pl_cw_train_incr_tap0_test.sv	Test case for Code word Training , with Increment command and tap 0 value
506.	srio_pl_cw_train_decr_tap0_test.sv	Test case for Code word Training , with decrement command and tap 0 value
507.	srio_pl_cw_train_incr_decr_tap0_test.sv	Test case for Code word Training , with Increment ,decrement command and tap 0 value
508.	srio_pl_cw_train_kind_disabled_test.sv	Test case for Code word Training , with both sides disabled
509.	srio_pl_cw_train_hold_test.sv	Test case for Code word Training , with hold command
510.	srio_pl_cw_train_initialize_test.sv	Test case for Code word Training , with initialize command
511.	srio_pl_cw_train_preset_test.sv	Test case for Code word Training , with preset command
512.	srio_pl_cw_train_preset_random_test.sv	Test case for Code word Training, with preset command and random tap value.
513.	srio_pl_cw_train_initialize_random_test.sv	Test case for Code word Training , with initialize command and random tap value
514.	srio_pl_cw_train_hold_random_test.sv	Test case for Code word Training , with hold command and random tap value
515.	srio_pl_cw_train_incr_random_test.sv	Test case for Code word Training , with increment command and random tap value
516.	srio_pl_cw_train_decr_random_test.sv	Test case for Code word Training , with decrement command and random tap value
517.	srio_pl_cw_train1_cw_train_fail_test.sv	Test cases for Code word training path transitions, training 1 to training fail
518.	srio_pl_ns1_ns2_ns3_ns2_ns_sm_test.sv	Test case for sync state machine path transitions. Nosync1-nosync2-nosync3-nosync2-nosync.
519.	srio_pl_ns1_ns2_ns3_ns2_ns1_sm_test.sv	Test case for sync state machine path transitions Nosync1-nosync2-nosync3-nosync2-nosync1
520.	srio_pl_gen3_a_a2_a3_a4_sm_test.sv	Test case for align state machine path transitions. Aligned-aligned2-aligned3-aligned4
521.	srio_pl_gen3_a3_a4_a5_a3_sm_test.sv	Test case for align state machine path transitions. aligned3-aligned4-aligned5-aligned3
522.	srio_pl_gen3_a3_a4_a6_a3_sm_test .sv	Test case for align state machine path transitions. aligned3-aligned4-aligned6-aligned3
523.	srio_pl_gen3_ns2_ns3_ns1_sm_test.sv	Test case for sync state machine path transitions Nosync1-nosync2-nosync3-nosync1
524.	srio_pl_ct_mode_vc_support_transmit_mode_test.sv	Test case for CT mode VC support with transmits mode packet transactions.
525.	srio_txrx_model_test .sv	Test cases for txrx model
526.	srio_pl_asymmetry_rcv_s1xmrcv_rwn_test.sv	Test case for Asymmetry State machines state transition between seek_1x_mode_rcv to rwn state
527.	srio_pl_align_reset_sm_test .sv	Test case for align reset.
528.	srio_pl_env1_sop_link_req_env2_disabled_test.sv	Test case for sop link request input status with env2 disabled
529.	srio_pl_env1_sop_link_req_rst_dev_env2_disabled_test.sv	Test case for sop link request reset with env2 disabled
530.	srio_pl_env1_sop_stomp_env2_dis	Test case for sop stomp with env2 disabled

	abled_test .sv	
531.	srio_pl_env1_sop_restart_rty_env2_disabled_test.sv	Test case for sop restart from retry with env2 disabled
532.	srio_pl_env1_sop_eop_env2_disabled_test .sv	Test case for sop – eop with env2 disabled
533.	srio_pl_sop_stomp_callback_test .sv	Test cases for sop with stomp
534.	srio_pl_cw_retrain_timeout_test.sv	Test case for code retrain timeout for all state.
535.	srio_pl_asymmetry_rcv_s1xmrcv_are_test.sv	Test case for Asymmetry State machines state transition between seek_1x_mode_rcv to are state
536.	srio_pl_asymmetry_rcv_s2xmrcv_are_test.sv	Test case for Asymmetry State machines state transition between seek_2x_mode_rcv to are state
537.	srio_pl_asymmetry_rcv_2x_recovery_to_are_test.sv	Test case for Asymmetry State machines state transition between 2x_recovery to are state
538.	srio_pl_asymmetry_rcv_1x_recovery_to_are_test.sv	Test case for Asymmetry State machines state transition between 1x_recovery to are state
539.	srio_pl_force_1xmode_lane0_2x_support_test.sv	Test case for force 1x mode lane 0 with 2x mode support.
540.	srio_pl_asymmetry_rcv_1x_mode_rcv_to_are_test.sv	Test case for Asymmetry State machines state transition between 1x_mode to are
541.	srio_pl_asymmetry_rcv_2x_mode_rcv_to_are_test.sv	Test case for Asymmetry State machines state transition between 2x_mode to are state
542.	srio_pl_asymmetry_rcv_1xmrcv_1xmrcva_test.sv	Test case for Asymmetry State machines state transition between 1x_mode_rcv to 1x_mode_rcv_ack state
543.	srio_pl_asymmetry_rcv_2xmrcv_2xmrcva_test.sv	Test case for Asymmetry State machines state transition between 2x_mode_rcv to 2x_mode_rcv_ack state
544.	srio_pl_sop_nwrite_eop_test.sv	Test case for sop nwrite and eop.
545.	srio_pl_asymmetry_rcv_x1mrcv_x1rec_x1mrcv_test.sv	Test case for Asymmetry State machines state transition between 1x_mode_rcv to 1x_recovery to 1x_mode_rcv state
546.	srio_pl_asymmetry_rcv_x2mrcv_x2rec_x2mrcv_test.sv	Test case for Asymmetry State machines state transition between 2x_mode_rcv to 2x_recovery to 2x_mode_rcv state
547.	srio_pl_asymmetry_rcv_x2mr_x2rec_x2rn_x2rec_are_ari_test.sv	Test case for Asymmetry Receive width state machines transition path
548.	srio_pl_asymmetry_rcv_x1mr_x1rec_x1rn_x1rec_are_ari_test.sv	Test case for Asymmetry Receive width state machines transition path
549.	srio_pl_cw_retrain_timeout_lane2_test .sv	Test case for code word retrains timeout for all state with lane 2.
550.	srio_pl_cw_retrain_timeout_lanes4_test.sv	Test case for code word retrains timeout for all state with lane 4.
551.	srio_pl_cw_retrain_timeout_lanes8_test.sv	Test case for code word retrains timeout for all state with lane 8.
552.	srio_pl_cw_retrain_timeout_lanes16_test.sv	Test case for code word retrains timeout for all state with lane 16.
553.	srio_pl_cw_retrain_trnd_ret0_ret_f	Test case for code retrain , retraining 0 to fail

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554.	srio_pl_cw_retrain_trnd_ret1_ret_fail_test.sv	Test case for code retrain , retraining 1 to fail
555.	srio_pl_asymmetry_x2mx_sx1mx_sx1mx2_sx1mx3_xwn_x2mx_test.sv	Test case for Asymmetry Receive width state machines transition path
556.	srio_pl_asymmetry_x2mx_sx1mx_sx1mx1_sx1mx2_axe_axi_test.sv	Test case for Asymmetry Receive width state machines transition path
557.	srio_pl_asymmetry_x1mx_x1mxa_test.sv	Test case for Asymmetry Transmit width state machines transition between 1x_mode_xmt to 1x_mode_xmt_ack
558.	srio_pl_asymmetry_x2mx_x2mxa_test.sv	Test case for Asymmetry Transmit width state machines transition between 2x_mode_xmt to 2x_mode_xmt_ack
559.	srio_pl_cw_retrain_timeout_1_test.sv	Test case for code word retrains timeout for all state and with normal operation
560.	srio_pl_cw_retrain_timeout_retrain5_lanes16_test.sv	Test case for code word retrain timeout for retrain 5 state with lane 16
561.	srio_pl_cw_retrain_retrain5_lanes16_test.sv	Test case for code word retrain ,for retrain5 state with lane 16
562.	srio_pl_cw_retrain_retrain4_timeout_lanes8_test.sv	Test case for code word retrain ,for retrain4 state with lane 16 timeout
563.	srio_pl_cw_retrain_retrain5_lanes8_test.sv	Test case for code word retrain, for getting retrains 5 in 8 lanes.
564.	srio_pl_cw_retrain_retrain5_timeout_lanes8_test.sv	Test case for code retrains, retrain5 to timeout in lanes 8.
565.	srio_pl_cw_retrain_trnd_ret2_ret_fail_test .sv	Test case for code retrain , retraining 2 to fail
566.	srio_pl_sync_break_all_lanes_test.sv	Test cases for sync break in all lanes.
567.	srio_pl_cw_retrain_retrain5_lanes2_test.sv	Test case for code word retrain, for getting retrains 5 in 2 lanes.
568.	srio_pl_cw_retrain_retrain5_lanes4_test.sv	Test case for code word retrain, for getting retrains 5 in 4 lanes.
569.	srio_pl_cw_retrain_retrain5_timeout_lanes4_test.sv	Test case for code retrain, retrain5 to timeout in lanes 8.
570.	srio_pl_ns1_ns2_ns1_ns2_sm_all_lanes_test.sv	Test case for sync path transitions. Nosync1-nosync2-nosync1-nosync2
571.	srio_pl_ns1_ns2_ns_sm_all_lanes_test.sv	Test case for sync path transitions. Nosync1-nosync2-nosync
572.	srio_pl_sync_sm_all_lanes_test.sv	Test case for sync path transitions.
573.	srio_pl_ns1_ns2_ns3_ns2_ns_sm_all_lanes_test.sv	Test case for sync path transitions. Nosync1-nosync2-nosync3-nosync2
574.	srio_pl_gen3_ns2_ns3_ns1_sm_all_lanes_test.sv	Test case for sync path transitions. Nosync1-nosync2-nosync3-nosync1
575.	srio_pl_ns1_ns2_ns3_ns2_ns1_sm_all_lanes_test.sv	Test case for sync path transitions. Nosync1-nosync2-nosync3-nosync1 for all lanes.
576.	srio_pl_asymmetry_1x_port_req_test.sv	Test case for 1x_mode transmit command port request to change link partner width
577.	srio_pl_asymmetry_2x_port_req_test.sv	Test case for 2x_mode transmit command port request to change link partner width

578.	srio_pl_asymmetry_4x_port_req_test.sv	Test case for 4x_mode transmit command port request to change link partner width
579.	srio_pl_asymmetry_8x_port_req_test.sv	Test case for 8x_mode transmit command port request to change link partner width
580.	srio_pl_asymmetry_16x_port_req_test.sv	Test case for 16x_mode transmit command port request to change link partner width
581.	srio_pl_sop_link_req_inp_stat_callback_test.sv	Test case for sop link request input status transition.
582.	srio_pl_sop_restart_rty_callback_test.sv	Test case for sop restart from retry transition
583.	srio_pl_sop_link_req_rst_dev_callback_test.sv	Test case for sop link request reset transition
584.	srio_pl_gen3_sop_eop_padded_cs_test.sv	Test case for sop eop padded
585.	srio_pl_gen3_eop_padded_cs_test.sv	Test case for eop padded transactions
586.	srio_pl_link_req_rst_4_b2b_cs_test.sv	Test case for link request 4 times transaction.
587.	srio_pl_link_req_rst_3_b2b_status_cs_link_req_rst_test.sv	Test case for link request 3 times transaction and status CS and link request reset
588.	srio_pl_link_req_rst_3_b2b_non_status_cs_link_req_rst_test.sv	Test case for link request 3 times transaction and non-status CS and link request reset
589.	srio_pl_link_req_rst_2_b2b_non_status_cs_2_link_req_rst_test.sv	Test case for link request 2 times transaction and non-status CS and 2 link request reset
590.	srio_pl_link_req_rst_1_b2b_non_status_cs_3_link_req_rst_test.sv	Test case for link request 1 times transaction and non-status CS and 3 link request reset
591.	srio_pl_link_req_rst_1_b2b_status_cs_3_link_req_rst_test.sv	Test case for link request 1 times transaction and status CS and 3 link request reset
592.	srio_pl_link_req_rst_2_b2b_status_cs_2_link_req_rst_test.sv	Test case for link request 2 times transaction and status CS and 2 link request reset
593.	srio_pl_link_req_rst_b2b_status_cs_link_req_rst_test.sv	Test case for link request 1 times transaction and status CS and link request reset
594.	srio_pl_link_req_rst_port_4_b2b_cs_test.sv	Test case for link request reset port 4 times transaction.
595.	srio_pl_link_req_rst_port_3_b2b_status_cs_link_req_rst_port_test.sv	Test case for link request 3 times transaction and status CS and link request reset port
596.	srio_pl_link_req_rst_port_3_b2b_non_status_cs_link_req_rst_port_test.sv	Test case for link request 3 times transaction and non-status CS and link request reset port
597.	srio_pl_link_req_rst_port_2_b2b_non_status_cs_2_link_req_rst_port_test.sv	Test case for link request 2 times transaction and non-status CS and 2 link request reset port
598.	srio_pl_link_req_rst_port_1_b2b_status_cs_3_link_req_rst_port_test.sv	Test case for link request 1 times transaction and status CS and 3 link request reset port
599.	srio_pl_link_req_rst_port_1_b2b_non_status_cs_3_link_req_rst_port_test.sv	Test case for link request 1 times transaction and non-status CS and 3 link request reset port
600.	srio_pl_link_req_rst_port_2_b2b_status_cs_2_link_req_rst_port_test.	Test case for link request 2 times transaction and status CS and 2 link request reset port

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601.	srio_pl_link_req_rst_port_b2b_status_cs_link_req_rst_port_test.sv	Test case for link request 1 times transaction and status CS and link request reset port
602.	srio_pl_pkt_retry_cs_reset_test.sv	Test case for packet retry with reset
603.	srio_pl_pkt_retry_cs_ors_reset_test.sv	Test case for packet retry with reset in ORS state
604.	srio_pl_reset_na2_na_test.sv	Test case for reset in not aligned 2
605.	srio_pl_reset_na1_na_test.sv	Test case for reset in not aligned 1
606.	srio_pl_align_error_2_sm_test.sv	Test case for align error for 2 times.
607.	srio_pl_gen3_reset_na2_na_test.sv	Test case for reset in not aligned 2
608.	srio_pl_gen3_reset_na3_na_test.sv	Test case for reset in not aligned 3
609.	srio_pl_cw_retrain_keep_alive_ret0_lanes2_test.sv	Test case for code word retrain ,from keep alive to retraining in lanes 2
610.	srio_pl_cw_retrain_keep_alive_ret0_lanes4_test.sv	Test case for code word retrain ,from keep alive to retraining in lanes 4
611.	srio_pl_cw_retrain_keep_alive_ret0_lanes8_test.sv	Test case for code word retrain ,from keep alive to retraining in lanes 8
612.	srio_pl_cw_retrain_keep_alive_ret0_lanes16_test.sv	Test case for code word retrain ,from keep alive to retraining in lanes 16
613.	srio_pl_cw_retrain_keep_alive_ret0_lanes1_test.sv	Test case for code word retrain ,from keep alive to retraining in lane 1
614.	srio_pl_reset_a1_na_a_test.sv	Test case for reset in aligned 1
615.	srio_pl_reset_a2_na_a_test.sv	Test case for reset in aligned 2
616.	srio_pl_reset_a3_na_a_test.sv	Test case for reset in aligned 3
617.	srio_pl_gen3_reset_na1_na_test.sv	Test case for reset in not aligned 1
618.	srio_pl_gen3_reset_a_na_test.sv	Test case for reset in aligned
619.	srio_pl_gen3_reset_a3_na_test.sv	Test case for reset in aligned 3
620.	srio_pl_gen3_reset_a4_na_test.sv	Test case for reset in aligned 4
621.	srio_pl_gen3_reset_a5_na_test.sv	Test case for reset in aligned 5
622.	srio_pl_gen3_reset_a7_na_test.sv	Test case for reset in aligned 7
623.	srio_pl_gen3_reset_a6_na_test.sv	Test case for reset in aligned 6
624.	srio_pl_gen3_reset_a1_na_test.sv	Test case for reset in aligned 1
625.	srio_pl_gen3_reset_a2_na_test.sv	Test case for reset in aligned 2
626.	srio_pl_gen3_reset_ns3_ns_test.sv	Test case for reset in no sync 3
627.	srio_pl_gen3_reset_ns4_ns_test.sv	Test case for reset in no sync 4
628.	srio_pl_gen3_reset_s_ns_test.sv	Test case for reset in sync
629.	srio_pl_gen3_reset_s1_ns_test.sv	Test case for reset in sync 1
630.	srio_pl_gen3_reset_s2_ns_test.sv	Test case for reset in sync2
631.	srio_pl_gen3_reset_ns1_ns_test.sv	Test case for reset in no sync 1
632.	srio_pl_sync_signal_detect_ns1_ns_test.sv	Test case for signal detect in no sync 1
633.	srio_pl_sync_signal_detect_ns3_ns_test.sv	Test case for signal detect in no sync 3
634.	srio_pl_sync_signal_detect_s_ns_test.sv	Test case for signal detect in sync
635.	srio_pl_sync_signal_detect_s1_ns_test.sv	Test case for signal detect in sync 1
636.	srio_pl_sync_signal_detect_s3_ns_test.sv	Test case for signal detect in sync3
637.	srio_pl_sync_signal_detect_s4_ns_t	Test case for signal detect in sync4

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638.	srio_pl_random_acc_gen_kind_test .sv	Test case for acc gen kind with PL_RANDOM
639.	srio_pl_ies_oes_force_reinit_err_test.sv	Test for Link Initialize as zero at Input-Error-state and Output-Error-state
640.	srio_pl_idle2_cs_marker_corrupt_test.sv	Test case for idle 2 cs marker corrupt.
641.	srio_pl_2xmode_1xmode_ln0_test.sv	Test case for test transition from 2x mode to 1xmode_ln0
642.	srio_pl_2xmode_1xmode_ln1_test.sv	Test case for test transition from 2x mode to 1xmode_ln1
643.	srio_pl_pkt_ackid_error_test .sv	Test case for corrupted ack_id values
644.	srio_pl_pkt_illegal_prio_error_test.sv	Test case for corrupted priority values
645.	srio_pl_pkt_illegal_crf_error_test.sv	Test case for corrupted CRF values

7. Functional Coverage

Following table lists the functional coverage points available in this release.

S.No	Cover Group	Cover Point
Logical Layer		
1.	CG_LL_TX_PATH	CP_LL_TX_TXN_ID
2.	CG_LL_RX_PATH	CP_LL_RX_TXN_ID
3.	CG_LL_TX_PATH	CP_LL_TX_ATOMIC_TYPES
4.	CG_LL_RX_PATH	CP_LL_RX_ATOMIC_TYPES
5.	CG_LL_TX_PATH	CP_LL_TX_FTYPE
6.	CG_LL_RX_PATH	CP_LL_RX_FTYPE
7.	CG_LL_TX_PATH	CP_LL_TX_TTYPE
8.	CG_LL_RX_PATH	CP_LL_RX_TTYPE
9.	CG_LL_TX_PATH	CP_LL_TX_TYPE2_TTYPE
10.	CG_LL_TX_PATH	CP_LL_TX_TYPE5_TTYPE
11.	CG_LL_TX_PATH	CP_LL_TX_NREAD_RESP_TYPE
12.	CG_LL_TX_PATH	CP_LL_TX_NREAD_RESP_STATUS
13.	CG_LL_TX_PATH	CP_LL_TX_NWRITE_R_RESP_TYPE
14.	CG_LL_TX_PATH	CP_LL_TX_NWRITE_R_RESP_STATUS
15.	CG_LL_TX_PATH	CP_LL_TX_TYPE8_TTYPE
16.	CG_LL_TX_PATH	CP_LL_TX_TYPE10_TTYPE
17.	CG_LL_TX_PATH	CP_LL_TX_TYPE11_TTYPE
18.	CG_LL_TX_PATH	CP_LL_TX_TYPE13_TTYPE
19.	CG_LL_RX_PATH	CP_LL_RX_TYPE2_TTYPE
20.	CG_LL_RX_PATH	CP_LL_RX_TYPE5_TTYPE
21.	CG_LL_RX_PATH	CP_LL_RX_TYPE8_TTYPE
22.	CG_LL_RX_PATH	CP_LL_RX_TYPE10_TTYPE
23.	CG_LL_RX_PATH	CP_LL_RX_TYPE11_TTYPE
24.	CG_LL_RX_PATH	CP_LL_RX_TYPE13_TTYPE
25.	CG_LL_TX_PATH	CP_LL_TX_MAINT_PRIORITY
26.	CG_LL_TX_PATH	CP_LL_TX_MAINT_PRIORITY_ORDER
27.	CG_LL_TX_PATH	CP_LL_TX_WRITE_TXN_PRIORITY

28.	CG_LL_TX_PATH	CP_LL_TX_WDPTR
29.	CG_LL_RX_PATH	CP_LL_RX_WDPTR
30.	CG_LL_TX_PATH	CP_LL_TX_RDSIZE
31.	CG_LL_RX_PATH	CP_LL_RX_RDSIZE
32.	CG_LL_TX_PATH	CP_LL_TX_WRSIZE
33.	CG_LL_RX_PATH	CP_LL_RX_WRSIZE
34.	CG_LL_TX_PATH	CP_LL_TX_ADDR
35.	CG_LL_RX_PATH	CP_LL_RX_ADDR
36.	CG_LL_TX_PATH	CP_LL_TX_EXT_ADDR
37.	CG_LL_RX_PATH	CP_LL_RX_EXT_ADDR
38.	CG_LL_TX_PATH	CP_LL_TX_XAMSBS
39.	CG_LL_RX_PATH	CP_LL_RX_XAMSBS
40.	CG_LL_TX_PATH	CR_LL_TX_TYPE2_WDPTR_RDSIZE
41.	CG_LL_RX_PATH	CR_LL_RX_TYPE2_WDPTR_RDSIZE
42.	CG_LL_TX_PATH	CR_LL_TX_TYPE5_WDPTR_WRSIZE
43.	CG_LL_RX_PATH	CR_LL_RX_TYPE5_WDPTR_WRSIZE
44.	CG_LL_TX_PATH	CR_LL_TX_TYPE5_ATOMIC_VALID_SIZE
45.	CG_LL_RX_PATH	CR_LL_RX_TYPE5_ATOMIC_VALID_SIZE
46.	CG_LL_TX_PATH	CR_LL_TX_TYPE2_ATOMIC_VALID_SIZE
47.	CG_LL_RX_PATH	CR_LL_RX_TYPE2_ATOMIC_VALID_SIZE
48.	CG_LL_TX_PATH	CR_LL_TX_TYPE5_ATOMIC_INVALID_SIZE
49.	CG_LL_RX_PATH	CR_LL_RX_TYPE5_ATOMIC_INVALID_SIZE
50.	CG_LL_TX_PATH	CR_LL_TX_TYPE2_ATOMIC_INVALID_SIZE
51.	CG_LL_RX_PATH	CR_LL_RX_TYPE2_ATOMIC_INVALID_SIZE
52.	CG_LL_TX_PATH	CP_LL_TX_ATOMIC_INC_RESP_TYPE
53.	CG_LL_TX_PATH	CP_LL_TX_ATOMIC_INC_RESP_STATUS
54.	CG_LL_TX_PATH	CP_LL_TX_ATOMIC_DEC_RESP_TYPE
55.	CG_LL_TX_PATH	CP_LL_TX_ATOMIC_DEC_RESP_STATUS
56.	CG_LL_TX_PATH	CP_LL_TX_ATOMIC_SET_RESP_TYPE
57.	CG_LL_TX_PATH	CP_LL_TX_ATOMIC_SET_RESP_STATUS
58.	CG_LL_TX_PATH	CP_LL_TX_ATOMIC_CLR_RESP_TYPE
59.	CG_LL_TX_PATH	CP_LL_TX_ATOMIC_CLR_RESP_STATUS
60.	CG_LL_TX_PATH	CP_LL_TX_ATOMIC_SWAP_RESP_TYPE
61.	CG_LL_TX_PATH	CP_LL_TX_ATOMIC_SWAP_RESP_STATUS
62.	CG_LL_TX_PATH	CP_LL_TX_ATOMIC_COMP_RESP_TYPE
63.	CG_LL_TX_PATH	CP_LL_TX_ATOMIC_COMP_RESP_STATUS
64.	CG_LL_TX_PATH	CP_LL_TX_ATOMIC_TEST_RESP_TYPE
65.	CG_LL_TX_PATH	CP_LL_TX_ATOMIC_TEST_RESP_STATUS
66.	CG_LL_RX_PATH	CP_LL_RX_ATOMIC_INC_RESP_TYPE
67.	CG_LL_RX_PATH	CP_LL_RX_ATOMIC_INC_RESP_STATUS
68.	CG_LL_RX_PATH	CP_LL_RX_ATOMIC_DEC_RESP_TYPE
69.	CG_LL_RX_PATH	CP_LL_RX_ATOMIC_DEC_RESP_STATUS
70.	CG_LL_RX_PATH	CP_LL_RX_ATOMIC_SET_RESP_TYPE
71.	CG_LL_RX_PATH	CP_LL_RX_ATOMIC_SET_RESP_STATUS
72.	CG_LL_RX_PATH	CP_LL_RX_ATOMIC_CLR_RESP_TYPE
73.	CG_LL_RX_PATH	CP_LL_RX_ATOMIC_CLR_RESP_STATUS
74.	CG_LL_RX_PATH	CP_LL_RX_ATOMIC_SWAP_RESP_TYPE
75.	CG_LL_RX_PATH	CP_LL_RX_ATOMIC_SWAP_RESP_STATUS
76.	CG_LL_RX_PATH	CP_LL_RX_ATOMIC_COMP_RESP_TYPE

77.	CG_LL_RX_PATH	CP_LL_RX_ATOMIC_COMP_RESP_STATUS
78.	CG_LL_RX_PATH	CP_LL_RX_ATOMIC_TEST_RESP_TYPE
79.	CG_LL_RX_PATH	CP_LL_RX_ATOMIC_TEST_RESP_STATUS
80.	CG_LL_TX_PATH	CR_LL_TX_FTYPE_XAMSBS_SRCTID
81.	CG_LL_RX_PATH	CR_LL_RX_FTYPE_XAMSBS_SRCTID
82.	CG_LL_TX_PATH	CP_LL_TX_NWRITE_INVALID_PAYLOAD_LEN
83.	CG_LL_TX_PATH	CP_LL_TX_MAINT_WRITE_INVALID_PAYLOAD_LEN
84.	CG_LL_TX_PATH	CR_LL_TX_MAINT_RD_WDPTR_RDSIZE
85.	CG_LL_RX_PATH	CR_LL_RX_MAINT_RD_WDPTR_RDSIZE
86.	CG_LL_TX_PATH	CR_LL_TX_MAINT_WR_WDPTR_WRSIZE
87.	CG_LL_RX_PATH	CR_LL_RX_MAINT_WR_WDPTR_WRSIZE
88.	CG_LL_TX_PATH	CP_LL_TX_MAINT_CONFIG_OFFSET
89.	CG_LL_TX_PATH	CP_LL_TX_MAINT_SRCTID
90.	CG_LL_TX_PATH	CP_LL_TX_MAINT_TARGET_TID
91.	CG_LL_RX_PATH	CP_LL_TX_MAINT_STATUS
92.	CG_LL_TX_PATH	CP_LL_RX_MAINT_STATUS
93.	CG_LL_RX_PATH	CP_LL_RX_MAINT_CONFIG_OFFSET
94.	CG_LL_RX_PATH	CP_LL_RX_MAINT_SRCTID
95.	CG_LL_RX_PATH	CP_LL_RX_MAINT_TARGET_TID
96.	CG_LL_TX_PATH	CP_LL_TX_RESP_TXN
97.	CG_LL_TX_PATH	CP_LL_TX_RESP_TARGET_TID
98.	CG_LL_TX_PATH	CP_LL_TX_IO_RESP_STATUS
99.	CG_LL_RX_PATH	CP_LL_RX_RESP_TXN
100.	CG_LL_RX_PATH	CP_LL_RX_RESP_TARGET_TID
101.	CG_LL_RX_PATH	CP_LL_RX_IO_RESP_STATUS
102.	CG_LL_TX_PATH	CP_LL_TX_MSG_MSGLEN
103.	CG_LL_TX_PATH	CP_LL_TX_MSG_MSGSEG
104.	CG_LL_TX_PATH	CP_LL_TX_MSG_XMBOX
105.	CG_LL_TX_PATH	CP_LL_TX_MSG_SSIZE
106.	CG_LL_TX_PATH	CP_LL_TX_MSG_MBOX
107.	CG_LL_TX_PATH	CP_LL_TX_MSG_LETTER
108.	CG_LL_TX_PATH	CR_LL_TX_MSG_SINGLE_XMBOX_MBOX_LETTER
109.	CG_LL_TX_PATH	CR_LL_TX_MSG_MULTI_SEG_SSIZE_MBOX_LETTER
110.	CG_LL_RX_PATH	CP_LL_RX_MSG_MSGLEN
111.	CG_LL_RX_PATH	CP_LL_RX_MSG_MSGSEG
112.	CG_LL_RX_PATH	CP_LL_RX_MSG_MSGSEG
113.	CG_LL_RX_PATH	CP_LL_RX_MSG_XMBOX
114.	CG_LL_RX_PATH	CP_LL_RX_MSG_SSIZE
115.	CG_LL_RX_PATH	CP_LL_RX_MSG_MBOX
116.	CG_LL_RX_PATH	CP_LL_RX_MSG_LETTER
117.	CG_LL_RX_PATH	CR_LL_RX_MSG_SINGLE_XMBOX_MBOX_LETTER
118.	CG_LL_RX_PATH	CR_LL_RX_MSG_MULTI_SEG_SSIZE_MBOX_LETTER
119.	CG_LL_TX_PATH	CP_LL_TX_MSG_OUT_ORDER
120.	CG_LL_RX_PATH	CP_LL_RX_MSG_OUT_ORDER
121.	CG_LL_TX_PATH	CP_LL_TX_MSG_INTERLEAVE
122.	CG_LL_RX_PATH	CP_LL_RX_MSG_INTERLEAVE
123.	CG_LL_TX_PATH	CP_LL_TX_DOORBELL_RESP_TYPE
124.	CG_LL_TX_PATH	CP_LL_TX_DOORBELL_RESP_STATUS
125.	CG_LL_RX_PATH	CP_LL_RX_DOORBELL_RESP_TYPE

126.	CG_LL_RX_PATH	CP_LL_RX_DOORBELL_RESP_STATUS
127.	CG_LL_TX_PATH	CP_LL_TX_MSG_RESP_TYPE
128.	CG_LL_TX_PATH	CP_LL_TX_MSG_RESP_STATUS
129.	CG_LL_RX_PATH	CP_LL_RX_MSG_RESP_TYPE
130.	CG_LL_RX_PATH	CP_LL_RX_MSG_RESP_STATUS
131.	CG_LL_TX_PATH	CP_LL_TX_MSG_RESP_TARGET_TID
132.	CG_LL_RX_PATH	CP_LL_RX_MSG_RESP_TARGET_TID
133.	CG_LL_TX_PATH	CR_LL_TX_MSG_RESP_STATUS_TARGET_TID
134.	CG_LL_RX_PATH	CR_LL_RX_MSG_RESP_STATUS_TARGET_TID
135.	CG_LL_TX_PATH	CP_LL_TX_MSG_PRIORITY
136.	CG_LL_RX_PATH	CP_LL_RX_MSG_PRIORITY
137.	CG_LL_TX_PATH	CP_TL_TX_TT_VALID
138.	CG_LL_RX_PATH	CP_TL_RX_TT_VALID
139.	CG_LL_TX_PATH	CR_TX_TT_FTYPE
140.	CG_LL_TX_PATH	CR_TX_TT_TTYPE
141.	CG_LL_TX_PATH	CR_TX_TT_TYPE2_TTYPE
142.	CG_LL_TX_PATH	CR_TX_TT_TYPE5_TTYPE
143.	CG_LL_TX_PATH	CR_TX_TT_TYPE8_TTYPE
144.	CG_LL_TX_PATH	CR_TX_TT_TYPE10_TTYPE
145.	CG_LL_TX_PATH	CR_TX_TT_TYPE11_TTYPE
146.	CG_LL_TX_PATH	CR_TX_TT_TYPE13_TTYPE
147.	CG_LL_RX_PATH	CR_RX_TT_FTYPE
148.	CG_LL_RX_PATH	CR_RX_TT_TTYPE
149.	CG_LL_RX_PATH	CR_RX_TT_TYPE2_TTYPE
150.	CG_LL_RX_PATH	CR_RX_TT_TYPE5_TTYPE
151.	CG_LL_RX_PATH	CR_RX_TT_TYPE8_TTYPE
152.	CG_LL_RX_PATH	CR_RX_TT_TYPE10_TTYPE
153.	CG_LL_RX_PATH	CR_RX_TT_TYPE11_TTYPE
154.	CG_LL_RX_PATH	CR_RX_TT_TYPE13_TTYPE
155.	CG_LL_TX_PATH	CP_LL_TX_GSM_REQ_TTYPE
156.	CG_LL_RX_PATH	CP_LL_RX_GSM_REQ_TTYPE
157.	CG_LL_TX_PATH	CP_LL_TX_GSM_REQ_SRCTID
158.	CG_LL_RX_PATH	CP_LL_RX_GSM_REQ_SRCTID
159.	CG_LL_TX_PATH	CR_LL_TX_GSM_REQ_SRCTID
160.	CG_LL_RX_PATH	CR_LL_RX_GSM_REQ_SRCTID
161.	CG_LL_TX_PATH	CR_LL_TX_GSM_REQ_WDPTR_RDSIZE
162.	CG_LL_RX_PATH	CR_LL_RX_GSM_REQ_WDPTR_RDSIZE
163.	CG_LL_TX_PATH	CR_LL_TX_GSM_REQ_TTYPE_WDPTR_WRSIZE
164.	CG_LL_RX_PATH	CR_LL_RX_GSM_REQ_TTYPE_WDPTR_WRSIZE
165.	CG_LL_TX_PATH	CP_LL_TX_GSM_RD_O_RESP_TYPE
166.	CG_LL_TX_PATH	CP_LL_TX_GSM_RD_O_RESP_STATUS
167.	CG_LL_TX_PATH	CP_LL_TX_GSM_RD_O_O_RESP_TYPE
168.	CG_LL_TX_PATH	CP_LL_TX_GSM_RD_O_O_RESP_STATUS
169.	CG_LL_TX_PATH	CP_LL_TX_GSM_IO_RD_O_RESP_TYPE
170.	CG_LL_TX_PATH	CP_LL_TX_GSM_IO_RD_O_RESP_STATUS
171.	CG_LL_TX_PATH	CP_LL_TX_GSM_RD_H_RESP_TYPE
172.	CG_LL_TX_PATH	CP_LL_TX_GSM_RD_H_RESP_STATUS
173.	CG_LL_TX_PATH	CP_LL_TX_GSM_RD_O_H_RESP_TYPE
174.	CG_LL_TX_PATH	CP_LL_TX_GSM_RD_O_H_RESP_STATUS

175.	CG_LL_TX_PATH	CP_LL_TX_GSM_IO_RD_H_RESP_TYPE
176.	CG_LL_TX_PATH	CP_LL_TX_GSM_IO_RD_H_RESP_STATUS
177.	CG_LL_TX_PATH	CP_LL_TX_GSM_D_H_RESP_TYPE
178.	CG_LL_TX_PATH	CP_LL_TX_GSM_D_H_RESP_STATUS
179.	CG_LL_TX_PATH	CP_LL_TX_GSM_I_H_RESP_TYPE
180.	CG_LL_TX_PATH	CP_LL_TX_GSM_I_H_RESP_STATUS
181.	CG_LL_TX_PATH	CP_LL_TX_GSM_TLBIE_RESP_TYPE
182.	CG_LL_TX_PATH	CP_LL_TX_GSM_TLBIE_RESP_STATUS
183.	CG_LL_TX_PATH	CP_LL_TX_GSM_TLBSYNC_RESP_TYPE
184.	CG_LL_TX_PATH	CP_LL_TX_GSM_TLBSYNC_RESP_STATUS
185.	CG_LL_TX_PATH	CP_LL_TX_GSM_IRD_H_RESP_TYPE
186.	CG_LL_TX_PATH	CP_LL_TX_GSM_IRD_H_RESP_STATUS
187.	CG_LL_TX_PATH	CP_LL_TX_GSM_FLUSH_WO_D_RESP_TYPE
188.	CG_LL_TX_PATH	CP_LL_TX_GSM_FLUSH_WO_D_RESP_STATUS
189.	CG_LL_TX_PATH	CP_LL_TX_GSM_IK_SH_RESP_TYPE
190.	CG_LL_TX_PATH	CP_LL_TX_GSM_IK_SH_RESP_STATUS
191.	CG_LL_TX_PATH	CP_LL_TX_GSM_DK_SH_RESP_TYPE
192.	CG_LL_TX_PATH	CP_LL_TX_GSM_DK_SH_RESP_STATUS
193.	CG_LL_TX_PATH	CP_LL_TX_GSM_CASTOUT_RESP_TYPE
194.	CG_LL_TX_PATH	CP_LL_TX_GSM_CASTOUT_RESP_STATUS
195.	CG_LL_TX_PATH	CP_LL_TX_GSM_FLUSH_WD_RESP_TYPE
196.	CG_LL_TX_PATH	CP_LL_TX_GSM_FLUSH_WD_RESP_STATUS
197.	CG_LL_RX_PATH	CP_LL_RX_GSM_RD_O_RESP_TYPE
198.	CG_LL_RX_PATH	CP_LL_RX_GSM_RD_O_RESP_STATUS
199.	CG_LL_RX_PATH	CP_LL_RX_GSM_RD_O_O_RESP_TYPE
200.	CG_LL_RX_PATH	CP_LL_RX_GSM_RD_O_O_RESP_STATUS
201.	CG_LL_RX_PATH	CP_LL_RX_GSM_IO_RD_O_RESP_TYPE
202.	CG_LL_RX_PATH	CP_LL_RX_GSM_IO_RD_O_RESP_STATUS
203.	CG_LL_RX_PATH	CP_LL_RX_GSM_RD_H_RESP_TYPE
204.	CG_LL_RX_PATH	CP_LL_RX_GSM_RD_H_RESP_STATUS
205.	CG_LL_RX_PATH	CP_LL_RX_GSM_RD_O_H_RESP_TYPE
206.	CG_LL_RX_PATH	CP_LL_RX_GSM_RD_O_H_RESP_STATUS
207.	CG_LL_RX_PATH	CP_LL_RX_GSM_IO_RD_H_RESP_TYPE
208.	CG_LL_RX_PATH	CP_LL_RX_GSM_IO_RD_H_RESP_STATUS
209.	CG_LL_RX_PATH	CP_LL_RX_GSM_D_H_RESP_TYPE
210.	CG_LL_RX_PATH	CP_LL_RX_GSM_D_H_RESP_STATUS
211.	CG_LL_RX_PATH	CP_LL_RX_GSM_I_H_RESP_TYPE
212.	CG_LL_RX_PATH	CP_LL_RX_GSM_I_H_RESP_STATUS
213.	CG_LL_RX_PATH	CP_LL_RX_GSM_TLBIE_RESP_TYPE
214.	CG_LL_RX_PATH	CP_LL_RX_GSM_TLBIE_RESP_STATUS
215.	CG_LL_RX_PATH	CP_LL_RX_GSM_TLBSYNC_RESP_TYPE
216.	CG_LL_RX_PATH	CP_LL_RX_GSM_TLBSYNC_RESP_STATUS
217.	CG_LL_RX_PATH	CP_LL_RX_GSM_IRD_H_RESP_TYPE
218.	CG_LL_RX_PATH	CP_LL_RX_GSM_IRD_H_RESP_STATUS
219.	CG_LL_RX_PATH	CP_LL_RX_GSM_FLUSH_WO_D_RESP_TYPE
220.	CG_LL_RX_PATH	CP_LL_RX_GSM_FLUSH_WO_D_RESP_STATUS
221.	CG_LL_RX_PATH	CP_LL_RX_GSM_IK_SH_RESP_TYPE
222.	CG_LL_RX_PATH	CP_LL_RX_GSM_IK_SH_RESP_STATUS
223.	CG_LL_RX_PATH	CP_LL_RX_GSM_DK_SH_RESP_TYPE

224.	CG_LL_RX_PATH	CP_LL_RX_GSM_DK_SH_RESP_STATUS
225.	CG_LL_RX_PATH	CP_LL_RX_GSM_CASTOUT_RESP_TYPE
226.	CG_LL_RX_PATH	CP_LL_RX_GSM_CASTOUT_RESP_STATUS
227.	CG_LL_RX_PATH	CP_LL_RX_GSM_FLUSH_WD_RESP_TYPE
228.	CG_LL_RX_PATH	CP_LL_RX_GSM_FLUSH_WD_RESP_STATUS
229.	CG_LL_TX_PATH	CP_LL_TX_GSM_REQ_DATA_PAYLOAD
230.	CG_LL_TX_PATH	CP_LL_TX_IO_ERROR_RESP
231.	CG_LL_RX_PATH	CP_LL_RX_IO_ERROR_RESP
232.	CG_LL_TX_PATH	CP_LL_TX_MSG_ERROR_RESP
233.	CG_LL_RX_PATH	CP_LL_RX_MSG_ERROR_RESP
234.	CG_LL_TX_PATH	CP_LL_TX_GSM_ERROR_RESP
235.	CG_LL_RX_PATH	CP_LL_RX_GSM_ERROR_RESP
236.	CG_LL_TX_PATH	CP_LL_TX_MSG_FORMAT_ERR_INVALID_SIZE
237.	CG_LL_TX_PATH	CP_LL_TX_MSG_FORMAT_ERR_INVALID_SEG
238.	CG_LL_TX_PATH	CR_LL_TX_MSG_FORMAT_ERR_INVALID_SIZE_SEGMENT
239.	CG_LL_TX_PATH	CP_LL_TX_IO_ILLEGAL_TRANS_DEC
240.	CG_LL_TX_PATH	CP_LL_TX_IO_RESP_ILLEGAL_TRANS_DEC
241.	CG_LL_TX_PATH	CP_LL_TX_MSG_ILLEGAL_TRANS_DEC
242.	CG_LL_TX_PATH	CP_LL_TX_MSG_RESP_ILLEGAL_TRANS_DEC
243.	CG_LL_TX_PATH	CP_LL_TX_GSM_ILLEGAL_TRANS_DEC
244.	CG_LL_TX_PATH	CP_LL_TX_GSM_RESP_ILLEGAL_TRANS_DEC
245.	CG_LL_TX_PATH	CP_TL_TX_ILLEGAL_TARGET
246.	CG_LL_TX_PATH	CP_LL_TX_IO_ILLEGAL_TRANS_TARGET
247.	CG_LL_TX_PATH	CP_LL_TX_GSM_ILLEGAL_TRANS_TARGET
248.	CG_LL_TX_PATH	CP_LL_TX_MSG_REQ_TIMEOUT
249.	CG_LL_TX_PATH	CP_LL_TX_RESP_TIMEOUT
250.	CG_LL_TX_PATH	CP_LL_TX_UNEXPECTED_IO_RESP
251.	CG_LL_TX_PATH	CP_LL_TX_UNEXPECTED_MAINT_RESP
252.	CG_LL_TX_PATH	CP_LL_TX_UNEXPECTED_MSG_RESP
253.	CG_LL_TX_PATH	CP_LL_TX_UNSUPP_IO_TXN
254.	CG_LL_TX_PATH	CP_LL_TX_UNSUPP_MSG_TXN
255.	CG_LL_TX_PATH	CP_LL_TX_UNSUPP_GSM_TXN
256.	CG_LL_TX_PATH	CP_LL_TX_CONSECUTIVE_IO_ERROR_RESP
257.	CG_LL_TX_PATH	CP_LL_TX_CONSECUTIVE_MSG_ERROR_RESP
258.	CG_LL_TX_PATH	CP_LL_TX_IO_GOOD_ERROR_RESP
259.	CG_LL_TX_PATH	CP_LL_TX_MSG_GOOD_ERROR_RESP
260.	CG_LL_TX_PATH	CP_LL_TX_BACK2BACK_MSG_INVALID_SIZE
261.	CG_LL_TX_PATH	CP_LL_TX_BACK2BACK_MSG_INVALID_SEGMENT
262.	CG_LL_TX_PATH	CR_LL_TX_BACK2BACK_MSG_INVALID_SIZE_SEGMENT
263.	CG_LL_TX_PATH	CP_LL_TX_CONSECUTIVE_MSG_VALID_INVALID_SIZE
264.	CG_LL_TX_PATH	CP_LL_TX_CONSECUTIVE_MSG_VALID_INVALID_SEGMENT
265.	CG_LL_TX_PATH	CP_LL_TX_PDU_LENGTH
266.	CG_LL_RX_PATH	CP_LL_RX_PDU_LENGTH
267.	CG_LL_TX_PATH	CP_LL_TX_PDU_COS
268.	CG_LL_RX_PATH	CP_LL_RX_PDU_COS

269.	CG_LL_TX_PATH	CP_LL_TX_PDU_MTU
270.	CG_LL_RX_PATH	CP_LL_RX_PDU_MTU
271.	CG_LL_TX_PATH	CR_LL_TX_PDU_LENGTH_MTU
272.	CG_LL_RX_PATH	CR_LL_RX_PDU_LENGTH_MTU
273.	CG_LL_TX_PATH	CP_LL_TX_PDU_S
274.	CG_LL_RX_PATH	CP_LL_RX_PDU_S
275.	CG_LL_TX_PATH	CP_LL_TX_PDU_E
276.	CG_LL_RX_PATH	CP_LL_RX_PDU_E
277.	CG_LL_TX_PATH	CP_LL_TX_PDU_O
278.	CG_LL_RX_PATH	CP_LL_RX_PDU_O
279.	CG_LL_TX_PATH	CP_LL_TX_PDU_P
280.	CG_LL_RX_PATH	CP_LL_RX_PDU_P
281.	CG_LL_TX_PATH	CP_LL_TX_PDU_XH
282.	CG_LL_RX_PATH	CP_LL_RX_PDU_XH
283.	CG_LL_TX_PATH	CP_LL_TX_PDU_STREAM_ID
284.	CG_LL_RX_PATH	CP_LL_RX_PDU_STREAM_ID
285.	CG_LL_TX_PATH	CR_LL_TX_PDU_SINGLE_SEGMENT
286.	CG_LL_RX_PATH	CR_LL_RX_PDU_SINGLE_SEGMENT
287.	CG_LL_TX_PATH	CR_LL_TX_PDU_START_SEGMENT
288.	CG_LL_RX_PATH	CR_LL_RX_PDU_START_SEGMENT
289.	CG_LL_TX_PATH	CR_LL_TX_PDU_MIDDLE_SEGMENT
290.	CG_LL_RX_PATH	CR_LL_RX_PDU_MIDDLE_SEGMENT
291.	CG_LL_TX_PATH	CR_LL_TX_PDU_LAST_SEGMENT
292.	CG_LL_RX_PATH	CR_LL_RX_PDU_LAST_SEGMENT
293.	CG_LL_TX_PATH	CP_LL_TX_DATA_STREAM_INTERLEAVE
294.	CG_LL_RX_PATH	CP_LL_RX_DATA_STREAM_INTERLEAVE
295.	CG_LL_TX_PATH	CP_LL_TX_DATA_STREAM_FLOW_ID
296.	CG_LL_RX_PATH	CP_LL_RX_DATA_STREAM_FLOW_ID
297.	CG_LL_TX_PATH	CR_LL_TX_PDU_LENGTH_MTU_FLOW_ID
298.	CG_LL_RX_PATH	CR_LL_RX_PDU_LENGTH_MTU_FLOW_ID
299.	CG_LL_TX_PATH	CR_LL_TX_PDU_S_E_FLOW_ID
300.	CG_LL_RX_PATH	CR_LL_RX_PDU_S_E_FLOW_ID
301.	CG_LL_TX_PATH	CP_LL_TX_TM_TMOP
302.	CG_LL_RX_PATH	CP_LL_RX_TM_TMOP
303.	CG_LL_TX_PATH	CP_LL_TX_TM_WC
304.	CG_LL_RX_PATH	CP_LL_RX_TM_WC
305.	CG_LL_TX_PATH	CP_LL_TX_TM_MASK
306.	CG_LL_RX_PATH	CP_LL_RX_TM_MASK
307.	CG_LL_TX_PATH	CP_LL_TX_TM_PARAMETER1
308.	CG_LL_RX_PATH	CP_LL_RX_TM_PARAMETER2
309.	CG_LL_TX_PATH	CP_LL_TX_TM_BASIC_TRAFFIC
310.	CG_LL_TX_PATH	CP_LL_TX_TM_RATE_BASED_TRAFFIC
311.	CG_LL_TX_PATH	CP_LL_TX_TM_CREDIT_BASED_TRAFFIC
312.	CG_LL_RX_PATH	CP_LL_RX_TM_BASIC_TRAFFIC
313.	CG_LL_RX_PATH	CP_LL_RX_TM_RATE_BASED_TRAFFIC
314.	CG_LL_RX_PATH	CP_LL_RX_TM_CREDIT_BASED_TRAFFIC
315.	CG_LL_TX_PATH	CP_LL_TX_XON_XOFF
316.	CG_LL_RX_PATH	CP_LL_RX_XON_XOFF
317.	CG_LL_TX_PATH	CP_LL_TX_FLOW_CTRL_FLOW_ID

318.	CG_LL_RX_PATH	CP_LL_RX_FLOW_CTRL_FLOW_ID
319.	CG_LL_TX_PATH	CP_LL_TX_FLOW_DEST_ID
320.	CG_LL_RX_PATH	CP_LL_RX_FLOW_DEST_ID
321.	CG_LL_TX_PATH	CP_LL_TX_FLOW_TGT_DEST_ID
322.	CG_LL_RX_PATH	CP_LL_RX_FLOW_TGT_DEST_ID
323.	CG_LL_TX_PATH	CP_LL_TX_FLOW_CTRL_FAM
324.	CG_LL_RX_PATH	CP_LL_RX_FLOW_CTRL_FAM
325.	CG_LL_TX_PATH	CP_LL_TX_FLOW_CTRL_SOC
326.	CG_LL_RX_PATH	CP_LL_RX_FLOW_CTRL_SOC
327.	CG_LL_TX_PATH	CR_LL_TX_FLOW_CTRL_XON_XOFF_FAM_FLOW_ID
328.	CG_LL_RX_PATH	CR_LL_RX_FLOW_CTRL_XON_XOFF_FAM_FLOW_ID
329.	CG_LL_TX_PATH	CP_LL_TX_FLOW_CTRL_PIPELINE_REQ_SINGLE_PDU
330.	CG_LL_RX_PATH	CP_LL_RX_FLOW_CTRL_PIPELINE_REQ_SINGLE_PDU
331.	CG_LL_TX_PATH	CP_LL_TX_FLOW_CTRL_PIPELINE_REQ_MULTI_PDU
332.	CG_LL_RX_PATH	CP_LL_RX_FLOW_CTRL_PIPELINE_REQ_MULTI_PDU
Transport Layer		
333.	CG_TL_TX_PATH	CP_TL_TX_TT_VALID
334.	CG_TL_RX_PATH	CP_TL_RX_TT_VALID
335.	CG_TL_TX_PATH	CP_TL_TX_TT_INVALID
336.	CG_TL_TX_PATH	CP_TL_TX_SOURCEID
337.	CG_TL_RX_PATH	CP_TL_RX_SOURCEID
338.	CG_TL_TX_PATH	CP_TL_TX_DESTINATION_ID
339.	CG_TL_RX_PATH	CP_TL_RX_DESTINATION_ID
Physical Layer		
340.	CG_PL	CP_PL_LANE_WIDTH
341.	CG_PL	CP_PL_DATA_RATE
342.	CG_PL	CR_PL_LANE_WIDTH_DATA_RATE
343.	CG_PL_TX	CP_PL_TX_ACK_ID
344.	CG_PL_RX	CP_PL_RX_ACK_ID
345.	CG_PL_TX	CP_PL_TX_CS_TYPE
346.	CG_PL_RX	CP_PL_RX_CS_TYPE
347.	CG_PL_TX	CP_PL_TX_VC
348.	CG_PL_RX	CP_PL_RX_VC
349.	CG_PL_TX	CP_PL_TX_PRIO
350.	CG_PL_RX	CP_PL_RX_PRIO
351.	CG_PL_TX	CP_PL_TX_CRF
352.	CG_PL_RX	CP_PL_RX_CRF
353.	CG_PL_TX	CR_PL_TX_VC_PRIO_CRF
354.	CG_PL_RX	CR_PL_RX_VC_PRIO_CRF
355.	CG_PL_TX	CP_PL_TX_FTYPE_TTYPE
356.	CG_PL_RX	CP_PL_RX_FTYPE_TTYPE
357.	CG_PL_TX	CR_PL_TX_VC_PRIO_CRF_FTYPE_TTYPE
358.	CG_PL_RX	CR_PL_RX_VC_PRIO_CRF_FTYPE_TTYPE
359.	CG_PL_TX	CP_PL_TX_PACKET_PAD_ZEROS
360.	CG_PL_RX	CP_PL_RX_PACKET_PAD_ZEROS
361.	CG_PL_TX	CP_PL_TX_PACKET_EARLY_CRC
362.	CG_PL_RX	CP_PL_RX_PACKET_EARLY_CRC
363.	CG_PL_TX	CP_PL_TX_PACKET_FINAL_CRC
364.	CG_PL_RX	CP_PL_RX_PACKET_FINAL_CRC

365.	CG_PL_TX	CR_PL_TX_PACKET_PAD_ZEROS_EARLY_CRC_FINAL_CRC
366.	CG_PL_RX	CR_PL_RX_PACKET_PAD_ZEROS_EARLY_CRC_FINAL_CRC
367.	CG_PL_TX	CP_PL_TX_PACKET_EARLY_CRC_CORRUPT
368.	CG_PL_TX	CP_PL_TX_PACKET_FINAL_CRC_CORRUPT
369.	CG_PL_TX	CP_PL_TX_PACKET_DOUBLE_EARLY_CRC_CORRUPT
370.	CG_PL_TX	CP_PL_TX_PACKET_DOUBLE_LAST_CRC_CORRUPT
371.	CG_PL_TX	CP_PL_TX_PACKET_LENGTH
372.	CG_PL_RX	CP_PL_RX_PACKET_LENGTH
373.	CG_PL_TX	CP_PL_TX_STYPE0
374.	CG_PL_RX	CP_PL_RX_STYPE0
375.	CG_PL_TX	CR_PL_TX_CSTYPE_STYPE0
376.	CG_PL_RX	CR_PL_RX_CSTYPE_STYPE0
377.	CG_PL_TX	CP_PL_TX_PARAMETER0
378.	CG_PL_RX	CP_PL_RX_PARAMETER0
379.	CG_PL_TX	CP_PL_TX_PARAMETER1
380.	CG_PL_RX	CP_PL_RX_PARAMETER1
381.	CG_PL_TX	CP_PL_TX_PACKET_NA_PARAM1
382.	CG_PL_RX	CP_PL_RX_PACKET_NA_PARAM1
383.	CG_PL_TX	CP_PL_TX_STYPE1
384.	CG_PL_RX	CP_PL_RX_STYPE1
385.	CG_PL_TX	CP_PL_TX_CMD
386.	CG_PL_RX	CP_PL_RX_CMD
387.	CG_PL_TX	CR_PL_TX_STYPE1_CMD
388.	CG_PL_RX	CR_PL_RX_STYPE1_CMD
389.	CG_PL_TX	CR_PL_TX_CS_TYPE_STYPE1_CMD
390.	CG_PL_TX	CR_PL_RX_CS_TYPE_STYPE1_CMD
391.	CG_PL_TX	CP_PL_TX_SCS_CORRUPT_CRC
392.	CG_PL_TX	CP_PL_TX_LCS_CORRUPT_CRC
393.	CG_PL_TX	CR_PL_TX_SCS_STYPE0_CORRUPT_CRC
394.	CG_PL_TX	CR_PL_TX_LCS_STYPE0_CORRUPT_CRC
395.	CG_PL_TX	CR_PL_TX_SCS_STYPE1_CMD_CORRUPT_CRC
396.	CG_PL_TX	CR_PL_TX_LCS_STYPE1_CMD_CORRUPT_CRC
397.	CG_PL_TX	CP_PL_TX_RESET_DEV_CMD_B2B
398.	CG_PL_TX	CP_PL_TX_IDLE1
399.	CG_PL_TX	CP_PL_TX_IDLE2
400.	CG_PL_RX	CP_PL_RX_IDLE1
401.	CG_PL_RX	CP_PL_RX_IDLE2
402.	CG_PL_TX_SEQ	CP_PL_TX_PACKET_IDLE_SYMBOL_ERROR
403.	CG_PL_TX_SEQ	CP_PL_TX_CLOCK_COMP_SEQ
404.	CG_PL_RX_SEQ	CP_PL_RX_CLOCK_COMP_SEQ
405.	CG_PL_TX_SEQ	CP_PL_TX_MULTI_LANE_CLK_COMP_ERR
406.	CG_PL_TX_SEQ	CP_PL_TX_NO_CLK_COMP_ERR
407.	CG_PL_TX_SEQ	CP_PL_TX_A_CHARACTER_INTERVAL
408.	CG_PL_TX_SEQ	CP_PL_TX_IDLE2_CORRUPT
409.	CG_PL_TX_SEQ	CP_PL_TX_IDLE2_RANDOM_DATA_LENGTH
410.	CG_PL_RX_SEQ	CP_PL_RX_IDLE2_RANDOM_DATA_LENGTH

411.	CG_PL_TX_SEQ	CP_PL_TX_IDLE2_ACT_LINK_WIDTH
412.	CG_PL_RX_SEQ	CP_PL_RX_IDLE2_ACT_LINK_WIDTH
413.	CG_PL_RX_SEQ	CP_PL_RX_IDLE2_LANE_NUM
414.	CG_PL_TX_SEQ	CP_PL_TX_IDLE2_LANE_NUM
415.	CG_PL_TX_SEQ	CP_PL_TX_IDLE2_CS_FIELD_MARKER_CORRUPT
416.	CG_PL_TX_SEQ	CP_PL_TX_IDLE2_CS_FIELD_CORRUPT
417.	CG_PL_TX_SEQ	CP_PL_TX_IDLE2_CS_FIELD_CMD
418.	CG_PL_TX_SEQ	CP_PL_TX_IDLE2_CS_FIELD_RCVR_TRAINED
419.	CG_PL_TX_SEQ	CP_PL_TX_IDLE2_CS_FIELD_TAP_MINUS_1_STATUS
420.	CG_PL_TX_SEQ	CP_PL_TX_IDLE2_CS_FIELD_TAP_PLUS_1_STATUS
421.	CG_PL_TX_SEQ	CP_PL_TX_IDLE2_CS_FIELD_TAP_MINUS_1_CMD
422.	CG_PL_TX_SEQ	CP_PL_TX_IDLE2_CS_FIELD_TAP_PLUS_1_CMD
423.	CG_PL_TX_SEQ	CP_PL_TX_IDLE2_CS_FIELD_RST_EMP
424.	CG_PL_TX_SEQ	CP_PL_TX_IDLE2_CS_FIELD_PRESET_EMP
425.	CG_PL_TX_SEQ	CP_PL_TX_IDLE2_CS_FIELD_ACK
426.	CG_PL_TX_SEQ	CP_PL_TX_IDLE2_CS_FIELD_NACK
427.	CG_PL_TX_SEQ	CP_PL_TX_IDLE2_IDLE1
428.	CG_PL_TX_SEQ	CP_PL_TX_SYNC_SEQ
429.	CG_PL_TX_SEQ	CP_PL_RX_SYNC_SEQ
430.	CG_PL_SM_VARIABLE	CP_PL_SM_1X_MODE_DELIMITER
431.	CG_PL_SM_VARIABLE	CP_PL_SM_1X_MODE_DETECTED
432.	CG_PL_SM_VARIABLE	CP_PL_SM_2X_MODE_DELIMITER
433.	CG_PL_SM_VARIABLE	CP_PL_SM_2X_A_COL
434.	CG_PL_SM_VARIABLE	CP_PL_SM_NX_A_COL
435.	CG_PL_SM_VARIABLE	CP_PL_SM_2X_A_COUNTER
436.	CG_PL_SM_VARIABLE	CP_PL_SM_NX_A_COUNTER
437.	CG_PL_SM_VARIABLE	CP_PL_SM_2X_M_COUNTER
438.	CG_PL_SM_VARIABLE	CP_PL_SM_NX_M_COUNTER
439.	CG_PL_SM_VARIABLE	CP_PL_SM_2X_ALIGN_ERROR
440.	CG_PL_SM_VARIABLE	CP_PL_SM_NX_ALIGN_ERROR
441.	CG_PL_SM_VARIABLE	CP_PL_SM_D_COUNTER
442.	CG_PL_SM_VARIABLE	CP_PL_SM_DISC_TMR_DONE
443.	CG_PL_SM_VARIABLE	CP_PL_SM_DISC_TMR_START
444.	CG_PL_SM_VARIABLE	CP_PL_SM_DISC_TMR_EN
445.	CG_PL_SM_VARIABLE	CP_PL_SM_FORCE_1X_MODE
446.	CG_PL_SM_VARIABLE	CP_PL_SM_FORCE_LANER
447.	CG_PL_SM_VARIABLE	CP_PL_SM_FORCE_REINIT
448.	CG_PL_SM_VARIABLE	CP_PL_SM_I_COUNTER
449.	CG_PL_SM_VARIABLE	CP_PL_SM_IDLE_SELECTED
450.	CG_PL_SM_VARIABLE	CP_PL_SM_K_COUNTER
451.	CG_PL_SM_VARIABLE	CP_PL_SM_LANE_READY_N
452.	CG_PL_SM_VARIABLE	CP_PL_SM_LANE_SYNC_N
453.	CG_PL_SM_VARIABLE	CP_PL_SM_LANES01_DRVR_OE
454.	CG_PL_SM_VARIABLE	CP_PL_SM_LANES02_DRVR_OE
455.	CG_PL_SM_VARIABLE	CP_PL_SM_LANES13_DRVR_OE
456.	CG_PL_SM_VARIABLE	CP_PL_SM_N_LANES_ALIGNED
457.	CG_PL_SM_VARIABLE	CP_PL_SM_N_LANES_DRVR_OE
458.	CG_PL_SM_VARIABLE	CP_PL_SM_N_LANES_READY

459.	CG_PL_SM_VARIABLE	CP_PL_SM_PORT_INITIALIZED
460.	CG_PL_SM_VARIABLE	CP_PL_SM_RECEIVE_LANE1
461.	CG_PL_SM_VARIABLE	CP_PL_SM_RECEIVE_LANE2
462.	CG_PL_SM_VARIABLE	CP_PL_SM_RCVR_TRAINED_N
463.	CG_PL_SM_VARIABLE	CP_PL_SM_SIGNAL_DETECT_N
464.	CG_PL_SM_VARIABLE	CP_PL_SM_SILENCE_TIMER_DONE
465.	CG_PL_SM_VARIABLE	CP_PL_SM_SILENCE_TIMER_EN
466.	CG_PL_SM_VARIABLE	CP_PL_SM_V_COUNTER
467.	CG_PL_SYNC_SM_LANEX	CP_PL_SYNC_NEXT_STATE
468.	CG_PL_SYNC_SM_LANEX	CP_PL_RESET
469.	CG_PL_SYNC_SM_LANEX	CP_PL_SIGNAL_DETECT
470.	CG_PL_SYNC_SM_LANEX	CR_PL_SYNC_NEXT_STATE_RESET
471.	CG_PL_SYNC_SM_LANEX	CR_PL_SYNC_NEXT_STATE_SIGNAL_DETECT
472.	CG_PL_SYNC_SM_LANEX	CP_PL_SYNC_TO_NS
473.	CG_PL_SYNC_SM_LANEX	CP_PL_SYNC_TO_NS1
474.	CG_PL_SYNC_SM_LANEX	CP_PL_SYNC_TO_NS2
475.	CG_PL_SYNC_SM_LANEX	CP_PL_SYNC_TO_NS3
476.	CG_PL_SYNC_SM_LANEX	CP_PL_SYNC_TO_S
477.	CG_PL_SYNC_SM_LANEX	CP_PL_SYNC_TO_S1
478.	CG_PL_SYNC_SM_LANEX	CP_PL_SYNC_TO_S2
479.	CG_PL_SYNC_SM_LANEX	CP_PL_SYNC_TO_S3
480.	CG_PL_SYNC_SM_LANEX	CP_PL_SYNC_TO_S4
481.	CG_PL_SYNC_SM_LANEX	CP_PL_SYNC_PATH_TRANSITIONS
482.	CG_PL_LANE_ALIGN_2X	CP_PL_LANE_ALIGN_2X_NEXT_STATE
483.	CG_PL_LANE_ALIGN_2X	CP_PL_RESET
484.	CG_PL_LANE_ALIGN_2X	CR_PL_LANE_ALIGN_2X_NEXT_STATE_RESET
485.	CG_PL_LANE_ALIGN_2X	CP_PL_LANE_ALIGN_2X_TO_NA
486.	CG_PL_LANE_ALIGN_2X	CP_PL_LANE_ALIGN_2X_TO_NA1
487.	CG_PL_LANE_ALIGN_2X	CP_PL_LANE_ALIGN_2X_TO_NA2
488.	CG_PL_LANE_ALIGN_2X	CP_PL_LANE_ALIGN_2X_TO_A
489.	CG_PL_LANE_ALIGN_2X	CP_PL_LANE_ALIGN_2X_TO_A1
490.	CG_PL_LANE_ALIGN_2X	CP_PL_LANE_ALIGN_2X_TO_A2
491.	CG_PL_LANE_ALIGN_2X	CP_PL_LANE_ALIGN_2X_TO_A3
492.	CG_PL_LANE_ALIGN_2X	CP_PL_LANE_ALIGN_2X_TO_PATH_TRANSITIONS
493.	CG_PL_LANE_ALIGN_NX	CP_PL_LANE_ALIGN_NX_NEXT_STATE
494.	CG_PL_LANE_ALIGN_NX	CP_PL_RESET
495.	CG_PL_LANE_ALIGN_NX	CR_PL_LANE_ALIGN_NX_NEXT_STATE_RESET
496.	CG_PL_LANE_ALIGN_NX	CP_PL_LANE_ALIGN_NX_TO_NA
497.	CG_PL_LANE_ALIGN_NX	CP_PL_LANE_ALIGN_NX_TO_NA1
498.	CG_PL_LANE_ALIGN_NX	CP_PL_LANE_ALIGN_NX_TO_NA2
499.	CG_PL_LANE_ALIGN_NX	CP_PL_LANE_ALIGN_NX_TO_A
500.	CG_PL_LANE_ALIGN_NX	CP_PL_LANE_ALIGN_NX_TO_A1
501.	CG_PL_LANE_ALIGN_NX	CP_PL_LANE_ALIGN_NX_TO_A2
502.	CG_PL_LANE_ALIGN_NX	CP_PL_LANE_ALIGN_NX_TO_A3
503.	CG_PL_LANE_ALIGN_NX	CP_PL_LANE_ALIGN_NX_TO_PATH_TRANSITIONS
504.	CG_PL_LANE_ALIGN_NX	CP_PL_NUM_OF_LANES
505.	CG_PL_MODE_DETECT_SM	CP_PL_MODE_DETECT_NEXT_STATE
506.	CG_PL_MODE_DETECT_SM	CP_PL_RESET
507.	CG_PL_MODE_DETECT_SM	CP_PL_2_LANES_ALIGNED

508.	CG_PL_MODE_DETECT_SM	CP_PL_MODE_DETECT_TO_INITIALIZE
509.	CG_PL_MODE_DETECT_SM	CP_PL_MODE_DETECT_TO_GET_COLUMN
510.	CG_PL_MODE_DETECT_SM	CP_PL_MODE_DETECT_TO_X1_DELIMITER
511.	CG_PL_MODE_DETECT_SM	CP_PL_MODE_DETECT_TO_X2_DELIMITER
512.	CG_PL_MODE_DETECT_SM	CP_PL_MODE_DETECT_TO_SET_1X_MODE
513.	CG_PL_MODE_DETECT_SM	CP_PL_MODE_DETECT_TO_SET_2X_MODE
514.	CG_PL_MODE_DETECT_SM	CP_PL_MODE_DETECT_PATH_TRANSITIONS
515.	CG_PL_1X_2X_NX_INIT_SM	CP_PL_1X_2X_NX_INIT_NEXT_STATE
516.	CG_PL_1X_2X_NX_INIT_SM	CP_PL_RESET
517.	CG_PL_1X_2X_NX_INIT_SM	CP_PL_FORCE_REINIT
518.	CG_PL_1X_2X_NX_INIT_SM	CR_PL_1X_2X_NX_INIT_NEXT_STATE_RESET
519.	CG_PL_1X_2X_NX_INIT_SM	CR_PL_1X_2X_NX_INIT_NEXT_STATE_FORCE_REINIT
520.	CG_PL_1X_2X_NX_INIT_SM	CP_PL_1X_2X_NX_INIT_TO_SILENT
521.	CG_PL_1X_2X_NX_INIT_SM	CP_PL_1X_2X_NX_INIT_TO_SEEK
522.	CG_PL_1X_2X_NX_INIT_SM	CP_PL_1X_2X_NX_INIT_TO_DISCOVERY
523.	CG_PL_1X_2X_NX_INIT_SM	CP_PL_1X_2X_NX_INIT_TO_1X_RECOVERY
524.	CG_PL_1X_2X_NX_INIT_SM	CP_PL_1X_2X_NX_INIT_TO_2X_RECOVERY
525.	CG_PL_1X_2X_NX_INIT_SM	CP_PL_1X_2X_NX_INIT_TO_NX_MODE
526.	CG_PL_1X_2X_NX_INIT_SM	CP_PL_1X_2X_NX_INIT_TO_2X_MODE
527.	CG_PL_1X_2X_NX_INIT_SM	CP_PL_1X_2X_NX_INIT_TO_1X_MODE_LANE0
528.	CG_PL_1X_2X_NX_INIT_SM	CP_PL_1X_2X_NX_INIT_TO_1X_MODE_LANE1
529.	CG_PL_1X_2X_NX_INIT_SM	CP_PL_1X_2X_NX_INIT_TO_1X_MODE_LANE2
530.	CG_PL_1X_2X_NX_INIT_SM	CP_PL_1X_2X_NX_INIT_PATH_TRANSITIONS
531.	CG_PL_1X_2X_NX_INIT_SM	CP_PL_NUM_OF_LANES
532.	CG_PL_TX	CP_PL_SERIAL_TRAFFIC_MODE
533.	CG_PL_TX	CP_PL_SERIAL_TRAFFIC_VC
534.	CG_PL_TX	CP_PL_TX_CS_DELIMITER
535.	CG_PL_RX	CP_PL_RX_CS_DELIMITER
536.	CG_PL_TX	CP_PL_PORT_INITIALIZED
537.	CG_PL_TX	CR_PL_TX_IDLE1_PORT_INITIALIZED
538.	CG_PL_TX	CR_PL_TX_IDLE2_ PORT_INITIALIZED
539.	CG_PL_TX_SEQ	CP_PL_TX_CS_STATUS_BLOCKED
540.	CG_PL_TX	CP_PL_LINK_INITIALIZED
541.	CG_PL_TX	CR_PL_LINK_INITIALIZED_PORT_INITIALIZED_CS_DELIMITER
542.	CG_PL_TX	CP_PL_INPUT_ERROR_STOPPED_STATE_LINK_INIT
543.	CG_PL_TX	CP_PL_OUTPUT_ERROR_STOPPED_STATE_LINK_INIT
544.	CG_PL_TX	CP_PL_TX_EMBEDDED_CS_STYPE0
545.	CG_PL_TX	CP_PL_TX_EMBEDDED_CS_STYPE1
546.	CG_PL_TX	CP_PL_PACKET_DELIMIT_SEQ
547.	CG_PL_TX	CP_PL_ACK_ID_SEQ
548.	CG_PL_TX	CP_PL_BFM_RCVR_FLW_CTRL
549.	CG_PL_RX	CP_PL_DUT_RCVR_FLW_CTRL
550.	CG_PL_INPUT_PORT_RETRY_STATE	CP_PL_INPUT_PORT_RETRY_STATE
551.	CG_PL_INPUT_PORT_RETRY_STATE	CP_PL_INPUT_PORT_RETRY_TRANSITION
552.	CG_PL_OUTPUT_PORT_RETRY_STATE	CP_PL_OUTPUT_PORT_RETRY_STATE
553.	CG_PL_OUTPUT_PORT_RETRY_STATE	CP_PL_OUTPUT_PORT_RETRY_TRANSITION

554.	CG_PL_TX_SEQ	CP_PL_IDLE1_SEQ_CORRUPT
555.	CG_PL_TX_SEQ	CP_PL_IDLE2_SEQ_ERROR
556.	CG_PL_TX_SEQ	CP_PL_UNEXPECTED_PACKET_ACCEPTED
557.	CG_PL_TX_SEQ	CP_PL_UNEXPECTED_PACKET_NA
558.	CG_PL_TX_SEQ	CP_PL_ACK_CORRUPT_PACKET_ACKID
559.	CG_PL_TX_SEQ	CP_PL_LCS_ERR_END_DELIMITER
560.	CG_PL_TX_SEQ	CP_PL_BFM_TX_PACKET_ERR_INVALID_ACKID
561.	CG_PL_INPUT_PORT_ERROR_STATE	CP_PL_INPUT_PORT_ERROR_STATE
562.	CG_PL_INPUT_PORT_ERROR_STATE	CP_PL_INPUT_PORT_ERROR_TRANSITION
563.	CG_PL_OUTPUT_PORT_ERROR_STATE	CP_PL_OUTPUT_PORT_ERROR_STATE
564.	CG_PL_OUTPUT_PORT_ERROR_STATE	CP_PL_OUTPUT_PORT_ERROR_TRANSITION
565.	CG_PL_TX	CP_PL_TX_IDLE3
566.	CG_PL_RX	CP_PL_RX_IDLE3
567.	CG_PL_TX	CP_PL_TIMESTAMP_SUPPORT
568.	CG_PL_TX	CR_PL_TIMESTAMP_SUPPORT_CS_TYPE
569.	CG_PL_TX	CP_PL_TIMESTAMP_MASTER_SUPPORT
570.	CG_PL_TX	CP_PL_TIMESTAMP_SLAVE_SUPPORT
571.	CG_PL_RX	CR_BFM_RX_CS_TIMESTAMP_MASTER_SUPPORT_SLAVE_SUPPORT
572.	CG_PL_TX	CR_BFM_TX_CS_TIMESTAMP_MASTER_SUPPORT_SLAVE_SUPPORT
573.	CG_PL_TX	CP_BFM_TX_LINK_RESPONSE_INPUT_PORT_STATUS
574.	CG_PL_TX	CP_BFM_TX_LINK_RESPONSE_OUTPUT_PORT_STATUS
575.	CG_PL_RX	CP_BFM_RX_LINK_RESPONSE_INPUT_PORT_STATUS
576.	CG_PL_RX	CP_BFM_RX_LINK_RESPONSE_OUTPUT_PORT_STATUS
577.	CG_PL_TX	CP_BFM_TX_SOP_UNPADDED
578.	CG_PL_TX	CP_BFM_TX_SOP_PADDED
579.	CG_PL_RX	CP_BFM_RX_SOP_UNPADDED
580.	CG_PL_RX	CP_BFM_RX_SOP_PADDED
581.	CG_PL_TX	CP_PL_TX_RESET_PORT_CMD_B2B
582.	CG_GEN3_PL_LONG_RUN_LINK_TRAIN_SM	CP_PL_LONG_RUN_LINK_TRAIN_NEXT_STATE
583.	CG_GEN3_PL_LONG_RUN_LINK_TRAIN_SM	CP_PL_LONG_RUN_LINK_TRAIN_TO_UNTRAINED
584.	CG_GEN3_PL_LONG_RUN_LINK_TRAIN_SM	CP_PL_LONG_RUN_LINK_TRAIN_TO_DME_TRAINING0
585.	CG_GEN3_PL_LONG_RUN_LINK_TRAIN_SM	CP_PL_LONG_RUN_LINK_TRAIN_TO_DME_TRAINING1
586.	CG_GEN3_PL_LONG_RUN_LINK_TRAIN_SM	CP_PL_LONG_RUN_LINK_TRAIN_TO_DME_TRAINING2
587.	CG_GEN3_PL_LONG_RUN_LINK_TRAIN_SM	CP_PL_LONG_RUN_LINK_TRAIN_TO_DME_TRAINING_FAIL
588.	CG_GEN3_PL_LONG_RUN_LINK_TRAIN_SM	CP_PL_LONG_RUN_LINK_TRAIN_PATH_TRANSITIONS
589.	CG_GEN3_PL_LONG_RUN_LINK_TRAIN_SM	CP_PL_LONG_RUN_LINK_TRAIN_TO_TRAINED

590.	CG_GEN3_PL_SHORT_RUN_LINK_TRAIN_SM	CP_PL_SHORT_RUN_LINK_TRAIN_NEXT_STATE
591.	CG_GEN3_PL_SHORT_RUN_LINK_TRAIN_SM	CP_PL_SHORT_RUN_LINK_TRAIN_TO_UNTRAINED
592.	CG_GEN3_PL_SHORT_RUN_LINK_TRAIN_SM	CP_PL_SHORT_RUN_LINK_TRAIN_TO_CW_TRAINING0
593.	CG_GEN3_PL_SHORT_RUN_LINK_TRAIN_SM	CP_PL_SHORT_RUN_LINK_TRAIN_TO_CW_TRAINING1
594.	CG_GEN3_PL_SHORT_RUN_LINK_TRAIN_SM	CP_PL_SHORT_RUN_LINK_TRAIN_TO_CW_TRAINING_FAIL
595.	CG_GEN3_PL_SHORT_RUN_LINK_TRAIN_SM	CP_PL_SHORT_RUN_LINK_TRAIN_TO_TRAINED
596.	CG_GEN3_PL_SHORT_RUN_LINK_TRAIN_SM	CP_PL_SHORT_RUN_LINK_TRAIN_TO_KEEP_ALIVE
597.	CG_GEN3_PL_SHORT_RUN_LINK_TRAIN_SM	CP_PL_SHORT_RUN_LINK_TRAIN_TO_RETRAINING0
598.	CG_GEN3_PL_SHORT_RUN_LINK_TRAIN_SM	CP_PL_SHORT_RUN_LINK_TRAIN_TO_RETRAINING1
599.	CG_GEN3_PL_SHORT_RUN_LINK_TRAIN_SM	CP_PL_SHORT_RUN_LINK_TRAIN_TO_RETRAINING2
600.	CG_GEN3_PL_SHORT_RUN_LINK_TRAIN_SM	CP_PL_SHORT_RUN_LINK_TRAIN_TO_RETRAIN_FAIL
601.	CG_GEN3_PL_SHORT_RUN_LINK_TRAIN_SM	CP_PL_SHORT_RUN_LINK_TRAIN_PATH_TRANSITIONS
602.	CG_GEN3_PL_CW_LOCK_SM	CP_PL_CW_LOCK_NEXT_STATE
603.	CG_GEN3_PL_CW_LOCK_SM	CP_PL_CW_LOCK_TO_NO_LOCK
604.	CG_GEN3_PL_CW_LOCK_SM	CP_PL_CW_LOCK_TO_SLIP_ALIGNMENT
605.	CG_GEN3_PL_CW_LOCK_SM	CP_PL_CW_LOCK_TO_NO_LOCK1
606.	CG_GEN3_PL_CW_LOCK_SM	CP_PL_CW_LOCK_TO_NO_LOCK2
607.	CG_GEN3_PL_CW_LOCK_SM	CP_PL_CW_LOCK_TO_NO_LOCK3
608.	CG_GEN3_PL_CW_LOCK_SM	CP_PL_CW_LOCK_TO_LOCK
609.	CG_GEN3_PL_CW_LOCK_SM	CP_PL_CW_LOCK_TO_LOCK1
610.	CG_GEN3_PL_CW_LOCK_SM	CP_PL_CW_LOCK_TO_LOCK2
611.	CG_GEN3_PL_CW_LOCK_SM	CP_PL_CW_LOCK_TO_LOCK3
612.	CG_GEN3_PL_CW_LOCK_SM	CP_PL_CW_LOCK_PATH_TRANSITIONS
613.	CG_GEN3_PL_LANE_SYNC_SM	CP_PL_GEN3_LANE_SYNC_NEXT_STATE
614.	CG_GEN3_PL_LANE_SYNC_SM	CP_PL_RESET
615.	CG_GEN3_PL_LANE_SYNC_SM	CP_PL_CW_LOCK
616.	CG_GEN3_PL_LANE_SYNC_SM	CR_PL_GEN3_LANE_SYNC_NEXT_STATE_RESET
617.	CG_GEN3_PL_LANE_SYNC_SM	CR_PL_GEN3_LANE_SYNC_NEXT_STATE_CW_LOCK
618.	CG_GEN3_PL_LANE_SYNC_SM	CP_PL_GEN3_LANE_SYNC_TO_NO_SYNC
619.	CG_GEN3_PL_LANE_SYNC_SM	CP_PL_GEN3_LANE_SYNC_TO_NO_SYNC1
620.	CG_GEN3_PL_LANE_SYNC_SM	CP_PL_GEN3_LANE_SYNC_TO_NO_SYNC2
621.	CG_GEN3_PL_LANE_SYNC_SM	CP_PL_GEN3_LANE_SYNC_TO_NO_SYNC3
622.	CG_GEN3_PL_LANE_SYNC_SM	CP_PL_GEN3_LANE_SYNC_TO_NO_SYNC4
623.	CG_GEN3_PL_LANE_SYNC_SM	CP_PL_GEN3_LANE_SYNC_TO_SYNC
624.	CG_GEN3_PL_LANE_SYNC_SM	CP_PL_GEN3_LANE_SYNCTO_SYNC1
625.	CG_GEN3_PL_LANE_SYNC_SM	CP_PL_GEN3_LANE_SYNC_TO_SYNC2
626.	CG_GEN3_PL_LANE_SYNC_SM	CP_PL_GEN3_LANE_SYNC_PATH_TRANSITIONS

627.	CG_GEN3_PL_2X_LANE_ALIGN_SM	CP_PL_LANE_ALIGN_2X_NEXT_STATE
628.	CG_GEN3_PL_2X_LANE_ALIGN_SM	CP_PL_RESET
629.	CG_GEN3_PL_2X_LANE_ALIGN_SM	CR_PL_LANE_ALIGN_2X_NEXT_STATE_RESET
630.	CG_GEN3_PL_2X_LANE_ALIGN_SM	CP_PL_LANE_ALIGN_2X_TO_NA
631.	CG_GEN3_PL_2X_LANE_ALIGN_SM	CP_PL_LANE_ALIGN_2X_TO_NA1
632.	CG_GEN3_PL_2X_LANE_ALIGN_SM	CP_PL_LANE_ALIGN_2X_TO_NA2
633.	CG_GEN3_PL_2X_LANE_ALIGN_SM	CP_PL_LANE_ALIGN_2X_TO_NA3
634.	CG_GEN3_PL_2X_LANE_ALIGN_SM	CP_PL_LANE_ALIGN_2X_TO_A
635.	CG_GEN3_PL_2X_LANE_ALIGN_SM	CP_PL_LANE_ALIGN_2X_TO_A1
636.	CG_GEN3_PL_2X_LANE_ALIGN_SM	CP_PL_LANE_ALIGN_2X_TO_A2
637.	CG_GEN3_PL_2X_LANE_ALIGN_SM	CP_PL_LANE_ALIGN_2X_TO_A3
638.	CG_GEN3_PL_2X_LANE_ALIGN_SM	CP_PL_LANE_ALIGN_2X_TO_A4
639.	CG_GEN3_PL_2X_LANE_ALIGN_SM	CP_PL_LANE_ALIGN_2X_TO_A5
640.	CG_GEN3_PL_2X_LANE_ALIGN_SM	CP_PL_LANE_ALIGN_2X_TO_A6
641.	CG_GEN3_PL_2X_LANE_ALIGN_SM	CP_PL_LANE_ALIGN_2X_TO_A7
642.	CG_GEN3_PL_2X_LANE_ALIGN_SM	CP_PL_LANE_ALIGN_2X_PATH_TRANSITIONS
643.	CG_GEN3_PL_NX_LANE_ALIGN_SM	CP_PL_LANE_ALIGN_NX_NEXT_STATE
644.	CG_GEN3_PL_NX_LANE_ALIGN_SM	CP_PL_RESET
645.	CG_GEN3_PL_NX_LANE_ALIGN_SM	CR_PL_LANE_ALIGN_NX_NEXT_STATE_RESET
646.	CG_GEN3_PL_NX_LANE_ALIGN_SM	CP_PL_LANE_ALIGN_NX_TO_NA
647.	CG_GEN3_PL_NX_LANE_ALIGN_SM	CP_PL_LANE_ALIGN_NX_TO_NA1
648.	CG_GEN3_PL_NX_LANE_ALIGN_SM	CP_PL_LANE_ALIGN_NX_TO_NA2
649.	CG_GEN3_PL_NX_LANE_ALIGN_SM	CP_PL_LANE_ALIGN_NX_TO_NA3
650.	CG_GEN3_PL_NX_LANE_ALIGN_SM	CP_PL_LANE_ALIGN_NX_TO_A
651.	CG_GEN3_PL_NX_LANE_ALIGN_SM	CP_PL_LANE_ALIGN_NX_TO_A1
652.	CG_GEN3_PL_NX_LANE_ALIGN_SM	CP_PL_LANE_ALIGN_NX_TO_A2
653.	CG_GEN3_PL_NX_LANE_ALIGN_SM	CP_PL_LANE_ALIGN_NX_TO_A3
654.	CG_GEN3_PL_NX_LANE_ALIGN_SM	CP_PL_LANE_ALIGN_NX_TO_A4
655.	CG_GEN3_PL_NX_LANE_ALIGN_SM	CP_PL_LANE_ALIGN_NX_TO_A5
656.	CG_GEN3_PL_NX_LANE_ALIGN_SM	CP_PL_LANE_ALIGN_NX_TO_A6
657.	CG_GEN3_PL_NX_LANE_ALIGN_SM	CP_PL_LANE_ALIGN_NX_TO_A7
658.	CG_GEN3_PL_NX_LANE_ALIGN_SM	CP_PL_LANE_ALIGN_NX_PATH_TRANSITIONS
659.	CG_GEN3_PL_1X_2X_NX_PORT_INIT_SM	CP_PL_1X_2X_NX_INIT_NEXT_STATE
660.	CG_GEN3_PL_1X_2X_NX_PORT_INIT_SM	CP_PL_RESET
661.	CG_GEN3_PL_1X_2X_NX_PORT_INIT_SM	CP_PL_FORCE_REINIT
662.	CG_GEN3_PL_1X_2X_NX_PORT_INIT_SM	CR_PL_1X_2X_NX_INIT_NEXT_STATE_RESET
663.	CG_GEN3_PL_1X_2X_NX_PORT_INIT_SM	CR_PL_1X_2X_NX_INIT_NEXT_STATE_FORCE_REINIT
664.	CG_GEN3_PL_1X_2X_NX_PORT_INIT_SM	CP_PL_1X_2X_NX_INIT_TO_ASYM_MODE
665.	CG_GEN3_PL_1X_2X_NX_PORT_INIT_SM	CP_PL_1X_2X_NX_INIT_TO_SILENT
666.	CG_GEN3_PL_1X_2X_NX_PORT_INIT_SM	CP_PL_1X_2X_NX_INIT_TO_SEEK
667.	CG_GEN3_PL_1X_2X_NX_PORT_INIT_SM	CP_PL_1X_2X_NX_INIT_TO_DISCOVERY

668.	CG_GEN3_PL_1X_2X_NX_PORT_INIT_SM	CP_PL_1X_2X_NX_INIT_TO_1X_RETRAIN
669.	CG_GEN3_PL_1X_2X_NX_PORT_INIT_SM	CP_PL_1X_2X_NX_INIT_TO_1X_RECOVERY
670.	CG_GEN3_PL_1X_2X_NX_PORT_INIT_SM	CP_PL_1X_2X_NX_INIT_TO_1X_MODE_LANE0
671.	CG_GEN3_PL_1X_2X_NX_PORT_INIT_SM	CP_PL_1X_2X_NX_INIT_TO_1X_MODE_LANE1
672.	CG_GEN3_PL_1X_2X_NX_PORT_INIT_SM	CP_PL_1X_2X_NX_INIT_TO_1X_MODE_LANE2
673.	CG_GEN3_PL_1X_2X_NX_PORT_INIT_SM	CP_PL_1X_2X_NX_INIT_TO_NX_RETRAIN
674.	CG_GEN3_PL_1X_2X_NX_PORT_INIT_SM	CP_PL_1X_2X_NX_INIT_TO_2X_RETRAIN
675.	CG_GEN3_PL_1X_2X_NX_PORT_INIT_SM	CP_PL_1X_2X_NX_INIT_TO_NX_RECOVERY
676.	CG_GEN3_PL_1X_2X_NX_PORT_INIT_SM	CP_PL_1X_2X_NX_INIT_TO_2X_RECOVERY
677.	CG_GEN3_PL_1X_2X_NX_PORT_INIT_SM	CP_PL_1X_2X_NX_INIT_TO_NX_MODE
678.	CG_GEN3_PL_1X_2X_NX_PORT_INIT_SM	CP_PL_1X_2X_NX_INIT_TO_2X_MODE
679.	CG_GEN3_PL_1X_2X_NX_PORT_INIT_SM	CP_PL_NUM_OF_LANES
680.	CG_GEN3_PL_1X_2X_NX_PORT_INIT_SM	CG_GEN3_PL_1X_2X_NX_PORT_INIT_PATH_TRANSITIONS
681.	CG_GEN3_PL_RETRAIN_TRANSMIT_WIDTH_CTRL_SM	CP_PL_RETRAIN_TX_WIDTH_CTRL_NEXT_STATE
682.	CG_GEN3_PL_RETRAIN_TRANSMIT_WIDTH_CTRL_SM	CP_PL_RETRAIN_TX_WIDTH_CTRL_TO_IDLE
683.	CG_GEN3_PL_RETRAIN_TRANSMIT_WIDTH_CTRL_SM	CP_PL_RETRAIN_TX_WIDTH_CTRL_TO_XMT_WIDTH
684.	CG_GEN3_PL_RETRAIN_TRANSMIT_WIDTH_CTRL_SM	CP_PL_RETRAIN_TX_WIDTH_CTRL_TO_RETRAIN0
685.	CG_GEN3_PL_RETRAIN_TRANSMIT_WIDTH_CTRL_SM	CP_PL_RETRAIN_TX_WIDTH_CTRL_TO_RETRAIN1
686.	CG_GEN3_PL_RETRAIN_TRANSMIT_WIDTH_CTRL_SM	CP_PL_RETRAIN_TX_WIDTH_CTRL_TO_RETRAIN2
687.	CG_GEN3_PL_RETRAIN_TRANSMIT_WIDTH_CTRL_SM	CP_PL_RETRAIN_TX_WIDTH_CTRL_TO_RETRAIN3
688.	CG_GEN3_PL_RETRAIN_TRANSMIT_WIDTH_CTRL_SM	CP_PL_RETRAIN_TX_WIDTH_CTRL_TO_RETRAIN4
689.	CG_GEN3_PL_RETRAIN_TRANSMIT_WIDTH_CTRL_SM	CP_PL_RETRAIN_TX_WIDTH_CTRL_TO_RETRAIN5
690.	CG_GEN3_PL_RETRAIN_TRANSMIT_WIDTH_CTRL_SM	CP_PL_RETRAIN_TX_WIDTH_CTRL_TO_RETRAIN_TIMEOUT
691.	CG_GEN3_PL_RETRAIN_TRANSMIT_WIDTH_CTRL_SM	CP_PL_RETRAIN_TX_WIDTH_CTRL_PATH_TRANSITIONS
692.	CG_GEN3_PL_TRANSMIT_WIDTH_CMD_SM	CP_PL_TX_WIDTH_CMD_NEXT_STATE

693.	CG_GEN3_PL_TRANSMIT_WIDTH_CMD_SM	CP_PL_TX_WIDTH_CMD_TO_CMD2
694.	CG_GEN3_PL_TRANSMIT_WIDTH_CMD_SM	CP_PL_TX_WIDTH_CMD_TO_CMD3
695.	CG_GEN3_PL_TRANSMIT_WIDTH_CMD_SM	CP_PL_TX_WIDTH_CMD_TO_CMD_IDLE
696.	CG_GEN3_PL_TRANSMIT_WIDTH_CMD_SM	CP_PL_TX_WIDTH_CMD_TO_CMD1
697.	CG_GEN3_PL_TRANSMIT_WIDTH_CMD_SM	CP_PL_TX_WIDTH_CMD_TO_PATH_TRANSITIONS
698.	CG_GEN3_PL_TRANSMIT_WIDTH_SM	CP_PL_TX_WIDTH_NEXT_STATE
699.	CG_GEN3_PL_TRANSMIT_WIDTH_SM	CP_PL_ASYM_MODE
700.	CG_GEN3_PL_TRANSMIT_WIDTH_SM	CP_PL_PISM_SILENT
701.	CG_GEN3_PL_TRANSMIT_WIDTH_SM	CP_PL_TX_WIDTH_TO_ASYM_XMT_EXIT
702.	CG_GEN3_PL_TRANSMIT_WIDTH_SM	CP_PL_TX_WIDTH_TO_ASYM_XMT_IDLE
703.	CG_GEN3_PL_TRANSMIT_WIDTH_SM	CP_PL_TX_WIDTH_TO_XMT_WIDTH_NACK
704.	CG_GEN3_PL_TRANSMIT_WIDTH_SM	CP_PL_TX_WIDTH_TO_SEEK_1X_MODE_XMT
705.	CG_GEN3_PL_TRANSMIT_WIDTH_SM	CP_PL_TX_WIDTH_TO_SEEK_1X_MODE_XMT1
706.	CG_GEN3_PL_TRANSMIT_WIDTH_SM	CP_PL_TX_WIDTH_TO_SEEK_1X_MODE_XMT2
707.	CG_GEN3_PL_TRANSMIT_WIDTH_SM	CP_PL_TX_WIDTH_TO_SEEK_1X_MODE_XMT3
708.	CG_GEN3_PL_TRANSMIT_WIDTH_SM	CP_PL_TX_WIDTH_TO_1X_MODE_XMT_ACK
709.	CG_GEN3_PL_TRANSMIT_WIDTH_SM	CP_PL_TX_WIDTH_TO_1X_MODE_XMT
710.	CG_GEN3_PL_TRANSMIT_WIDTH_SM	CP_PL_TX_WIDTH_TO_SEEK_2X_MODE_XMT
711.	CG_GEN3_PL_TRANSMIT_WIDTH_SM	CP_PL_TX_WIDTH_TO_SEEK_2X_MODE_XMT1
712.	CG_GEN3_PL_TRANSMIT_WIDTH_SM	CP_PL_TX_WIDTH_TO_SEEK_2X_MODE_XMT2
713.	CG_GEN3_PL_TRANSMIT_WIDTH_SM	CP_PL_TX_WIDTH_TO_SEEK_2X_MODE_XMT3
714.	CG_GEN3_PL_TRANSMIT_WIDTH_SM	CP_PL_TX_WIDTH_TO_SEEK_2X_MODE_XMT_ACK
715.	CG_GEN3_PL_TRANSMIT_WIDTH_SM	CP_PL_TX_WIDTH_TO_SEEK_2X_MODE_XMT
716.	CG_GEN3_PL_TRANSMIT_WIDTH_SM	CP_PL_TX_WIDTH_TO_SEEK_NX_MODE_XMT
717.	CG_GEN3_PL_TRANSMIT_WIDTH_SM	CP_PL_TX_WIDTH_TO_SEEK_NX_MODE_XMT1
718.	CG_GEN3_PL_TRANSMIT_WIDTH_SM	CP_PL_TX_WIDTH_TO_SEEK_NX_MODE_XMT2
719.	CG_GEN3_PL_TRANSMIT_WIDTH_SM	CP_PL_TX_WIDTH_TO_SEEK_NX_MODE_XMT3
720.	CG_GEN3_PL_TRANSMIT_WIDTH_SM	CP_PL_TX_WIDTH_TO_NX_MODE_XMT_ACK
721.	CG_GEN3_PL_TRANSMIT_WIDTH_SM	CP_PL_TX_WIDTH_TO_NX_MODE_XMT
722.	CG_GEN3_PL_TRANSMIT_WIDTH_SM	CP_PL_TX_WIDTH_PATH_TRANSITIONS
723.	CG_GEN3_PL_RECEIVE_WIDTH_CMD_SM	CP_PL_RX_WIDTH_CMD_NEXT_STATE
724.	CG_GEN3_PL_RECEIVE_WIDTH_CMD_SM	CP_PL_RX_WIDTH_CMD_TO_RCV_WIDTH_CMD2
725.	CG_GEN3_PL_RECEIVE_WIDTH_CMD_SM	CP_PL_RX_WIDTH_CMD_TO_RCV_WIDTH_CMD3
726.	CG_GEN3_PL_RECEIVE_WIDTH_CMD_SM	CP_PL_RX_WIDTH_CMD_TO_RCV_WIDTH_CMD_IDLE
727.	CG_GEN3_PL_RECEIVE_WIDTH_CMD_SM	CP_PL_RX_WIDTH_CMD_TO_RCV_WIDTH_CMD1
728.	CG_GEN3_PL_RECEIVE_WIDTH_CMD_SM	CP_PL_RX_WIDTH_CMD_PATH_TRANSITIONS
729.	CG_GEN3_PL_RECEIVE_WIDTH_SM	CP_PL_RX_WIDTH_NEXT_STATE
730.	CG_GEN3_PL_RECEIVE_WIDTH_SM	CP_PL_ASYM_MODE
731.	CG_GEN3_PL_RECEIVE_WIDTH_SM	CP_PL_PISM_SILENT

732.	CG_GEN3_PL_RECEIVE_WIDTH_SM	CP_PL_RX_WIDTH_TO_ASYM_RCV_EXIT
733.	CG_GEN3_PL_RECEIVE_WIDTH_SM	CP_PL_RX_WIDTH_TO_ASYM_RCV_IDLE
734.	CG_GEN3_PL_RECEIVE_WIDTH_SM	CP_PL_RX_WIDTH_TO_RCV_WIDTH_NACK
735.	CG_GEN3_PL_RECEIVE_WIDTH_SM	CP_PL_RX_WIDTH_TO_SEEK_1X_MODE_RCV
736.	CG_GEN3_PL_RECEIVE_WIDTH_SM	CP_PL_RX_WIDTH_TO_1X_MODE_RCV_ACK
737.	CG_GEN3_PL_RECEIVE_WIDTH_SM	CP_PL_RX_WIDTH_TO_SEEK_1X_RETRAIN
738.	CG_GEN3_PL_RECEIVE_WIDTH_SM	CP_PL_RX_WIDTH_TO_1X_RECOVERY
739.	CG_GEN3_PL_RECEIVE_WIDTH_SM	CP_PL_RX_WIDTH_TO_1X_MODE_RCV
740.	CG_GEN3_PL_RECEIVE_WIDTH_SM	CP_PL_RX_WIDTH_TO_SEEK_2X_MODE_RCV
741.	CG_GEN3_PL_RECEIVE_WIDTH_SM	CP_PL_RX_WIDTH_TO_2X_MODE_RCV_ACK
742.	CG_GEN3_PL_RECEIVE_WIDTH_SM	CP_PL_RX_WIDTH_TO_SEEK_2X_RETRAIN
743.	CG_GEN3_PL_RECEIVE_WIDTH_SM	CP_PL_RX_WIDTH_TO_SEEK_2X_RECOVERY
744.	CG_GEN3_PL_RECEIVE_WIDTH_SM	CP_PL_RX_WIDTH_TO_SEEK_2X_MODE_RCV
745.	CG_GEN3_PL_RECEIVE_WIDTH_SM	CP_PL_RX_WIDTH_TO_SEEK_NX_MODE_RCV
746.	CG_GEN3_PL_RECEIVE_WIDTH_SM	CP_PL_RX_WIDTH_TO_NX_MODE_RCV_ACK
747.	CG_GEN3_PL_RECEIVE_WIDTH_SM	CP_PL_RX_WIDTH_TO_NX_RETRAIN
748.	CG_GEN3_PL_RECEIVE_WIDTH_SM	CP_PL_RX_WIDTH_TO_NX_RECOVERY
749.	CG_GEN3_PL_RECEIVE_WIDTH_SM	CP_PL_RX_WIDTH_TO_NX_MODE_RCV
750.	CG_GEN3_PL_RECEIVE_WIDTH_SM	CP_PL_RX_WIDTH_PATH_TRANSITIONS
751.	CG_GEN3_PL_TX_CODE_WORD_LANE n	CP_PL_TX_TYPE_NOT_TYPE
752.	CG_GEN3_PL_TX_CODE_WORD_LANE n	CP_PL_TX_INVERTED
753.	CG_GEN3_PL_TX_CODE_WORD_LANE n	CR_PL_TX_TYPE_NOT_TYPE_INVERTED
754.	CG_GEN3_PL_TX_CODE_WORD_LANE n	CP_PL_TX_CC_TYPE
755.	CG_GEN3_PL_TX_CODE_WORD_LANE n	CP_PL_TX_DATA_TYPE
756.	CG_GEN3_PL_TX_CODE_WORD_LANE n	CP_PL_TX_CSB_DATA_00
757.	CG_GEN3_PL_TX_CODE_WORD_LANE n	CP_PL_TX_CSE_DATA_00
758.	CG_GEN3_PL_TX_CODE_WORD_LANE n	CR_PL_TX_CC_TYPE_DATA_TYPE
759.	CG_GEN3_PL_RX_CODE_WORD_LANE n	CP_PL_RX_TYPE_NOT_TYPE
760.	CG_GEN3_PL_RX_CODE_WORD_LANE n	CP_PL_RX_INVERTED
761.	CG_GEN3_PL_RX_CODE_WORD_LANE n	CR_PL_RX_TYPE_NOT_TYPE_INVERTED
762.	CG_GEN3_PL_RX_CODE_WORD_LANE n	CP_PL_RX_CC_TYPE
763.	CG_GEN3_PL_RX_CODE_WORD_LANE n	CP_PL_RX_DATA_TYPE
764.	CG_GEN3_PL_RX_CODE_WORD_LANE n	CR_PL_RX_CC_TYPE_DATA_TYPE
765.	CG_GEN3_PL_RX_CODE_WORD_LANE n	CP_PL_RX_CSB_DATA_00
766.	CG_GEN3_PL_RX_CODE_WORD_LANE	CP_PL_RX_CSE_DATA_00

	n	
767.	CG_GEN3_PL_TX_OS_LANEn	CP_PL_TX_SKIP_OS
768.	CG_GEN3_PL_TX_OS_LANEn	CP_PL_TX_INCORRECT_SKIP
769.	CG_GEN3_PL_TX_OS_LANEn	CP_PL_TX_SEED_OS
770.	CG_GEN3_PL_TX_OS_LANEn	CP_PL_TX_MULTI_LANE_OS_NONALIGN
771.	CG_GEN3_PL_TX_OS_LANEn	CP_PL_LANE_SYNC_N
772.	CG_GEN3_PL_TX_OS_LANEn	CP_PL_TX_STATUS_CONTROL_OS
773.	CG_GEN3_PL_RX_OS_LANEn	CP_PL_RX_SKIP_OS
774.	CG_GEN3_PL_RX_OS_LANEn	CP_PL_RX_SEED_OS
775.	CG_GEN3_PL_RX_OS_LANEn	CP_PL_LANE_SYNC_N
776.	CG_GEN3_PL_RX_OS_LANEn	CP_PL_RX_STATUS_CONTROL_OS
777.	CG_GEN3_PL_TERMINATING_PKT_LENGTH2	CP_PL_TX_PACKET_BOUNDARY
778.	CG_GEN3_PL_TX_SEEDOS_LINKREQ_SEQ	CP_PL_TX_SEED_OS_LINK_REQUEST_CS
779.	CG_GEN3_PL_TX_SEEDOS_LINKREQ_SEQ	CP_PL_LANE_WIDTH
780.	CG_GEN3_PL_TX_SEEDOS_LINKREQ_SEQ	CR_PL_SEEDOS_LINKREQ_LANEWIDTH
781.	CG_GEN3_PL_CRC	CP_PL_TX_CORRUPT_CRC32
782.	CG_GEN3_PL_LENGTH	CP_PL_TX_PACKET_LENGTH
783.	CG_GEN3_PL_TERMINATING_PKT_LENGTH1	CP_PL_TX_PACKET_BOUNDARY
784.	CG_GEN3_PL_RX_AET_TAP_CMDSTS_LANEn	CP_PL_TX_EQUALIZER_TAP
785.	CG_GEN3_PL_RX_AET_TAP_CMDSTS_LANEn	CP_PL_TX_EQUALIZER_CMD
786.	CG_GEN3_PL_RX_AET_TAP_CMDSTS_LANEn	CP_PL_TX_EQUALIZER_STATUS
787.	CG_GEN3_PL_RX_AET_TAP_CMDSTS_LANEn	CP_PL_TX_EQUALIZER_CMD_STATUS
788.	CG_GEN3_PL_TX_AET_LANEn	CP_PL_TX_LANE
789.	CG_GEN3_PL_TX_AET_LANEn	CP_PL_LANE_DEGRADED_N
790.	CG_GEN3_PL_TX_AET_LANEn	CP_PL_LANE_TRAINED_N
791.	CG_GEN3_PL_TX_AET_LANEn	CP_PL_10G_RETRAIN_ENABLE_N
792.	CG_GEN3_PL_TX_AET_LANEn	CR_PL_LANE_DEGRADED_TRAINED_10G_RETRAIN_ENABLE_N
793.	CG_GEN3_PL_RX_AET_TAP_CMDSTS_LANEn	CP_PL_RX_EQUALIZER_TAP
794.	CG_GEN3_PL_RX_AET_TAP_CMDSTS_LANEn	CP_PL_RX_EQUALIZER_CMD
795.	CG_GEN3_PL_RX_AET_TAP_CMDSTS_LANEn	CP_PL_RX_EQUALIZER_STATUS
796.	CG_GEN3_PL_RX_AET_TAP_CMDSTS_LANEn	CR_PL_RX_EQUALIZER_CMD_STATUS
797.	CG_GEN3_PL_RX_AET_LANEn	CP_PL_RX_LANE
798.	CG_GEN3_PL_RX_AET_LANEn	CP_PL_LANE_DEGRADED_N
799.	CG_GEN3_PL_RX_AET_LANEn	CP_PL_LANE_TRAINED_N
800.	CG_GEN3_PL_RX_AET_LANEn	CP_PL_10G_RETRAIN_ENABLE_N
801.	CG_GEN3_PL_RX_AET_LANEn	CR_PL_LANE_DEGRADED_TRAINED_10G_RETRAIN

		_ENABLE_N
802.	CG_GEN3_PL_ASYMMETRY	CP_PL_ASYMMETRY_MODE
803.	CG_GEN3_PL_ASYMMETRY	CP_PL_TX_WIDTH_PORT_REQ
804.	CG_GEN3_PL_ASYMMETRY	CR_PL_TX_WIDTH_PORT_CMD_ASYM
805.	CG_GEN3_PL_TSG	CP_PL_TSG_UNINTERRUPTED
806.	CG_GEN3_PL_FRAME_LOCK_SM	CP_PL_GEN3_FRAME_LOCK_NEXT_STATE
807.	CG_GEN3_PL_FRAME_LOCK_SM	CP_PL_GEN3_FRAME_LOCK_TO_RSTCNT
808.	CG_GEN3_PL_FRAME_LOCK_SM	CP_PL_GEN3_FRAME_LOCK_TO_GNM
809.	CG_GEN3_PL_FRAME_LOCK_SM	CP_PL_GEN3_FRAME_LOCK_TO_TM
810.	CG_GEN3_PL_FRAME_LOCK_SM	CP_PL_GEN3_FRAME_LOCK_TO_VM_IVM
811.	CG_GEN3_PL_FRAME_LOCK_SM	CP_PL_GEN3_FRAME_LOCK_TO_INF
812.	CG_GEN3_PL_FRAME_LOCK_SM	CP_PL_GEN3_FRAME_LOCK_TO_SLIP
813.	CG_GEN3_PL_FRAME_LOCK_SM	CP_PL_GEN3_FRAME_LOCK_PATH_TRANSITIONS
814.	CG_GEN3_PL_C0_COEFF_UPDATE_SM	CP_PL_GEN3_PL_C0_COEFF_UPDATE_NEXT_STATE
815.	CG_GEN3_PL_C0_COEFF_UPDATE_SM	CP_PL_GEN3_PL_C0_COEFF_UPDATE_NU
816.	CG_GEN3_PL_C0_COEFF_UPDATE_SM	CP_PL_GEN3_PL_C0_COEFF_UPDATE_UPCOEFF
817.	CG_GEN3_PL_C0_COEFF_UPDATE_SM	CP_PL_GEN3_PL_C0_COEFF_UPDATE_UP
818.	CG_GEN3_PL_C0_COEFF_UPDATE_SM	CP_PL_GEN3_PL_C0_COEFF_UPDATE_MAX
819.	CG_GEN3_PL_C0_COEFF_UPDATE_SM	CP_PL_GEN3_PL_C0_COEFF_UPDATE_MIN
820.	CG_GEN3_PL_C0_COEFF_UPDATE_SM	CP_PL_GEN3_PL_C0_COEFF_UPDATE_PATH
821.	CG_GEN3_PL_CP1_COEFF_UPDATE_SM	CP_PL_GEN3_PL_CP1_COEFF_UPDATE_NEXT_STATE
822.	CG_GEN3_PL_CP1_COEFF_UPDATE_SM	CP_PL_GEN3_PL_CP1_COEFF_UPDATE_NU
823.	CG_GEN3_PL_CP1_COEFF_UPDATE_SM	CP_PL_GEN3_PL_CP1_COEFF_UPDATE_UPCOEFF
824.	CG_GEN3_PL_CP1_COEFF_UPDATE_SM	CP_PL_GEN3_PL_CP1_COEFF_UPDATE_UP
825.	CG_GEN3_PL_CP1_COEFF_UPDATE_SM	CP_PL_GEN3_PL_CP1_COEFF_UPDATE_MAX
826.	CG_GEN3_PL_CP1_COEFF_UPDATE_SM	CP_PL_GEN3_PL_CP1_COEFF_UPDATE_MIN
827.	CG_GEN3_PL_CP1_COEFF_UPDATE_SM	CP_PL_GEN3_PL_CP1_COEFF_UPDATE_PATH
828.	CG_GEN3_PL_CN1_COEFF_UPDATE_SM	CP_PL_GEN3_PL_CN1_COEFF_UPDATE_NEXT_STATE
829.	CG_GEN3_PL_CN1_COEFF_UPDATE_SM	CP_PL_GEN3_PL_CN1_COEFF_UPDATE_NU
830.	CG_GEN3_PL_CN1_COEFF_UPDATE_SM	CP_PL_GEN3_PL_CN1_COEFF_UPDATE_UPCOEFF
831.	CG_GEN3_PL_CN1_COEFF_UPDATE_SM	CP_PL_GEN3_PL_CN1_COEFF_UPDATE_UP
832.	CG_GEN3_PL_CN1_COEFF_UPDATE_SM	CP_PL_GEN3_PL_CN1_COEFF_UPDATE_MAX
833.	CG_GEN3_PL_CN1_COEFF_UPDATE_SM	CP_PL_GEN3_PL_CN1_COEFF_UPDATE_MIN
834.	CG_GEN3_PL_CN1_COEFF_UPDATE_SM	CP_PL_GEN3_PL_CN1_COEFF_UPDATE_PATH

8. Tools Used

Tools Used	Version	Vendor	Platform
IUS	Incisive_12.10.020	Cadence	Linux
VCS	vcs-mx_vI-2014.03	Synopsys	Linux
Questa	Questa_10.1d	Mentor	Linux
UVM	1.1c	Accellera	Linux