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I used Part A for Part B, so the code is the total code for both parts.

Final Code:

```
1  library IEEE;
2  USE IEEE.std_logic_1164.ALL;
3  USE IEEE.numeric_std.ALL;
4
5  ENTITY Hw5A IS
6  GENERIC(len_in: INTEGER := 8);
7  PORT (input: IN std_logic_vector ((len_in-1) DOWNT0 0);
8       hamming_weight: OUT INTEGER RANGE 0 TO len_in;
9       oneCounter: OUT BIT_VECTOR ((len_in-1) DOWNT0 0));
10 END ENTITY;
11
12 ARCHITECTURE concurrent OF Hw5A IS
13     TYPE integer_array IS array (0 to len_in) of integer range 0 to len_in;
14     SIGNAL internal: integer_array;
15 BEGIN
16     internal(0) <= 0;
17     -----Part A-----
18     Hammweightcalc: for i in 1 to len_in GENERATE
19         internal (i) <= internal(i-1) + 1 when input(i-1) = '1' else internal(i-1);
20     END GENERATE;
21     hamming_weight <= internal(len_in);
22     -----Part B-----
23
24     sorting: for j in 0 to len_in-1 GENERATE
25         oneCounter((len_in-1)-j) <= '1' WHEN j < internal(len_in) ELSE '0';
26     END GENERATE;
27
28 END ARCHITECTURE;
```

Final Circuit:

