Scalable Transmission Line and Inductor Models for CMOS Millimeter-Wave Design

James Brinkhoff, *Member, IEEE*, Kok Siang Steve Koh, Kai Kang, and Fujiang Lin, *Senior Member, IEEE*

***Abstract*—A new equivalent-circuit model for transmission lines and inductors on silicon is proposed. The SPICE-compatible model is suitable for time-domain simulators. It is able to fit the frequency-dependent behavior of the RLGC parameters well into the millimeter-wave range. The model is extracted from electromagnetic simulations with a simple analytic procedure with no need for tuning or optimization. A method for making the model scalable with both line length and width (or inductor diameter) is proposed. Based on this new model, a scalable measurement deembedding methodology is proposed, that can greatly reduce wafer area needed for test and deembedding structures. The fully scalable model results are compared with measurements of devices fabricated in a 90 nm CMOS process.**

***Index Terms*—CMOS millimeter-wave integrated circuits, deembedding, inductors, integrated circuit modeling, monolithic microwave integrated circuits (MMICs), scalable models, transmission lines.**

I. Introduction

DEVELOPING products for the consumer market using millimeter-wave technology is now feasible, largely due to the possibility of implementing these systems with inexpensive silicon CMOS technology [1]. With gate lengths shorter than 130 nm, nMOS f_T and $f_{\max}$ can exceed 100 GHz [2]. The systems that are under development include high data-rate WPAN devices operating in the 60 GHz band, and automotive radar in the 77 GHz band [3].

Most foundries provide models that are verified up to 20 GHz. Usually no transmission line models are provided, and the inductors are too large to be used in millimeter wave circuits (values of less than 100 pH are often called for). Thus, it is currently necessary for designers to develop their own passive models, and to augment the active device models so they are accurate at millimeter-wave frequencies [1].

Inductors and transmission lines have frequency-dependent behavior caused, for example, by the conductive substrate, and by skin and proximity effects [4]. This requires the elemental RLGC model to be expanded to capture the frequency-dependence of the series and shunt components. A model widely used for inductors and transmission lines is described in [5] and [6], together with extraction methodologies. However, the model is often not able to describe the correct frequency-dependent behavior over a wide range of frequencies. Due to this, the direct extraction methodologies often do not provide a good fit between the model and electromagnetic (EM) simulations or measurements, and additional tuning or optimization is required.

Usually each model for millimeter-wave design is suitable for a fixed device—e.g., an inductor with a set diameter or a microstrip line with a set width [6]. Thus, a large number of discrete models have to be generated so that all the sizes that are likely to be needed in a design are available. Though this approach can yield models with good accuracy, it is very time consuming to generate a sufficiently large model library, and may require significant silicon area for test structures and many computationally expensive EM simulations. In addition, optimization and tuning of circuits is difficult because only discrete device sizes are available.

Another issue for millimeter-wave device modeling is measurement deembedding. The pads and interconnects connecting to the devices on wafer must be deembedded so the electrical performance at the device terminals can be determined [7]. Previously, a new set of deembedding structures was required for each test device dimension [8]. In addition, many deembedding methods do not take account of distributed effects, which limits the range of frequencies and interconnect lengths they are valid for. A deembedding methodology that includes distributed effects, and is scalable up to a certain interconnect length was presented in [9]. It is desirable to have a method that is scalable with interconnect line length *and* width, so that measurements of many varieties of devices can be easily deembedded

The first aim of this study was to develop a more accurate and flexible series and shunt model, applicable to transmission lines and inductors, and facilitating a simple extraction methodology. The model, described in Section II was required to fit the component behavior well after an analytic direct extraction procedure without requiring tuning or optimization. The second aim was to develop a robust and simple method to make the new model scalable, which is explained in Section III. A third aim was to develop a scalable measurement deembedding methodology, making use of the new model. This is described in Section IV, along with numerous verifications of the model with measurements and EM simulations. Conclusions are drawn in Section V

II. Elemental Model

A similar model structure can be used for microstrip lines, coplanar waveguides (CPWs) and inductors. The model consists of a series branch to account for the inductance and series resistance loss. A shunt branch accounts for the capacitance to ground, and substrate and dielectric losses. Elements that are

Manuscript received June 09, 2008; revised September 24, 2008. First published November 18, 2008; current version published December 05, 2008.

The authors are with the Institute of Microelectronics, Agency for Science, Technology and Research (A*STAR), Singapore, 117685 (e-mail: james_b@ieee.org; KOHK0021@ntu.edu.sg; kangk@ime.a-star.edu.sg; linfj@ime.a-star.edu.sg).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TMTT.2008.2007337

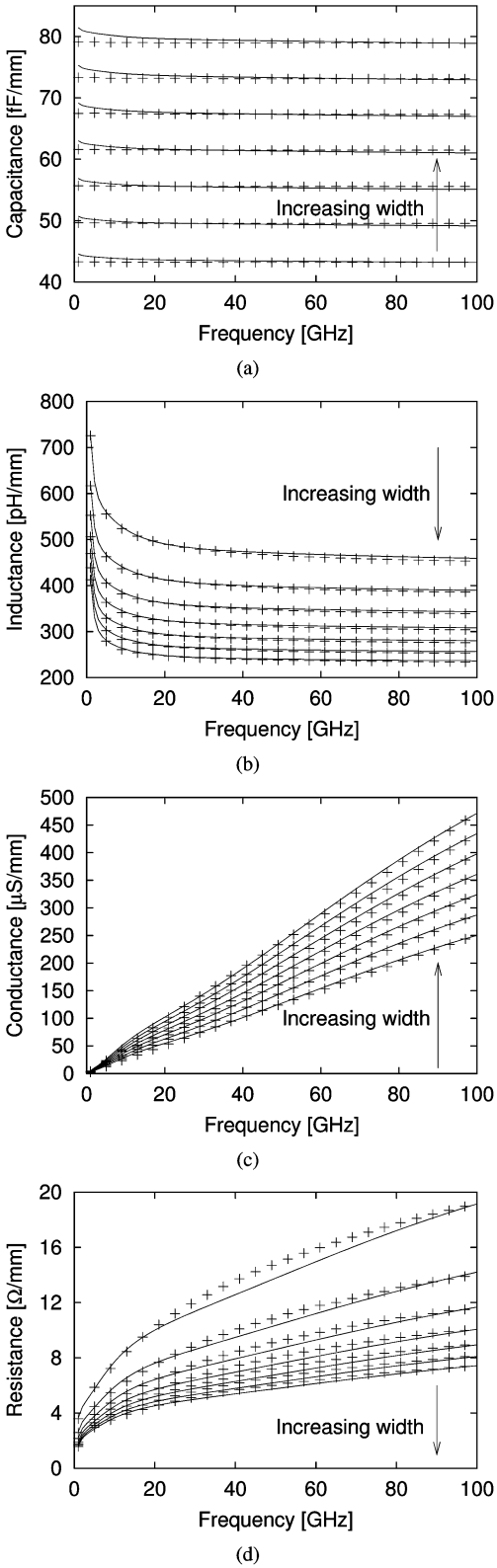

Fig. 1. RLGC per millimeter of microstrip lines with widths from 3 to 15 μm. The points are from EM simulations, the lines are from the new model.

shielded from the semiconducting silicon, such as microstrip lines, have small shunt conductance. CPWs and inductors over silicon have larger shunt conductance, but may have higher inductive quality factors [1].

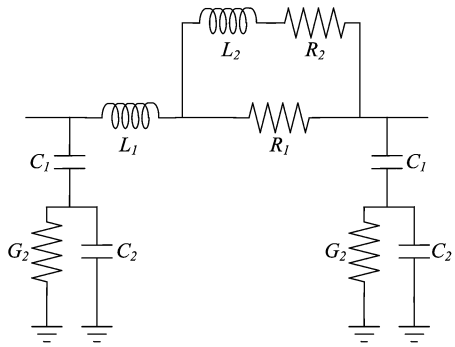

Fig. 2. Previous transmission line and inductor model.

For the purposes of introducing the new model, the focus will be on microstrip lines. The use of the model with other device types will be developed in Section IV. The microstrip structure consists of a ground plane on the bottom metal and a signal line on the top metal. An EM simulation of 212 μm long microstrip lines, with widths swept from 3 to 15 μm (giving characteristic impedances from 40 to 70 Ω) was performed. The frequency range was 1–100 GHz. The dielectric and metal specifications corresponded to a nine-metal 90 nm CMOS process. The Telegrapher's equation RLGC parameters for the transmission lines were extracted using the method in [10]. The RLGC parameters are shown in Fig. 1. Both EM simulations and the results from the new model are shown.

All of the parameters in Fig. 1 are frequency-dependent. In the microstrip case, the shunt loss is small, so the capacitance does not vary significantly with frequency. A small variation may be attributed to dielectric losses. The aim of this section is to describe a model that is able to fit the frequency dependence of the parameters in Fig. 1.

Causality is a key requirement for models to be used in time-domain simulations. Causality is ensured in the models presented in this paper by their implementation as passive equivalent circuits with all negative real poles [11]. The equivalent circuit is designed to be flexible enough to fit the frequency-dependent behavior of a variety of passive 2-port devices. All frequency-domain impedance and admittance formulae are derived directly from the equivalent circuits and are used only to understand the behavior of the model and to develop an analytic extraction procedure. The model is not implemented in the frequency domain, but rather as a SPICE-compatible netlist.

A. Series Model

As seen in Fig. 1, the series model must be more complex than a simple combination of a constant inductance and resistance, in order to fit the frequency dependent behavior. The inductance drops and the resistance rises as the frequency increases. These phenomena have been attributed to the skin and proximity effects [4].

A model that attempts to capture this behavior has been presented in a number of papers, for example, [5] for interconnects and [6] for inductors. The model is shown in Fig. 2. The frequency-dependent resistance and inductance derived from the equivalent circuit are

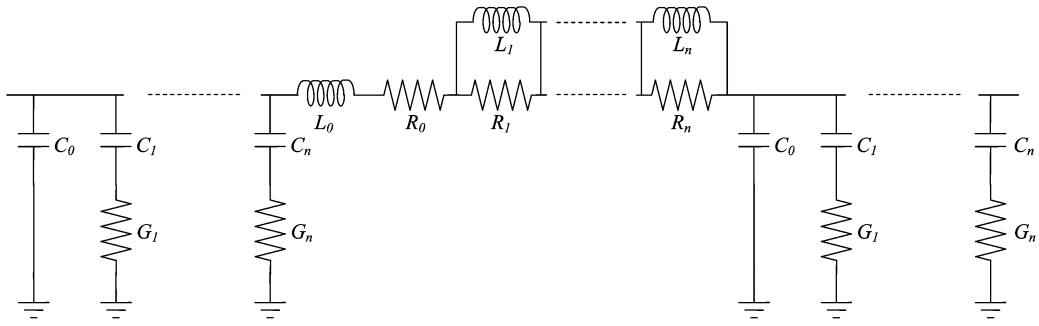

Fig. 3. New transmission line and inductor model.

$$R(\omega) = \frac{R_1 R_2}{R_1 + R_2} \frac{1 + \left(\frac{\omega}{\omega_1}\right)^2}{1 + \left(\frac{\omega}{\omega_2}\right)^2} \tag{1}$$

$$L(\omega) = L_1 + \left(\frac{R_1}{R_1 + R_2}\right)^2 \frac{L_2}{1 + \left(\frac{\omega}{\omega_2}\right)^2} \tag{2}$$

where $\omega_2 = (R_1 + R_2)/L_2$ and $\omega_1 = \omega_2\sqrt{(R_2/(R_1 + R_2))}$.

From (1), the resistance behavior is as follows:

- constant for $\omega \ll \omega_1$;
- rises for $\omega_1 < \omega < \omega_2$;
- becomes constant for $\omega \gg \omega_2$.

These characteristics do not describe the true behavior in Fig. 1. Instead, the resistance (and conductance) rise monotonically with frequency, with no observable constant regions even well into the millimeter-wave regime. This was also observed in [12]. These factors make the extraction of this model difficult. The frequency-asymptotic extraction method [5] relies on the RLGC parameters settling to constant values at low and high frequencies. Because this is not the true behavior of the transmission lines, manual optimization or tuning is required to improve the fit after analytic extraction.

To solve these issues, we propose a new empirical model this is able to fit the RLGC parameters well, shown in Fig. 3. This model is not physical. The reasons an empirical model are proposed are threefold.

- No physical model exists that can describe all of the frequency-dependent behavior that is seen in the wide range of inductor and transmission line components currently in use in silicon monolithic microwave integrated circuits (MMICs) because of the multitude of complex interactions that exist from dc to millimeter-wave frequencies.
- Optimization of the parameters of physical models is usually needed to ensure sufficient accuracy. However, if an empirical model with simple analytic parameter extraction is the starting point, optimization may not be needed.
- A physical model is valid only for a small range of physical structures. An empirical model has the possibility of being useful for a wide range of devices.

The equivalent circuit configuration in Fig. 3 was chosen because it is simple to analyze, parameter extraction can be done analytically leading to a close fit to data without requiring optimization, and it is easily extendable to fit a wide frequency range. In addition, it satisfies the important requirements of causality and stability for time-domain simulations [12].

The series model, shown in Fig. 3, consists of the dc resistance R_0 and high frequency inductance L_0. A number of cascaded sections of parallel R–L networks are added to this, each with a different corner frequency. The ith one consists of R_i and L_i, with corner frequency $\omega_i = (R_i/L_i)$. The model can easily be extended to fit the monotonically rising resistance (Fig. 1) over any frequency range, simply by adding more sections. In this study, three sections are used, which can adequately fit the behavior of microstrip lines past 100 GHz. For a model with n cascaded parallel sections, the frequency dependent resistance and inductance can be derived from the equivalent circuit model of Fig. 3 as

$$R(\omega) = R_0 + \sum_{i=1}^{n} R_i \frac{\left(\frac{\omega}{\omega_i}\right)^2}{1 + \left(\frac{\omega}{\omega_i}\right)^2} \tag{3}$$

$$L(\omega) = L_0 + \sum_{i=1}^{n} L_i \frac{1}{1 + \left(\frac{\omega}{\omega_i}\right)^2}. \tag{4}$$

As explained in [12], this model is a modified Debye approximation of the function $Z_s(\omega) = R(\omega) + j\omega L(\omega)$. Provided all the R_i and L_i are positive, Z_s has all real negative poles. It satisfies the Kramers–Kronig dispersion relation, and is thus causal [11], [12], crucial for time-domain simulations.

If the model has three corner frequencies ($n = 3$), the five unknowns are R_0, R_1, R_2, R_3 and L_0. The other inductance values depend on the corresponding resistances as follows:

$$L_i = \frac{R_i}{\omega_i}. \tag{5}$$

Five equations can be created by solving (3) and (4) at ω_1, ω_2 and ω_3. If we choose the corner frequencies such that

$$\frac{\omega_2}{\omega_1}, \frac{\omega_3}{\omega_2} \geq 10 \tag{6}$$

and assume that all the R_i are of a similar order of magnitude (which can be verified after extraction), the equations can be simplified into the following form:

$$R(\omega_1) = R_0 + \frac{1}{2}R_1 \tag{7}$$

$$R(\omega_2) = R_0 + R_1 + \frac{1}{2}R_2 \tag{8}$$

$$R(\omega_3) = R_0 + R_1 + R_2 + \frac{1}{2}R_3 \tag{9}$$

$$L(\omega_1) = L_0 + \frac{1}{2}\frac{R_1}{\omega_1} + \frac{R_2}{\omega_2} + \frac{R_3}{\omega_3} \tag{10}$$

$$L(\omega_2) = L_0 + \frac{1}{2}\frac{R_2}{\omega_2} + \frac{R_3}{\omega_3}. \tag{11}$$

It is possible to extract the coefficients from a different set of equations to those in (7)–(11). However, we note that the inductance becomes quite flat at high frequencies, as seen in Fig. 1. Therefore $L(\omega_3)$ was not used, because there is little difference between $L(\omega_2)$ and $L(\omega_3)$.

One way of solving for R_1 using (7)–(11) is as follows:

$$R_1 = 2\frac{(L(\omega_1) - L(\omega_2))\omega_2 - (R(\omega_2) - R(\omega_1))}{\frac{\omega_2}{\omega_1} - 1}. \tag{12}$$

All the other parameters can be solved using (7)–(11) and (5). For this study, the EM simulations ran from 1 to 100 GHz. In this case, the corner frequencies were chosen to be $\omega_1 = 2\pi 10^9$ rad/s, $\omega_2 = 2\pi 10^{10}$ rad/s, and $\omega_3 = 2\pi 10^{11}$ rad/s. In some cases, the corner frequencies may be adjusted to better fit the model to the device in frequency regions where the characteristics are changing rapidly.

Fig. 1(a) and (b) shows the results of using this extraction method to fit the R and L behavior of EM simulations of microstrip lines with a range of widths. No tuning or optimization was performed, and the model can fit the simulated behavior well.

B. Shunt Model

The commonly used shunt model is shown in Fig. 2. This model has a physical basis. For devices with no substrate shielding, C_1 corresponds to the oxide capacitance, C_2 and G_2 to the silicon substrate capacitance and conductance. G_2 and C_2 can also be used to model the oxide dielectric losses of microstrip lines. The frequency-dependent conductance and capacitance derived from one side of the equivalent circuit model in Fig. 2 are

$$G(\omega) = \frac{\frac{\omega^2 C_1^2}{G_2}}{1 + \left(\frac{\omega}{\omega_1}\right)^2} \tag{13}$$

$$C(\omega) = C_1\frac{1 + \left(\frac{\omega}{\omega_2}\right)^2}{1 + \left(\frac{\omega}{\omega_1}\right)^2} \tag{14}$$

where $\omega_1 = G_2/(C_1 + C_2)$ and $\omega_2 = \omega_1\sqrt{((C_1 + C_2)/C2)}$. Though the model is physically based, it is not complex enough to fit the frequency-dependent admittance of the variety of transmission lines or inductors used in millimeter-wave design, over a sufficiently wide range of frequencies. It could be made more accurate by adding additional G–C sections, but the analysis and corresponding parameter extraction becomes increasingly complex.

A new shunt model, which is analogous to the series model, is shown in Fig. 3. This model is not based on the physical structure of the device. Being empirical, it enables simplified analysis and effective extraction to fit the measured or simulated characteristics. Additional G–C sections can be added without complicating the analysis and extraction, to model more complex devices, or to fit the data over a larger frequency range.

The frequency-dependent conductance and capacitance derived from one side of Fig. 3 are

$$G(\omega) = \sum_{i=1}^{n} G_i\frac{\left(\frac{\omega}{\omega_i}\right)^2}{1 + \left(\frac{\omega}{\omega_i}\right)^2} \tag{15}$$

$$C(\omega) = C_0 + \sum_{i=1}^{n} C_i\frac{1}{1 + \left(\frac{\omega}{\omega_i}\right)^2}. \tag{16}$$

The shunt admittance $Y_s = G(\omega) + j\omega C(\omega)$ can also be shown to be a Debye fitting model [12], and causal. In the case of transmission lines, the G and C computed from EM simulations or measurements using [10] are halved to account for the fact that there are shunt networks on the input and output of Fig. 3 to make it symmetrical. For inductors, the input and output shunt networks must be solved independently, to account for the device asymmetry.

One way of extracting the coefficients, using (15) and (16) is

$$G_1 = 2G(\omega_1) \tag{17}$$

$$G_2 = 2(G(\omega_2) - G_1) \tag{18}$$

$$G_3 = 2(G(\omega_3) - G_2 - G_1) \tag{19}$$

$$C_0 = C(\omega_3) - \frac{C_3}{2} \tag{20}$$

where the other C coefficients can be calculated with

$$C_i = \frac{G_i}{\omega_i}. \tag{21}$$

Fig. 1(c)–(d) shows the results of using this extraction method to fit the G and C behavior of EM simulations of microstrip lines with a range of widths. The same corner frequencies used for the series model, described in Section II-A, were used for the shunt model. No tuning or optimization was performed, and the model can fit the EM simulations well.

III. Scalability

For transmission lines, the model can be easily scaled in length simply by multiplying each component in the equivalent circuit by length (as all the components are per unit length). A number of the pi sections in Fig. 3 must be cascaded to account

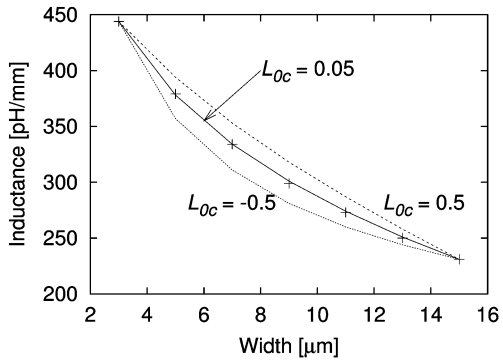

Fig. 4. Example of fitting an equation to the width dependence of the high frequency inductance L_0. Three values of the curvature parameter L_{0c} are shown. The lines are given by (22), and the points are from the EM simulations.

for distributed effects [5]. For frequencies up to 100 GHz, one pi section for every 50 μm is sufficient. For inductors, usually one or two sections is sufficient. A capacitor between the input and output ports of the model may be added describe inductor self-resonance effects [6].

Thus, it is simple to implement scalability with transmission line length. It is more complex to include scaling with microstrip width, CPW width or signal-to-ground spacing, or inductor diameter. The discussion below will use microstrip width as the scaling parameter, but the theory can equally apply to the other situations mentioned, and the model is able to fit these other structures as well.

Many of the elements of the model are nonlinear functions of width. After extracting R_i, L_i, G_i, and C_i (Fig. 3) as a function of width, using (5)–(12) and (17)–(21), scalability with width can be implemented by fitting a curve to each of these functions. For example, L_0 in Fig. 3 can be described by

$$L_0(w) = \left(L_{0a} + L_{0b} \times w^{L_{0c}}\right) \tag{22}$$

where w is the width in μm. An initial value for the curvature parameter L_{0c} is chosen. Then the other two parameters are found using the following equations:

$$L_{0a} = \frac{L_0(w_1)w_2^{L_{0c}} - L_0(w_2)w_1^{L_{0c}}}{w_2^{L_{0c}} - w_1^{L_{0c}}} \tag{23}$$

$$L_{0b} = \frac{L_0(w_2) - L_0(w_1)}{w_2^{L_{0c}} - w_1^{L_{0c}}}. \tag{24}$$

The smallest and largest widths can be used for w_1 and w_2. The modeled curve for L_0 (22) is then compared to the one extracted from the EM simulations, and the value of L_{0c} is adjusted so the curvature is correct. An example of this process is shown in Fig. 4, where $L_{0c} = 0.05$ was chosen. The coefficients for all the remaining components in Fig. 3 are found using the same curve fitting formula (22).

The complete scalable model was extracted from the EM simulations of the microstrip lines with a length of 212 μm and widths from 3 to 15 μm, corresponding to lines fabricated in a 90 nm CMOS process. The RLGC parameters of the lines as a function of frequency and width were extracted using the equations in [10]. Then, the shunt and series elements of the

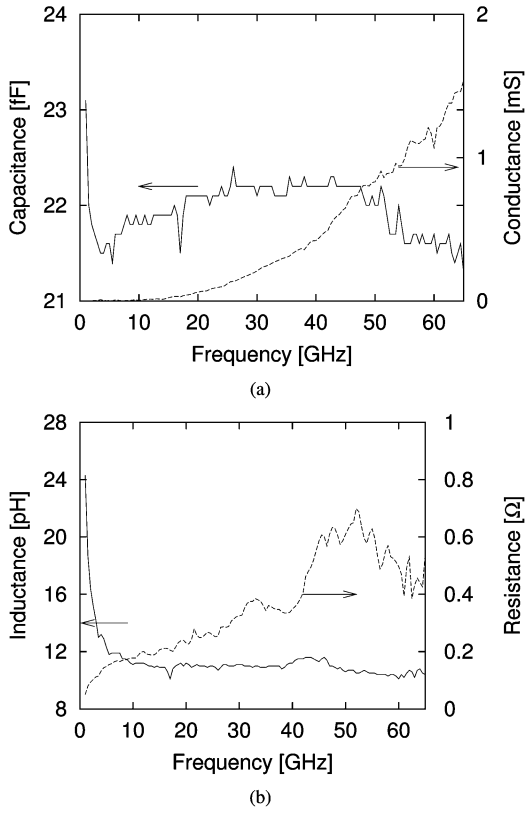

Fig. 5. Measured pad characteristics, used for deembedding the measurements.

TABLE I
SCALABLE MICROSTRIP MODEL PARAMETERS. $X = X_a + X_b w^{X_c}$

Component X	X_a	X_b	X_c
L_0	2.37×10^{-12}	-1.87×10^{-12}	0.05
L_1	1.92×10^{-13}	1.78×10^{-13}	−0.3
L_2	-7.99×10^{-15}	1.77×10^{-13}	−0.5
L_3	-7.07×10^{-15}	6.00×10^{-14}	−0.5
C_0	3.81×10^{-17}	2.95×10^{-18}	1
C_1	5.90×10^{-19}	5.28×10^{-20}	1
C_2	5.38×10^{-19}	5.90×10^{-20}	1
C_3	5.05×10^{-19}	4.79×10^{-20}	1
R_0	2.61×10^{-4}	6.95×10^{-3}	−1

equivalent circuit in Fig. 3 were computed using the equations in Sections II-A and B, as a function of width. Each of these components then had an equation such as (22) fit to them. Note that all the components are normalized to per μm.

The model was implemented in ADS and Cadence, with the length and width parameters available to the user. 16 pi sections were cascaded, making the model accurate for lines up to at least 800 μm long, up to 100 GHz. Fig. 1 shows the modeled RLGC versus frequency, comparing it with the EM simulated results, for a range of line widths. It can be seen that a single scalable model is able to fit the series impedance and shunt admittance very well.

IV. VERIFICATION

To verify the model, measurements and EM simulations of various structures in a nine metal 90 nm CMOS process were

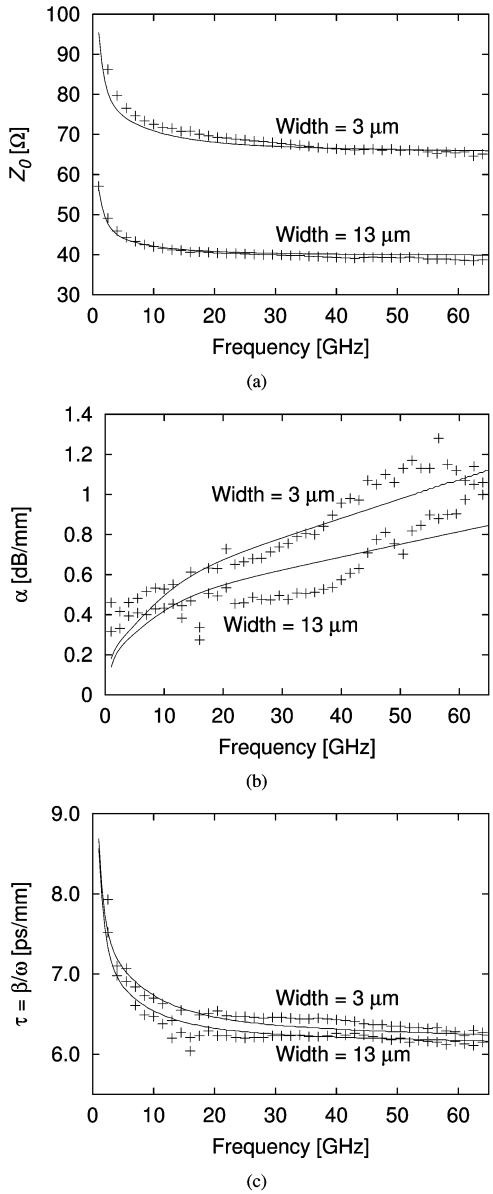

Fig. 6. Characteristic impedance, attenuation constant, and group delay for 424 μm long microstrip lines, with widths of 3 and 13 μm. The lines are the scalable model results, and the points are from the deembedded measurements.

performed. In all of the measurements, the vector network analyzer was calibrated to the probe tips using the LRRM method from Cascade Microtech, with a ceramic impedance standard substrate. Subsequent to the probe tip calibration, the pads used to test the passives fabricated on the CMOS chip had to be deembedded, using the L-2L [7] method. In addition, the microstrip lines connected between the pads and inductors were deembedded using a new method described in Section IV-B.

A. Microstrip Lines

Microstrip lines with widths of 3, 5, 9, and 13 μm, and lengths of 212 and 424 μm were fabricated in a 90 nm CMOS process. The lines included aluminium probe pads of size 72×48 μm^2, for 100 μm pitch probes. In order to characterize the line performance, the pads must first be deembedded from the measurements. The L-2L method [7] was used, as it enables the extraction of both the shunt and series components of the pad parasitics. The series components are dependent on the probe position. Therefore, care was taken to ensure the probes reached the same position on the pads for each contact. The series and shunt parasitics are shown in Fig. 5, extracted from the 212 and 424 μm long, 9 μm wide, lines. The parasitics were very similar for the lines of other widths, suggesting that the transition between the probe pad and microstrip line was not significant in determining the parasitics. Once the pad parasitics are determined, their effects can be deembedded from the measurements [7].

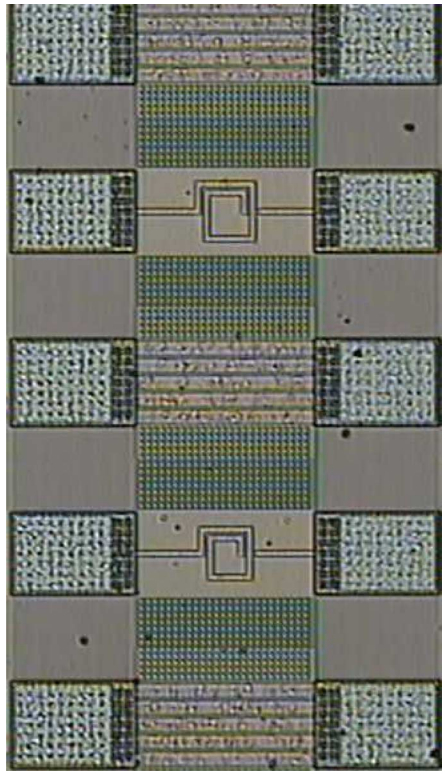

Fig. 7. Two fabricated inductors with diameters of 31 and 35 μm. The test structures are the same size, so can share ground pads. The pads are deembedded using [7], and the microstrip lines of varying lengths are deembedded using the new scalable model.

The EM simulations predicted higher inductance and lower capacitance than measurements by up to 15%. This could be explained by a mismatch between the physical dielectric parameters, and the ones entered in the EM simulator. The model that was extracted from EM simulations was tuned to fit the measurements. Only L_{0a}, L_{0b} and C_{0a} needed to be adjusted. The final model parameters (note that they are per μm) are given in Table I. The equations are entered into the equivalent circuit model file, corresponding to Fig. 3. For example,

$$L_0 = 2.37 \times 10^{-12} - 1.87 \times 10^{-12} \times w^{0.05} \qquad (25)$$

where w is the width of the microstrip line in μm. The remaining R and G values can be obtained using (5) and (21), with $\omega_1 = 2\pi 10^9$ rad/s, $\omega_2 = 2\pi 10^{10}$ rad/s and $\omega_3 = 2\pi 10^{11}$ rad/s.

The reader may be concerned to find negative values in Table I and (25) because a negative inductance, capacitance, or resistance in Fig. 3 may result in nonphysical behavior. However, the values in Table I are not the component values themselves, but

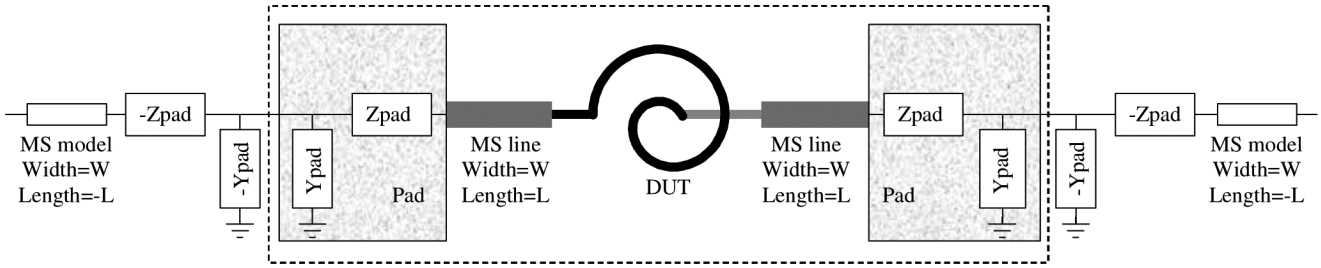

Fig. 8. Illustration of the deembedding procedure, which is scalable with the microstrip line interconnects length and width. The dashed box indicates the reference plane of the VNA measurements. First the pads are removed, then the microstrip lines, to obtain the characteristics of the device under test.

are parameters to describe the variation of the component values with device dimensions (microstrip line width in this case). For example, if the inductance L_0 decreases with microstrip width, as seen in Fig. 4, L_{0b} will be less than zero to describe the negative slope, because $L_0 = L_{0a} + L_{0b}w^{L_{0c}}$. Computing the component values from Table I over the range of microstrip line widths that they were extracted from, confirms that all the component values are indeed positive. Of course, care must be taken when trying to extrapolate the model beyond the range of device dimensions from which it was extracted.

The measured and simulated transmission line parameters for two 424 μm long lines are shown in Fig. 6. One of the lines is 3 μm wide, and the other one is 13 μm wide. The scalable model can predict the characteristic impedance (Z_0), attenuation constant (α) and group delay $(\tau = \beta/\omega)$ well, for lines with a large range of characteristic impedances. The measured attenuation constant is noisy because it is small for these short lines.

B. Inductors

Two of the fabricated inductors are shown in Fig. 7. They were placed over a ground plane. This lowers the Q, and increases the shunt capacitance. However, the behavior of the inductors in a millimeter-wave circuit is a lot more predictable because there is a well defined current return path, the component is isolated from the lossy substrate, and the influence of adjacent elements through capacitive or substrate coupling is not as significant. As a result, simulated and measured performance can be very close. A 60 GHz oscillator and modulator has been fabricated using these inductors and the measured carrier frequency agrees closely with that predicted by time-domain simulations.

Inductors with 1.5 turns and diameters from 19 to 43 μm were fabricated. These produced inductances from 25 to 100 pH, a useful range for, for example, 60 GHz circuits. These inductors were small enough that their self-resonant frequencies were above 100 GHz. If a larger inductor is needed that does exhibit self-resonance within the band of interest, simulations have shown that adding a capacitor between the input and output ports of the model can capture the behavior accurately, as explained in [6].

One section of the model in Fig. 3 was used to model the inductors. The input and output capacitances were not identical because the inductors were not symmetrical. Therefore, these capacitances can be extracted independently. The inductor model, scalable with diameter, was extracted from EM simulations using a similar procedure to that used for the microstrip lines.

The inductor measurements needed to be deembedded. The fabricated inductors were embedded between pads and 3 μm wide microstrip lines (see Fig. 7). The deembedding procedure was done in two steps, as illustrated in Fig. 8.

Step 1) The pad characteristics were determined (giving $Y_{\rm pad}$ and $Z_{\rm pad}$ shown in Fig. 5) and removed using the L-2L method of [7].

Step 2) The microstrip lines were removed by cascading the resulting T-parameters from step one with the scalable microstrip model with the width set at 3 μm and the length set to the negative of the interconnect length (Fig. 8).

This scalable deembedding method allows the wafer area to be greatly minimized. Each test structure does not require a separate set of deembedding structures, because only the microstrip line length changes, which is handled by the scalable model [9]. In addition, the test structure size can be standardized, and thus adjacent structures can share ground pads as shown in Fig. 7, because the microstrip length can be varied to suit each device size. In addition, and in contrast to lumped deembedding methods like open-short [8], this deembedding method also allows for distributed effects of electrically long interconnects at high frequencies to be accounted for, because it utilizes the distributed scalable model.

The measured and simulated inductance and input/output capacitance of the inductors are shown in Fig. 9. The resistance and conductance could not be measured accurately because they were very small. However, the model fit the EM simulated resistance and conductance very closely. After extraction from EM simulations, the model was tuned slightly to match the measurements, as explained in Section IV-A. The output capacitance is higher than the input capacitance because the underpass is on the output port of the inductors. A single scalable model is able to predict the inductor characteristics with varying diameters, as seen in Fig. 9.

C. CPWs

CPW structures do not have a ground plane and are thus exposed to the semiconducting substrate. The substrate effect will cause the shunt conductive loss to increase, depending on the signal-to-ground spacing [1].

No CPW structures were available on the test wafer. However, it was desirable to test the new model with an unshielded structure. Therefore, EM simulations of CPW lines were performed. Previous work has shown that EM simulations are able to predict the measured performance of transmission lines over

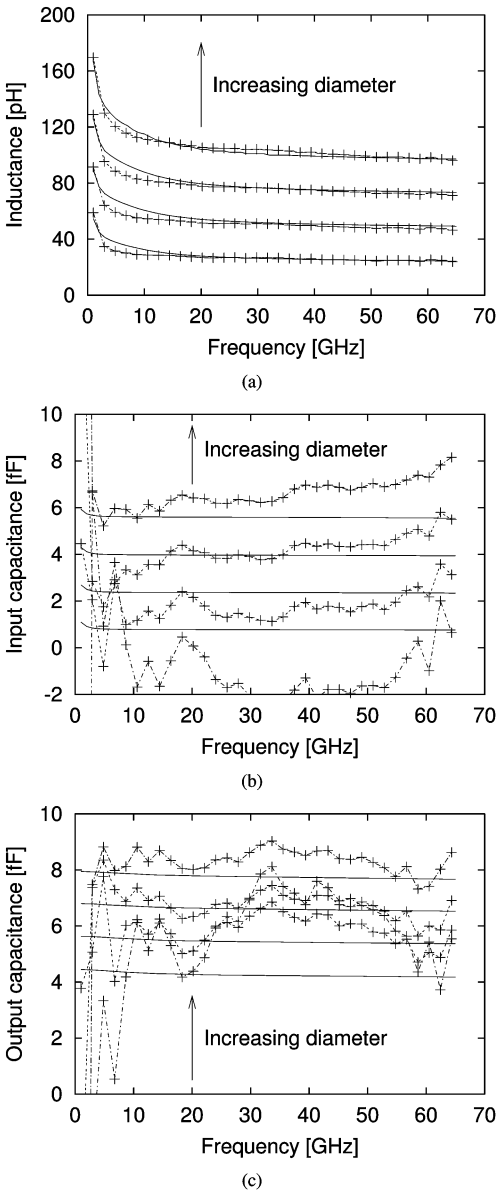

Fig. 9. Measured and modeled inductance and shunt input and output capacitance of the 1.5 turn lumped inductors, with diameters of 19, 27, 35, and 43 μm.

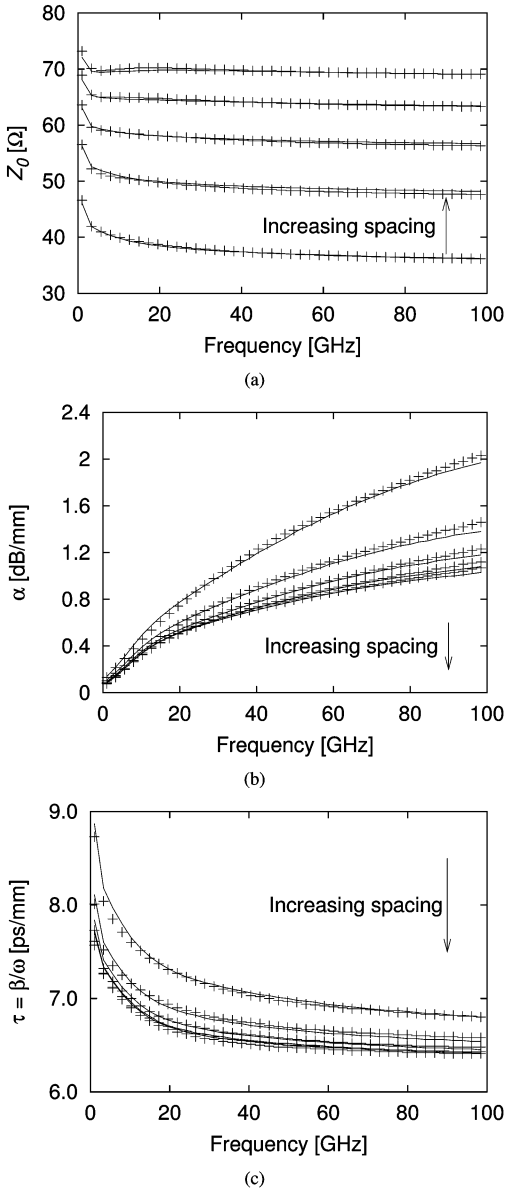

Fig. 10. EM simulated (points) and modeled (lines) transmission line parameters for a 212 μm long CPW line. The line is 8 μm wide, and the signal-to-ground spacing is varied from 2 to 10 μm in steps of 2 μm.

silicon up to 110 GHz [13]. This gives confidence in the validity of the simulations.

The signal line was 8 μm wide, the ground traces were on the same metal layer, and were 24 μm wide. The lines were 212 μm long, and the signal-to-ground spacing was varied from 2 to 10 μm in order to vary the characteristic impedance. The third corner frequency of the model was lowered to 65 GHz. This allowed the resistance characteristic to be extracted and fit more accurately, indicating that CPW lines may need more sections than microstrip lines in the model of Fig. 3, to account for the complex substrate interaction.

After extracting the model from EM simulations, the simulated and modeled transmission line parameters were compared. The results are shown in Fig. 10. They show that the scalable model in Fig. 3 is also useful for devices that do not have a ground plane.

V. Conclusion

A new scalable and SPICE-compatible model for millimeter-wave inductors and transmission lines for CMOS designs has been presented. The model is easily extracted, and fits the frequency-dependent RLGC parameters well. A method for implementing scalability, both with length and width (or inductor diameter), has been described. This enables millimeter-wave model library extraction and implementation to be greatly simplified. It will also enable continuous optimization of circuit performance, rather than relying on a number of discrete models for each inductor diameter or line width. The model has been used to implement a scalable deembedding methodology that reduces the amount of wafer area needed for deembedding structures. The model has been verified for microstrip lines, inductors and CPW lines by EM simulations and measurements.

ACKNOWLEDGMENT

The authors thank UMC for fabrication, K. C. Lim for layout, and Z. L. Teng for CAD support.

REFERENCES

[1] C. H. Doan, S. Emami, A. M. Niknejad, and R. W. Brodersen, "Millimeter-wave CMOS design," *IEEE J. Solid-State Circuits*, vol. 40, no. 1, pp. 144–155, Jan. 2005.

[2] S. P. Voinigescu, S. T. Nicolson, M. Khanpour, K. K. W. Tang, Y. H. K. Yau, N. Seyedfathi, A. Timonov, A. Nachman, G. Eleftheriades, P. Schvan, and M. T. Yang, "CMOS SOCs at 100 GHz: System architectures, device characterization, and IC design examples," in *IEEE ISCAS*, New Orleans, LA, May 2007, pp. 1971–1974.

[3] T. Suzuki, Y. Kawano, M. Sato, T. Hirose, and K. Joshin, "60 and 77 GHz power amplifiers in standard 90 nm CMOS," in *IEEE Int. Solid-State Circuits Conf. Tech. Dig.*, San Francisco, CA, Feb. 2008, pp. 562–563.

[4] J. Zheng, Y.-C. Hahm, V. K. Tripathi, and A. Weisshaar, "CAD-oriented equivalent-circuit modeling of on-chip interconnects on lossy silicon substrate," *IEEE Trans. Microw. Theory Tech.*, vol. 48, no. 9, pp. 1443–1451, Sep. 2000.

[5] S. Sun, R. Kumar, S. C. Rustagi, K. Mouthaan, and T. K. S. Wong, "Wideband lumped element model for on-chip interconnects on lossy silicon substrate," in *IEEE RFIC Symp. Dig.*, Jun. 2006, 4 pp.

[6] T. O. Dickson, M.-A. LaCroix, S. Boret, D. Gloria, R. Beerkens, and S. P. Voinigescu, "30–100-GHz inductors and transformers for millimeter-wave (Bi)CMOS integrated circuits," *IEEE Trans. Microw. Theory Tech.*, vol. 53, no. 1, pp. 123–133, Jan. 2005.

[7] J. Song, F. Ling, G. Flynn, W. Blood, and E. Demircan, "A de-embedding technique for interconnects," in *Elect. Perform. Electron. Packag.*, Cambridge, MA, Oct. 2001, pp. 129–132.

[8] A. Issaoun, Y. Z. Xiong, J. Shi, J. Brinkhoff, and F. Lin, "On the deembedding issue of CMOS multigigahertz measurements," *IEEE Trans. Microw. Theory Tech.*, vol. 55, no. 9, pp. 1813–1823, Sep. 2007.

[9] K. H. K. Yau, A. M. Mangan, P. Chevalier, P. Schvan, and S. P. Voinigescu, "A transmission-line based technique for de-embedding noise parameters," in *IEEE Int. Microelectron. Test Structures Conf.*, Tokyo, Japan, Mar. 2007, pp. 237–242.

[10] W. R. Eisenstadt and Y. Eo, "*S*-parameter-based IC interconnect transmission line characterization," *IEEE Trans. Comp., Hybrids, Manuf. Technol.*, vol. 15, no. 4, pp. 483–490, Aug.Aug. 1992.

[11] P. Triverio, S. Grivet-Talocia, M. S. Nakhla, F. G. Canavero, and R. Achar, "Stability, causality and passivity in electrical interconnect models," *IEEE Trans. Adv. Packag.*, vol. 30, no. 4, pp. 795–808, Nov. 2007.

[12] M. S. Sarto, A. Scarlatti, and C. L. Holloway, "On the use of fitting models for the time-domain analysis of problems with frequency-dependent parameters," in *IEEE Int. Electromagn. Compat. Symp.*, Montreal, QC, Canada, Aug. 2001, pp. 588–593.

[13] K. Kang, L. Nan, S. C. Rustagi, K. Mouthaann, J. Shi, R. Kumar, W.-Y. Yin, and L.-W. Li, "A wideband scalable and SPICE-compatible model for on-chip interconnects up to 110 GHz," *IEEE Trans. Microw. Theory Tech.*, vol. 56, no. 4, pp. 942–951, Apr. 2008.

James Brinkhoff (S'02–M'05) received the B.E. degree from the University of Tasmania, Tasmania, Australia, in 2001, and the Ph.D. degree from Macquarie University, Sydney, N.S.W., Australia, in 2005.

From 2005 to 2006, he was a Research Fellow involved with modeling the nonlinear behavior of GaAs HEMTs in microwave circuits. In 2006, he joined the Institute of Microelectronics, Singapore, where he is involved in modeling and design for millimeter-wave systems in CMOS. His research interests include nonlinear device characterization and analysis, modeling active and passive devices, and millimeter-wave circuit design.

Kok Siang Steve Koh was born in 1982. He is currently working toward the B.E. degree at Nanyang Technological University, Singapore.

He completed his intership attachment at the Institute of Microelectronics, Singapore, where he investigated scalable transmission line and inductor models for millimeter-wave design in CMOS.

Kai Kang was born in 1979. He received the B.Eng. degree in electrical engineering from Northwestern Polytechnical University, Shaanxi, China, in 2002, and the joint Ph.D. degree from the National University of Singapore, Singapore, and Ecole Supérieure D'électricité, Gif-sur-Yvette, France, in 2008.

From 2003 to 2006, he was a Research Scholar with the National University of Singapore. From 2005 to 2006, he was with the Laboratoire de Génie Electrique de Paris, Paris, France. Since October 2006, he has been a Senior Research Engineer with the Institute of Microelectronics, Singapore. His research interest is the modeling of on-chip passive devices and millimeter-wave circuits design in CMOS technology.

Fujiang Lin (M'93–SM'99) received the B.S. and M.S. degrees from the University of Science and Technology of China (USTC), Hefei, China, in 1982 and 1984, respectively, and the Dr.-Ing. degree from Universität Kassel, Kassel, Germany, in 1993, all in electrical engineering.

In 1995, he joined the Institute of Microelectronics (IME), Singapore, as a Member of Technical Staff, where he pioneered practical RF modeling for RF integrated circuit (IC) development. In 1999, he joined HP EEsof, as the Technical Director, where he established the Singapore Microelectronics Modeling Center, providing accurate state-of-the-art device and package characterization and modeling solution service worldwide. From 2001 to 2002, he started up and headed Transilica Singapore Pte. Ltd., a research and development design center of Transilica Inc., a Bluetooth and IEEE 802.11 a/b wireless system-on-chip (SoC) company. The company was acquired by Microtune Inc. After the closing of Transilica Singapore in 2002, he joined Chartered Semiconductor Manufacturing Ltd. (third largest foundry), as Director, where he led the SPICE modeling team in support of company business. In 2003, he rejoined IME as a Senior Member of Technical Staff, where he is currently focused on upstream research and development initiatives and leadership toward next waves. His current research interest is in the development of CMOS as a cost-effective technology platform for 60-GHz band millimeter-wave SoC. As an Adjunct Associate Professor with the National University of Singapore, Singapore, he is actively involved in educating and training postgraduate students. He has authored or coauthored over 70 scientific papers. He holds two patents.

Dr. Lin has served IEEE activities in different functions since 1995 including chair of the Singapore Microwave Theory and Techniques (MTT)/Antennas and Propagation (AP) Chapter, reviewer board member for the IEEE Microwave Theory and Techniques Society (IEEE MTT-S), and Technical Program Committee (TPC) member of ESSCRIC. He is initiator and co-organizer of international workshops and short courses at APMC'99, SPIE'00, ISAP'06, and IMS'07. Recently, he and his team initiated and organized the conference-style IEEE International Workshop on Radio-Frequency Integration Technology (RFIT), Singapore. He was the recipient of the 1998 Innovator Award presented by the *EDN Asia Magazine*.