S-Parameter-Based IC Interconnect Transmission Line Characterization

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Abstract— **A methodology for extracting high frequency IC interconnect transmission parameters directly from S-parameter measurements has been demonstrated using on-chip test structures. The methodology consists of: 1) building on-chip interconnect structures for microwave test, 2) characterizing and subtracting measurement system parasitics, 3) extracting the transmission line impedance and propagation constant (attenuation constant and phase constant) from the calibrated data, and 4) extracting the Telegrapher's Equation transmission parameters (R, L, C, and G). Additional on-chip calibration permits subtraction of pad parasitic effects.**

This methodology is demonstrated over a 45-MHz to 20-GHz frequency range using an example 1 cm long, 4-μm wide IC interconnect built in an advanced BiCMOS technology. Variation in interconnect impedance and capacitance indicate two signal propagation modes. Significant substrate-based loss is measured at microwave frequencies.

I. Introduction

HIGH-speed VLSI exhibits subnanosecond switching and requires clock signal propagation bandwidths above 1 GHz in order to maintain rise times. VLSI layout and simulation software must have accurate and verified interconnect models to calculate timing of critical paths and anticipate race condition for these bandwidths. Currently, many of these simulation models are built from dc capacitance and resistance measurements [1]–[3]. The values of the resistance and capacitance is assumed constant with frequency which is fundamentally incorrect [4]. This traditional approach will be too inaccurate for the next generation of IC's which have submicrometer interconnect widths and submicrometer spacing between interconnects.

In its simplest configuration, interconnect is a single microstrip line on a silicon IC. IC interconnect modeling can be divided into first level interconnect with lossy silicon substrate effects and upper level interconnect which is masked from substrate effects. Early work in first level IC interconnect modeling at microwave frequencies examined microstrip on SiO_2–Si substrates [5] and three possible modes of signal propagation were described. Interconnect on standard IC substrates exhibits a slow wave mode modeled by RC transmission line propagation at low frequencies. As frequency is increased, the microstrip exhibits a quasi-TEM mode. The previous work extracted impedance and propagation constants for wide interconnect (20–1600 μm) by measuring short circuit and open circuit impedances in customized test fixtures. Standard automated S-parameter techniques were not used for these characterizations.

This paper improves upon this earlier work by developing test structure layouts that characterize modern fine line lithography interconnect using standard on-chip microwave probing and S-parameter measurements. Moreover, this paper shows how to calculate substrate loss, substrate capacitance, conductor resistance, and conductor inductance of first level and upper level interconnect directly from S-parameter measurements. Strong frequency variations of model parameters are shown which prove that RC modeling of interconnect is fundamentally incorrect at high frequencies. In addition, basic propagation modes reported in earlier work are verified. Standard automated microwave test equipment can be used by IC designers and engineers to obtain similar results.

In the future, upper level interconnect will have high loss due to small interconnect conductor areas and will use novel interlayer dielectrics for reduced capacitance. Ultimately, it will be necessary for the IC industry to characterize these losses and novel dielectric properties directly from measurement and build a representative interconnect characterization database. From this database, accurate VLSI timing models and interconnect simulators can be developed for the next generation of IC interconnect. This paper is an important contribution in establishing this experimental database.

The paper is organized as follows. A characterization section reviews test structure design. Then transmission line parameter extraction is reported. Verification of the extraction algorithm using discretized models is presented followed by the discussion of a method to subtract the pad parasitics. Finally, the variation of interconnect impedance with frequency is reported and the paper is summarized.

II. Interconnect Characterization

Conventional small signal parameters, z-, y-, and $ABCD$-parameters, are not suitable for high frequency interconnect characterizations because open and short circuit terminations required to measure this data cannot be easily realized. "Short" circuit terminations have magnetically induced inductance and "open" circuit terminations have capacitance due to electric field fringing at high frequencies. On the other hand, S-parameters defined in terms of incident and reflected waves in a controlled 50-Ω measurement system readily characterize interconnect high frequency response [6].

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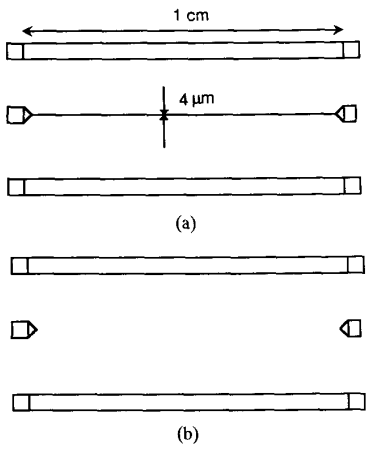

Fig. 1. IC interconnect high frequency test structure layout. (a) Test structure layout. (b) Open of the test structure.

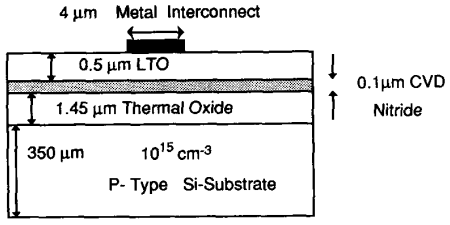

Fig. 2. IC interconnect wafer cross section.

In order to perform S-parameter measurements of IC interconnect, a test structure layout was designed as shown in Fig. 1. A 4-μm wide and 1-cm long (mask dimensions) Al line over a SiO_2 layer, a thin film nitride layer, and a Si substrate were characterized using S-parameters. The IC technology cross section of the test structures is shown on Fig. 2. An open structure for the pad calibration was developed which has the same layout as the interconnect test structure but is missing the center conductor. A Cascade Microtech Probe Station and an HP8510 Network Analyzer which operates from 45 MHz to 20 GHz measured the interconnect response. The measured data were transmitted to an HP series model 217 computer and ultimately to UNIX workstations for calibration and parameter extraction.

The S-parameter characterization of interconnect transmission is modeled in Fig. 3. Here, a piece of interconnect with characteristic impedance, Z and propagation constant, γ is placed in an S-parameter test system of impedance, $Z_0 = 50\ \Omega$. The incident power a_1 and a_2 and reflected power b_1 and b_2 are found and the resulting S-parameter matrix is determined.

Since there are many sources of bad S-parameter data such as external noise, equipment-based microwave resonances, or poor test structure design, an experimental technique that is very careful is essential. Therefore, characterization data meet the following criteria. Otherwise, the data are discarded.

1) The experimental data from different test structures with identical layout yielded nearly equal values during repeated measurements.

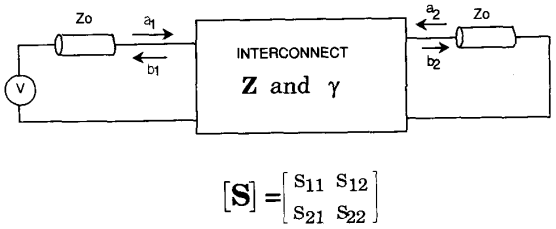

Fig. 3. S-parameter representation of interconnect transmission.

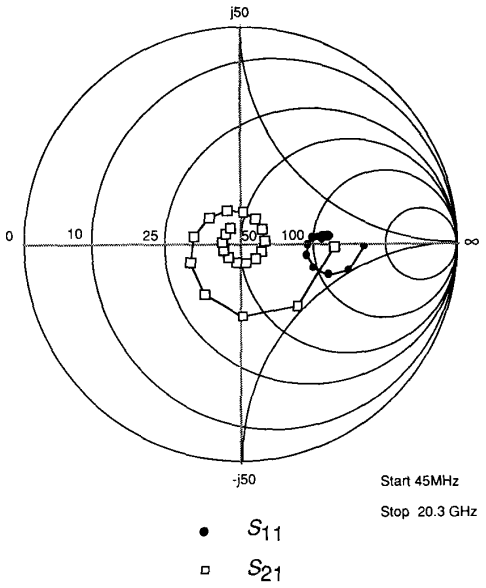

Fig. 4. Example S-parameter measurements (S_{11} and S_{21}) of 4-μm wide 1-cm long interconnect.

2) Since these IC interconnect structures were symmetrical, the S-parameters were symmetrical, $S_{ij} = S_{ji}$ and $S_{ii} = S_{jj}$.

Interconnect measurements require good equipment calibrations as well as a consistent elimination of the pad parasitic effects as discussed in Section VI. Scattering parameters characterizing the above interconnect test structure are shown in Fig. 4 (S_{11} and S_{21}). The S_{11} plot on the Smith Chart shows that the imaginary part of the interconnect characteristic impedance is changing from a capacitive reactance to an inductive reactance as the frequency increases. The S_{21} plot shows that the signal transmission becomes increasingly lossy as the frequency is increased.

III. IC Interconnect Transmission Parameter Extraction

Frequency variations of IC interconnect transmission parameters have been extracted directly from S-parameter measurement data. This information is essential for developing accurate and verified interconnect models. Once these transmission parameters are determined, the interconnect small signal frequency-domain response is known and the large time-domain response can be obtained by the inverse Fourier

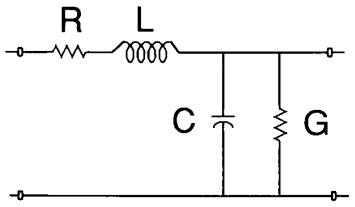

Fig. 5. Telegrapher's equation model representation of single conductor interconnect.

transform due to the linearity of the interconnect response with voltage.

Interconnect signal transmission is based on the solution of the classical Telegrapher's transmission line equation. A model has been developed that presents, in the frequency domain, the interconnect voltage and current in terms of propagation constant, γ and characteristic impedance, $\boldsymbol{Z}$. Then the impedance and propagation constant are described by four distributed transmission line parameters, $\boldsymbol{R}$, $\boldsymbol{L}$, $\boldsymbol{C}$, and $\boldsymbol{G}$. An infinitely small subsection of this model incorporating distributed circuit elements is shown in Fig. 5. These distributed circuit parameters describe per unit length values and not lumped element values that are assumed in SPICE. In this paper, IC interconnect circuit parameters, $\boldsymbol{Z}$, γ, $\boldsymbol{R}$, $\boldsymbol{L}$, $\boldsymbol{C}$, and $\boldsymbol{G}$ are shown to be functions of frequency.

To solve the Telegrapher's equation for IC interconnect-signal propagation requires an understanding of S-parameter-based interconnect test structure characterization. Single line IC interconnect transmission is represented by a two port network and is tested in a controlled ($\boldsymbol{Z}_0 = 50\ \Omega$) impedance microwave measurement system. The S-parameter responses measured from a lossy unmatched transmission line with parameters γ and $\boldsymbol{Z}$ in a $\boldsymbol{Z}_0$ impedance system are [7]

$$[S] = \frac{1}{D_s}\begin{bmatrix} \left(Z^2 - Z_0^2\right)\sinh\gamma l & 2ZZ_0 \\ 2ZZ_0 & \left(Z^2 - Z_0^2\right)\sinh\gamma l \end{bmatrix} \quad (1)$$

where

$$D_s = 2ZZ_0\cosh\gamma l + \left(Z^2 + Z_0^2\right)\sinh\gamma l.$$

Since the above matrix is symmetrical, it contains two independent linear equations. This S-parameter matrix is converted to $ABCD$ parameters [7] which incorporate the interconnect propagation constant $\gamma(\omega)$ and the impedance $\boldsymbol{Z}(\omega)$ more explicitly. The equivalent $ABCD$ matrix is

$$[\boldsymbol{ABCD}] = \begin{bmatrix} \cosh\gamma l & Z\sinh\gamma l \\ \frac{\sinh\gamma l}{Z} & \cosh\gamma l \end{bmatrix}. \quad (2)$$

The relationship between the S-parameters and the $ABCD$ matrix is [7]

$$\begin{aligned} \boldsymbol{A} &= (1 + S_{11} - S_{22} - \Delta S)/(2S_{21}) \\ \boldsymbol{B} &= (1 + S_{11} + S_{22} + \Delta S)Z_0/(2S_{21}) \\ \boldsymbol{C} &= (1 - S_{11} - S_{22} + \Delta S)/(2S_{21}Z_0) \\ \boldsymbol{D} &= (1 - S_{11} + S_{22} - \Delta S)/(2S_{21}) \end{aligned} \quad (3)$$

where

$$\Delta S = S_{11}S_{22} - S_{21}S_{12}$$

Equations (1)–(3) are combined to yield:

$$e^{-\gamma l} = \left\{\frac{1 - S_{11}^2 + S_{21}^2}{2S_{21}} \pm K\right\}^{-1} \quad (4)$$

where

$$K = \left\{\frac{\left(S_{11}^2 - S_{21}^2 + 1\right)^2 - \left(2S_{11}\right)^2}{\left(2S_{21}\right)^2}\right\}^{\frac{1}{2}} \quad (5)$$

$$Z^2 = Z_0^2\frac{\left(1 + S_{11}\right)^2 - S_{21}^2}{\left(1 - S_{11}\right)^2 - S_{21}^2}. \quad (6)$$

During the extraction of complex parameters γ and $\boldsymbol{Z}$ from $e^{-\gamma l}$ and $\boldsymbol{Z}^2$, the cyclically mapped phase output of the S-parameter network analyzer ($-180°$ to $+180°$) is converted to the true radian measurement phase which can be any real value. Also, extracted parameters with values that are not physically real, such as negative attenuation constants, must be corrected to be real solutions. The values that are not physical satisfy the Telegrapher's equation for propagation in the "negative" direction. Once γ and $\boldsymbol{Z}$ are determined, then from standard transmission line relationships:

$$\gamma = \sqrt{(R + j\omega L)(G + j\omega C)} = \alpha + j\beta \quad (7)$$

$$Z = \sqrt{\frac{(R + j\omega L)}{(G + j\omega C)}}. \quad (8)$$

Then

$$R = \mathrm{Re}\{\gamma Z\} \quad (9)$$

$$L = \mathrm{Im}\{\gamma Z\}/\omega \quad (10)$$

and

$$G = \mathrm{Re}\{\gamma/Z\} \quad (11)$$

$$C = \mathrm{Im}\{\gamma/Z\}/\omega. \quad (12)$$

Thus the Telegrapher's equation transmission line model parameters are determined by combining (9)–(12).

S-parameter data from the structures described in Section II (see Figs. 1 and 2) were used to extract interconnect line parameters $\boldsymbol{R}$, $\boldsymbol{L}$, $\boldsymbol{C}$, and $\boldsymbol{G}$. Variations of these four line parameters over 45 MHz to 20 GHz are graphed in Figs. 6–9. Additional low frequency test data are included as points "A" and "B" in Figs. 6 and 7.

The solid line plot in Fig. 6 shows that interconnect series resistance exhibits a weak increase with frequency and is relatively constant at high frequencies. This series resistance has a strong variation with the interconnect conductor width and thickness. Point A in this figure is the dc series resistance measured with FLUKE 8085A Digital Multimeter through the Cascade Microtech probe station. The dc resistance measurement is 130.3 Ω and the S-parameter-based 45-MHz measured resistance of the 1-cm line interconnect is 131.9 Ω.

The solid line in Fig. 7 shows that interconnect low frequency substrate capacitance is much larger than the substrate capacitance at high frequency. The capacitance is reduced because the interconnect propagation mode changes from slow wave mode to quasi-TEM mode as the frequency increases.

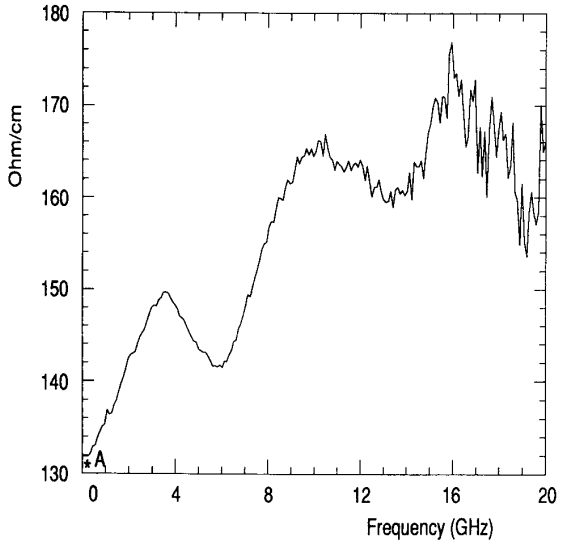

Fig. 6. Extracted series resistance per centimeter versus frequency of 4-μm wide interconnect. A dc measurement that agrees with the extracted 45-MHz data is shown at point A.

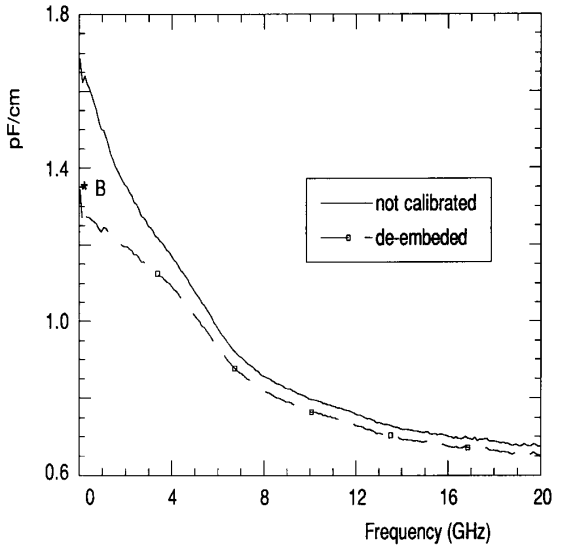

Fig. 7. Extracted series inductance per centimeter versus frequency of 4-μm wide interconnect. A 100-kHz capacitance measurement that agrees with the extracted 45-MHz data is shown at point B.

Point B in this figure is the interconnect substrate capacitance per unit length measured at 100 kHz by a KEITHLEY 590 CV Analyzer. The 100-kHz interconnect capacitance of 1.36 pF is self-consistent with the S-parameter-based 45-MHz capacitance of 1.34 pF for 1 cm of interconnect.

The inductance plot in Fig. 8 shows that inductance is relatively constant over frequency, but does gradually decrease from dc to 4 GHz. However, the reactive effect of a constant value of inductance on signal propagation increases linearly with frequency.

Interconnect on a silicon substrate exhibits small dielectric loss at low frequencies and increases monotonically to an asymptote as in Fig. 9. Note that this variation is extreme and the conductance scale is a log plot. Some papers in the literature assume that conductive dielectric loss is negligible at all frequencies. However, significant dielectric loss in silicon interconnect is measured at microwave frequencies as shown in Fig. 9.

The transmission line propagation constant and characteristic impedance variations with frequency are shown in Figs. 10–13. The propagation constant is separated into the attenuation constant (Fig. 10) and the phase constant (Fig. 11). The attenuation constant increases logarithmically with frequency, and the phase constant shows a linear relationship with frequency. For dc to 1-GHz frequencies the characteristic impedance makes a transition from a very high dc impedance to a constant high frequency quasi-TEM impedance. The magnitude of characteristic impedance is constant over frequencies greater than 1 GHz (Fig. 12). The phase of characteristic impedance varies linearly from negative to positive values with increased frequency and then is fixed at a positive value (0.1 rad/cm) beyond 5 GHz (Fig. 13). This phase change from negative to positive values with frequency shows that the transmission line impedance is capacitive at low frequency and slightly inductive at high frequency. This is explained in Section VI.

IV. Verification of Extraction Algorithm

In order to verify the utilized algorithm, the extracted $\boldsymbol{R}$, $\boldsymbol{L}$, $\boldsymbol{C}$, and $\boldsymbol{G}$ distributed circuit model was simulated in the frequency domain to calculate S-parameters using HSPICE [8]. The extraction process and verification process are shown in Fig. 14. For verification, the distributed circuit transmission model is segmented into a lumped circuit model representing a 1-cm long interconnect [9]. Here, a ten segment lumped model was built using $\boldsymbol{R_s} = \boldsymbol{R}(\omega) \cdot 1$ mm, $\boldsymbol{L_s} = \boldsymbol{L}(\omega) \cdot 1$ mm, $\boldsymbol{C_p} = \boldsymbol{C}(\omega) \cdot 1$ mm, and $\boldsymbol{G_p} = \boldsymbol{G}(\omega) \cdot 1$ mm for each segment. Different segmented models were calculated for six different frequencies. Each segment of the segmented model has the same topology as Fig. 5 but uses discrete lumped elements. This approximate verification model permits reversing the process of line parameter extraction from S-parameters.

HSPICE was used to calculate the approximate S-parameter response of these segmented lumped circuit models at the six frequencies. A comparison of the approximate HSPICE results and the measured S-parameters is made in Table I. The ten segment circuit model approximates magnitude and phase over 5 GHz fairly well. That is, up to 5 GHz, the maximum deviation between HSPICE simulation results and measurement data in magnitude is 12.8% and the maximum phase difference between the two is 22 deg. These calculations verify the $\boldsymbol{R}$, $\boldsymbol{L}$, $\boldsymbol{C}$, and $\boldsymbol{G}$ extraction algorithm. Arbitrarily good agreement can be achieved by using an appropriate number of model segments. The model elements $\boldsymbol{R_s}$, $\boldsymbol{L_s}$, $\boldsymbol{C_p}$, and $\boldsymbol{G_p}$ are dependent on frequency, so additional modeling work is required to derive the transient signal response. However, the accuracy of alternative model topologies can be investigated using this procedure.

TABLE I
COMPARISON OF SIMULATED S-PARAMETERS WITH MEASUREMENT DATA. THE MAGNITUDE (M) OF THE S-PARAMETERS IS ON A LINEAR SCALE AND THE PHASE (Ph) OF THE S-PARAMETERS IS REPORTED IN DEGREES

ITEM	IC Line Parameter (extracted by using EXTRACTION ALGORITHM)				MEASUREMENT S-Parameters		HSPICE SIMULATION (10 segment)	
Frequency	R (Ω/cm)	L (nH/cm)	C (pF/cm)	G (S/cm)	S_{11} M/Ph	S_{21} M/Ph	S_{11} M/Ph	S_{21} M/Ph
45 MHz	131.9	10.8	1.7	2.7e-5	0.554/-6.6	0.420/-21.6	0.568/0.0	0.430/0.0
1 GHz	136.9	11.0	1.5	1.8e-3	0.512/-13.2	0.389/-47.9	0.516/-9.47	0.388/-45.03
2 GHz	142.9	10.7	1.4	4.6e-3	0.428/-18.6	0.337/-88.0	0.440/-12.0	0.335/-84.65
5 GHz	143.5	10.1	1.1	1.4e-2	0.305/-.1	0.215/173.2	0.344/11.44	0.209/172.3
10 GHz	165.0	10.1	0.8	2.2e-2	0.374/4.3	0.121/31.3	0.677/-1.59	0.0005/3.948
20 GHz	166.0	9.1	0.7	2.8e-2	0.410/5.9	0.078/125.6	0.660/5.54	0.0001/134.2

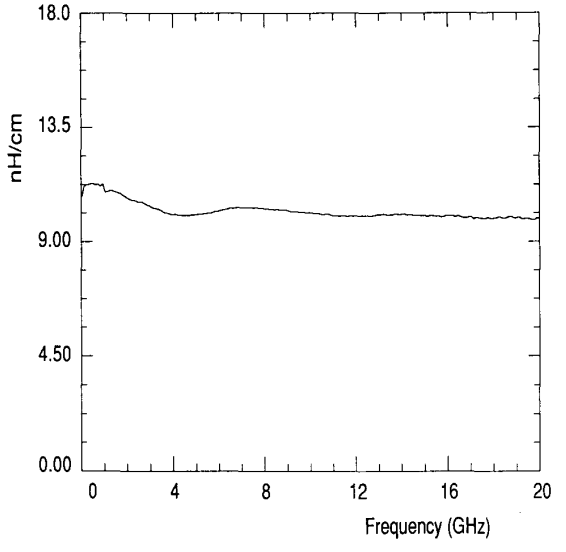

Fig. 8. Extracted substrate capacitance per centimeter versus frequency of 4-μm wide interconnect.

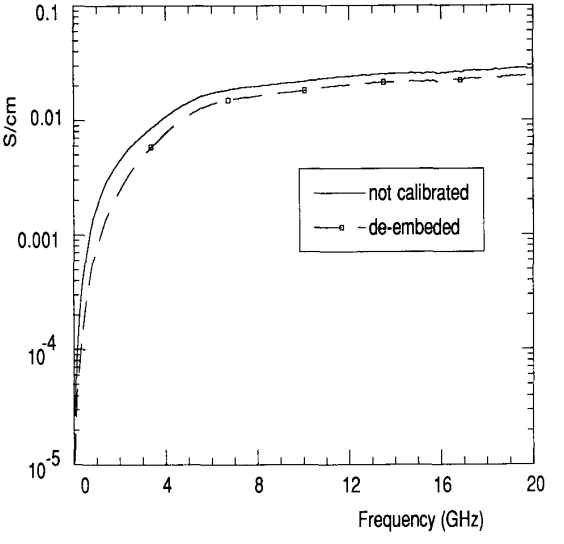

Fig. 9. Extracted substrate conductance per centimeter versus frequency of 4-μm wide interconnect.

V. Y-PARAMETER DEEMBEDDING

In general, pad parasitic response must be subtracted from test structure response in high frequency characterizations. High frequency deembedding techniques, which eliminate the capacitive effects of pads from the measurement data, have been reported in [10]. Enhancements in this technique that eliminate series resistances were subsequently proposed by [11]. The series resistance of the pads has a very small effect on IC interconnect extraction. Therefore, the basic y-parameter subtraction method developed by [10] was adapted to interconnect parameter extraction. Here, the parasitic effects of the pads were modeled as a bond pad capacitance $\boldsymbol{C_b}$ in series with a substrate resistance, $\boldsymbol{R}_{\text{sub}}$. Thus:

$$Y_{\text{pad}} = \frac{(\omega C_b)^2 R_{\text{sub}}}{1+(\omega R_{\text{sub}} C_b)^2} + j\,\frac{\omega C_b}{1+(\omega R_{\text{sub}} C_b)^2} \equiv G_{\text{pad}} + j\omega C_{\text{pad}}. \tag{13}$$

This definition of $\boldsymbol{G}_{\text{pad}}$ and $\boldsymbol{C}_{\text{pad}}$ models the effects of pad parasitics as a parallel circuit of $\boldsymbol{G}_{\text{pad}}$ and $\boldsymbol{C}_{\text{pad}}$ in the same topology as IC interconnect substrate $\boldsymbol{C}$ and $\boldsymbol{G}$ are shown in Fig. 5. From (13), it is evident that pad dielectric loss $\boldsymbol{G}_{\text{pad}}$ dominates as frequency increases. The measured test structure data include the effects of these pad parasitics. Thus with no accounting for parasitic effects:

$$e^{-\gamma} \equiv e^{-(\alpha+j\beta)} = |M| \angle -\theta$$

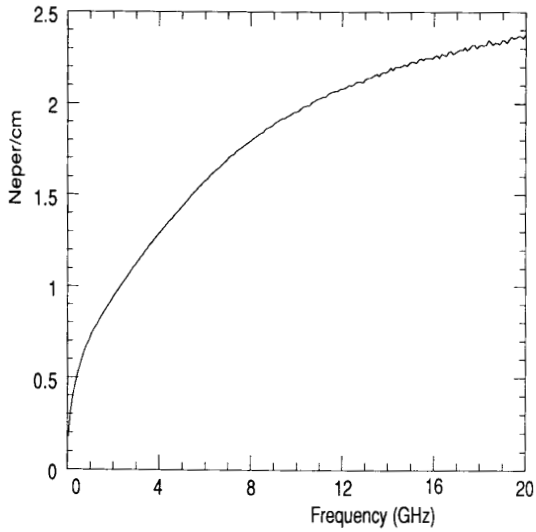

Fig. 10. Extracted attenuation per centimeter versus frequency of 4-μm wide interconnect.

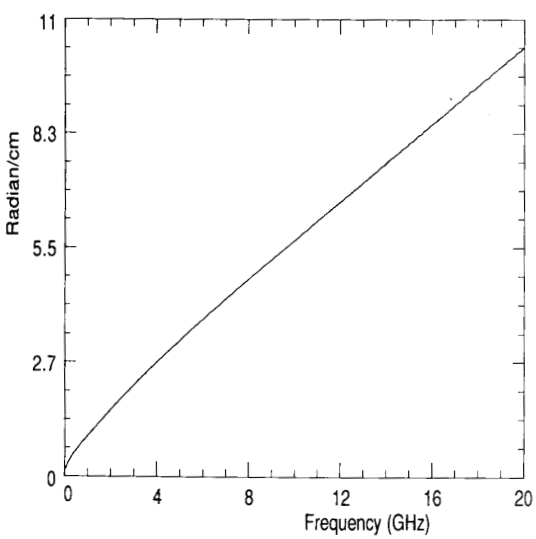

Fig. 11. Extracted phase per centimeter versus frequency of 4-μm wide interconnect.

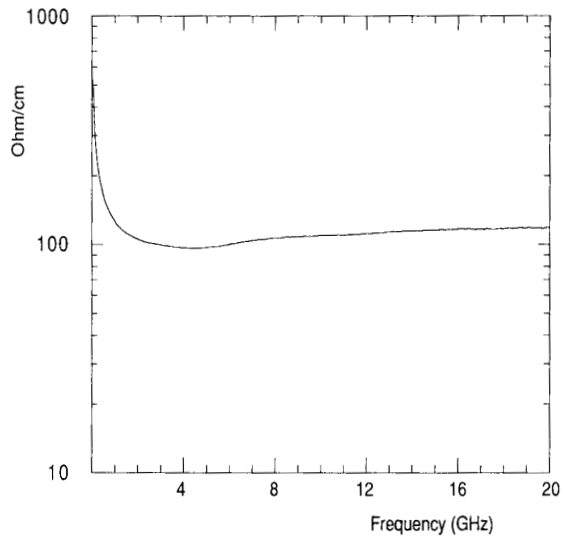

Fig. 12. Magnitude of the 4-μm wide interconnect characteristic impedance versus frequency.

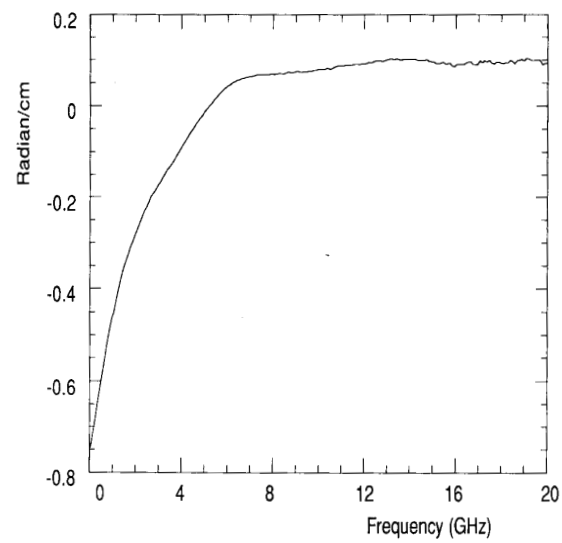

Fig. 13. Phase of the 4-μm wide interconnect characteristic impedance versus frequency.

where

$$\gamma = \sqrt{(R + j\omega L)(G + j\omega C)}. \tag{14}$$

After subtracting the effects of pad parasitics:

$$e^{-\gamma'} \equiv e^{-(\alpha' + j\beta')} = |M'| \angle -\theta'$$

where

$$\gamma' = \sqrt{(R + j\omega L)(G' + j\omega C')}. \tag{15}$$

Corrected transmission parameters $\boldsymbol{G}'$ and $\boldsymbol{C}'$ without the effects of pad parasitics, can be calculated by characterizing $\boldsymbol{G}_{\text{pad}}$ and $\boldsymbol{C}_{\text{pad}}$. Note, $\boldsymbol{G}' = \boldsymbol{G} - \boldsymbol{G}_{\text{pad}}$ and $\boldsymbol{C}' = \boldsymbol{C} - \boldsymbol{C}_{\text{pad}}$. By squaring (7):

$$\alpha^2 + \beta^2 = RG - \omega^2 LC \equiv k_1 \tag{16}$$

$$2\alpha\beta = \omega(GL + RC) \equiv k_2. \tag{17}$$

Therefore,

$$\alpha = \left\{ \frac{RG - \omega^2 LC}{2} + \frac{1}{4}\sqrt{(RG - \omega^2 LC)^2 + \omega^2 (LG + RC)^2} \right\}^{1/2} = \left\{ \frac{k_1 + \sqrt{k_1^2 + k_2^2}}{2} \right\}^{1/2} \tag{18}$$

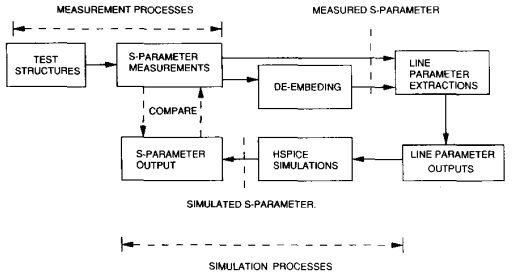

Fig. 14. HSPICE verification procedure of the extraction algorithm.

and

$$\beta = \frac{\omega(GL + RC)}{2\sqrt{\alpha}} = \frac{k_2}{2\sqrt{\alpha}}. \tag{19}$$

By dividing (14) and (15), and separating loss and phase terms

$$\alpha' = \alpha + \ln(M/M') \tag{20}$$

$$\beta' = \beta + \theta' - \theta. \tag{21}$$

Therefore, the deembedded interconnect propagation parameters are

$$C' = \frac{2\alpha'\beta' R - \omega L\left(\alpha'^2 - \beta'^2\right)}{\omega R^2 + \omega^3 L^2} \tag{22}$$

$$G' = \frac{R\left(\alpha'^2 - \beta'^2\right) + 2\omega L(\alpha'\beta')}{R^2 + \omega^2 L^2}. \tag{23}$$

The C' and G' are plotted (dotted line) in Fig. 7 and in Fig. 9. The capacitance curve in Fig. 7 shows that the pad parasitic capacitance is much larger at low frequencies and decreases strongly as the frequency is increased. The conductance curve in Fig. 9 shows that pad parasitic loss becomes much larger with increasing frequency.

VI. Impedance Variation with Frequency

Interconnect characteristic impedance is composed of a real resistive component and imaginary reactive component. A negative interconnect reactance is capacitive and a positive reactance is inductive. This is determined by examining and squaring (8):

$$Z^2 = \frac{R + j\omega L}{G + j\omega C} = \left(\frac{RG + \omega^2 LC}{G^2 + (\omega C)^2}\right) + j\left(\frac{\omega LG - \omega RC}{G^2 + (\omega C)^2}\right). \tag{24}$$

The real term in (24) is always positive and the imaginary term varies from negative to positive with increasing frequency as shown in Fig. 13. Consider the imaginary term:

$$\text{if } \left(\frac{\omega LG - \omega RC}{G^2 + (\omega C)^2}\right) < 0, \qquad RC > LG \tag{25}$$

$$\text{if } \left(\frac{\omega LG - \omega RC}{G^2 + (\omega C)^2}\right) > 0, \qquad LG > RC. \tag{26}$$

For the IC interconnect reported in this paper the reactive component turns from capacitive to inductive at roughly 5 GHz as shown in Fig. 13. In the figure, the phase of the interconnect impedance varies at low frequency indicating slow wave mode propagation while at high frequencies it is constant and close to 0 rad indicating quisi-TEM propagation. Equations (25) and (26) show that both conductance and inductance cannot be ignored in broad-band and fast-transient IC interconnect signal propagation.

VII. Discussion and Summary

A new technique for determining the distributed transmission line parameters from S-parameter measurements of IC interconnect measurement techniques as well as on-chip pad calibration, and algorithm verification are presented. Low frequency measurements of both series resistance and substrate capacitance confirm the extraction results.

This technique is useful for measuring and extracting interconnect performance of all types of IC interconnect conductors and dielectrics in a single interconnect configuration. From these results approximate limited bandwidth segmented models can be built. The accuracy of the segmented model can be compared to the S-parameter data using the procedure outlined in Section IV of this paper.

Future work should focus on developing databases that characterize very fine line IC interconnect performance and in developing methods of extracted coupled line parameters. Both of these will be extremely useful for the IC industry.

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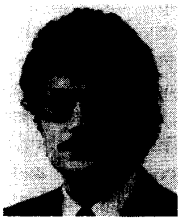

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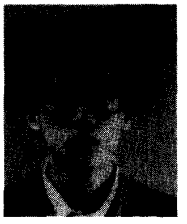

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