
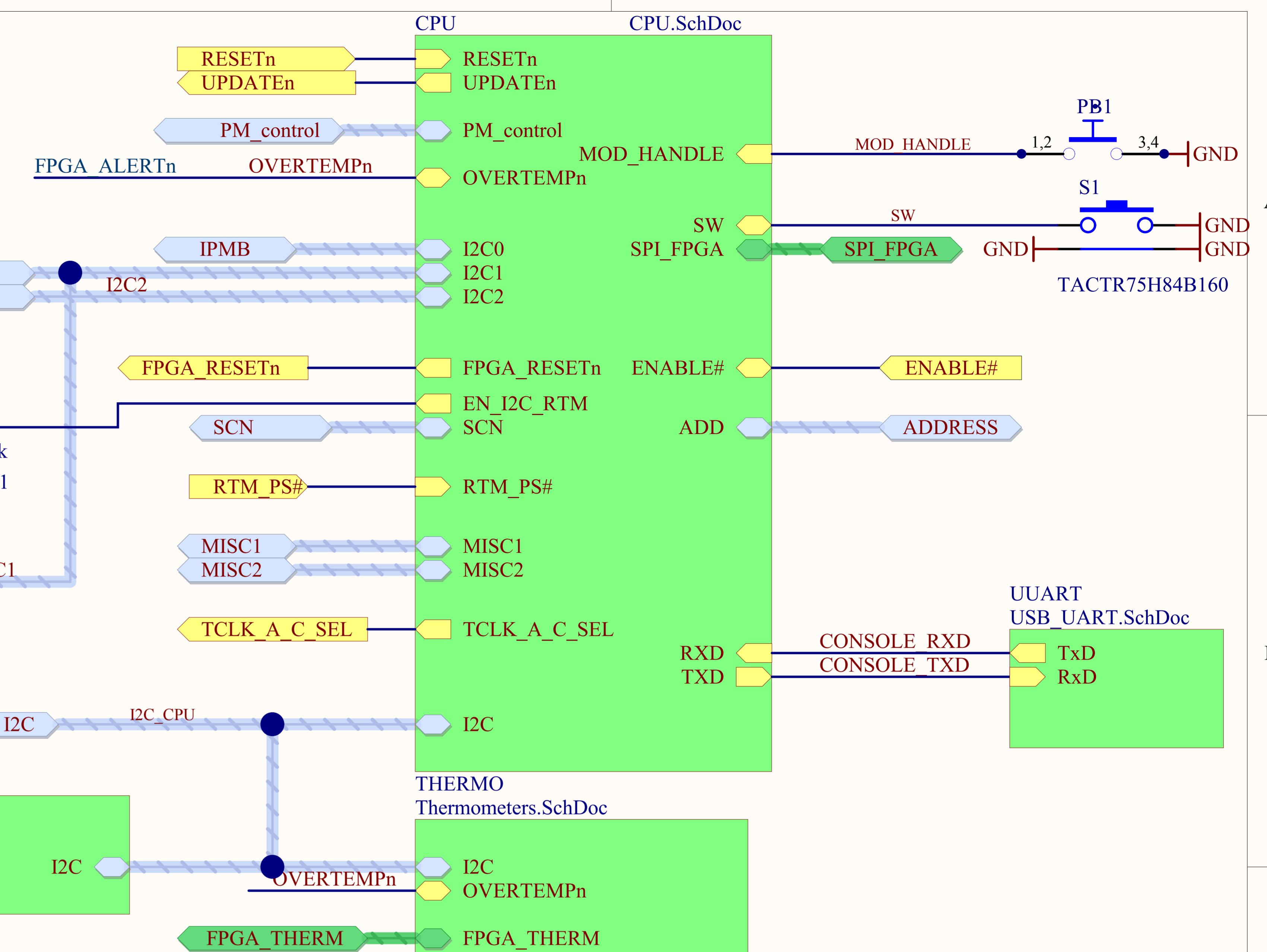
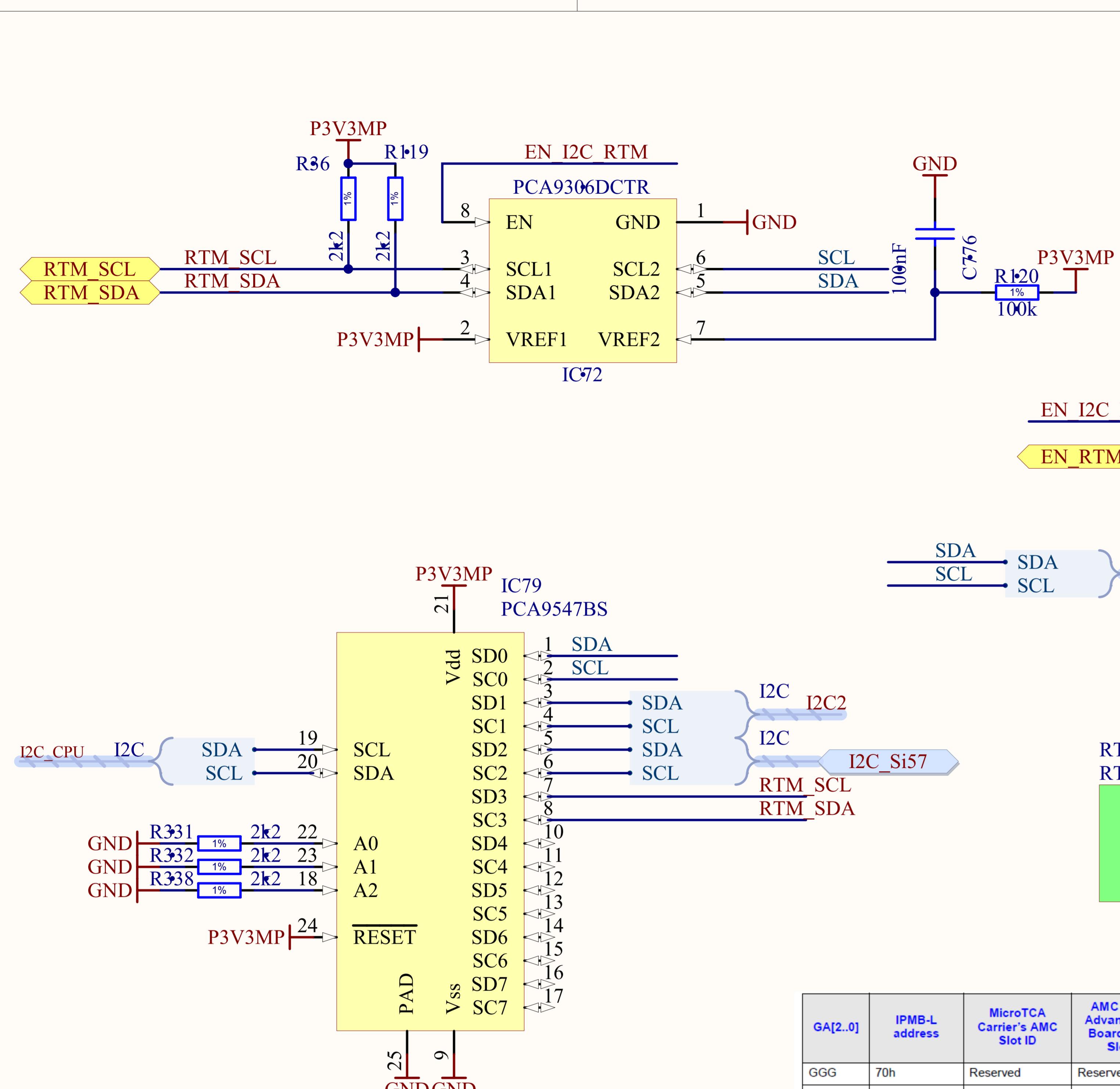


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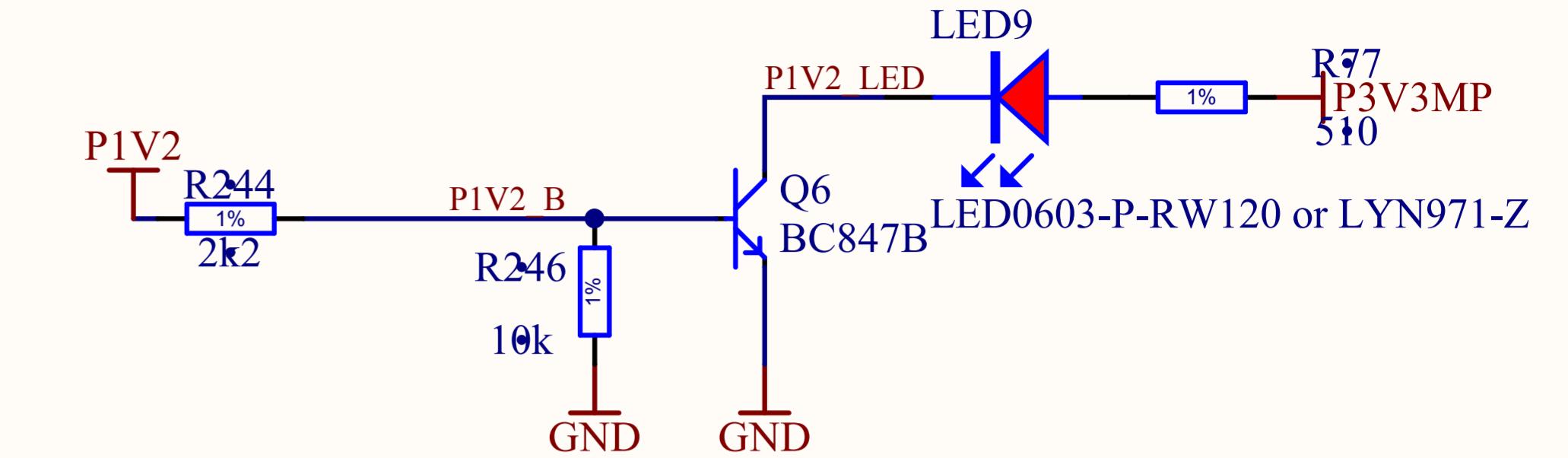
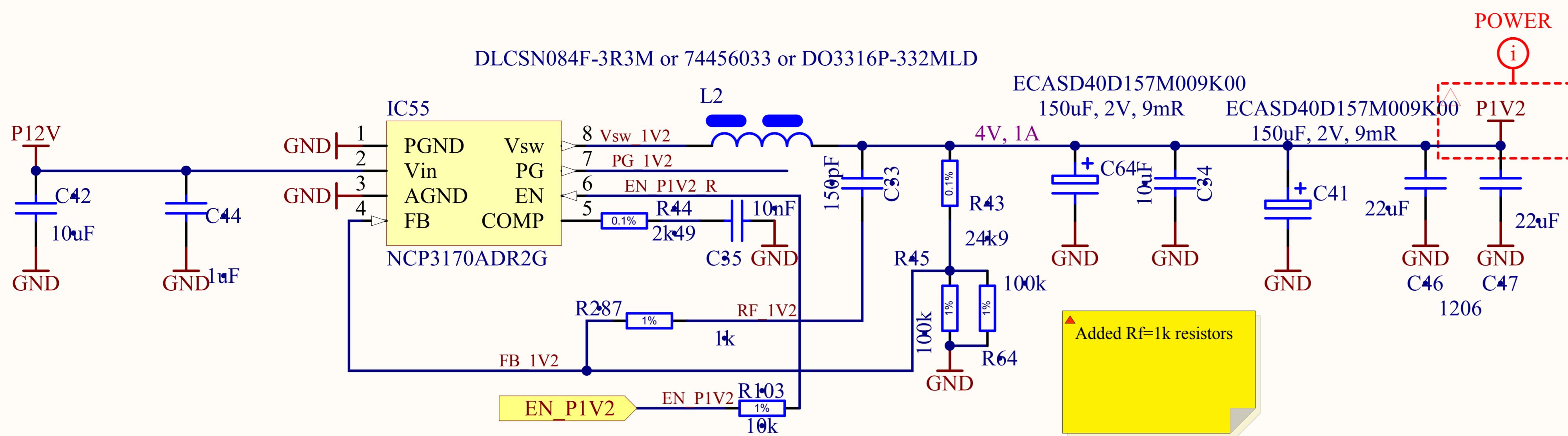
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File: C:\Users\...\FMC_connector.SchDoc	Drawn By:	



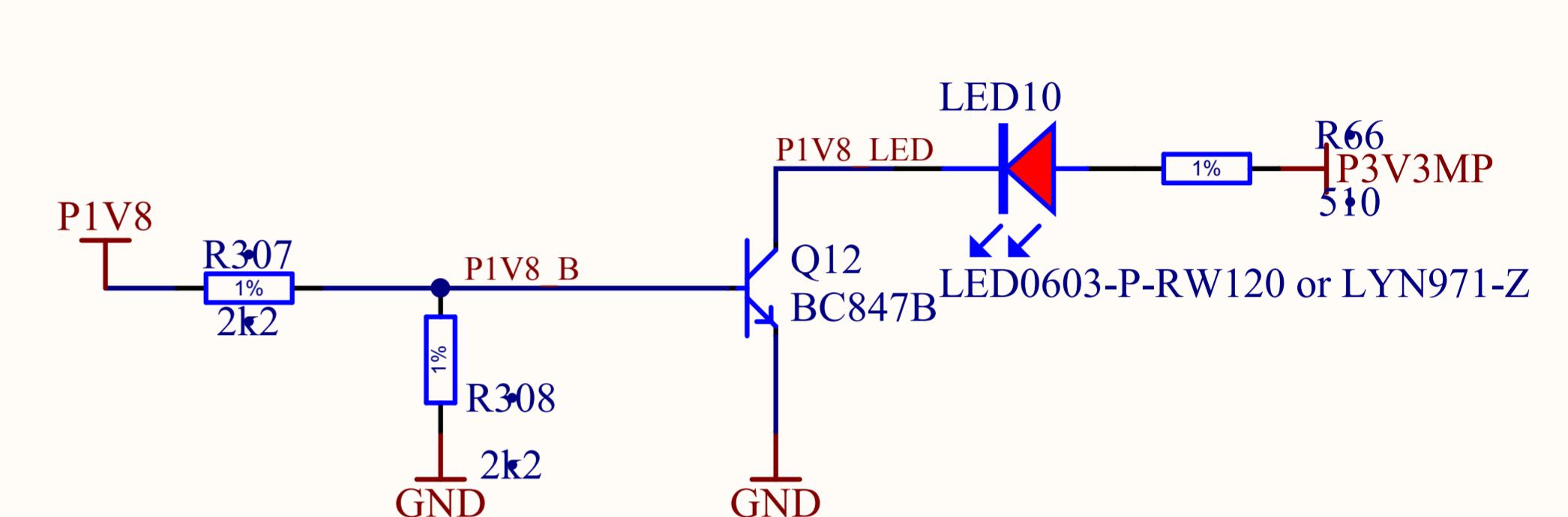
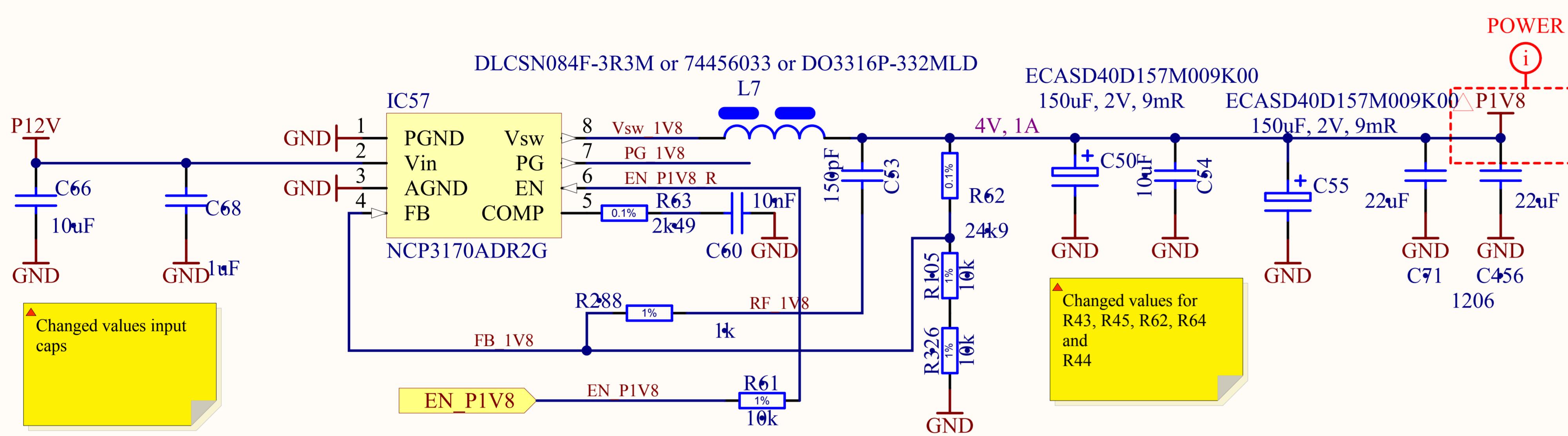


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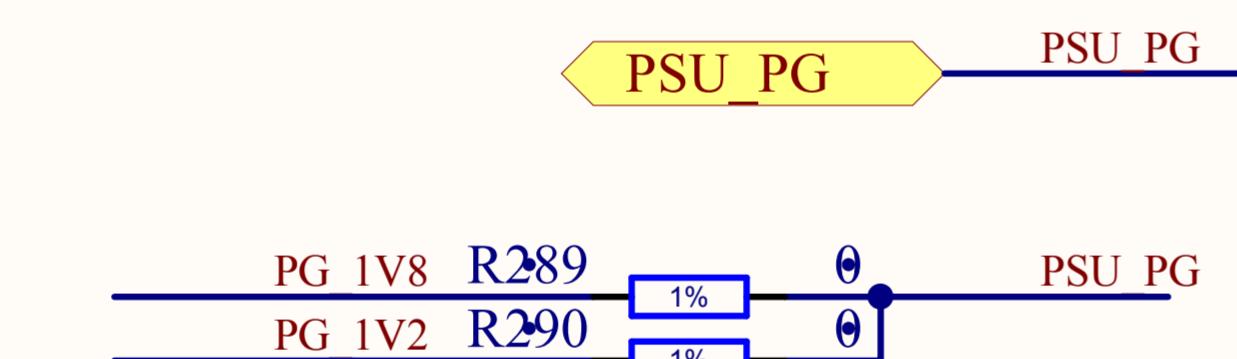
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B



C



VIN	Vout	Lout	R1	R2	Rf	Cf(pF)	Cc(nF)	Rc(k)	Cp(pF)	Resistance for Current Gain
12	0.8	1.8	24.9	NI	NI	NI	NI	15	3.6	
12	1.0	2.5	24.9	100	1	150	15	0.825	NI	4
12	1.1	2.5	24.9	66.5	1	150	10	2	NI	20
12	1.2	2.5	24.9	49.9	1	150	10	2	NI	20
12	1.5	3.6	24.9	28.7	1	150	10	2.49	NI	20
12	1.8	3.6	24.9	20	1	150	10	2.49	NI	20
12	2.5	4.7	24.9	11.8	1	150	8.2	3.74	NI	25
12	3.3	4.7	24.9	7.87	1	150	6.8	4.99	NI	27
12	5.0	7.2	24.9	4.75	1	150	3.9	10	NI	27

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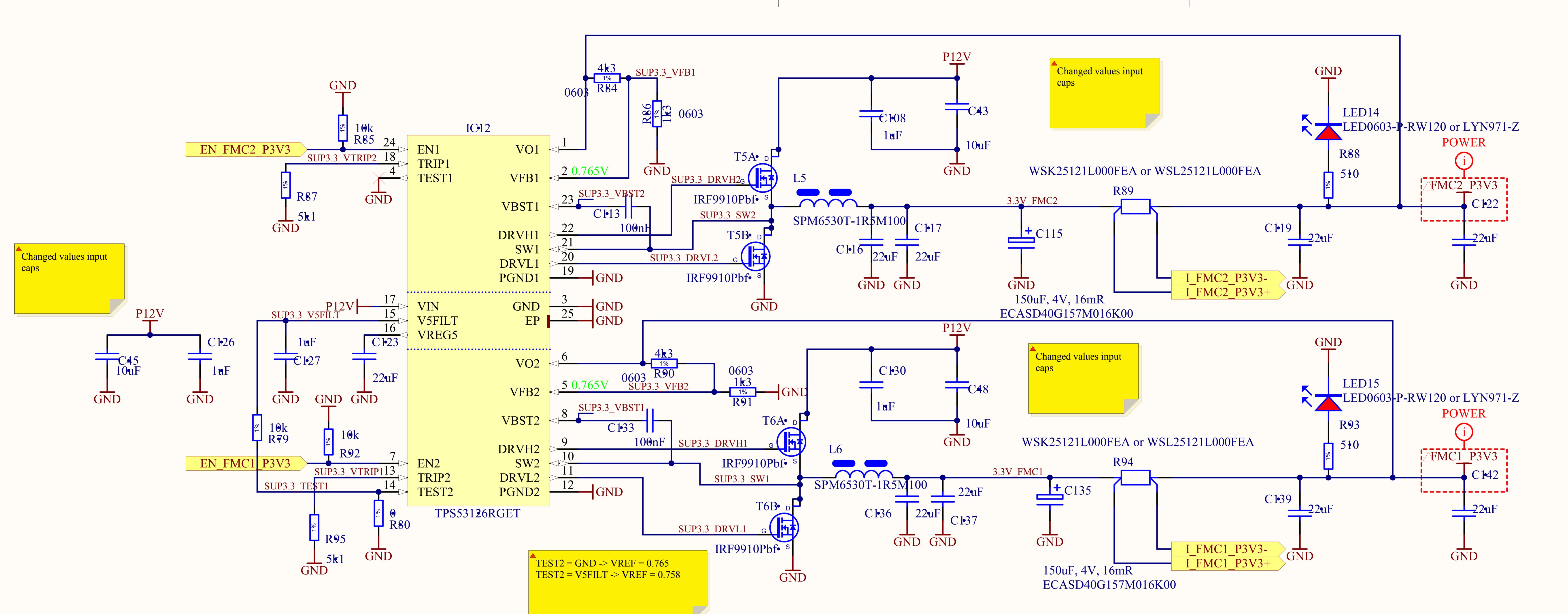
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Date: 2014-08-01

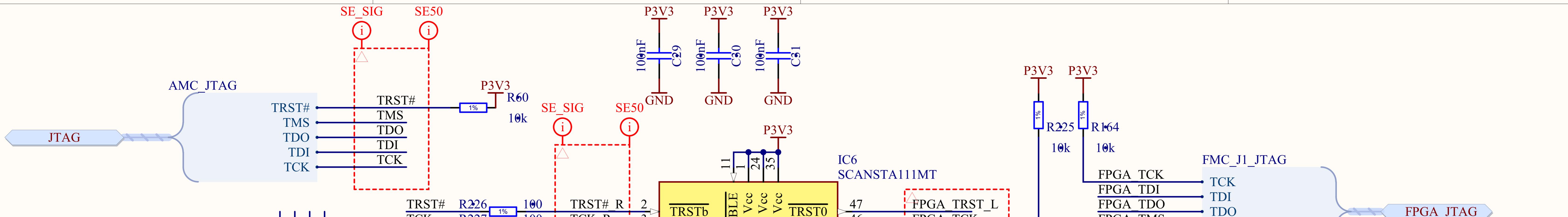
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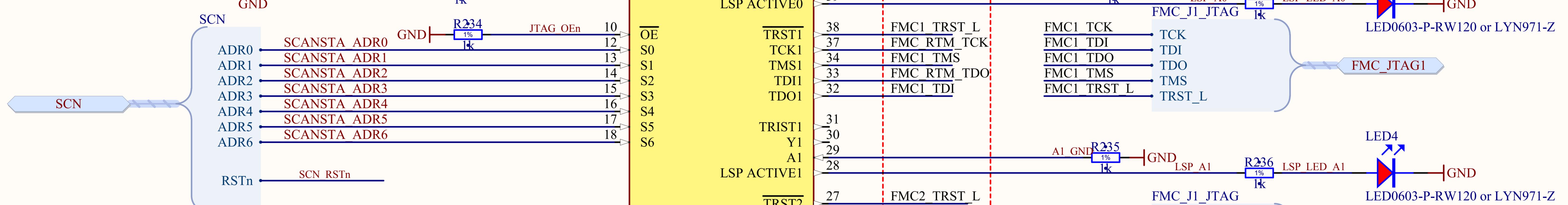
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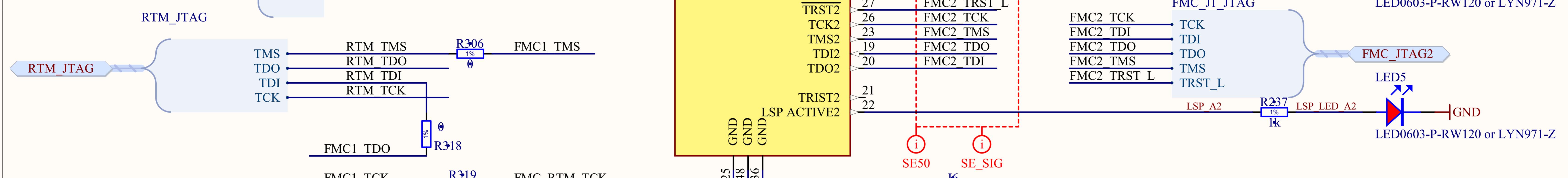
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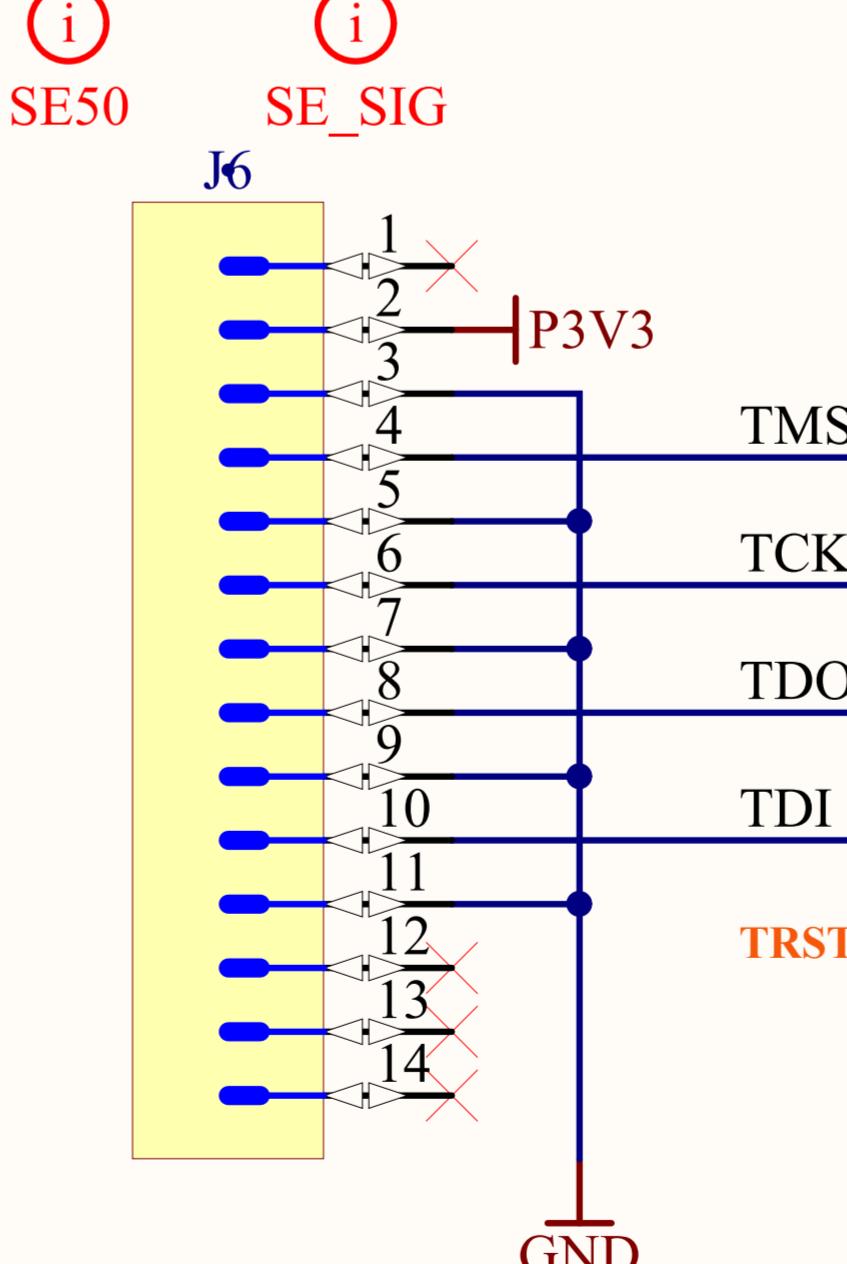
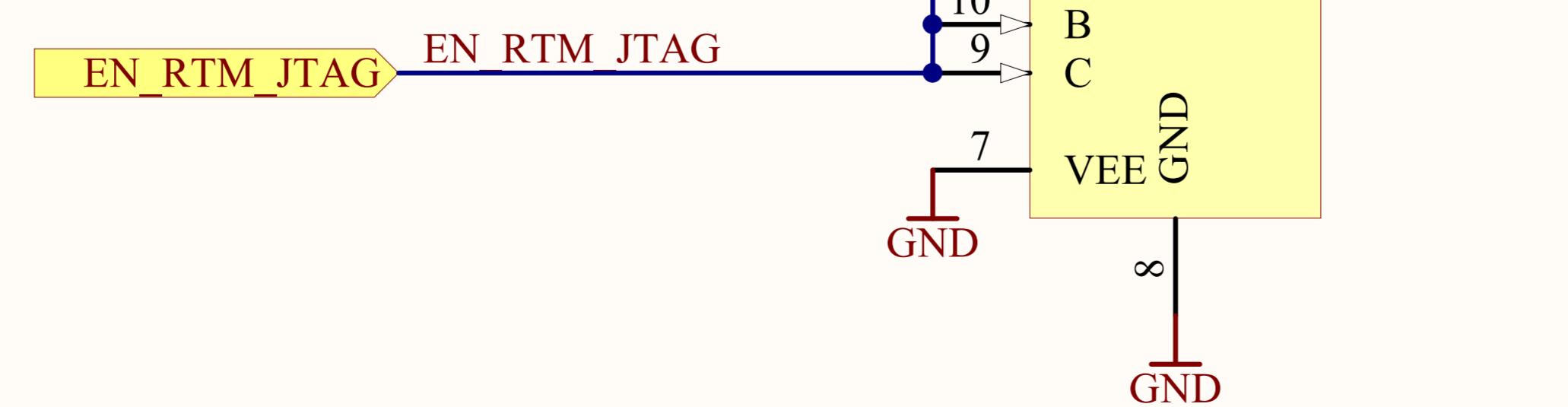
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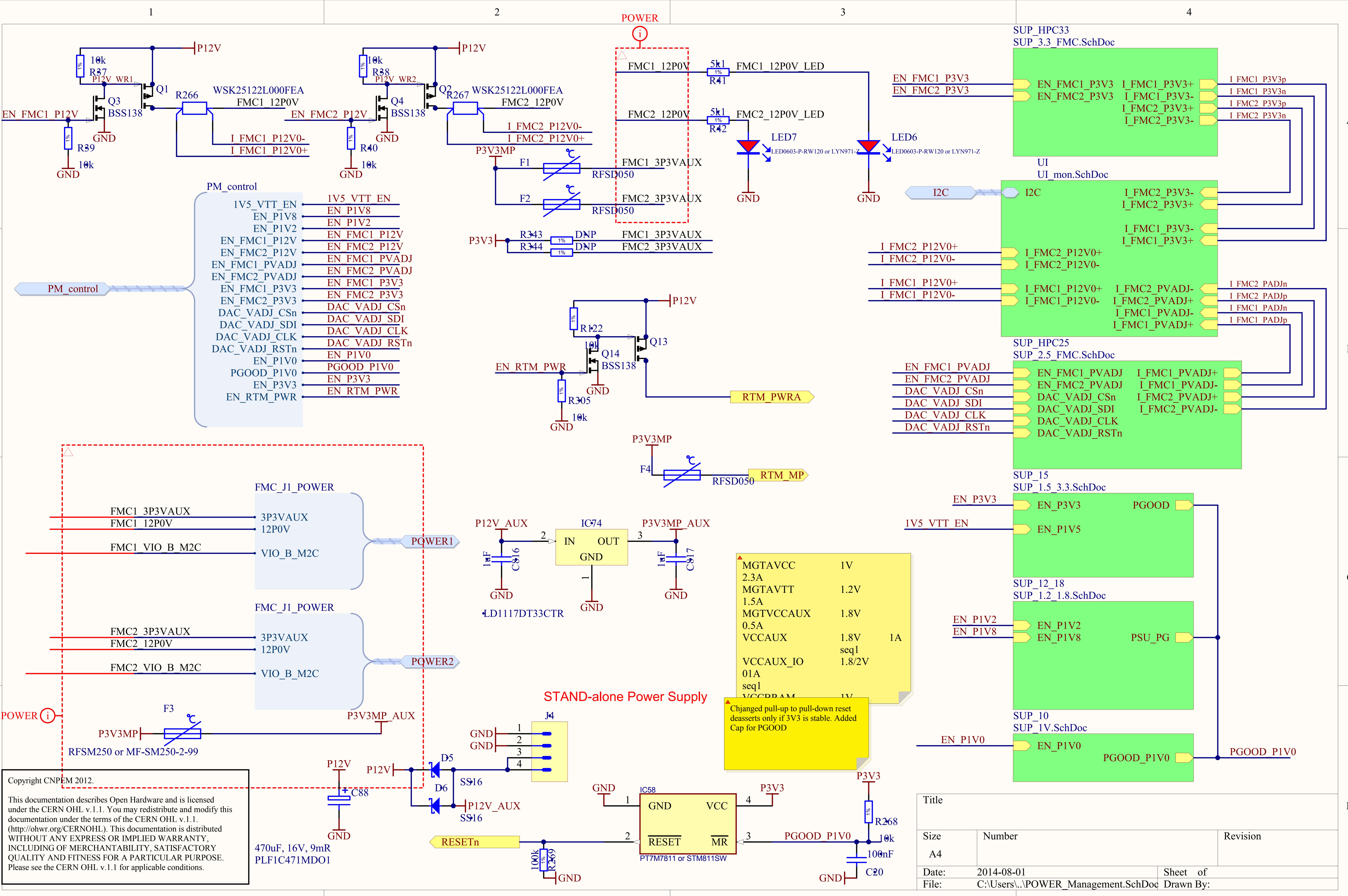
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
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
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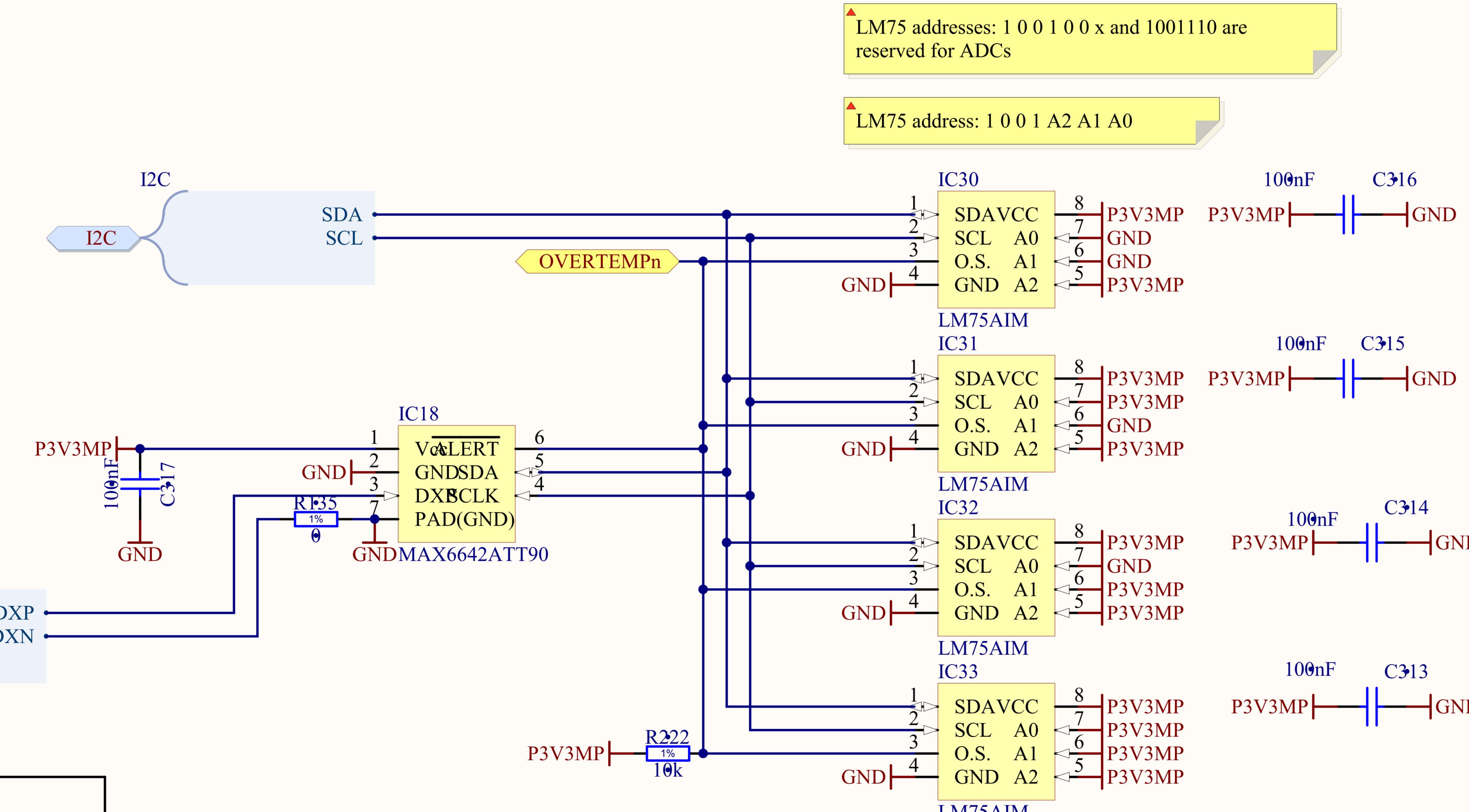
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Number

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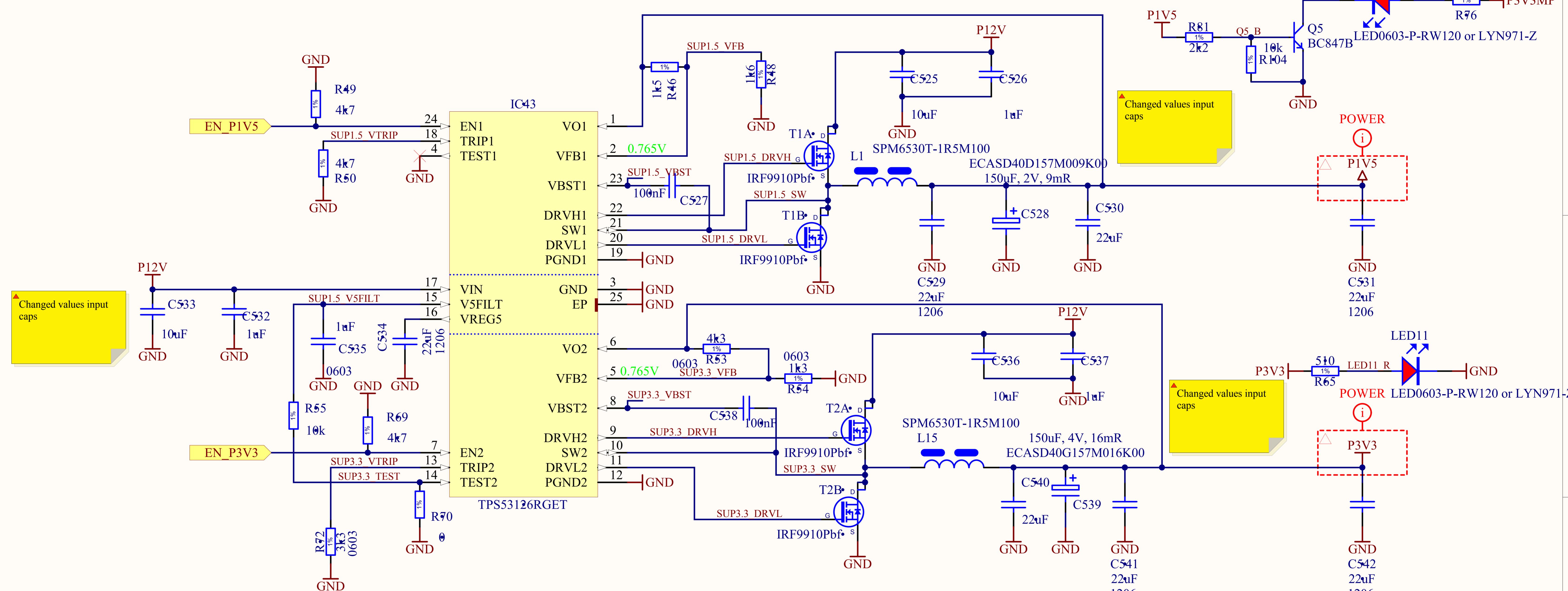
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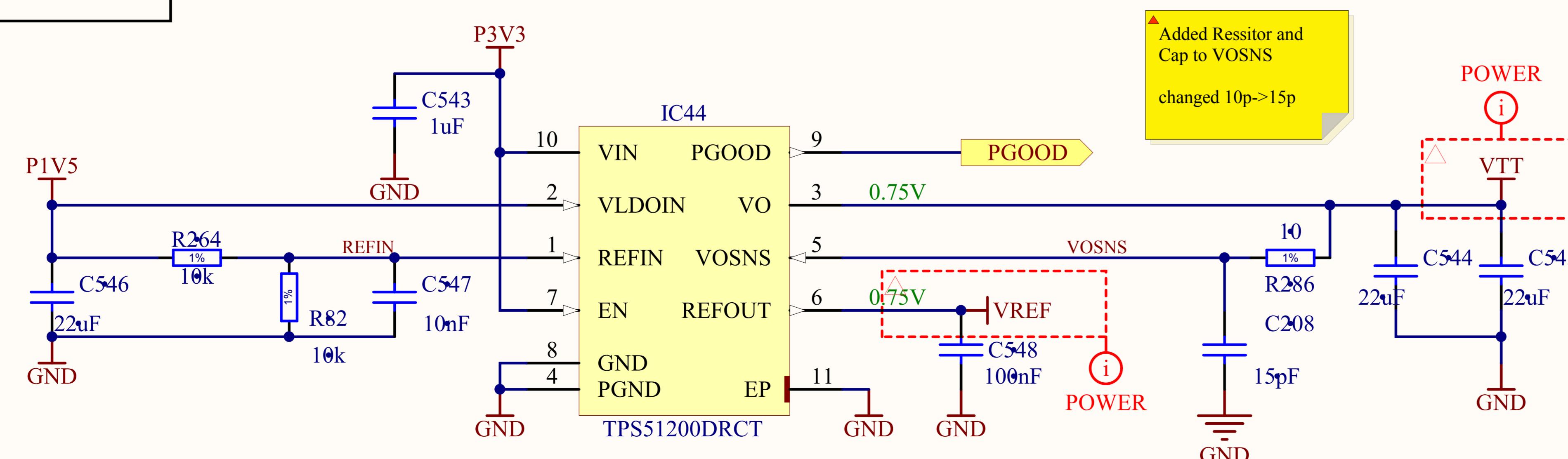
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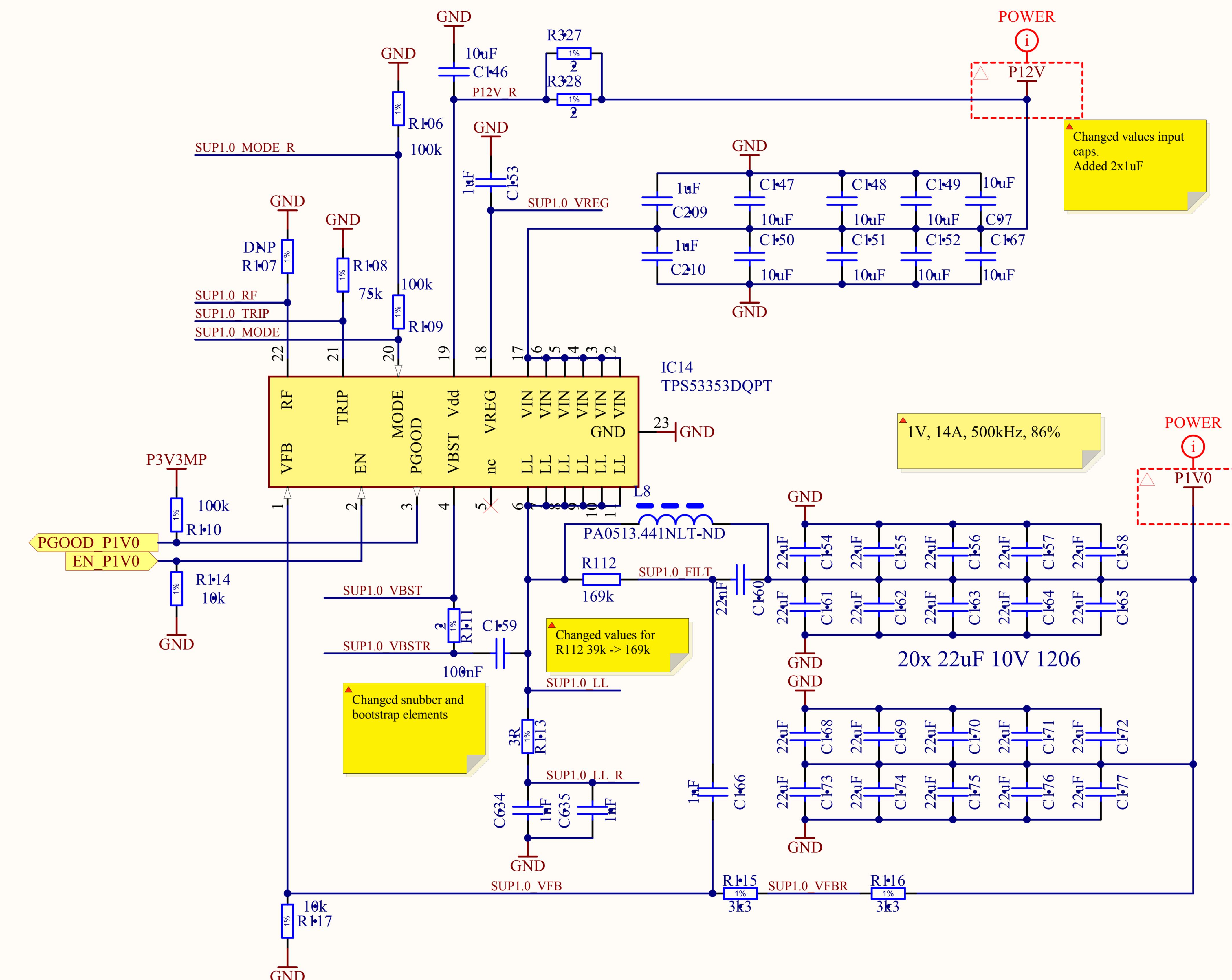
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R1	R2	Ir	Vout	R1/R2	Rerror	
330.0 ? %	100.0 ? %	7.650 mA		3.290 V	3.300	0.41
430.0 ? %	130.0 ? %	5.885 mA		3.295 V	3.308	0.18
1000.0 ? %	300.0 ? %	2.550 mA		3.315 V	3.333	0.59
1100.0 ? %	330.0 ? %	2.318 mA		3.315 V	3.333	0.59
1200.0 ? %	360.0 ? %	2.125 mA		3.315 V	3.333	0.59
1300.0 ? %	390.0 ? %	1.962 mA		3.315 V	3.333	0.59
2700.0 ? %	820.0 ? %	0.933 mA		3.284 V	3.293	0.64
3000.0 ? %	910.0 ? %	0.841 mA		3.287 V	3.297	0.51



Cannot open file  
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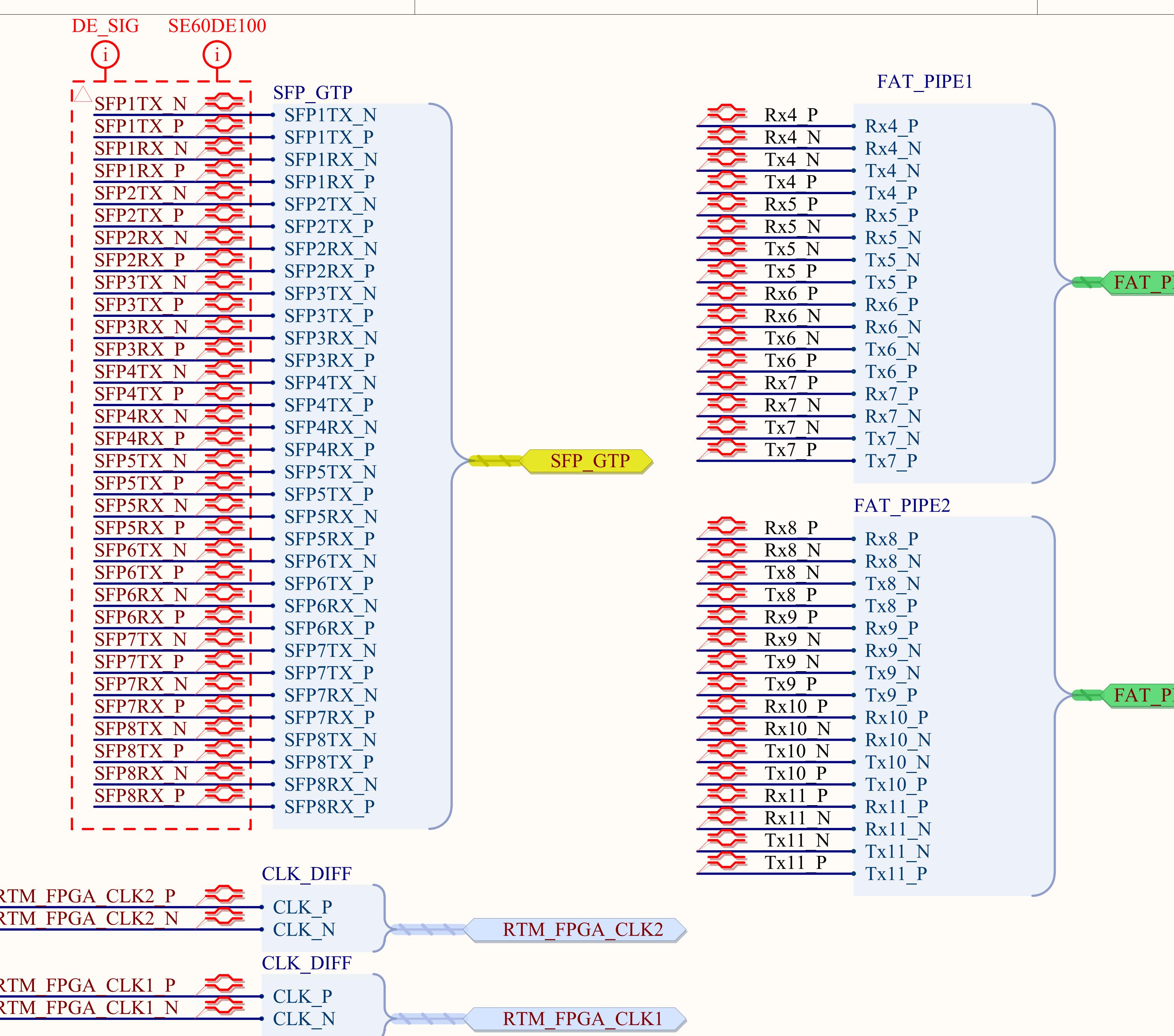
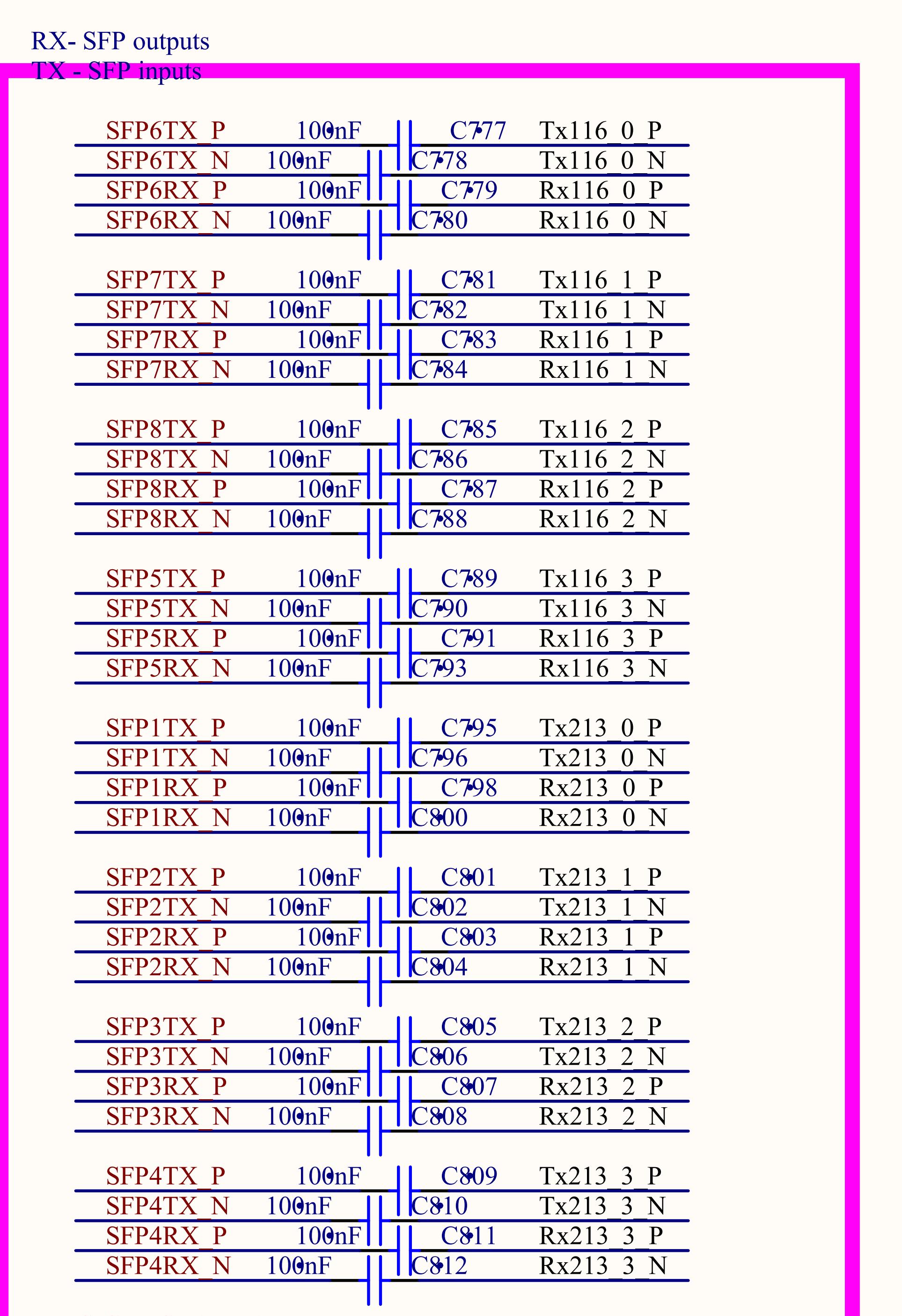
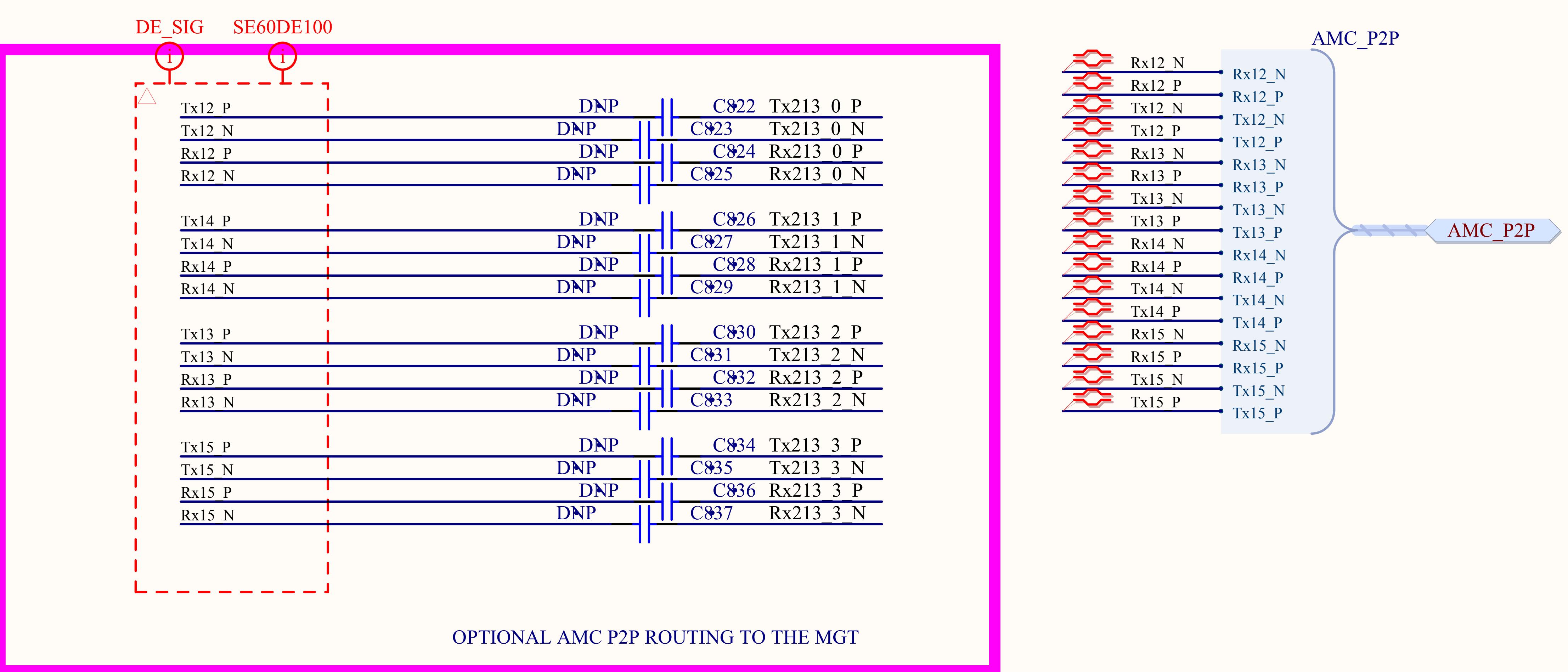


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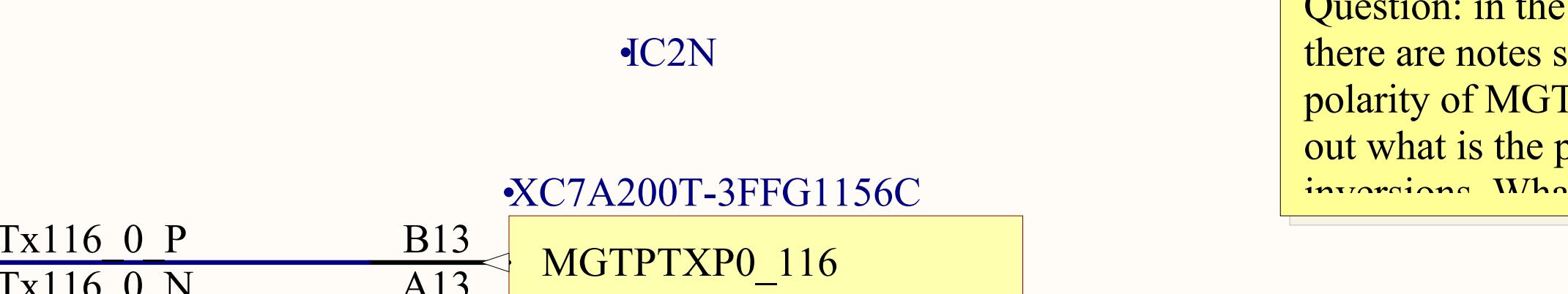
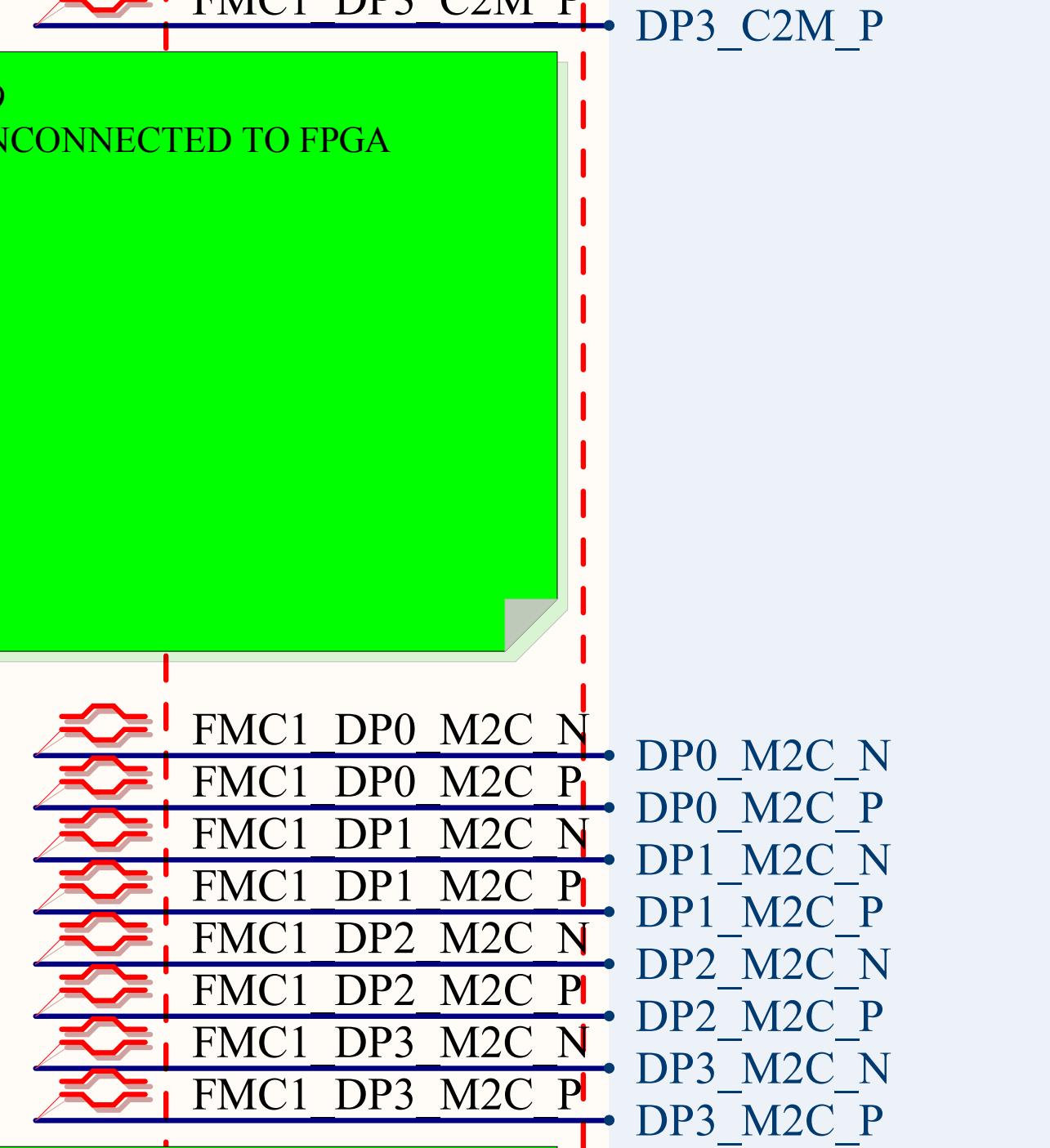
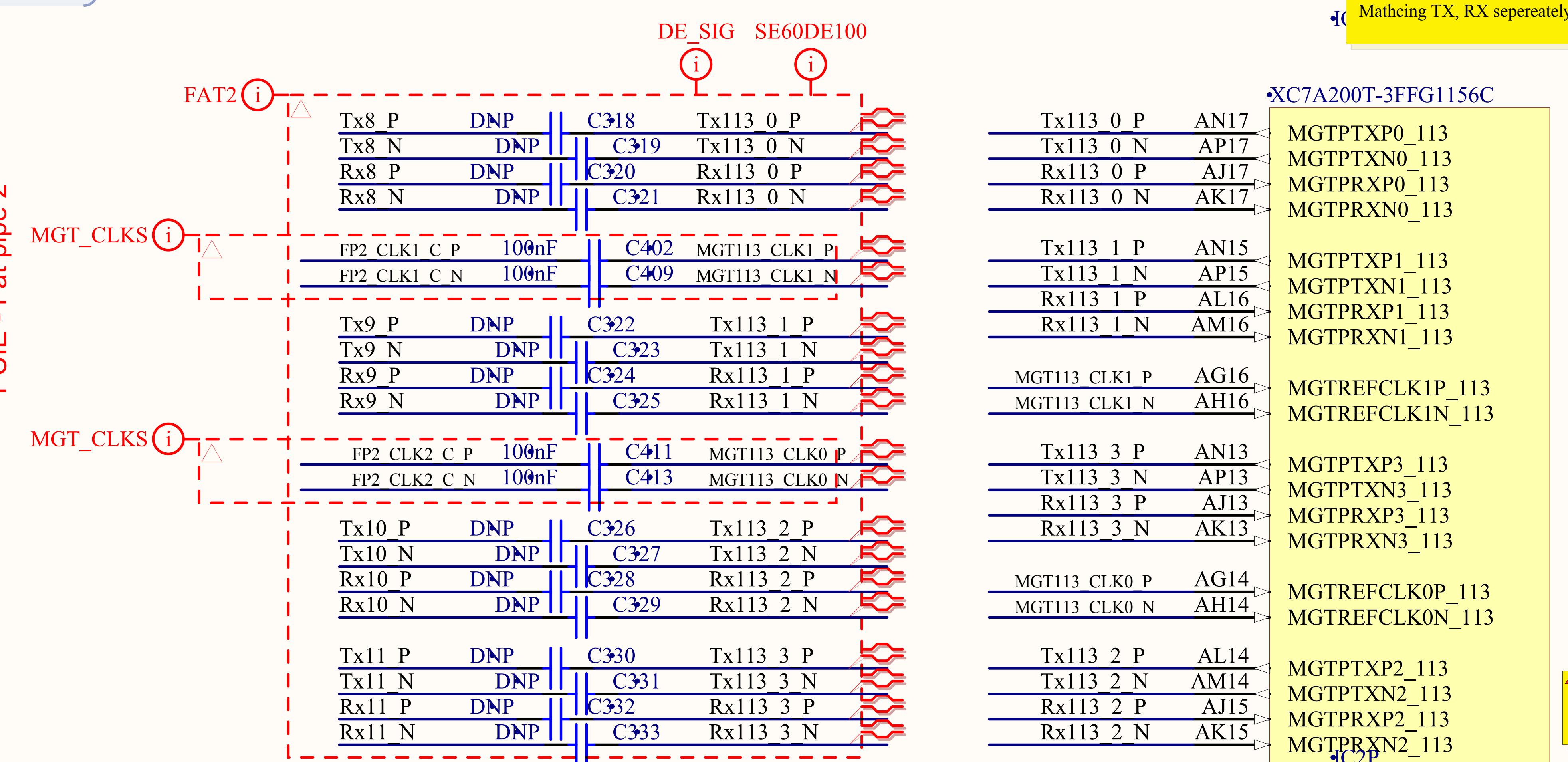
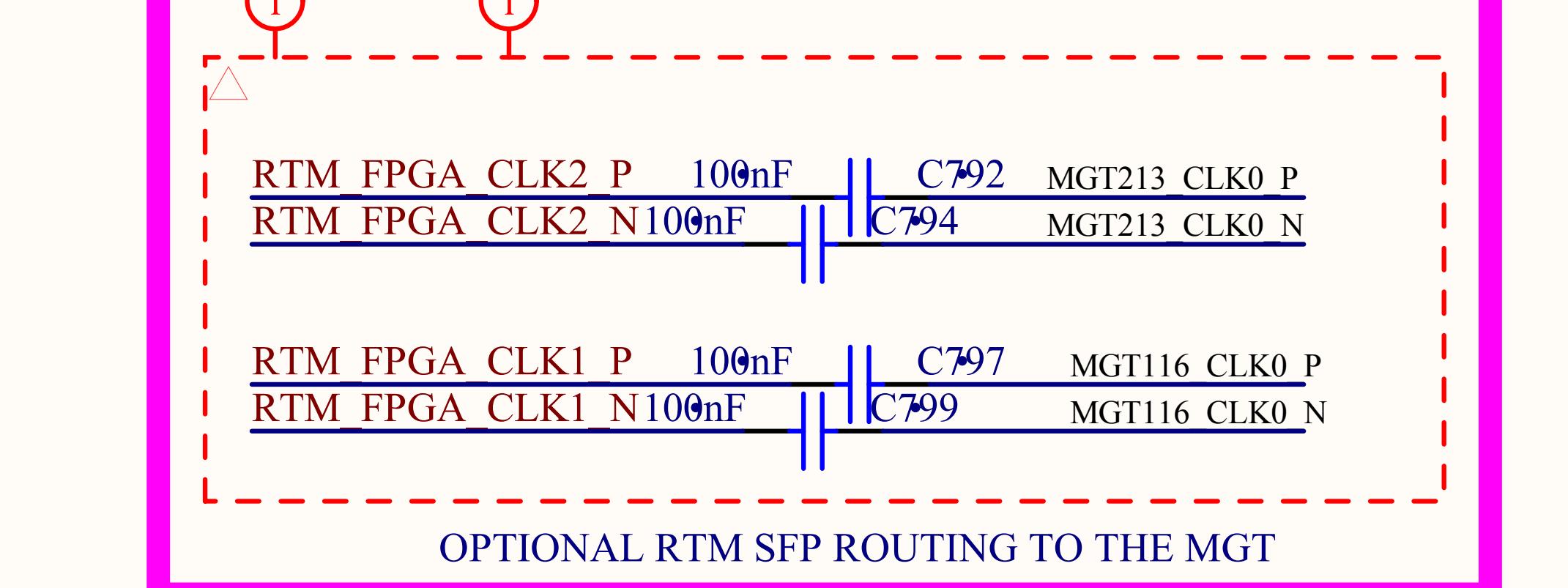
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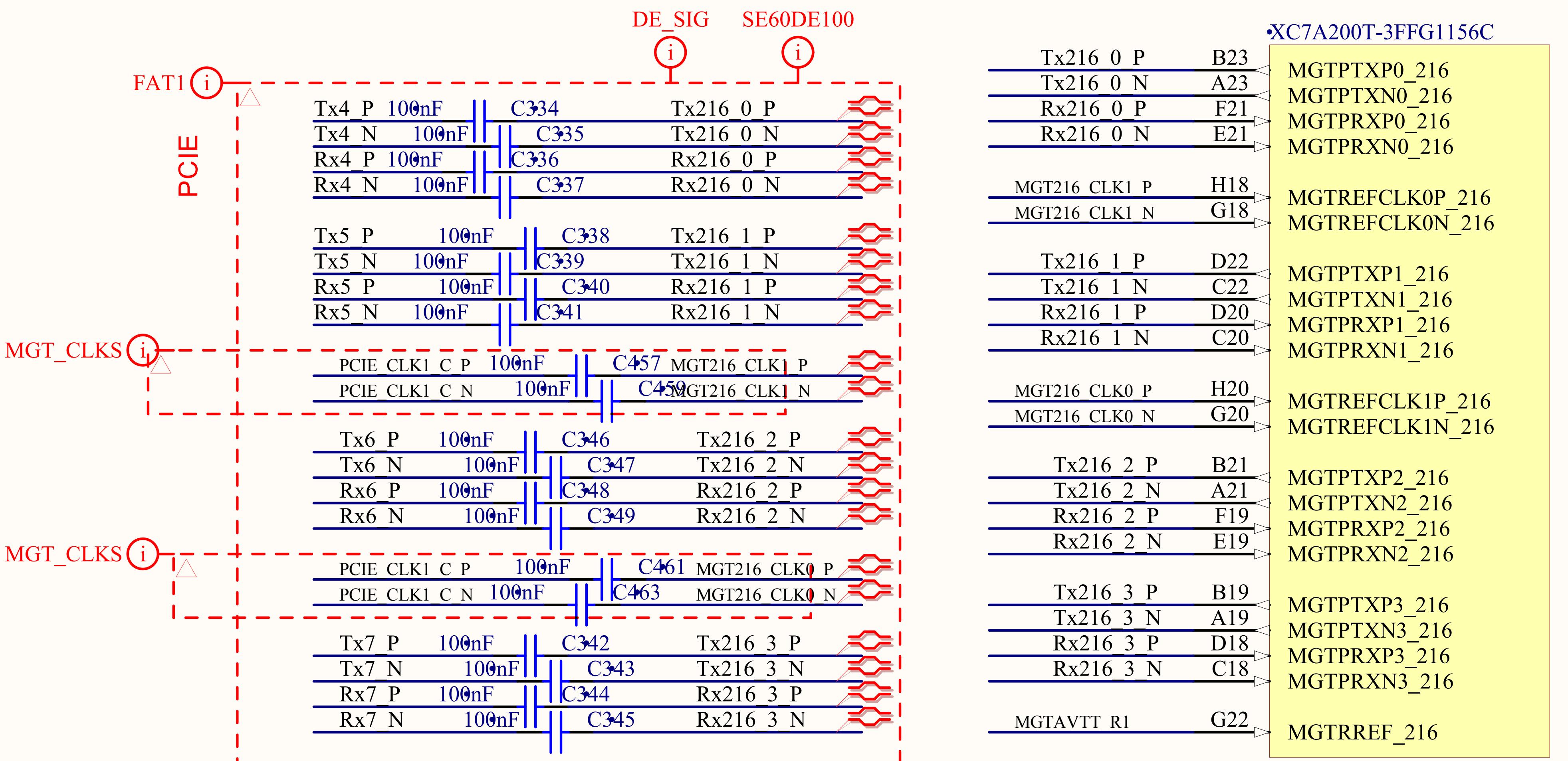


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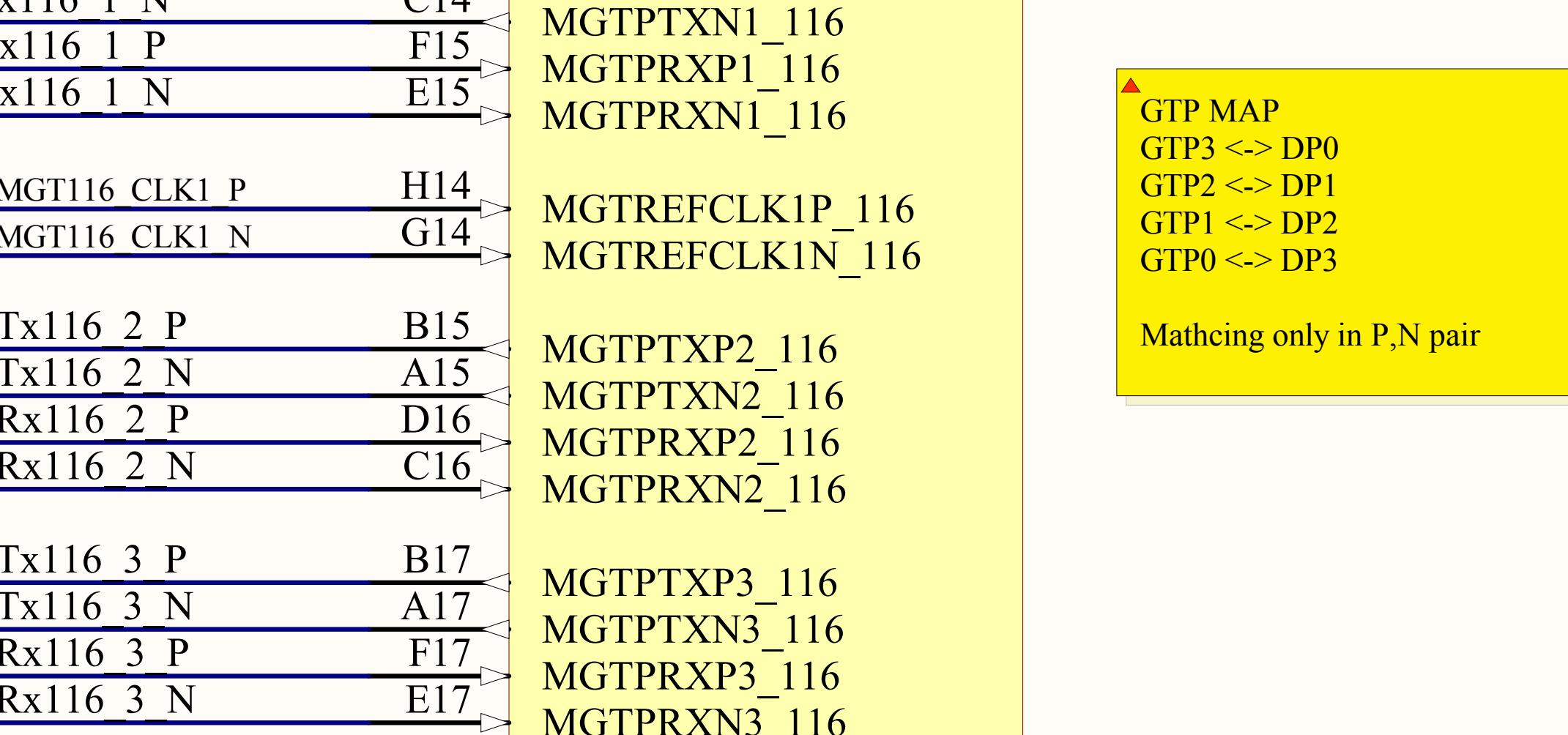
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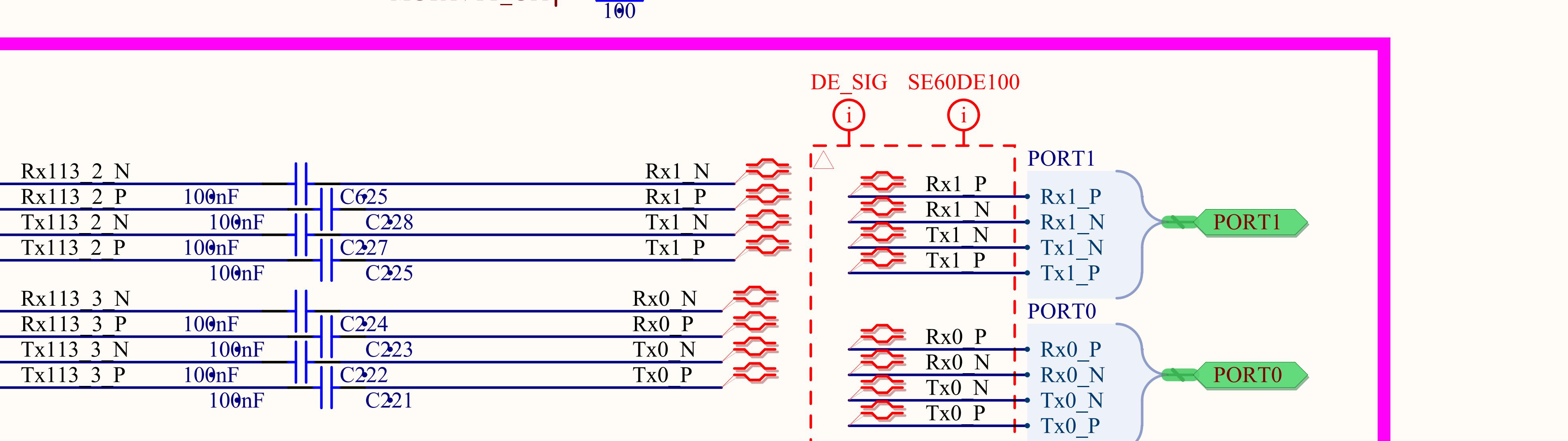
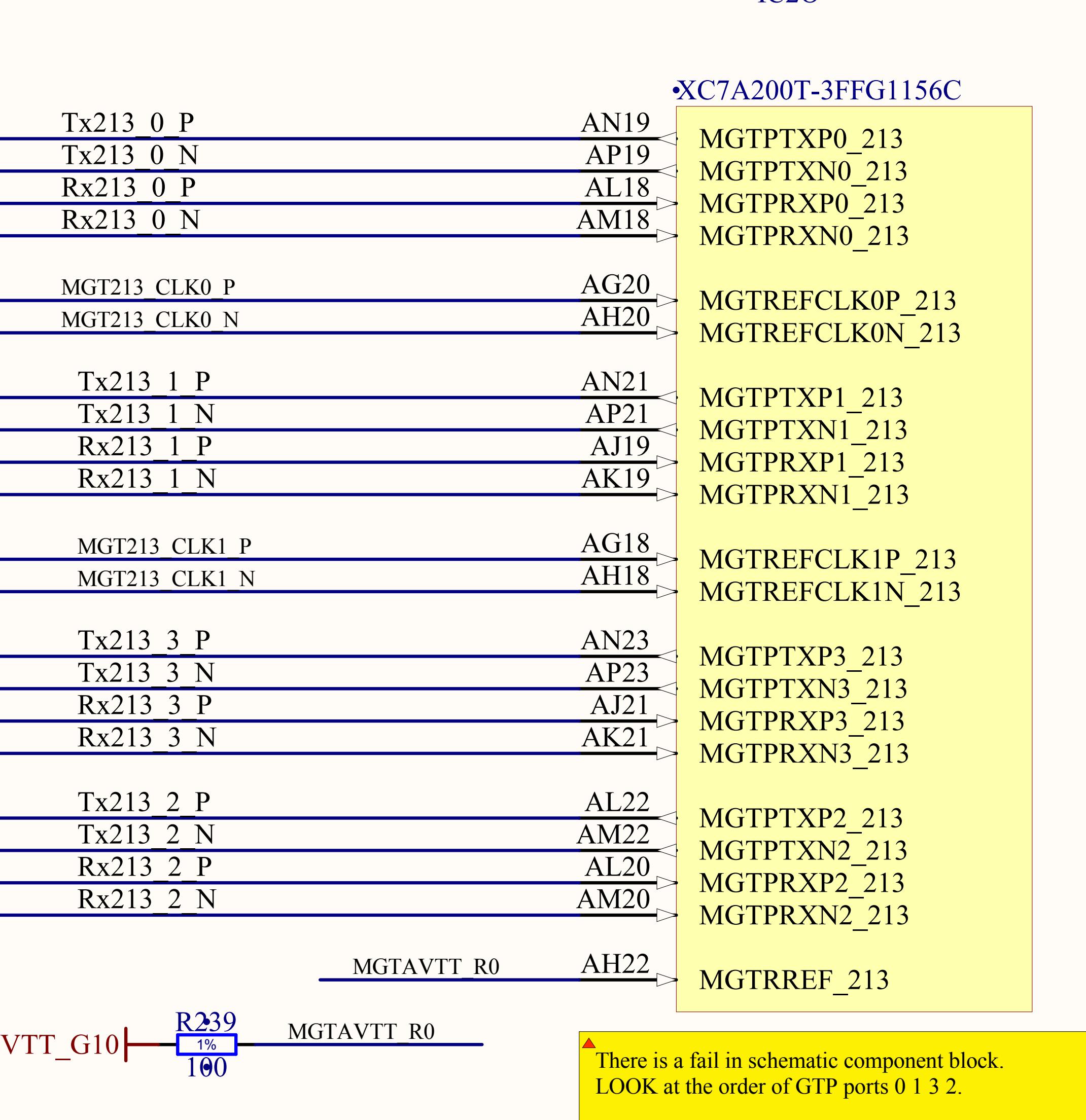
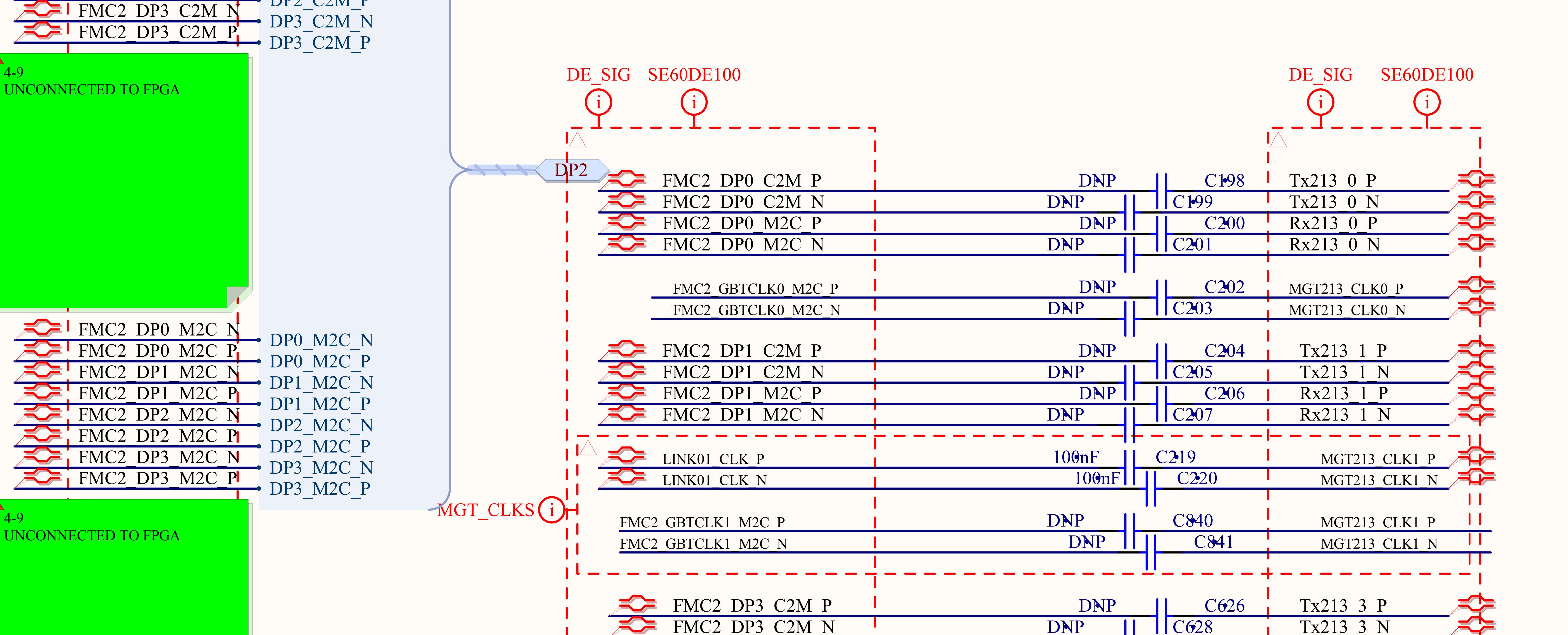
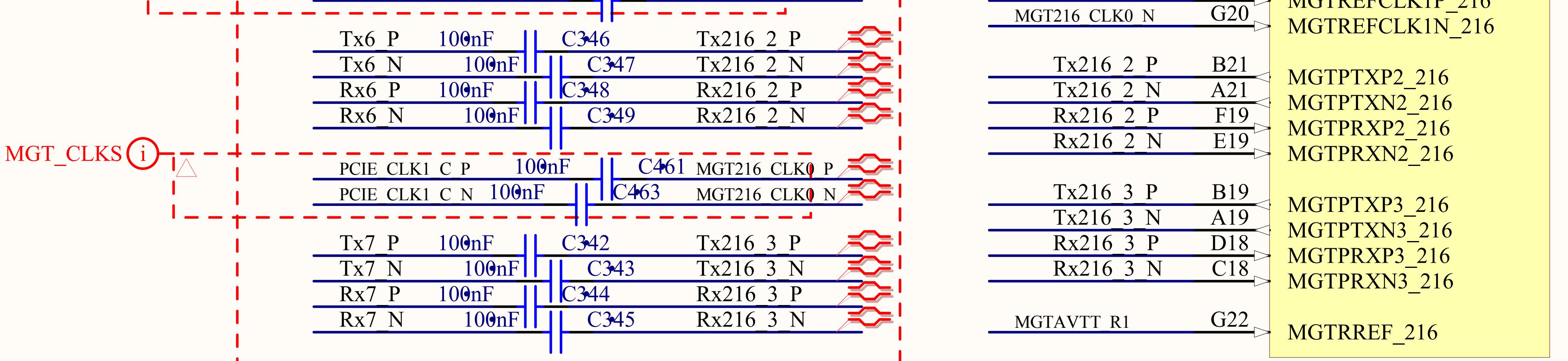
Question: in the MGT assignments, there are notes saying about inverted polarity of MGT lines. I couldn't figure out what is the pattern of such inversions. What is the reason for such inversions?



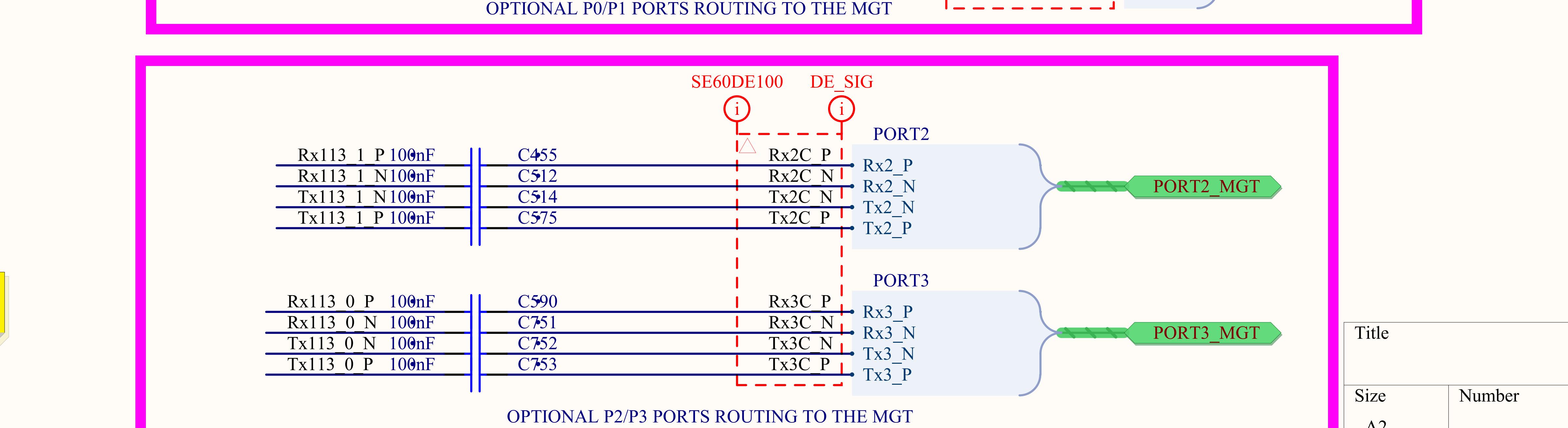
There is a error in schematic component block.  
LOOK at the order of GTP ports 0 1 3 2.



MAP  
3 <-> DP0  
2 <-> DP1  
1 <-> DP2  
0 <-> DP3

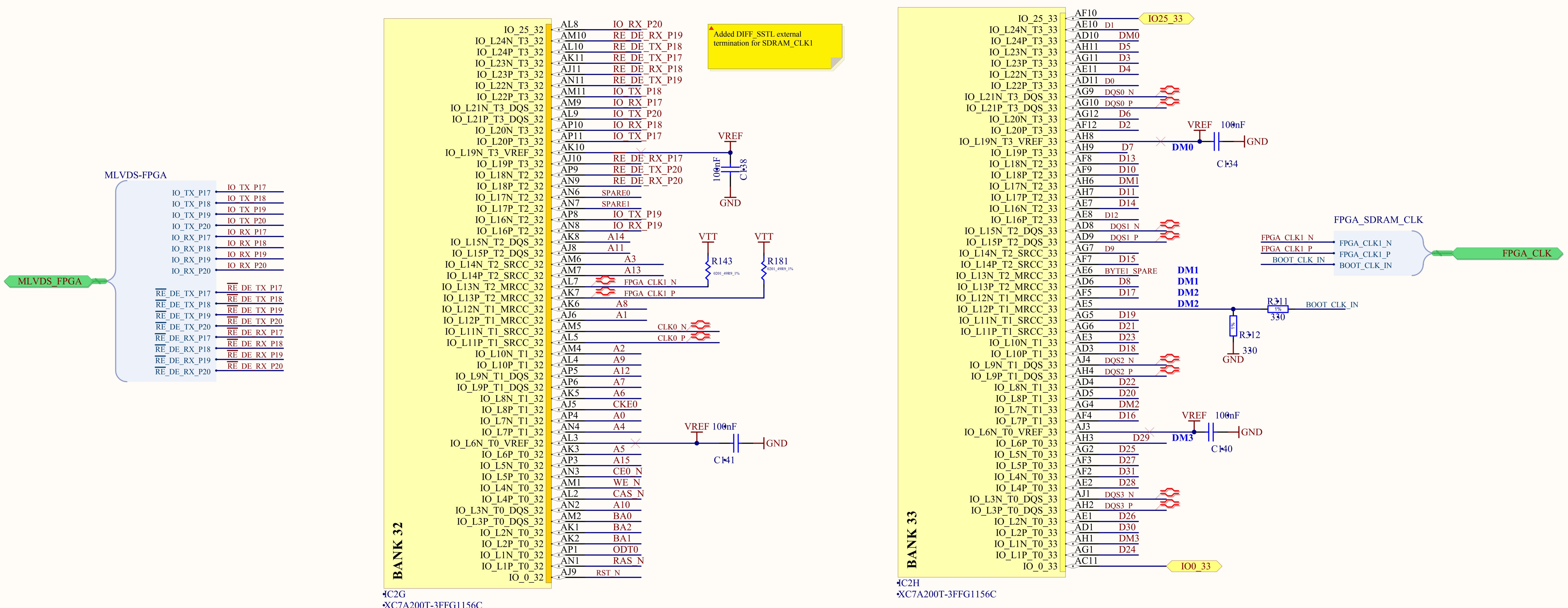


213



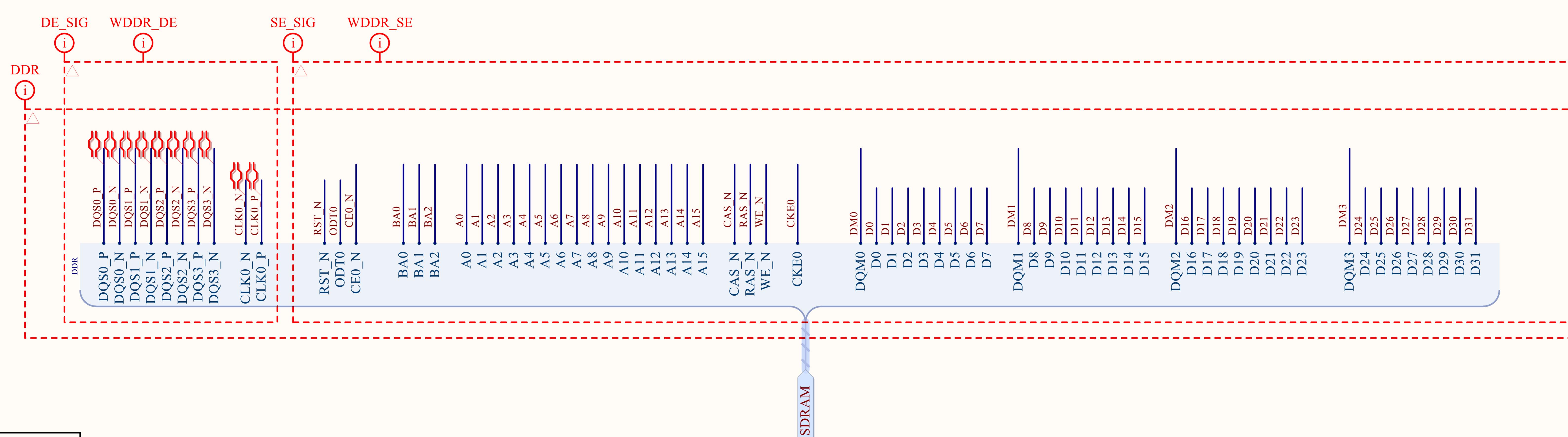
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A_MGT.SchDoc	Drawn By:

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
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
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
D

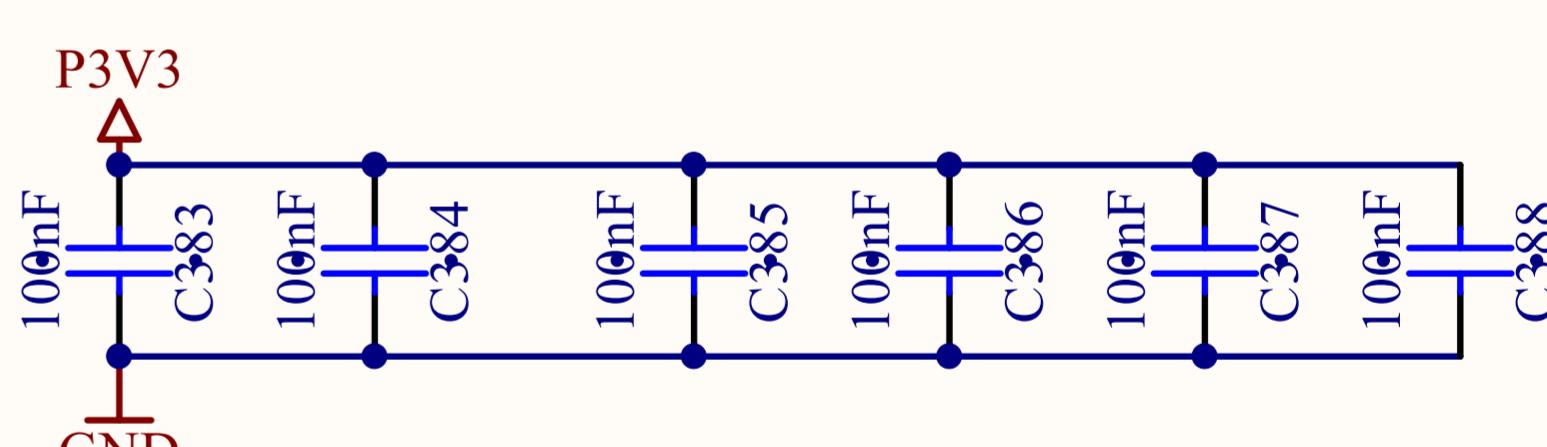
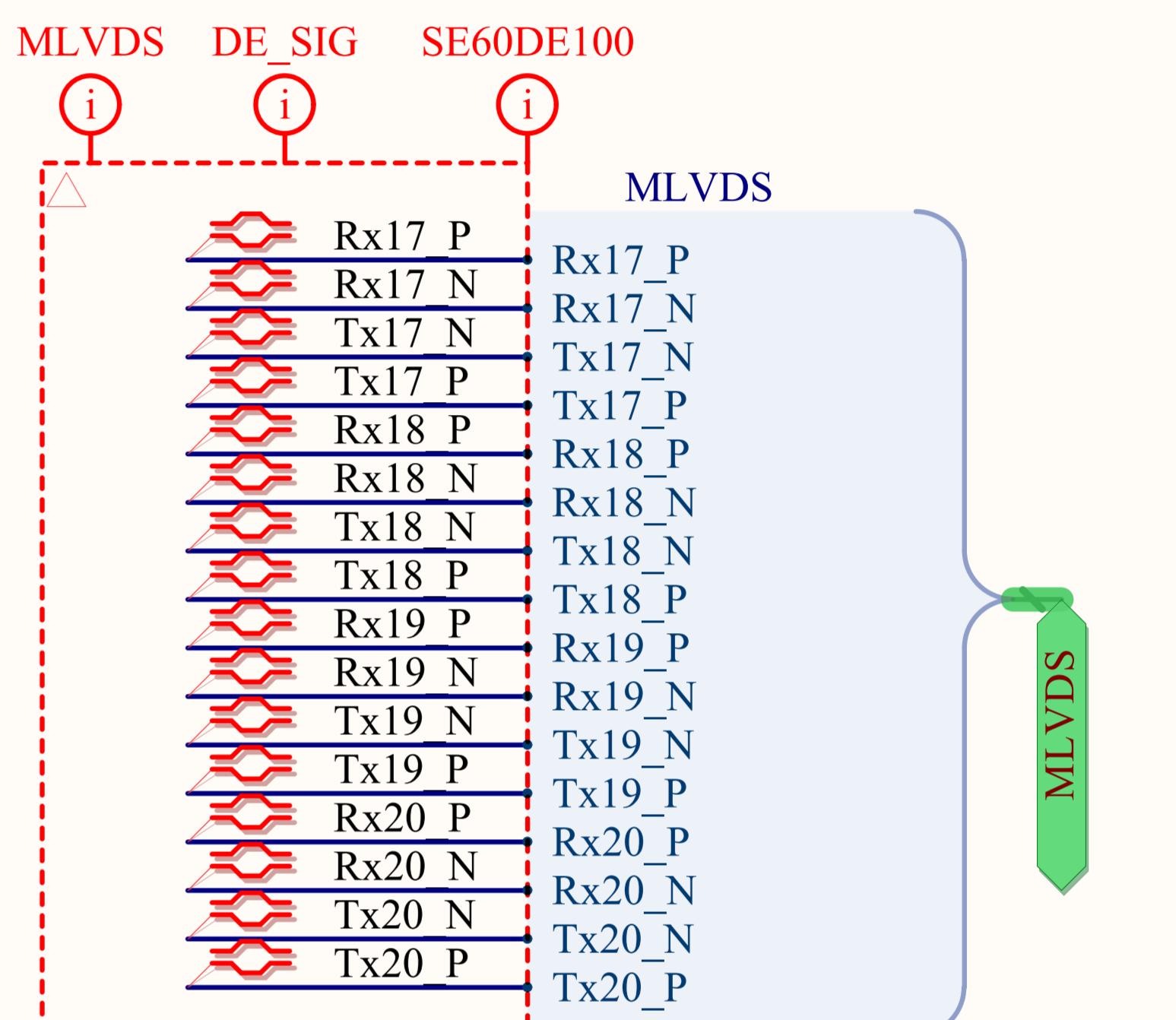
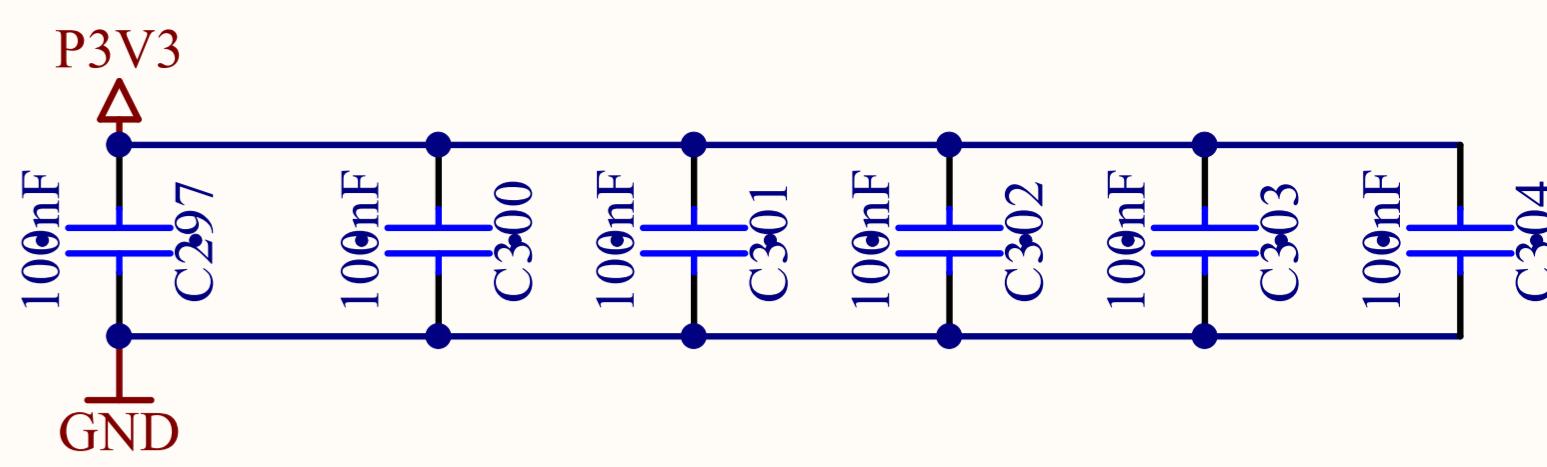
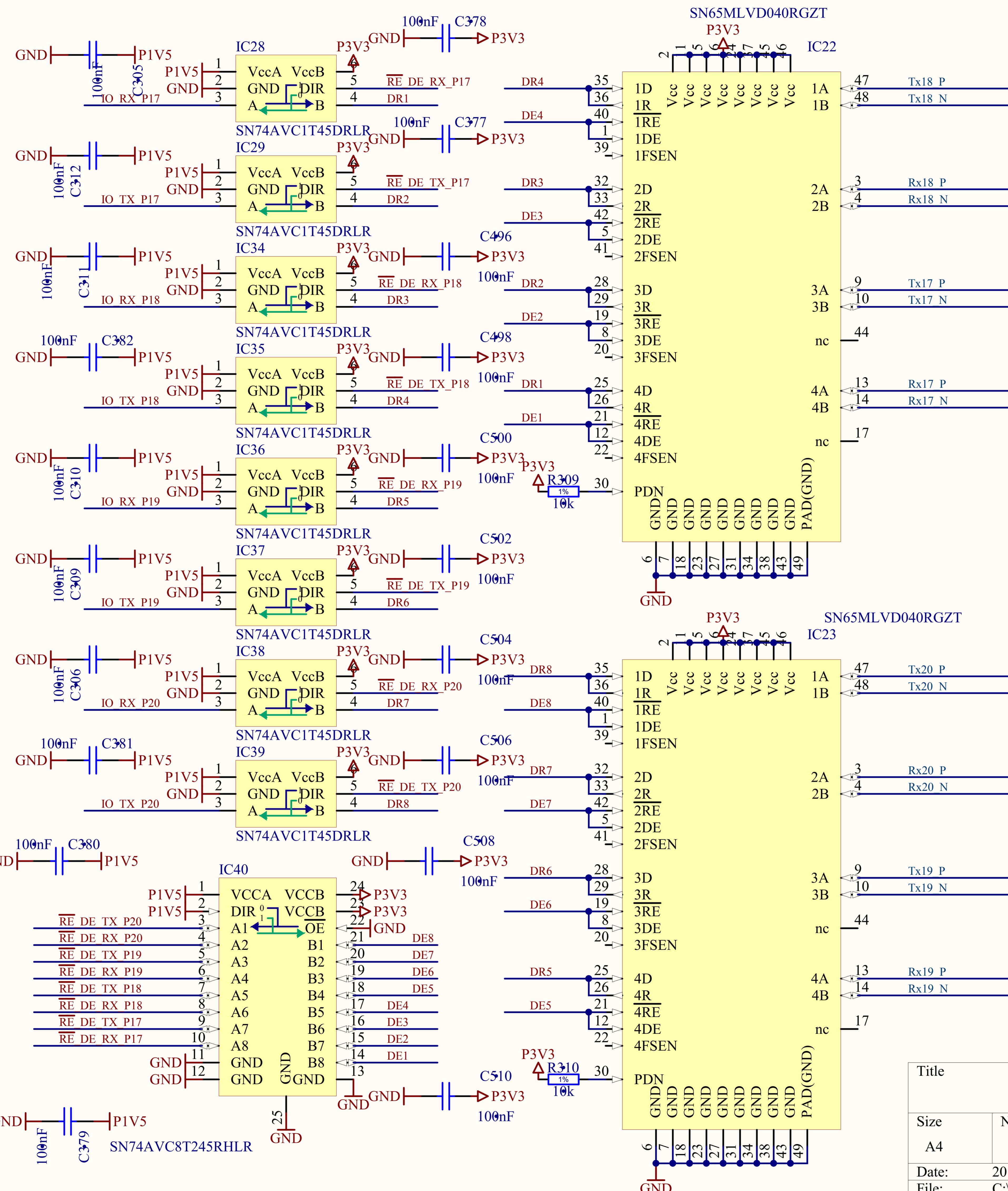
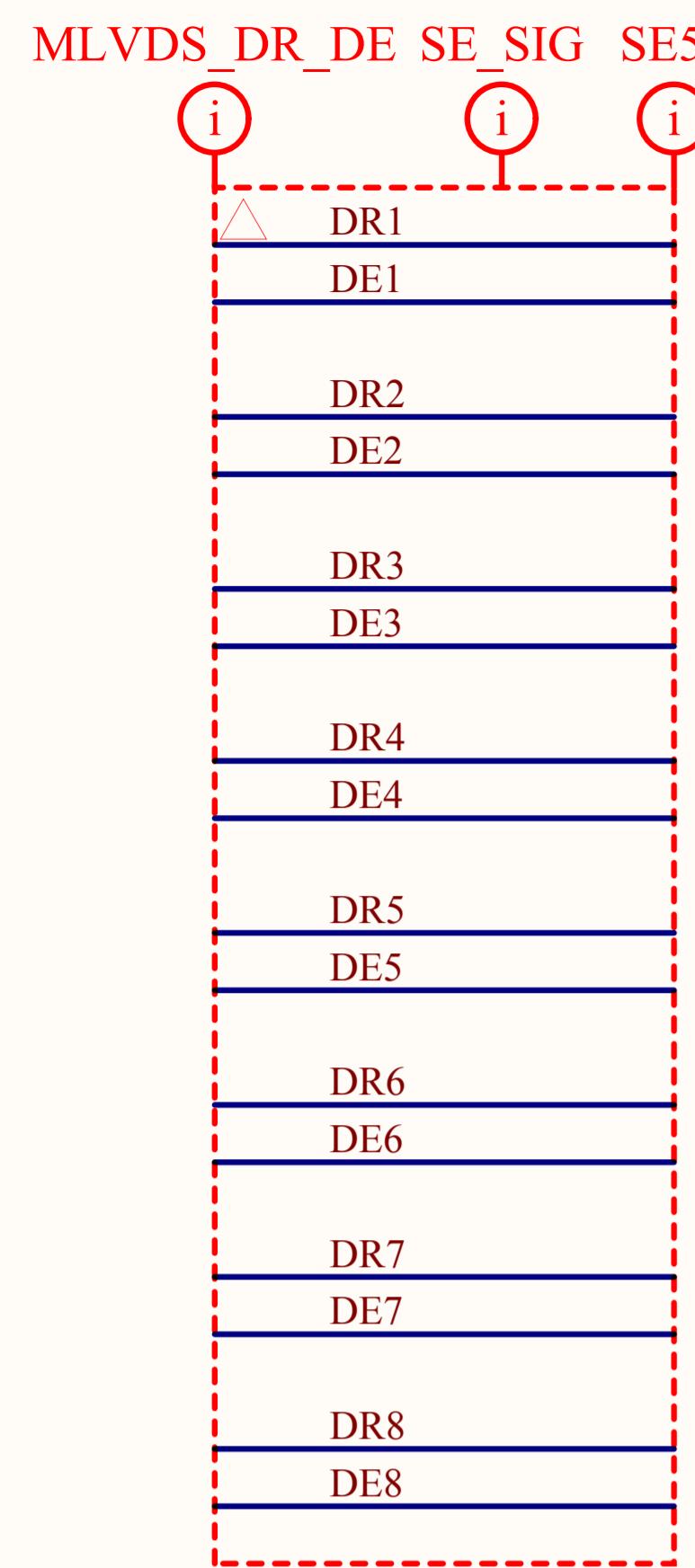
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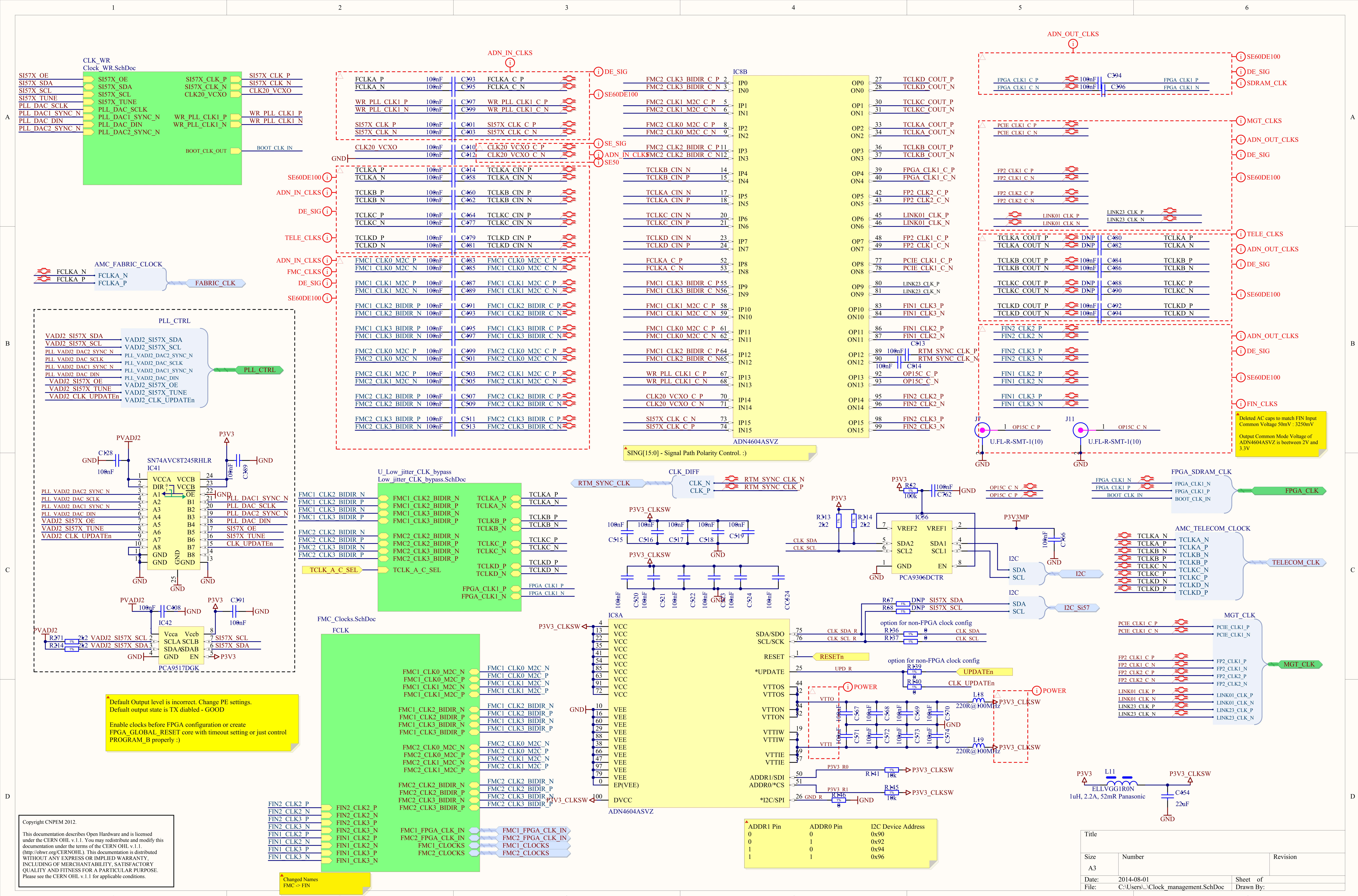




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
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File:	C:\Users\..\M-LVDS PHY.SchDoc	Drawn By:



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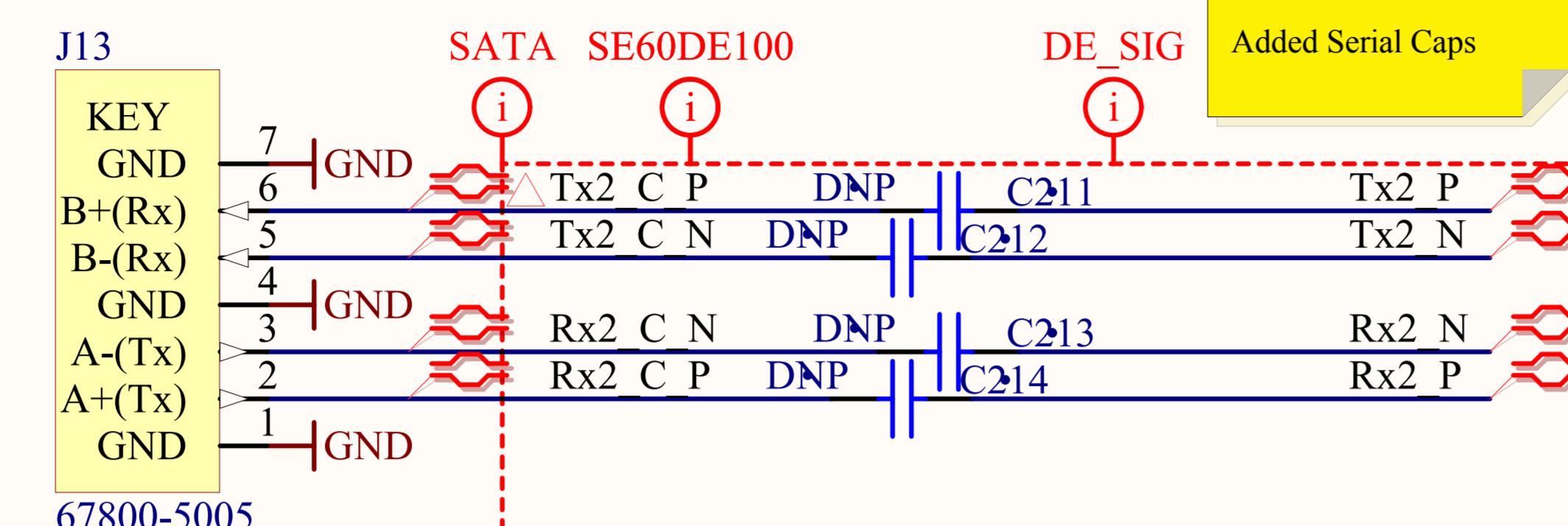


SATA naming is relative to HOST

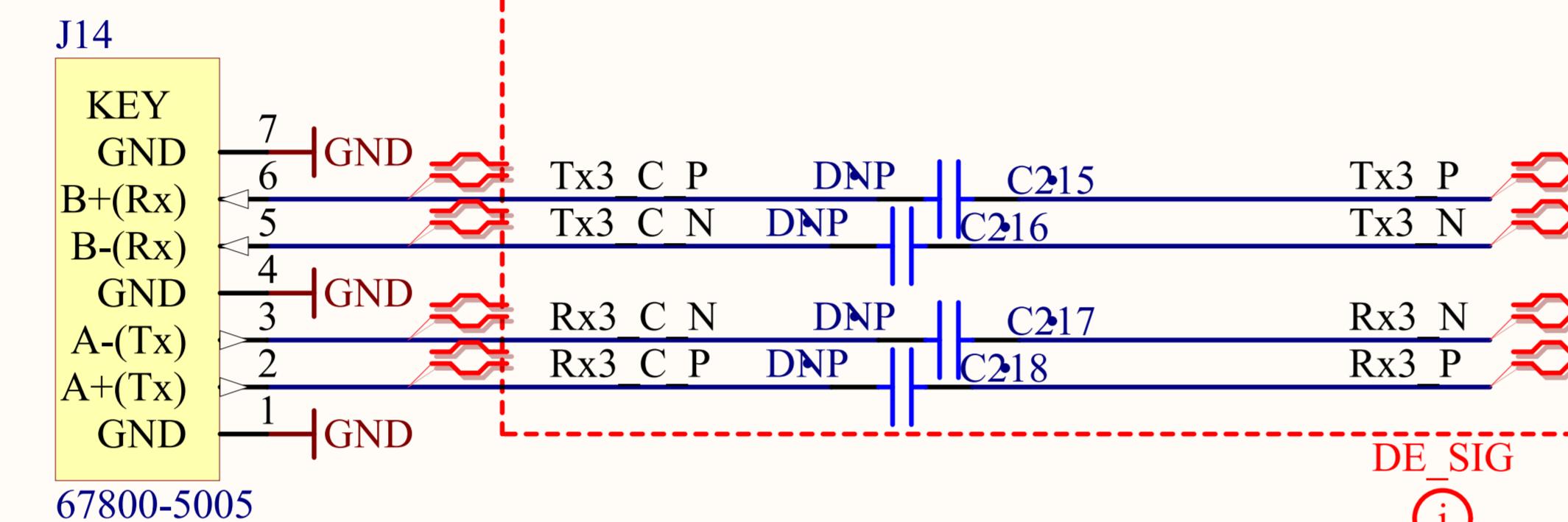
For normal SATA cables apply:

B = HOST SATA RX

A = HOST SATA TX



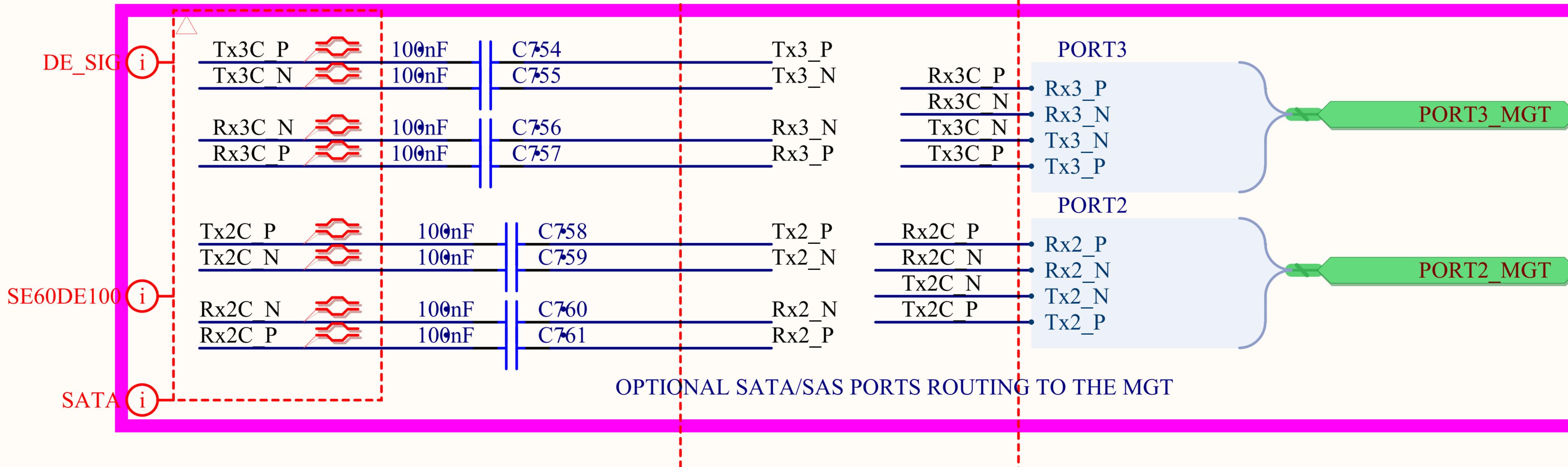
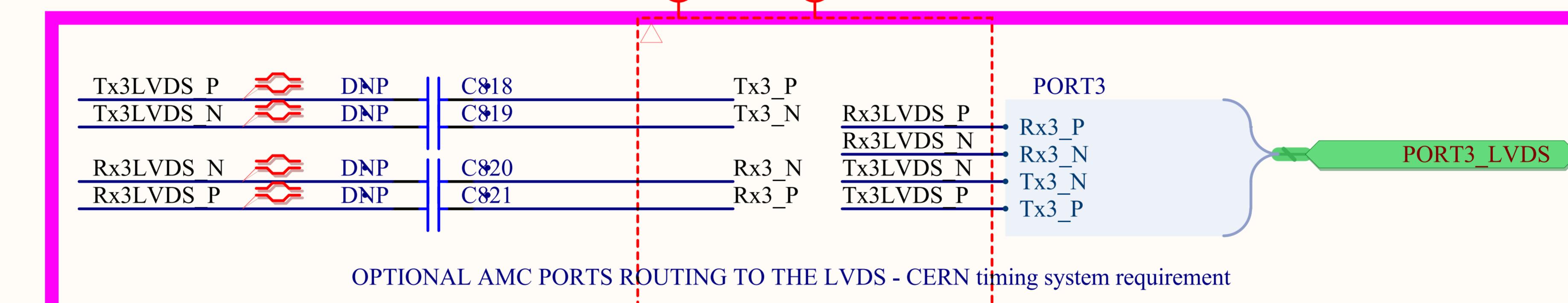
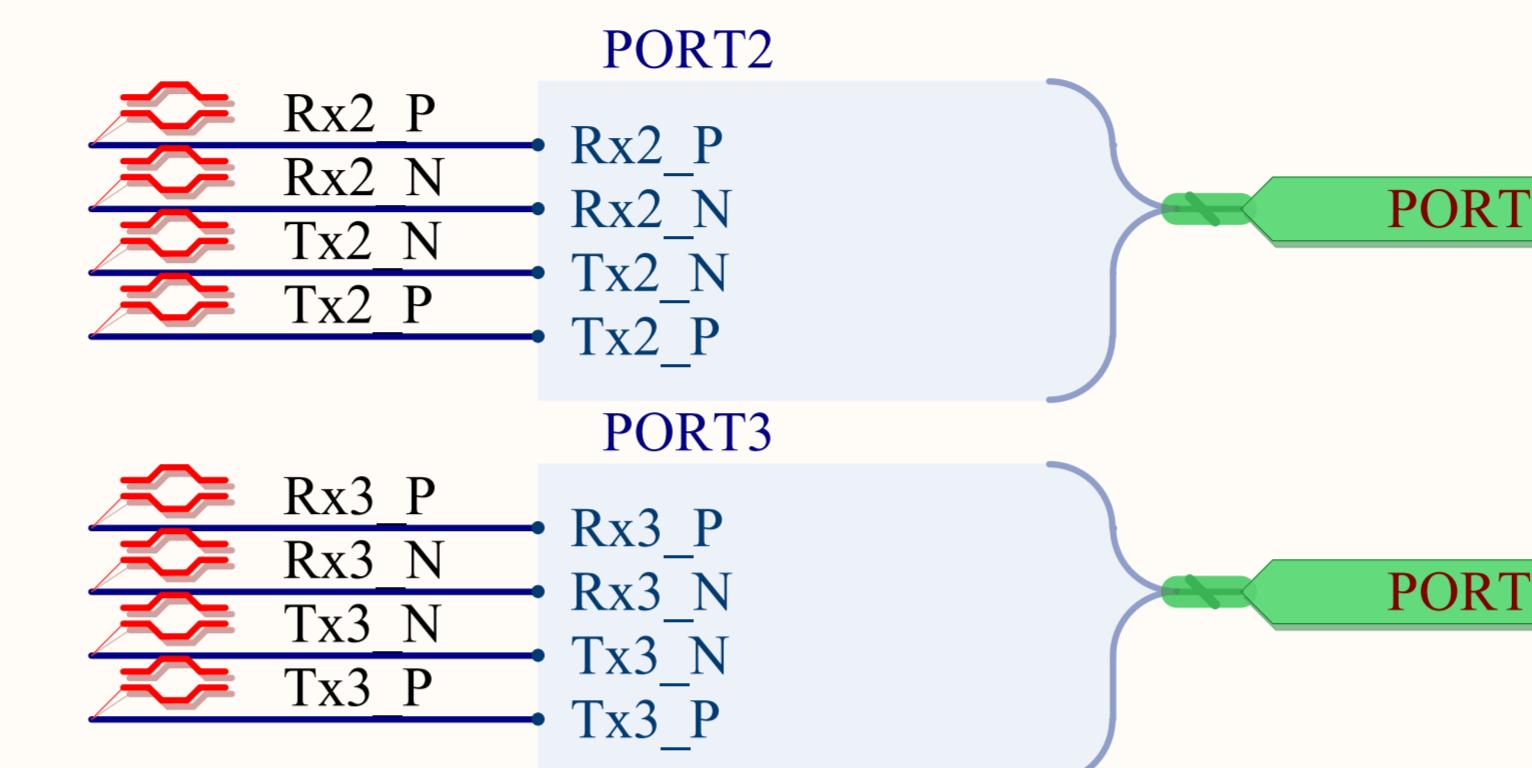
There also Exist a Cross-Over SATA Cable so always there is a possibility to change that



Apply to all AMC ports: see table 6-1 PICMG AMC.0 R2.0 1.5.11.2006

RXes are CARRIER-OUTPUT

TXes are CARRIER-INPUT



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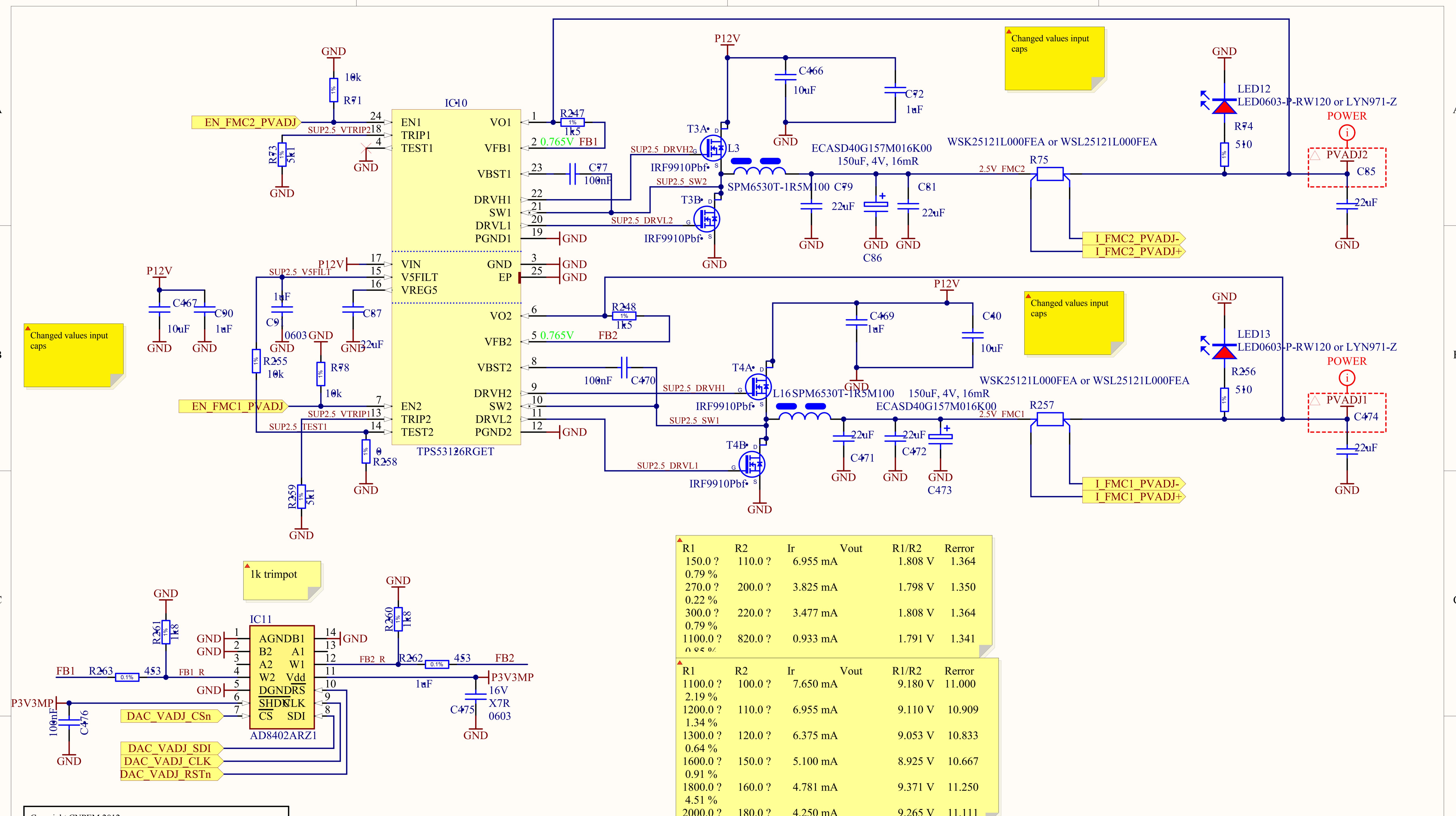
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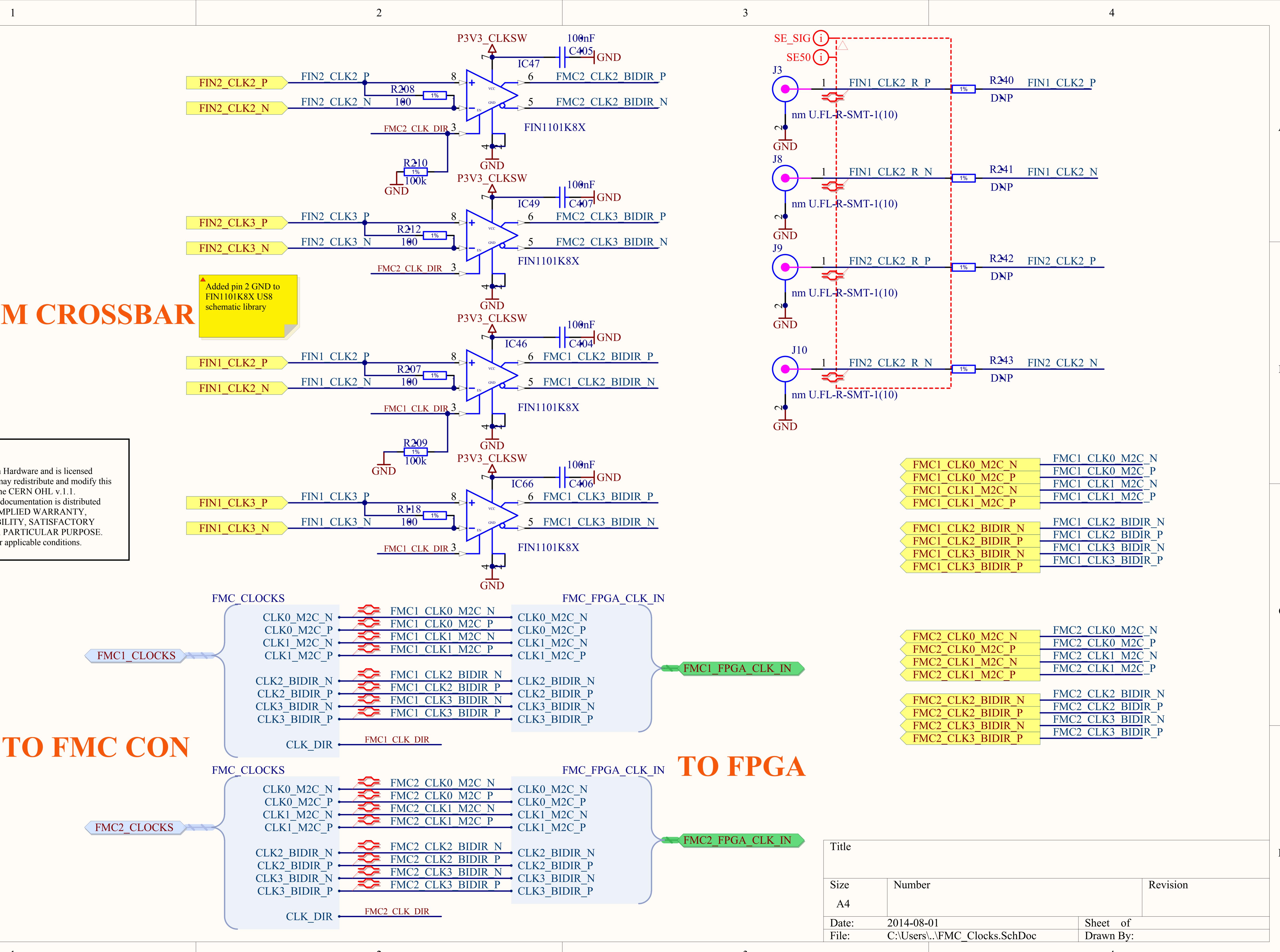
Date: 2014-08-01

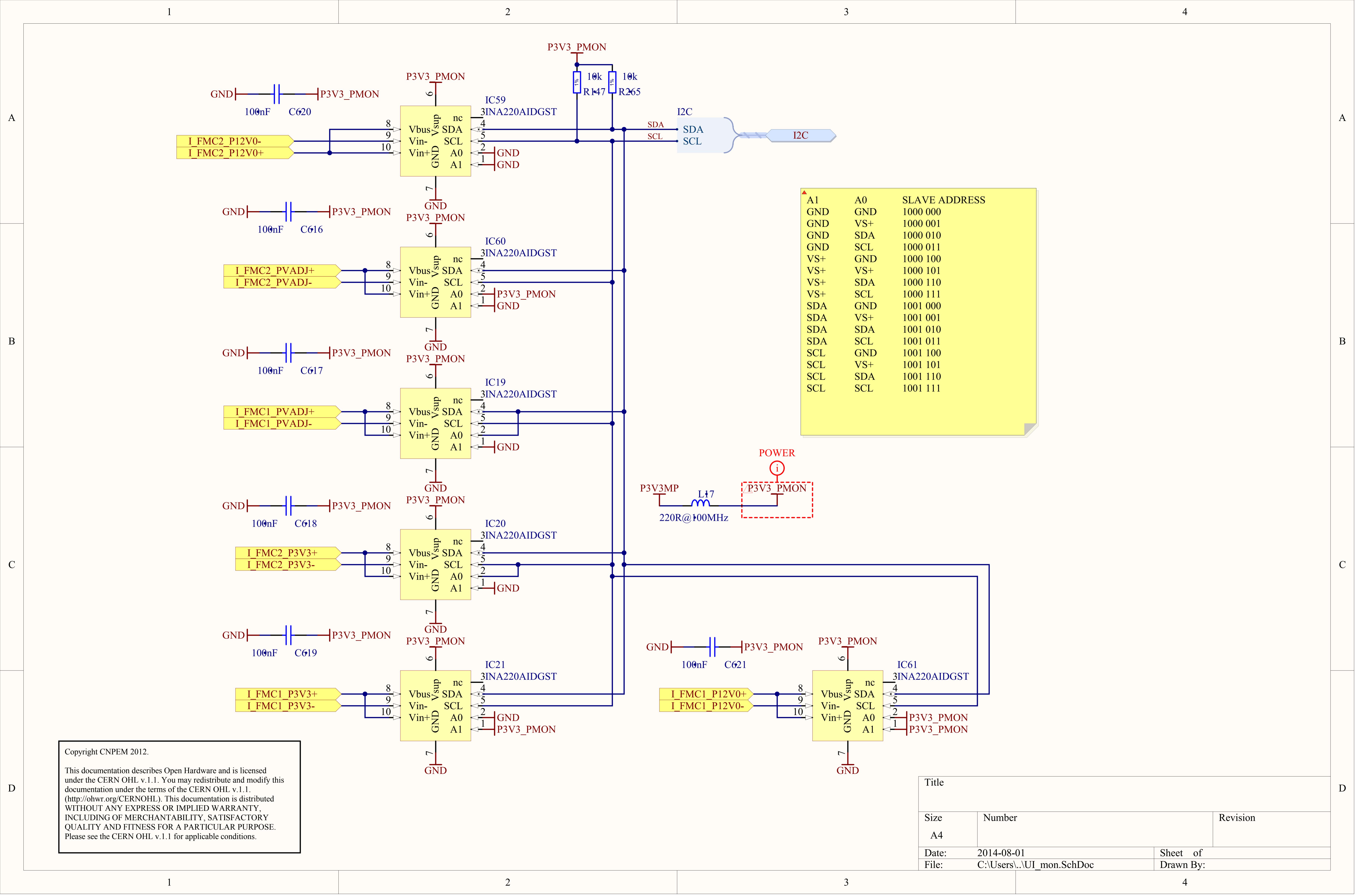
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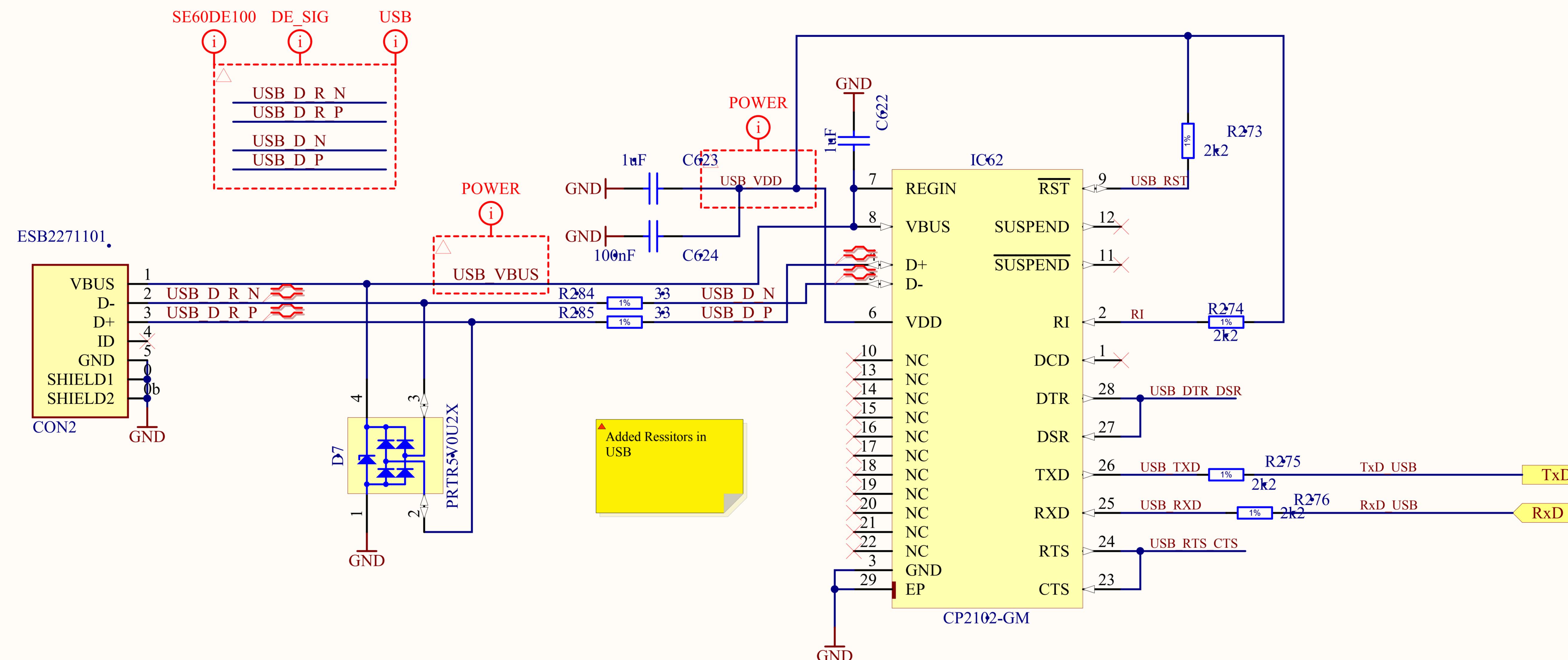






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A



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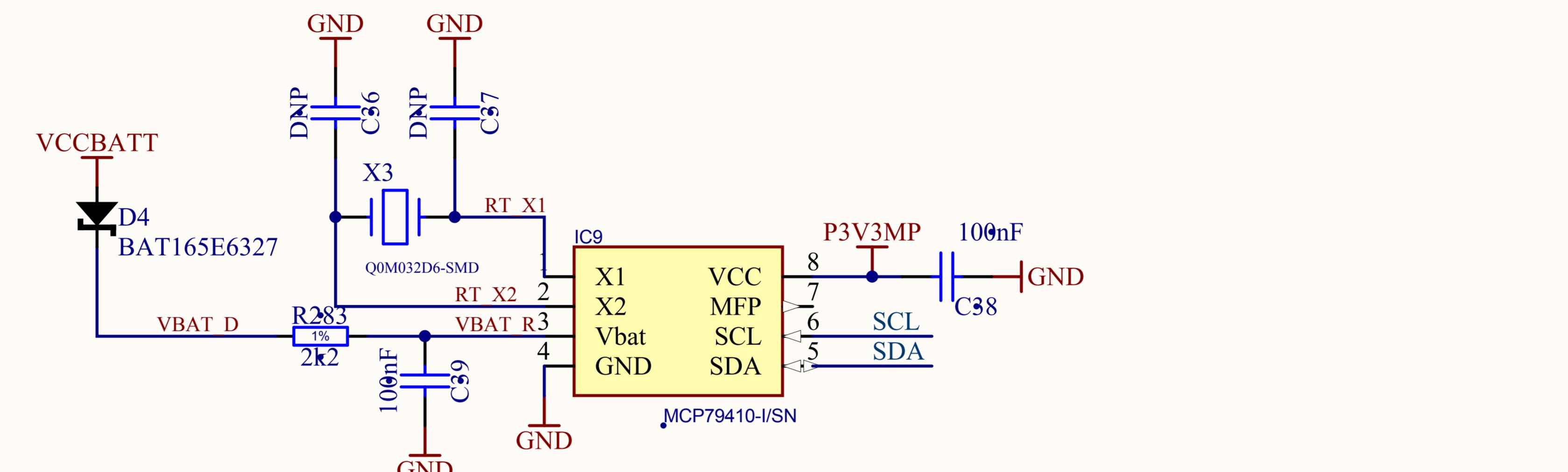
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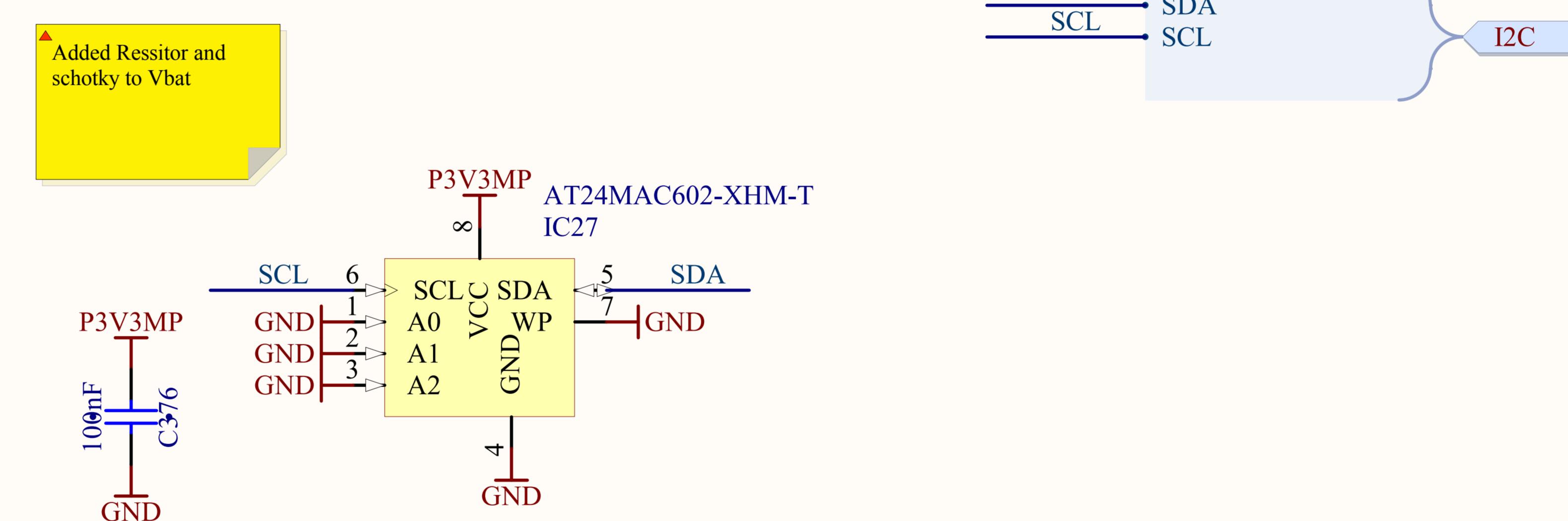
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Drawn By:

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B



C

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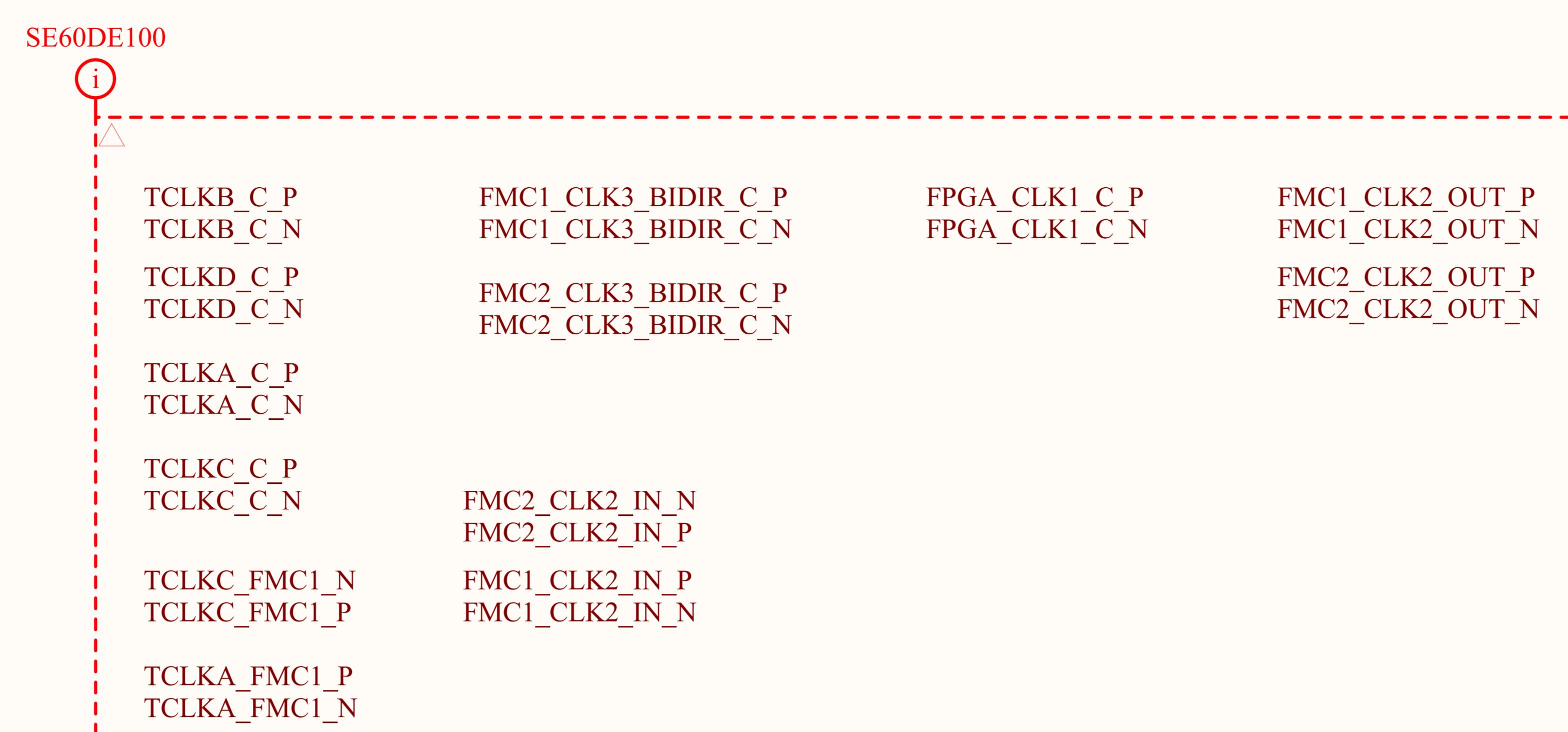
A

B


C

D

A



B



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