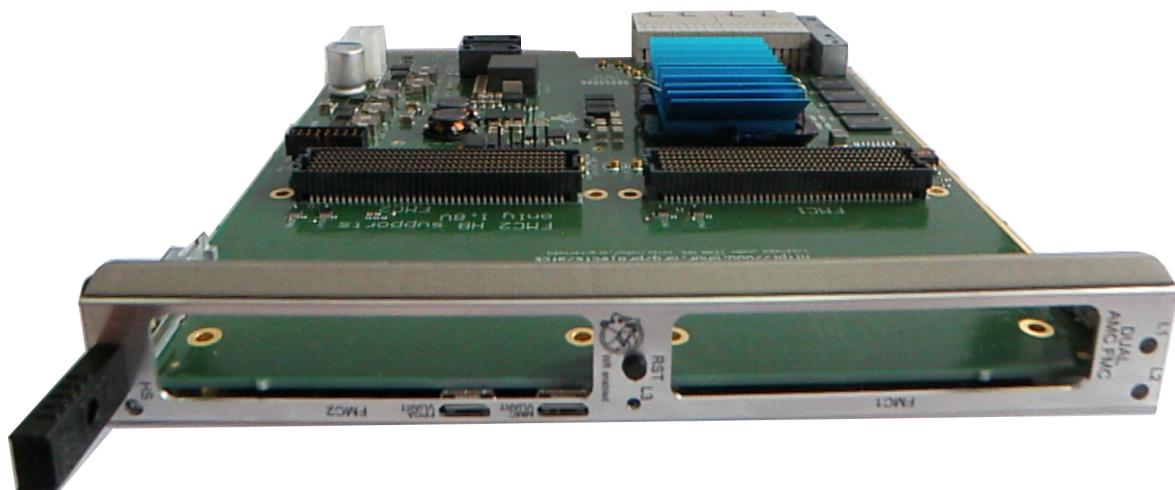


AMC FMC CARRIER - AFC
• Datasheet



v3.1(09.2015)

Document version:	1.0
Issue Date:	September 14, 2015
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Document title:	AFC - Datasheet

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1 Project description

The AMC FMC carrier is partially based on SPEC (supply, WR clocks) design. It was primary designed to support quad 16 bit ADC FMC boards for BPM back-end. Among many features, the card has very flexible clock circuit that enables any clock source to be connected to any clock input, including telecom clock, FMC clocks and FPGA.

2 Functional specifications

Programmable resources:

- Xilinx Artix-7 200T FFG1156 FPGA
- MMC: LPC1764FBD100, optionally Atxmega128A1U-AU

Memory:

- 2GB (16Gbit) DDR3 SDRAM (32-bit interface), 800MHz (clock)
- SPI Flash for FPGA configuration. Accessible by MMC
- SPI Flash for user data storage
- EEPROM with MAC and unique ID

Connectivity:

- 2 high pin count (HPC) slots for 2 single width mezzanines or 1 double width mezzanine
- Mini-USB connected to the MMC processor
- Mini-USB UART connected to FPGA or MMC
- Mini-USB connected to the IPMI processor
- Stand-alone power connector (12V, 3.3V aux)
- SATA connector for Port2, Port3 with possibility of switching to FPGA GTP
- GTP connected to FMC1 (x4), FMC2(x4), FP1(x4), FP2(x4), Port0, Port1, RTM(x8), selected by capacitor placement
- RTM connector with 8 GTP routed to it. Compatible with rtm-sfp8 module

Supply:

- Monitoring of voltage and Power supply for FPGA, memory, FMCs - programmable VADJ 1.8-3.3V (independent for each FMC)
- Current of all FMC buses
- Stand-alone power connector

Clocking:

- Clock distribution circuit compatible with White Rabbit
- Clock crossbar, 16 inputs x 16 outputs

Other:

- Temperature, voltage and current monitoring for critical power buses
- Temperature monitoring: FMC1, FMC2, supply, FPGA core, DDR memory
- JTAG multiplexer (SCANSTA) for FMC access, local JTAG port and remote debug/Chipscope via Ethernet

3 Product view

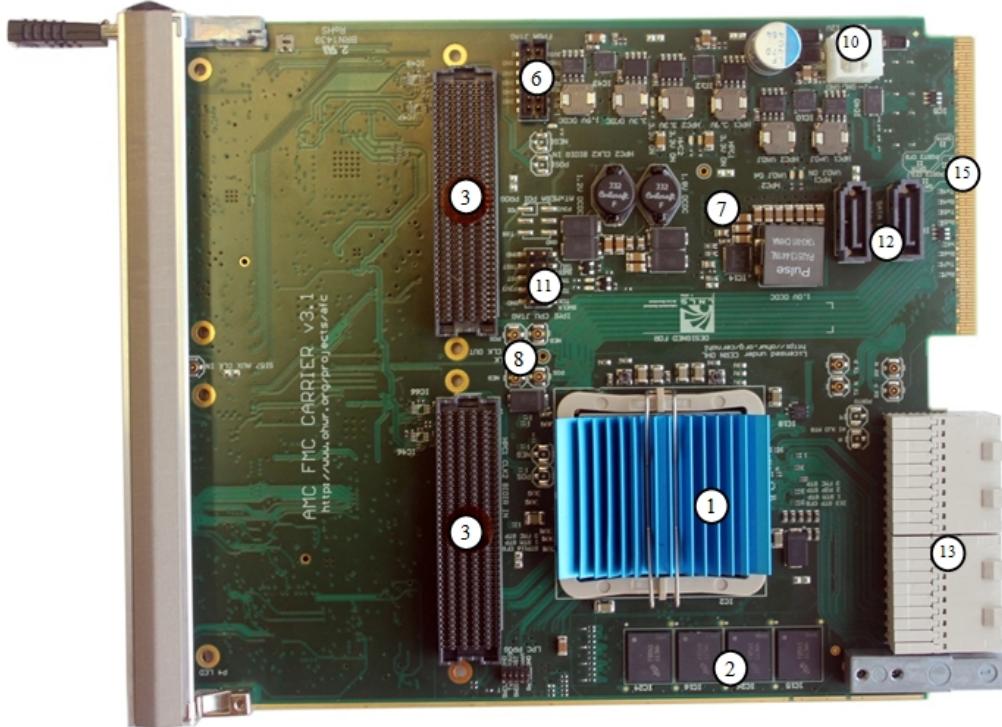


Figure 1: Top view

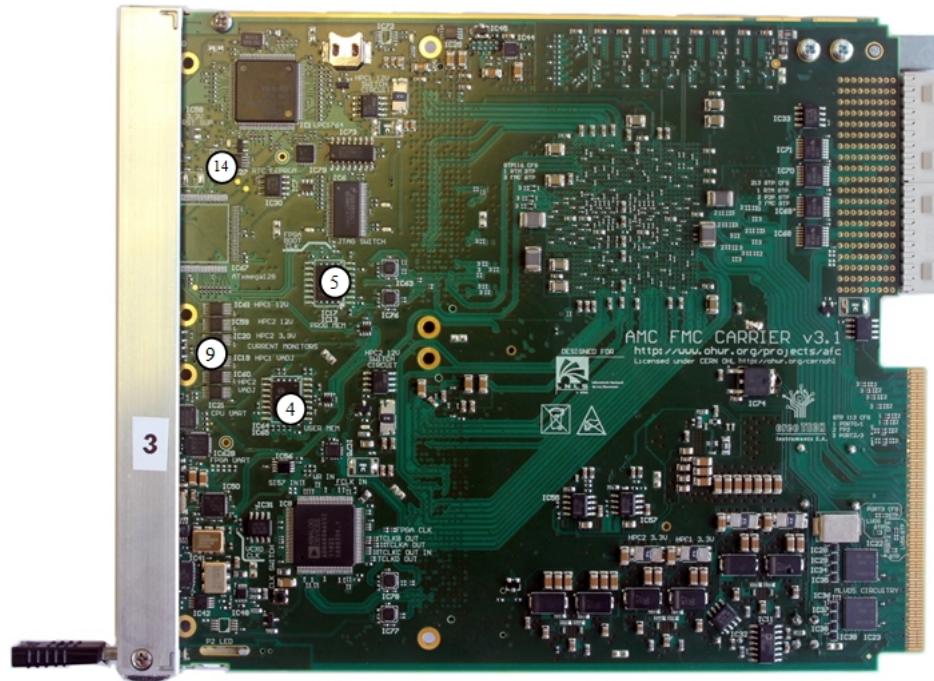


Figure 2: Bottom view

Callout	Component Description
1	Xilinx Artix-7 200T FFG1156 FPGA
2	2 GB DDR3 SDRAM (32-bit interface)
3	2 high pin count (HPC) slots for 2 single width mezzanines or 1 double width mezzanine
4	SPI Flash for FPGA configuration
5	SPI Flash for user data storage
6	JTAG multiplexer (SCANSTA) for FMC access
7	Power supply for FPGA, memory, FMCs - programmable VADJ 1.8-3.3V
8	Clock distribution circuit compatible with WR
9	Temperature, voltage and current monitoring for critical power buses
10	Stand-alone power connector
11	JTAG connected to the IPMI processor
12	SATA connector for Port2, Port3 with possibility of switching to FPGA MGT
13	MGT connected to FMC1, FMC2, Fat Pipe 1, Fat Pipe 2 (optional), Port0, Port1, Port2 (optional), Port3 (optional), RTM (optional)
14	EEPROM with MAC and unique ID
15	RTM connector with 8 GTP routed to it. Compatible with RTM-SFP8 module

4 Routing

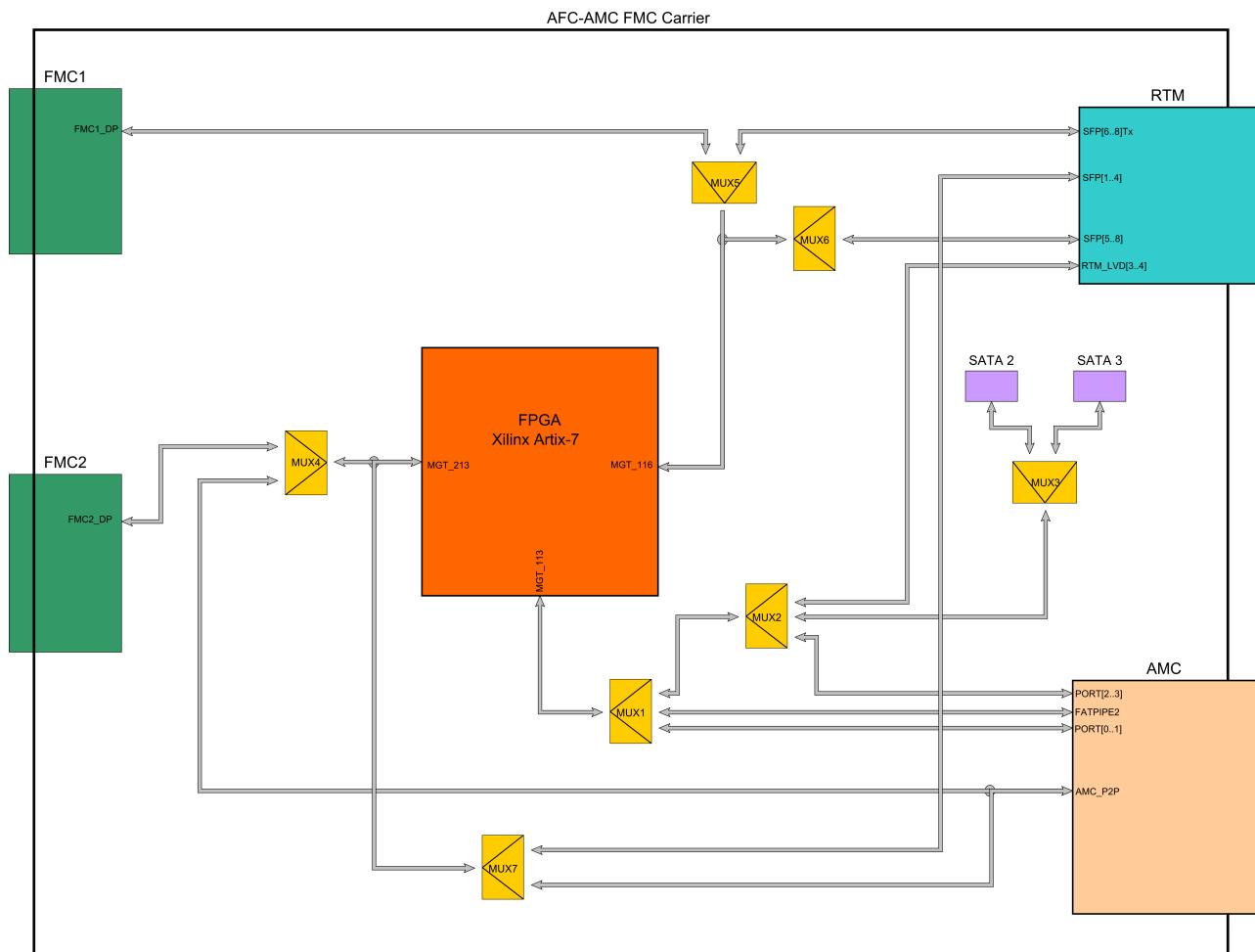


Figure 3: Block scheme

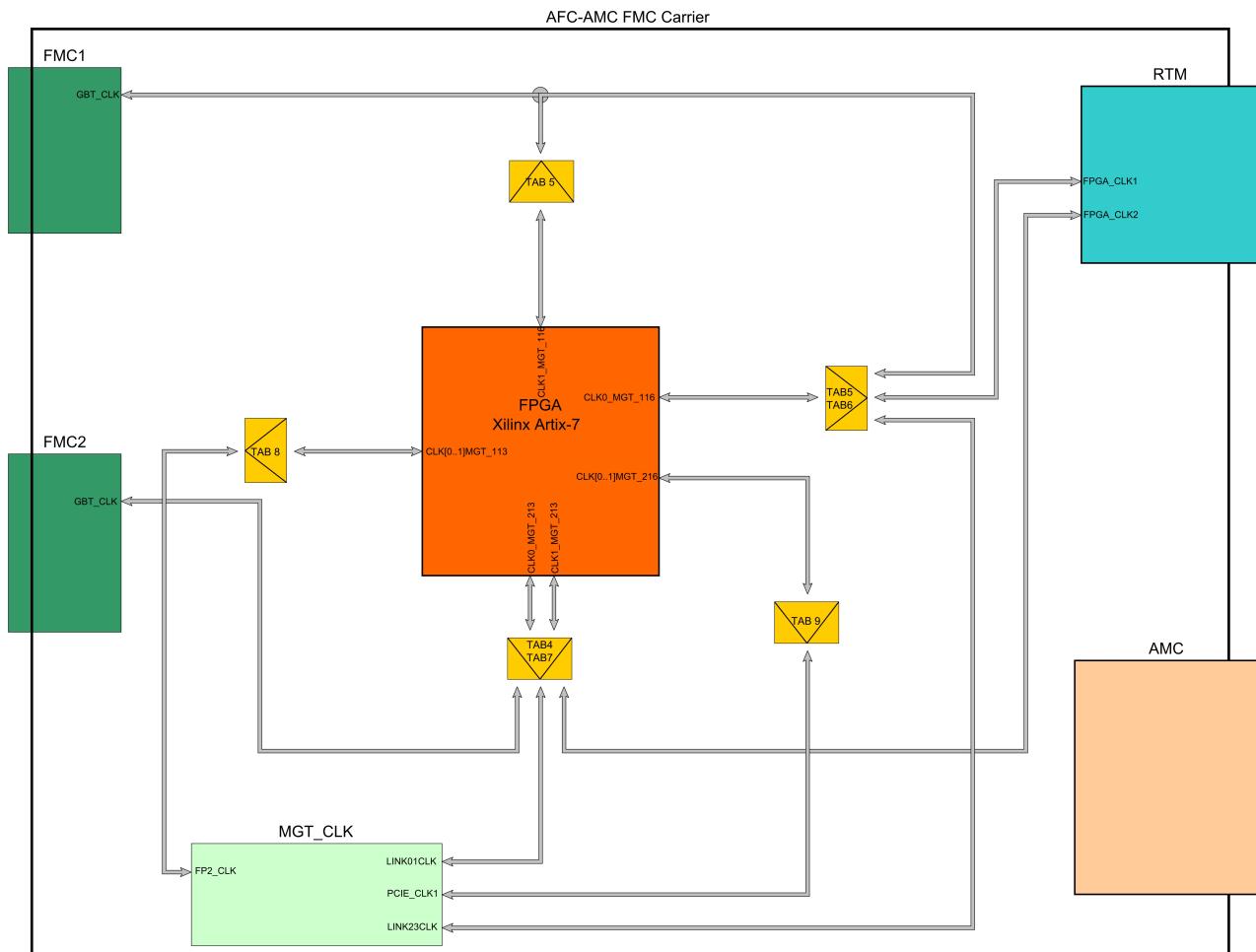


Figure 4: CLK block scheme

Each MUX is multi/demultiplexer and allows to connect FPGA with respective connector, and point to respective tab in 4.1 section.

4.1 Options

This section describes selection options with capacitors and major connections. Image below shows sections on the board where mounting pads are located.

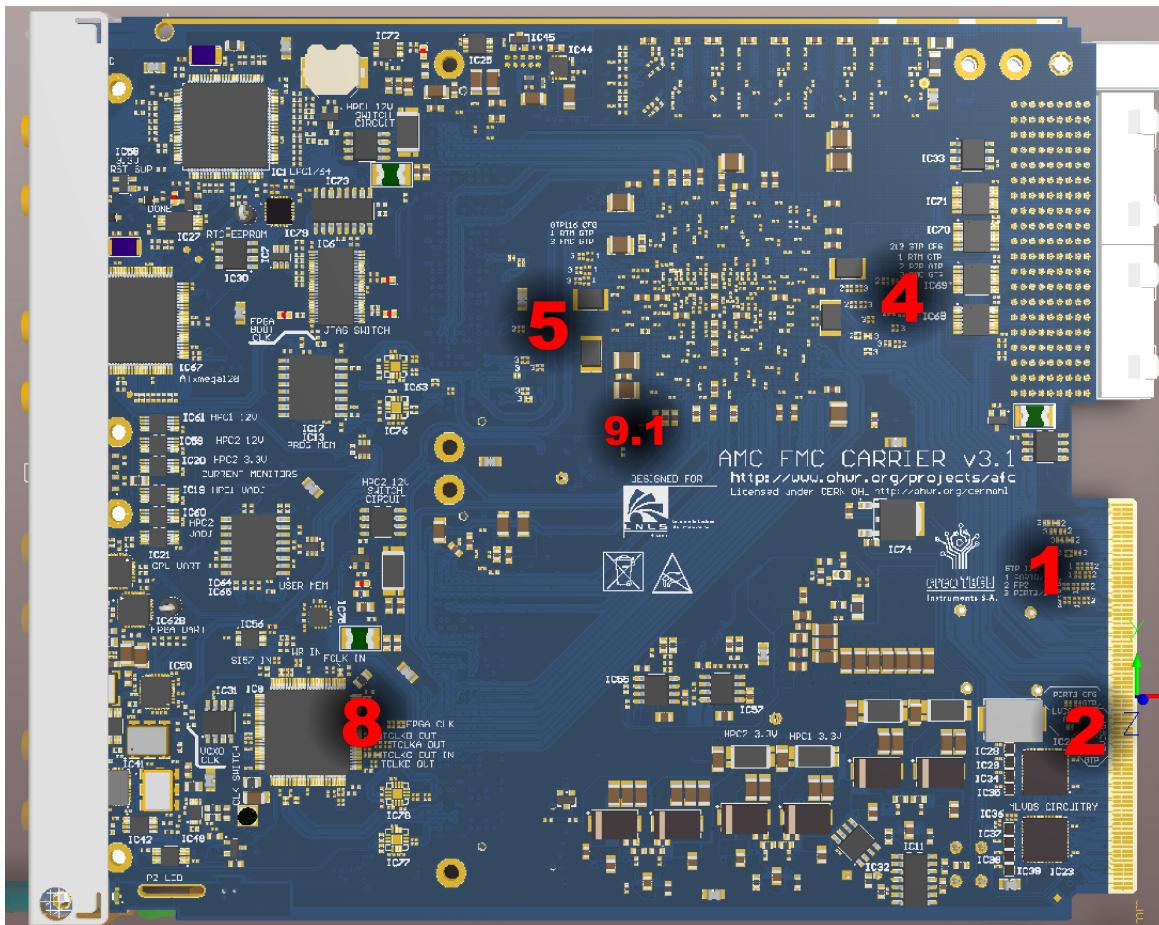


Figure 5: Top side

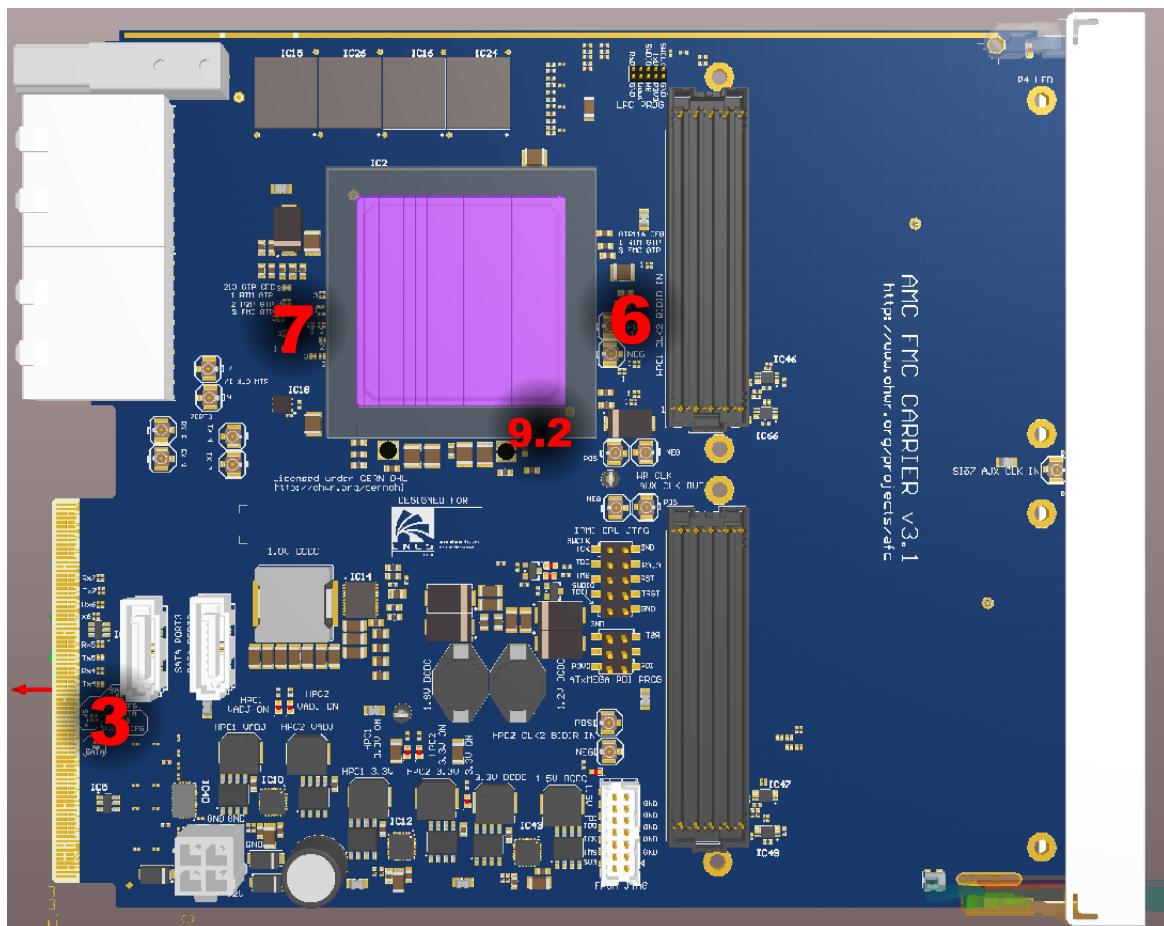


Figure 6: Bottom side

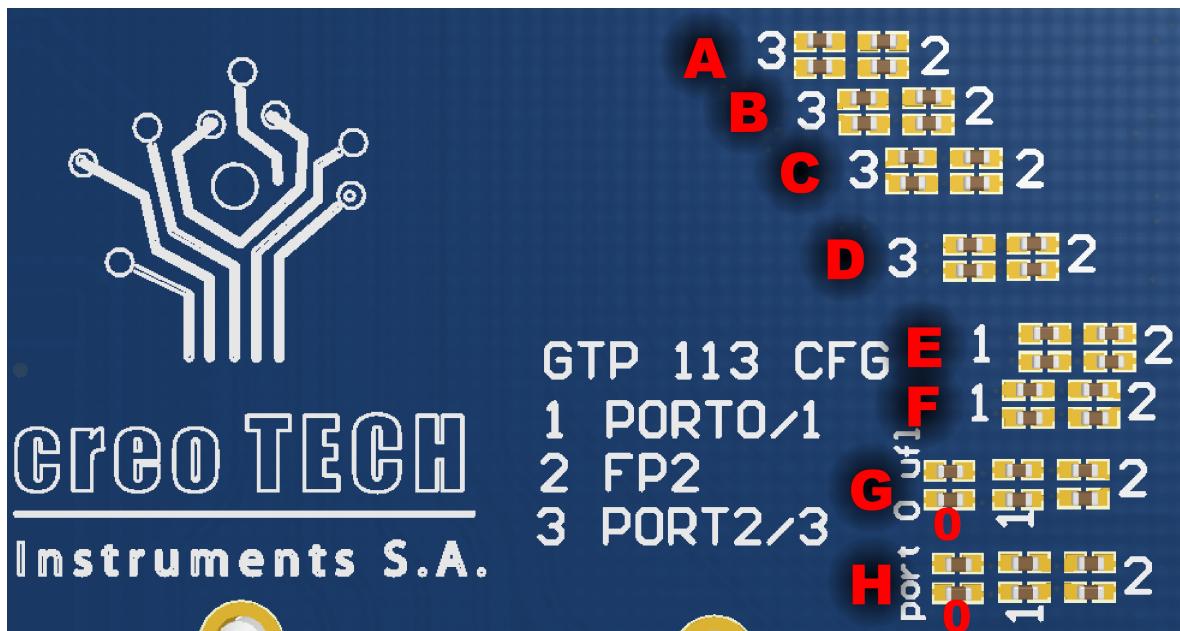


Image 1

Table 1

symbol on Image 1	FPGA MGT P/N signal(ball)	Mounted pair of capacitors			
		0	1	2	3
A	PRXP0_113 (AJ17) PRXN0_113 (AK17)			FATPIPE2 RX8 AMC 88 (P) AMC 87 (N)	look at Table 2
B	PTXP0_113 (AN17) PTXN0_113 (AP17)			FATPIPE2 TX8 AMC (P) 91 AMC (N) 90	look at Table 2
C	PRXP1_113 (AL16) PRXN1_113 (AM16)			FATPIPE2 RX9 AMC (P) 94 AMC (N) 93	look at Table 2
D	PTXP1_113 (AN15) PTXN1_113 (AP15)			FATPIPE2 TX9 AMC (P) 97 AMC (N) 96	look at Table 2
E	PRXP2_113 (AJ15) PRXN2_113 (AK15)		PORT1 RX1 AMC (P) 23 AMC (N) 24	FATPIPE2 RX10 AMC (P) 100 AMC (N) 99	
F	PTXP2_113 (AL14) PTXN2_113 (AM14)		PORT1 TX1 AMC (P) 20 AMC (N) 21	FATPIPE2 TX10 AMC (P) 103 AMC (N) 102	
G	PRXP3_113 (AJ13) PRXN3_113 (AK13)	PORT0 RX0 UFL-J18(P) UFL-J19(N)	PORT0 RX0 AMC (P) 14 AMC (N) 15	FATPIPE2 RX11 AMC (P) 106 AMC (N) 105	
H	PTXP3_113 (AN13) PTXN3_113 (AP13)	PORT0 TX0 UFL-J21(P) UFL-J20(N)	PORT0 TX0 AMC (P) 11 AMC (N) 12	FATPIPE2 TX11 AMC (P) 109 AMC (N) 108	

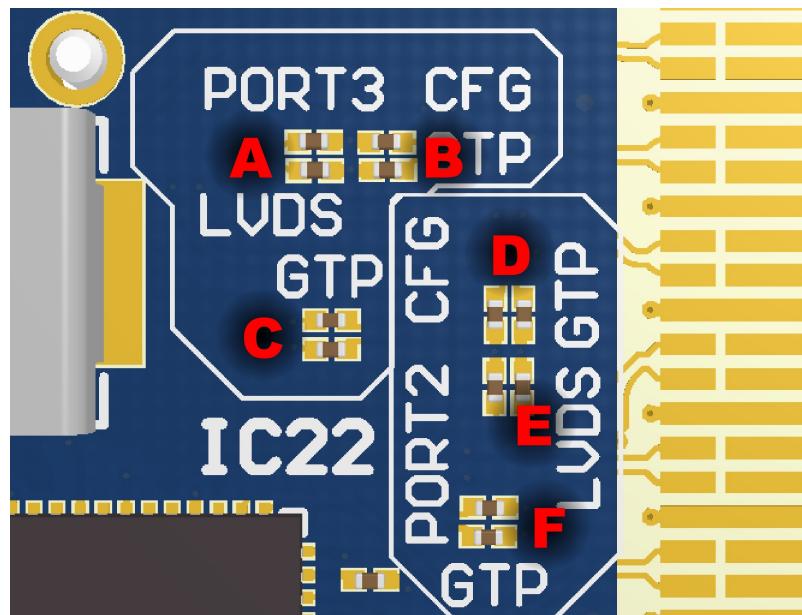


Image 2

Table 2

Mounted capacitors on Image 2	connection		Mount
A	PORT3 RX3	RTM_LVD3 IO_L1P_T0_36 (L12) (P) IO_L1N_T0_36 (K12) (N)	
B	PORT3 RX3	AMC 38 (P) AMC 39 (N)	A3 capacitors shown on Image 1
C	PORT2 RX2	AMC 32 (P) AMC 33 (N)	C3 capacitors shown on Image 1
D	PORT3 TX3	AMC 35 (P) AMC 36 (N)	B3 capacitors shown on Image 1
E	PORT3 TX3	RTM_LVD4 IO_L4P_T0_36 (H11) (P) IO_L4N_T0_36 (G11) (N)	
F	PORT2 TX2	AMC 29 (P) AMC 30 (N)	D3 capacitors shown on Image 1

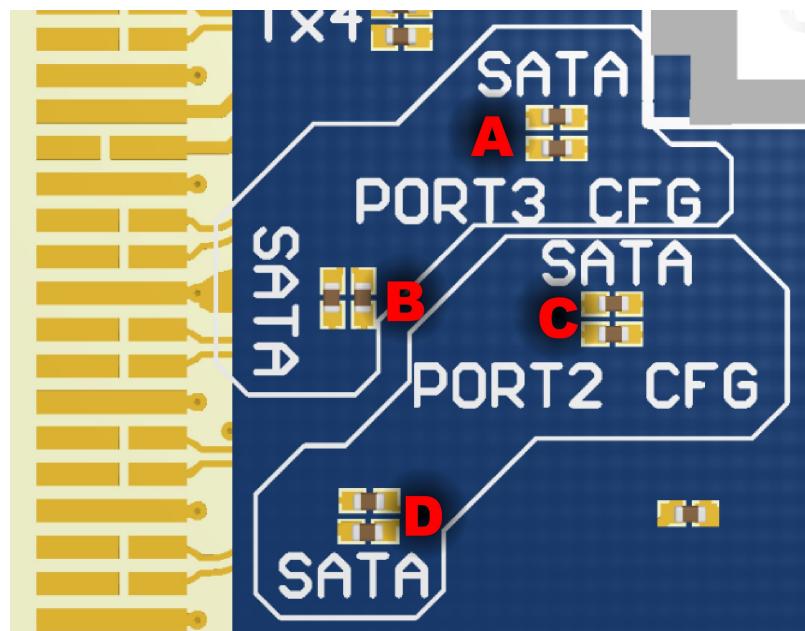


Image 3

Table 3

symbol on Image 12	connection	
A	PORT3 RX3	SATA 3 TX
B	PORT3 TX3	SATA 3 RX
C	PORT2 RX2	SATA 2 TX
D	PORT2 TX2	SATA2 RX

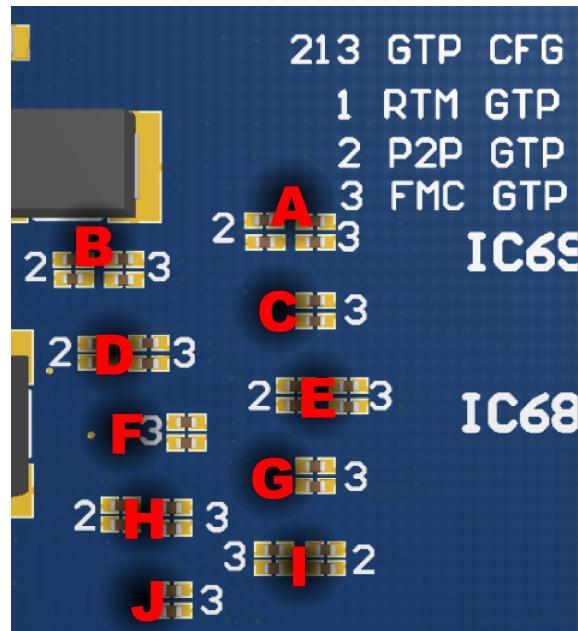


Image 4

Table 4

symbol on Image 4	FPGA MGT P/N signal (ball)	Mounted pair of capacitors	
		2	3
A	PTXP0_213 (AN19) PTXN0_213 (AP19)	AMC_P2P TX12 AMC (P) 115 AMC (N) 114	FMC2_DP0_C2M FMC C2 (P) FMC C3 (N)
B	PRXP1_213 (AJ19) PRXN1_213 (AK19)	AMC_P2P RX14 AMC (P) 124 AMC (N) 123	FMC2_DP1_M2C FMC A2 (P) FMC A3 (N)
C	REFCLK0P_213 (AG20) REFCLK0N_213 (AH20)		FMC2_GBTCLK0_M2C FMC D4 (P) FMC D5 (N)
D	PRXP0_213 (AL18) PRXN0_213 (AM18)	AMC_P2P RX12 AMC (P) 112 AMC (N) 111	FMC2_DP0_M2C FMC C6 (P) FMC C7 (N)
E	PRXP2_213 (AL20) PRXN2_213 (AM20)	AMC_P2P RX13 AMC (P) 118 AMC (N) 117	FMC2_DP2_M2C FMC A6 (P) FMC A7 (N)
F	PRXP3_213 (AJ21) PRXP3_213 (AK21)	AMC_P2P RX15 AMC (P) 130 AMC (N) 129	FMC2_DP3_M2C FMC A10 (P) FMC A11 (N)
G	REFCLK1P_213 (AG18) REFCLK1N_213 (AH18)		FMC2_GBTCLK1_M2C FMC B20 (P) FMC B21 (N)
H	PTXP1_213 (AN21) PTXN1_213 (AP21)	AMC_P2P TX14 AMC (P) 127	FMC2_DP1_C2M FMC A22 (P)

		AMC (N) 126	FMC A23 (N)
I	PTXP2_213 (AL22) PTXN2_213 (AM22)	AMC_P2P TX13 AMC (P) 121 AMC (N) 120	FMC2_DP2_C2M FMC A26 (P) FMC A27 (N)
J	PTXP3_213 (AN23) PTXN3_213 (AP23)		FMC2_DP3_C2M FMC A30 (P) FMC A31 (N)

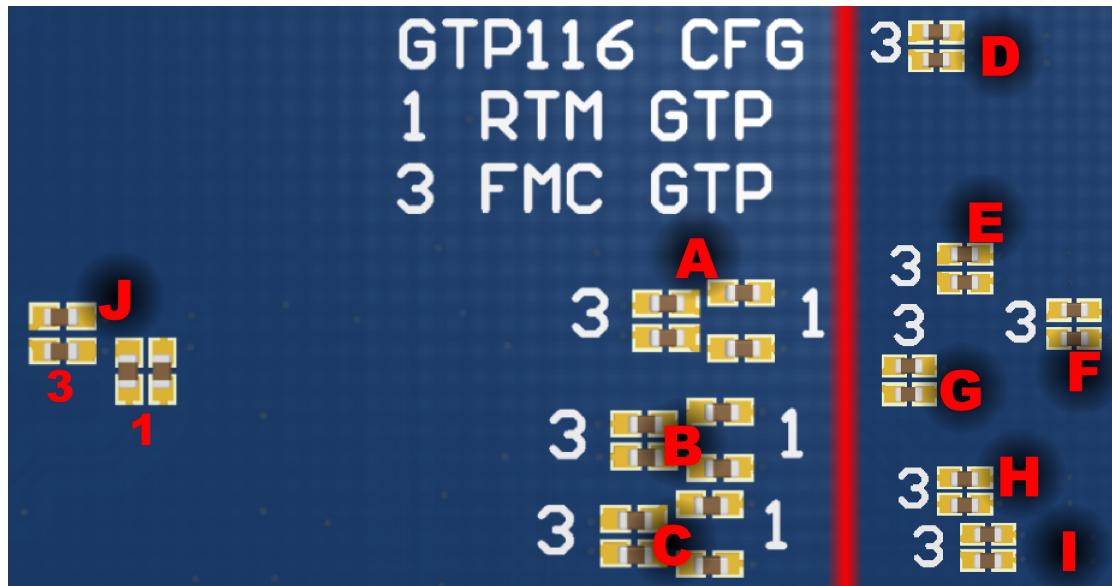


Image 5

Table 5

symbol on Image 5	FPGA MGT P/N signal (ball)	Mounted pair of capacitors	
		1	3
A	PTXP0_116 (B13) PTXN0_116 (A13)	SFP6TX RTM E5 (P) RTM F5 (N)	FMC1_DP3_C2M FMC A30 (P) FMC A31 (N)
B	PTXP1_116 (D14) PTXN1_116 (C14)	SFP7TX RTM E4 (P) RTM F4 (N)	FMC1_DP2_C2M FMC A26 (P) FMC A27 (N)
C	PTXP2_116 (B15) PTXN2_116 (A15)	SFP8TX RTM E3 (P) RTM F3 (N)	FMC1_DP1_C2M FMC A22 (P) FMC A23 (N)
D	PRXP0_116 (F13) PRXN0_116 (E13)		FMC1_DP3_M2C FMC A10 (P) FMC A11 (N)
E	PRXP3_116 (F17) PRXN3_116 (E17)		FMC1_DP0_M2C FMC C6 (P) FMC C7 (N)
F	PRXP1_116 (F15) PRXN1_116 (E15)		FMC1_DP2_M2C FMC A6 (P) FMC A7 (N)
G	REFCLK1P_116 (H14) REFCLK1N_116 (G14)		GBTCLK0_M2C FMC D4 (P) FMC D5 (N)
H	PTXP3_116 (B17) PTXN3_116 (A17)		FMC1_DP0_C2M FMC C2 (P) FMC C3 (N)

I	PRXP2_116 (D16) PRXN2_116 (C16)		FMC1_DP1_M2C FMC A2 (P) FMC A3 (N)
J	REFCLK0P_116 (H16) REFCLK0N_116 (G16)	LINK23_CLK	FMC1_GBTCLK1_M2C FMC B20 (P) FMC B21 (N)

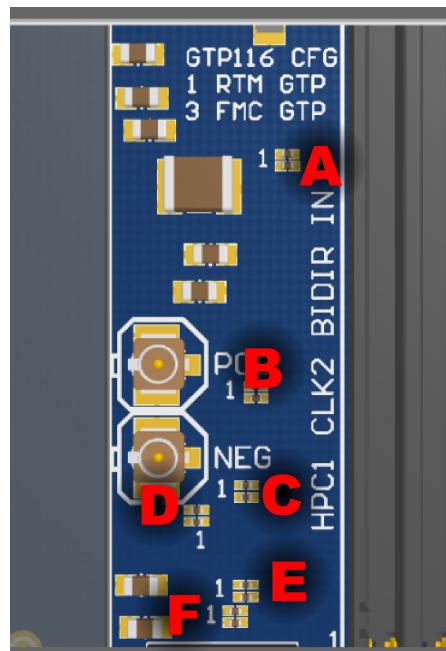


Image 6

Table 6

symbol on Image 6	connection	
A	MGTREFCLK0P_116 (H16) MGTREFCLK0N_116 (G16)	RTM FPGA CLK1
B	MGTPRXP0_116 (F13) MGTPRXN0_116 (E13)	SFP6RX
C	MGTPRXP3_116 (F17) MGTPRXN3_116 (E17)	SFP5RX
D	MGTPRXP1_116 (F15) MFTPRXN1_116 (E15)	SFP7RX
E	MGTPTXP3_116 (B17) MGTPTXN3_116 (A17)	SFP5TX
F	MGTPRXP2_116 (D16) MGTPRXN2_116 (C16)	SFP8RX

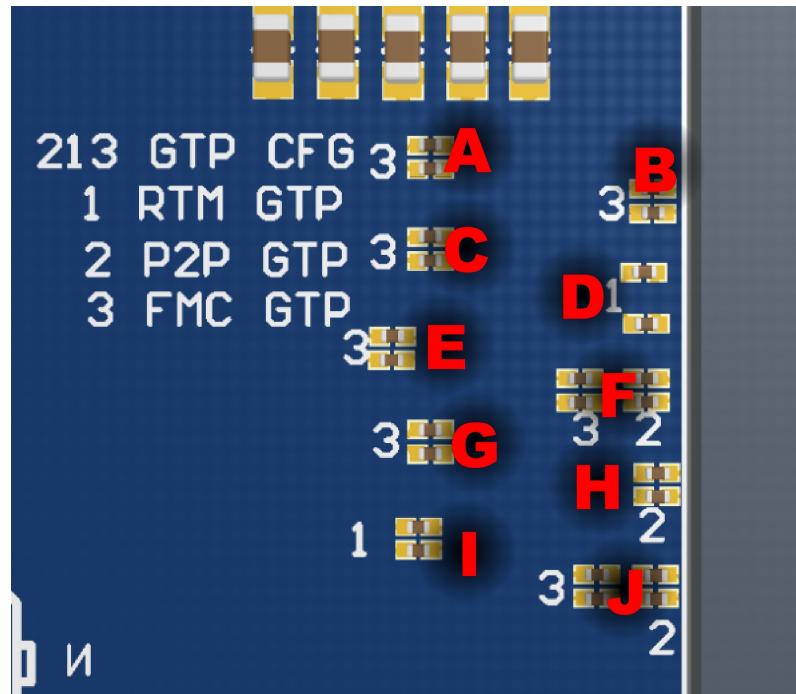


Image 7

Table 7

symbol on Image 7	FPGA MGT P/N signal(ball)	Mounted pair of capacitors		
		1	2	3
A	PTXP0_213 (AN19) PTXN0_213 (AP19)			SFP1TX RTM E10 (P) RTM F10(N)
B	PRXP1_213 (AJ19) PRXN1_213 (AK19)			SFP2RX RTM C9 (P) RTM D9 (N)
C	REFCLK0P_213 (AG20) REFCLK0N_213 (AH20)			RTM_FPGA_CLK2 RTM A9 (P) RTM B9 (N)
D	PRXP0_213 (AL18) PRXN0_213 (AM18)	SFP1RX RTM C10 (P) RTM D10 (N)		
E	PRXP2_213 (AL20) PRXN2_213 (AM20)			SFP3RX RTM C8 (P) RTM D8(N)
F	PRXP3_213 (AJ21) PRXN3_213 (AK21)		AMC_P2P_RX15 AMC (P) 130 AMC (N) 129	SFP4RX RTM C7 (P) RTM D7 (N)
G	REFCLK1P_213 (AG18) REFCLK1N_213 (AH18)			LINK01_CLK IC8B_OP6_45 (P) IC8B_ON6_46 (N)

H	PTXP1_213 (AN21) PTXN1_213 (AP21)		SFP2TX RTM E9 (P) RTM F9 (N)	
I	PTXP2_213 (AL22) PTXN2_213 (AM22)	SFP3TX RTM E8 (P) RTM F8 (N)		
J	PTXP3_213 (AN23) PTXP3_213 (AP23)		AMC_P2P TX15 AMC (P) 133 AMC (N) 132	SFP4TX RTM E7 (P) RTM F7(N)

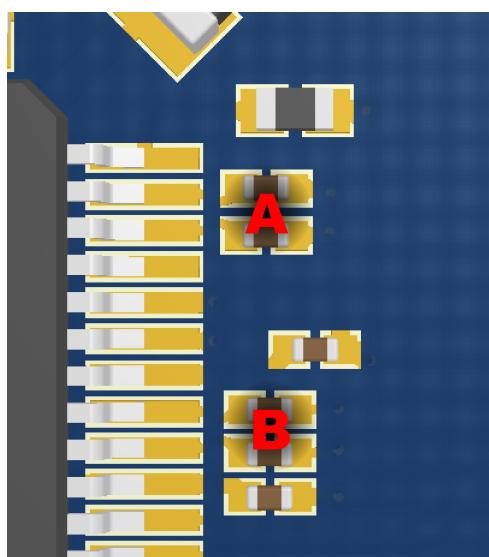


Image 8

Table 8

symbol on Image 8	connection	
A	MGTREFCLK1P_113 (AG16) MGTREFCLK1N_113 (AH16)	FP2_CLK1
B	MGTREFCLK0P_113 (AG14) MGTREFCLK0N_113 (AH14)	FP2_CLK2



Image 9.1

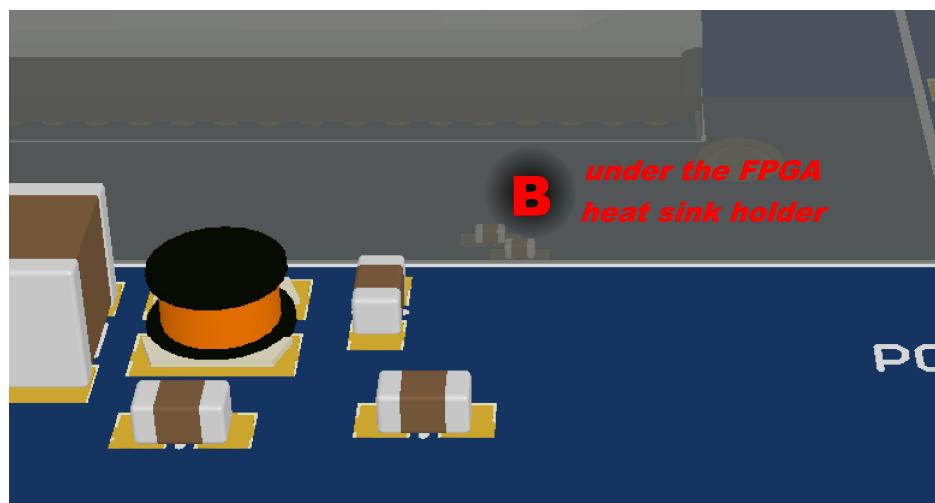


Image 9.2

Table 9

symbol on Image 9	connection	
A	PCIE-CLK1	MGTREFCLK0P_216 (H18)
B		MGTREFCLK0N_216 (G18)
		MGTREFCLK1P_216 (H20)
		MGTREFCLK1N_216 (G20)

Table 10

	FPGA MGT P/N signal (ball)	connector pin
MLVDS_RX19	IO_L21N_T3_DQS_32(AM9)	AMC (P) 142 AMC(N) 141
MLVDS_TX17	IO_L23N_T3_32(AK11)	AMC (P) 145 AMC(N) 144
MLVDS_RX18	IO_L23P_T3_32(AJ11)	AMC (P) 148 AMC(N) 147
MLVDS_TX18	IO_L24P_T3_32(AL10)	AMC (P) 151 AMC(N) 150
MLVDS_RX19	IO_L24N_T3_32(AM10)	AMC (P) 154 AMC(N) 153
MLVDS_TX19	IO_L22N_T3_32(AN11)	AMC (P) 157 AMC(N) 156
MLVDS_RX20	IO_25_32 (AL8)	AMC (P) 160 AMC(N) 159
MLVDS_TX20	IO_L21P_T3_DQS_32(AL9)	AMC (P) 163 AMC(N) 162

Table 11

	FPGA MGT P/N signal (ball)	connector pin
RTM_LVD0	IO_L2P_T0_AD12N_35(N9) IO_L2N_T0_AD12N_35(M9)	RTM (P) A6 RTM (N) B6
RTM_LVD1	IO_L21P_T3_DQS_35(U10) IO_L21N_T3_DQS_35(T10)	RTM (P) E7 RTM (N) F7
RTM_LVD2	IO_L24P_T3_35(U9) IO_L24N_T3_35(T9)	RTM (P) E6 RTM (N) F6
RTM_LVD3	IO_L1P_T0_36(L12) IO_L1N_T0_36(K12)	look at table 2 RTM (P) E5 RTM (N) F5
RTM_LVD4	IO_L4P_T0_36(H11) IO_L4N_T0_36(G11)	look at table 2 RTM (P) A5 RTM (N) B5
RTM_LVD5	IO_L7P_T1_13(AD31) IO_L7N_T1_13(AE31)	RTM (P) E9 RTM (N) F9
RTM_LVD6	IO_L15P_T2_DQS_13(AD26) IO_L15N_T2_DQS_13(AE26)	RTM (P) E10 RTM (N) F10
RTM_LVD7	IO_L22P_T3_13(AC24) IO_L22N_T3_13(AD24)	RTM (P) E8 RTM (N) F8

Table 12 - FMC

No	FMC signal	FPGA P/N signal (ball) - FMC1	FPGA P/N signal (ball) -FMC2
1	DP[0..3]_M2C[C2M]	look at table: 4,5	look at table: 4,5
2	DP[4..9]_M2C[C2M]	N/C	N/C
LA			
3	LA00_CC_P (G6)	IO_L11P_T1_SRCC_36(K7)	IO_L14P_T2_SRCC_13(AE28)
	LA00_CC_N (G7)	IO_L11N_T1_SRCC_36(K6)	IO_L14N_T2_SRCC_13(AF28)
4	LA01_CC_P (D8)	IO_L14P_T2_SRCC_36(J6)	IO_L11P_T1_SRCC_13(AF29)
	LA01_CC_N (D9)	IO_L14N_T2_SRCC_36(J5)	IO_L11N_T1_SRCC_13(AF30)
5	LA02_P (H7)	IO_L10P_T1_36(G7)	IO_L10P_T1_13(AG31)
	LA02_N (H8)	IO_L10N_T1_36(G6)	IO_L10N_T1_13(AH31)
6	LA03_P (G9)	IO_L22P_T3_36(H1)	IO_L21P_T3_DQS_13(AG24)
	LA03_N (G10)	IO_L22N_T3_36(G1)	IO_L21N_T3_DQS_13(AH24)
7	LA04_P (H10)	IO_L21P_T3_DQS_36(K1)	IO_L16P_T2_13(AC26)
	LA04_N (H11)	IO_L21N_T3_DQS_36(J1)	IO_L16N_T2_13(AC27)
8	LA05_P (D11)	IO_L17P_T2_36(H4)	IO_L3P_T0_DQS_13(AH33)
	LA05_N (D12)	IO_L17N_T2_36(H3)	IO_L3N_T0_DQS_13(AH34)
9	LA06_P (C10)	IO_L16P_T2_36(L5)	IO_L20P_T3_13(AE23)
	LA06_N (C11)	IO_L16N_T2_36(K5)	IO_L20N_T3_13(AF23)
10	LA07_P (H13)	IO_L24P_T3_36(K3)	IO_L17P_T2_13(AG27)
	LA07_N (H14)	IO_L24N_T3_36(K2)	IO_L17N_T2_13(AH27)
11	LA08_P (G12)	IO_L15P_T2_DQS_36(F3)	IO_L24P_T3_13(AD25)
	LA08_N (G13)	IO_L15N_T2_DQS_36(F2)	IO_L24N_T3_13(AE25)
12	LA09_P (D14)	IO_L18P_T2_36(J4)	IO_L23P_T3_13(AF25)
	LA09_N (D15)	IO_L18N_T2_36(J3)	IO_L23N_T3_13(AG25)
13	LA10_P (C14)	IO_L20P_T3_36(H2)	IO_L5P_T0_13(AG32)
	LA10_N (C15)	IO_L20N_T3_36(G2)	IO_L5N_T0_13(AH32)
14	LA11_P (H16)	IO_L23P_T3_36(M2)	IO_L8P_T1_13(AD30)
	LA11_N (H17)	IO_L23N_T3_36(L2)	IO_L8N_T1_13(AE30)
15	LA12_P (G15)	IO_L9P_T1_DQS_36(L8)	IO_L18P_T2_13(AE27)
	LA12_N (G16)	IO_L9N_T1_DQS_36(K8)	IO_L18N_T2_13(AF27)
16	LA13_P (D17)	IO_L2P_T0_36(G10)	IO_L1P_T0_13(AF34)
	LA13_N (D18)	IO_L2N_T0_36(G9)	IO_L1N_T0_13(AG34)
17	LA14_P (C18)	IO_L8P_T1_36(H9)	IO_L4P_T0_13(AE33)
	LA14_N (C19)	IO_L8N_T1_36(H8)	IO_L4N_T0_13(AF33)
18	LA15_P (H19)	IO_L3P_T0_DQS_36(K11)	IO_L9P_T1_DQS_13(AD28)
	LA15_N (H20)	IO_L3N_T0_DQS_36(J11)	IO_L9N_T1_DQS_13(AD29)
19	LA16_P (G18)	IO_L5P_T0_36(L10)	IO_L2P_T0_13(AD33)
	LA16_N (G19)	IO_L5N_T0_36(L9)	IO_L2N_T0_13(AD34)
20	LA17_CC_P (D20)	IO_L14P_T2_SRCC_35(T5)	IO_L14P_T2_SRCC_14(AB31)
	LA17_CC_N (D21)	IO_L14N_T2_SRCC_35(T4)	IO_L14N_T2_SRCC_14(AB32)
21	LA18_CC_P (C21)	IO_L11P_T1_SRCC_35(P4)	IO_L11P_T1_SRCC_14(W30)
	LA18_CC_N (C22)	IO_L11N_T1_SRCC_35(P3)	IO_L11N_T1_SRCC_14(W31)
22	LA19_P (H22)	IO_L18P_T2_35(U5)	IO_L21P_T3_DQS_14(AB26)
	LA19_N (H23)	IO_L18N_T2_35(U4)	IO_L21N_T3_DQS_A06_D22_14(AB27)
23	LA20_P (G21)	IO_L20P_T3_35(R10)	IO_L24P_T3_A01_D17_14(AB24)
	LA20_N (G22)	IO_L20N_T3_35(P10)	IO_L24N_T3_A00_D16_14(AB25)
24	LA21_P (H25)	IO_L1P_T0_AD4P_35(M7)	IO_L16P_T2_CSLB_14(AA32)
	LA21_N (H26)	IO_L1N_T0_AD4N_35(M6)	IO_L16N_T2_A15_D31_14(AA33)
25	LA22_P (G24)	IO_L8P_T1_AD14P_35(M5)	IO_L23P_T3_A03_D19_14(AA24)
	LA22_N (G25)	IO_L8N_T1_AD14N_35(M4)	IO_L23N_T3_A03_D18_14(AA25)
26	LA23_P (D23)	IO_L10P_T1_AD15P_35(N3)	IO_L5P_T0_D06_14(W25)

	LA23_N (D24)	IO_L10N_T1_AD15N_35(N2)	IO_L5N_T0_D07_14(J25)
27	LA24_P (H28) LA24_N (H29)	IO_L4P_T0_35(M11) IO_L4N_T0_35(M10)	IO_L10P_T1_D14_14(Y32) IO_L10N_T1_D15_14(Y33)
28	LA25_P (G27) LA25_N (G28)	IO_L3P_T0_DQS_AD5P_35(N8) IO_L3N_T0_DQS_AD5N_35(N7)	IO_L22P_T3_A05_D21_14(AA29) IO_L22N_T3_A04_D20_14(AB29)
29	LA26_P (D26) LA26_N (D27)	IO_L17P_T2_35(T3) IO_L17N_T2_35(T2)	IO_L17P_T2_A14_D30_14(AC31) IO_L17N_T2_A13_D29_14(AC32)
30	LA27_P (C26) LA27_N (C27)	IO_L15P_T2_DQS_35(R3) IO_L15N_T2_DQS_35(R2)	IO_L20P_T3_A08_D24_14(AA27) IO_L20N_T3_A07_D23_14(AA28)
31	LA28_P (H31) LA28_N (H32)	IO_L23P_T3_35(T8) IO_L23N_T3_35(T7)	IO_L4P_T0_D04_14(W28) IO_L4N_T0_D05_14(W98)
32	LA29_P (G30) LA29_N (G31)	IO_L5P_T0_AD13P_35(P9) IO_L5N_T0_AD13N_35(P8)	IO_L15P_T2_DQS_RDWR_B_14(AC33) IO_L15N_T2_DQS_DOUT_CSO_B_14(AC34)
33	LA30_P (H34) LA30_N (H35)	IO_L7P_T1_AD6P_35(N1) IO_L7N_T1_AD6N_35(M1)	IO_L8P_T1_D11_14(W33) IO_L8N_T1_D12_14(W34)
34	LA31_P (G33) LA31_N (G34)	IO_L22P_T3_35(U7) IO_L22N_T3_35(U6)	IO_L7P_T1_D09_14(V31) IO_L7N_T1_D10_14(V32)
35	LA32_P (H37) LA32_N (H38)	IO_L9P_T1_DQS_AD7P_35(R1) IO_L9N_T1_DQS_AD7N_35(P1)	IO_L18P_T2_A12_D28_14(AA34) IO_L18N_T2_A11_D29_14(AB34)
36	LA33_P (G36) LA33_N (G37)	IO_L16P_T2_35(U2) IO_L16N_T2_35(U1)	IO_L9P_T1_DQS_14(V33) IO_L9N_T1_DQS_D13_14(V34)
HA			
37	HA00_CC_P(F4) HA00_CC_N(F5)	IO_L13P_T2_MRCC_16(J29) IO_L13N_T2_MRCC_16(H29)	IO_L12P_T1_MRCC_12(AL30) IO_L12N_T1_MRCC_12(AM30)
38	HA01_CC_P(E2) HA01_CC_N(E3)	IO_L11P_T1_SRCC_16(L28) IO_L11N_T1_SRCC_16(K28)	IO_L13P_T2_MRCC_12(AL28) IO_L13N_T2_MRCC_12(AL29)
39	HA02_P(K7) HA02_N(K8)	IO_L20P_T3_16(K33) IO_L20N_T3_16(J34)	IO_L10P_T1_12(AN31) IO_L10N_T1_12(AP31)
40	HA03_P(J6) HA03_N(J7)	IO_L14P_T2_SRCC_16(K30) IO_L14N_T2_SRCC_16(J30)	IO_L21P_T3_DQS_12(AM26) IO_L21N_T3_DQS_12(AN26)
41	HA04_P(F7) HA04_N(F8)	IO_L24P_T3_16(L33) IO_L24N_T3_16(L34)	IO_L19P_T3_12(AJ25) IO_L19N_T3_VREF_12(AK25)
42	HA05_P(E6) HA05_N(E7)	IO_L23P_T3_16(J33) IO_L23N_T3_16(H34)	IO_L23P_T3_12(AL25) IO_L23N_T3_12(AM25)
43	HA06_P(K10) HA06_N(K11)	IO_L9P_T1_DQS_16(L27) IO_L9N_T1_DQS_16(K27)	IO_L6P_T0_12(AL32) IO_L6N_T0_12(AM32)
44	HA07_P(J9) HA07_N(J10)	IO_L9P_T1_DQS_16(L27) IO_L9N_T1_DQS_16(K27)	IO_L8P_T1_12(AM31) IO_L8N_T1_12(AN32)
45	HA08_P(F10) HA08_N(F11)	IO_L18P_T2_16(L29) IO_L18N_T2_16(L30)	IO_L22P_T3_12(AM27) IO_L22N_T3_12(AN27)
46	HA09_P(E9) HA09_N(E10)	IO_L16P_T2_16(K31) IO_L16N_T2_16(J31)	IO_L20P_T3_12(AJ26) IO_L20N_T3_12(AK26)
47	HA10_P(K13) HA10_N(K14)	IO_L19P_T3_16(H32) IO_L19N_T3_16(G32)	IO_L24P_T3_12(AP25) IO_L24N_T3_12(AP26)
48	HA11_P(J12) HA11_N(J13)	IO_L5P_T0_16(M25) IO_L5N_T0_16(L25)	IO_L4P_T0_12(AK33) IO_L4N_T0_12(AL33)
49	HA12_P(F13) HA12_N(F14)	IO_L21P_T3_DQS_16(H33) IO_L21N_T3_DQS_16(G34)	IO_L16P_T2_12(AM29) IO_L16N_T2_12(AN29)
50	HA13_P(E12) HA13_N(E13)	IO_L4P_T0_16(K25) IO_L4N_T0_16(J25)	IO_L17P_T2_12(AN28) IO_L17N_T2_12(AP28)
51	HA14_P(J15) HA14_N(J16)	IO_L1P_T0_16(M24) IO_L1N_T0_16(L24)	IO_L3P_T0_DQS_12(AN34) IO_L3N_T0_DQS_12(AP34)
52	HA15_P(F16) HA15_N(F17)	IO_L15P_T2_DQS_16(G29) IO_L15N_T2_DQS_16(G30)	IO_L11P_T1_SRCC_12(AJ29) IO_L11N_T1_SRCC_12(AK30)

53	HA16.P(E15) HA16.N(E16)	IO_L17P_T2_16(H31) IO_L17N_T2_16(G31)	IO_L18P_T2_12(AK27) IO_L18N_T2_12(AL27)
54	HA17.CC_P(K16) HA17.CC_N(K17)	IO_L12P_T1_MRCC_16(J28) IO_L12N_T1_MRCC_16(H28)	IO_L14P_T2_SRCC_12(AJ28) IO_L14N_T2_SRCC_12(AK28)
55	HA18.P(J18) HA18.N(J19)	IO_L7P_T1_16(H27) IO_L7N_T1_16(G27)	IO_L5P_T0_12(AN33) IO_L5N_T0_12(AP33)
56	HA19.P(F19) HA19.N(F20)	IO_L8P_T1_16(H26) IO_L8N_T1_16(G26)	IO_L9P_T1_DQS_12(AJ30) IO_L9N_T1_DQS_12(AK31)
57	HA20.P(E18) HA20.N (E19)	IO_L10P_T1_16(K26) IO_L10N_T1_16(J26)	IO_L7P_T1_12(AJ31) IO_L7N_T1_12(AK32)
58	HA21.P (K19) HA21.N(K20)	IO_L3P_T0_DQS_16(G24) IO_L3N_T0_DQS_16(G25)	IO_L15P_T2_DQS_12(AP29) IO_L15N_T2_DQS_12(AP30)
59	HA22.P(J21) HA22.N(J22)	IO_L6P_T0_16(J24) IO_L6N_T0_VREF_16(H24)	IO_L1P_T0_12(AL34) IO_L1N_T0_12(AM34)
60	HA23.P(K22) HA23.N(K23)	IO_L2P_T0_16(K23) IO_L2N_T0_16(J23)	IO_L2P_T0_12(AJ33) IO_L2N_T0_12(AJ34)
HB			
61	HB00_CC_P(K25) HB00_CC_N(K26)	IO_L12P_T1_MRCC_34(W5) IO_L12N_T1_MRCC_34(Y5)	IO_L11P_T1_SRCC_15(U29) IO_L11N_T1_SRCC_15(T29)
62	HB01_P(J24) HB01_N(J25)	IO_L3P_T0_DQS_34(W9) IO_L3N_T0_DQS_34(W8)	IO_L2P_T0_AD8P_15(N26) IO_L2N_T0_AD8N_15(M27)
63	HB02_P(F22) HB02_N(F23)	IO_L2P_T0_34(V9) IO_L2N_T0_34(V8)	IO_L22P_T3_A17_15(N34) IO_L22N_T3_A16_15(M34)
64	HB03_P(E21) HB03_N(E22)	IO_L1P_T0_34(W10) IO_L1N_T0_34(Y10)	IO_L23P_T3_FOE_B_15(U34) IO_L23N_T3_FWE_B_15(T34)
65	HB04_P(F25) HB04_N(F26)	IO_L5P_T0_34(Y8) IO_L5N_T0_34(Y9)	IO_L5P_T0_AD9P_15(U26) IO_L5N_T0_AD9N_15(U27)
66	HB05_P(E24) HB05_N(E25)	IO_L23P_T3_34(AA10) IO_L23N_T3_34(AA9)	IO_L24P_T3_RS1_15(P33) IO_L24N_T3_RS0_15(P34)
67	HB06_CC_P(K28) HB06_CC_N(K29)	IO_L11P_T1_SRCC_34(V4) IO_L11N_T1_SRCC_34(W4)	IO_L13P_T2_MRCC_15(R30) IO_L13N_T2_MRCC_15(P30)
68	HB07_P(J27) HB07_N(J28)	IO_L24P_T3_34(AB10) IO_L24N_T3_34(AB9)	IO_L4P_T0_15(P24) IO_L4N_T0_15(N24)
69	HB08_P(F28) HB08_N(F29)	IO_L10P_T1_34(V3) IO_L10N_T1_34(W3)	IO_L1P_T0_AD0P_15(R26) IO_L1N_T0_AD0N_15(P26)
70	HB09_P(E27) HB09_N(E28)	IO_L8P_T1_34(V2) IO_L8N_T1_34(V1)	IO_L9P_T1_DQS_AD3P_15(T28) IO_L9N_T1_DQS_AD3N_15(R28)
71	HB10_P(K31) HB10_N(K32)	IO_L4P_T0_34(V7) IO_L4N_T0_34(V6)	IO_L3P_T0_DQS_AD1P_15(U25) IO_L3N_T0_DQS_AD1N_15(T25)
72	HB11_P(J30) HB11_N(J31)	IO_L4P_T0_34(V7) IO_L4N_T0_34(V6)	IO_L7P_T1_15(W1) IO_L7N_T1_15(Y1)
73	HB12_P(J31) HB12_N(J32)	IO_L20P_T3_34(AC7) IO_L20N_T3_34(AC6)	IO_L17P_T2_A26_15(N31) IO_L17N_T2_A25_15(M32)
74	HB13_P(E30) HB13_N(E31)	IO_L9P_T1_DQS_34(Y3) IO_L9N_T1_DQS_34(Y2)	IO_L8P_T1_AD10P_15(N27) IO_L8N_T1_AD10N_15(N28)
75	HB14_P(K34) HB14_N(K35)	IO_L17P_T2_34(AC2) IO_L17N_T2_34(AC1)	IO_L16P_T2_A28_15(R31) IO_L16N_T2_A27_15(P31)
76	HB15_P(J33) HB15_N(J34)	IO_L22P_T3_34(AC9) IO_L22N_T3_34(AC8)	IO_L14P_T2_SRCC_15(U30) IO_L14N_T2_SRCC_15(T30)
77	HB16_P(F34) HB16_N(F35)	IO_L15P_T2_DQS_34(AB2) IO_L15N_T2_DQS_34(AB1)	IO_L18P_T2_A24_15(U31) IO_L18N_T2_A23_15(U32)
78	HB17_CC_P(K37) HB17_CC_N(K38)	IO_L13P_T2_MRCC_34(AA5) IO_L13N_T2_MRCC_34(AA4)	IO_L12P_T1_MRCC_15(P28) IO_L12N_T1_MRCC_15(P29)
79	HB18_P(J36)	IO_L21P_T3_DQS_34(AB7)	IO_L10P_T1_AD11P_15(N29)

	HB18_N(J37)	IO_L21N_T3_DQS_34(AB6)	IO_L10N_T1_AD11N_15(M29)
80	HB19_P(E33) HB19_N(E34)	IO_L14P_T2_SRCC_34(AB5) IO_L14N_T2_SRCC_34(AB4)	IO_L15P_T2_DQS_15(M30) IO_L15N_T2_DQS_15(M31)
81	HB20_P(F37) HB20_N(F38)	IO_L16P_T2_34(AA3) IO_L16N_T2_34(AA2)	IO_L20P_T3_A20_15(N32) IO_L20N_T3_A19_15(N33)
82	HB21_P(E36) HB21_N(E37)	IO_L18P_T2_34(AC4) IO_L18N_T2_34(AC3)	IO_L21P_T3_DQS_15(T33) IO_L21N_T3_DQS_A18_15(R33)
		GBT_CLK	
83	GBTCLK0_M2C_P (D4) GBTCLK0_M2C_N (D5)	look at table 4	
84	GBTCLK1_M2C_P (B20) GBTCLK1_M2C_N (B21)	look at table 4	
		FMC_CLOCKS	
85	CLK0_M2C_P (H4) CLK0_M2C_N (H5)	H7 H6	AA30 AB30
86	CLK1_M2C_P (G2) CLK1_M2C_N (G3)	P5 N4	AG29 AH29
87	CLK2_BIDIR_P (K4) CLK2_BIDIR_N (K5)	G5 G4	AH28 AH29
88	CLK3_BIDIR_P (J2) CLK3_BIDIR_P (J3)	R6 R5	Y30 Y31

5 Compatible products

<http://creotech.pl/product-scientific/fmc-dio-32chtl>

<http://creotech.pl/product-scientific/fmc-adc-250m-16b-4cha>

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