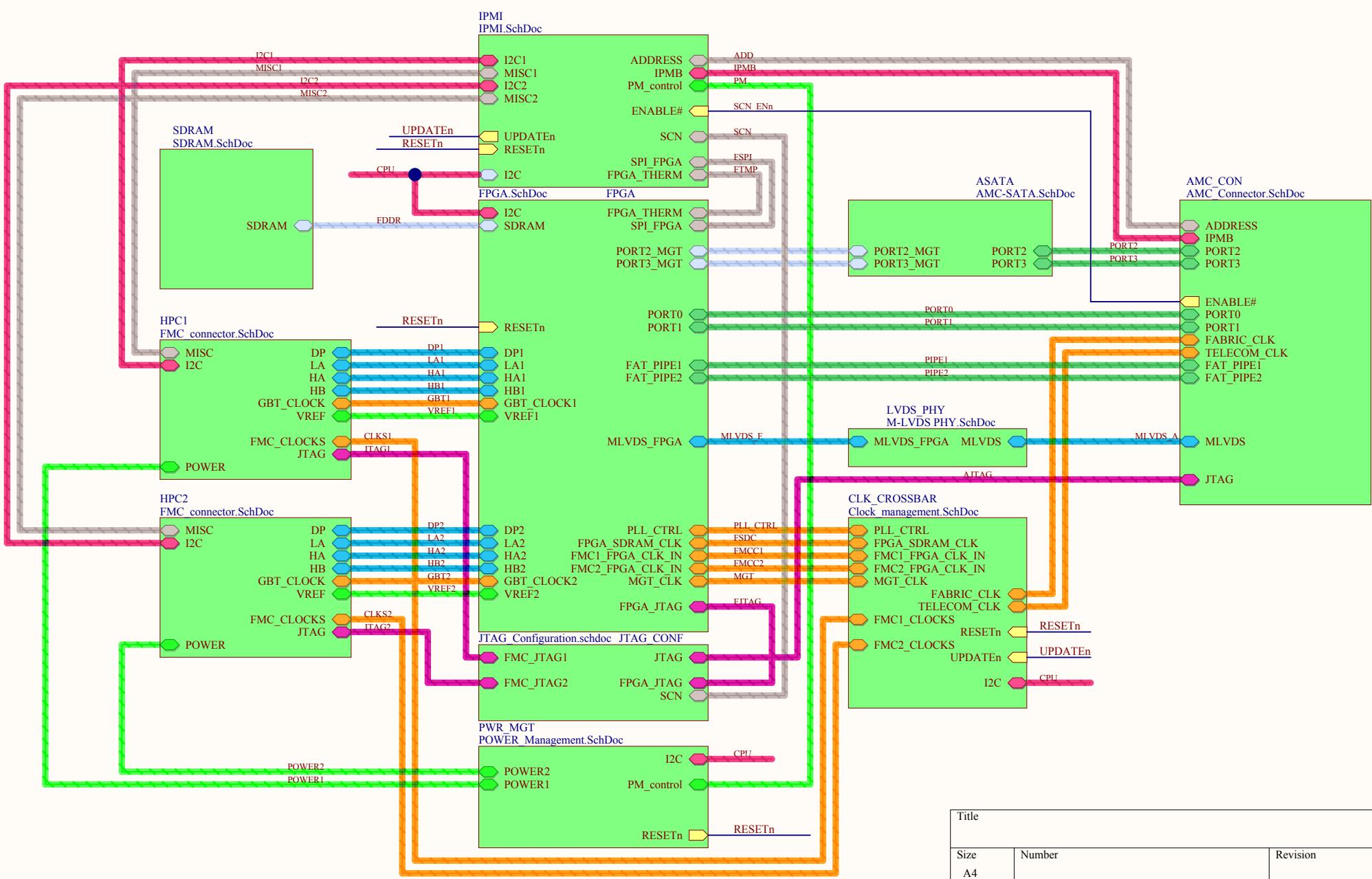
Sheet Title **AMC Top Sheet**Project Title **ProjectTitle****ProjectOrganization****ProjectAddress1****ProjectAddress2****ProjectAddress3****ProjectAddress4**Size: **A3**

Item:

Revision:

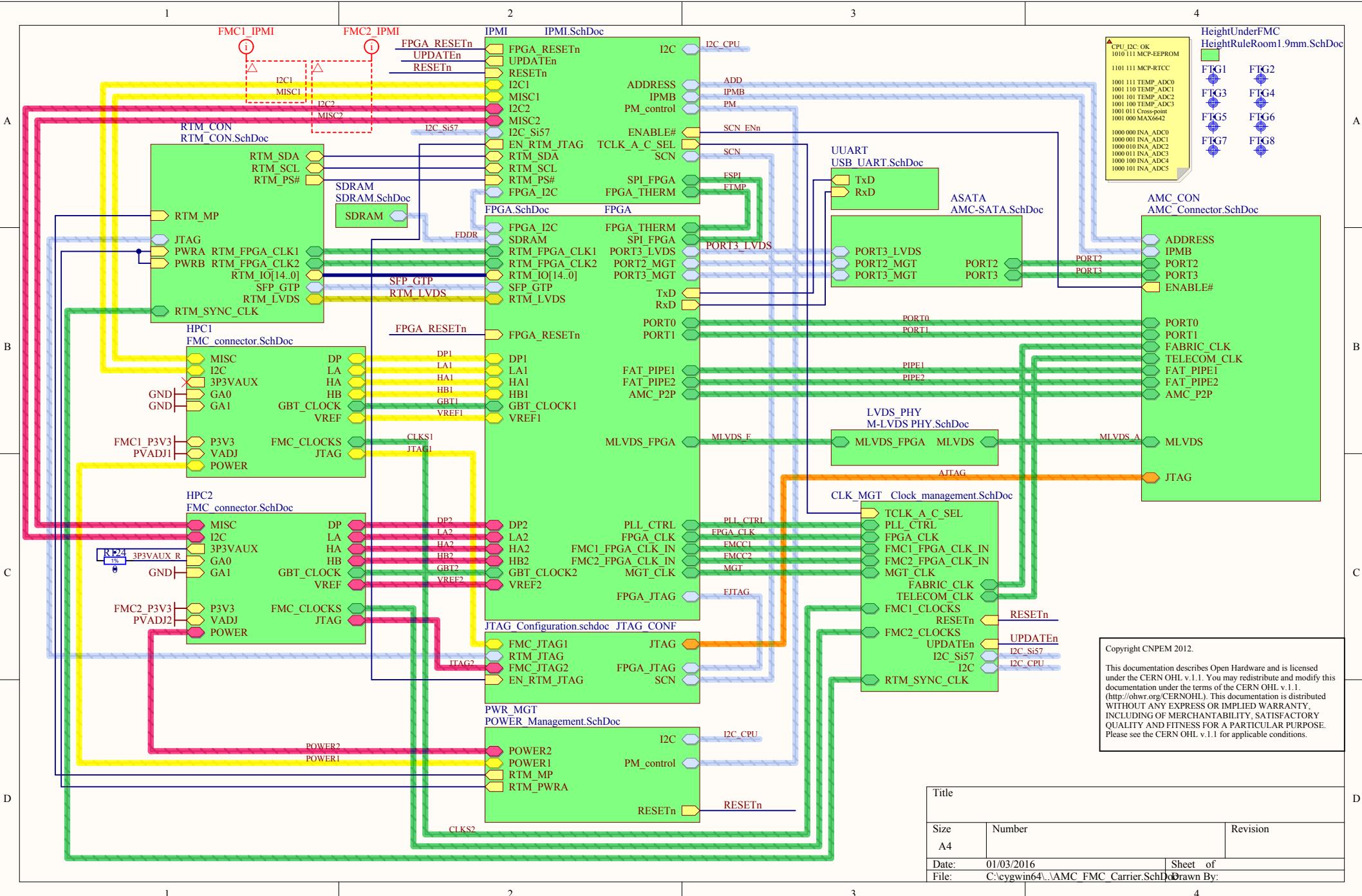
Date: **01/03/2016**Time: **09:46:06**Sheet **1** of **30**File: **AMC Connector.SchDoc**

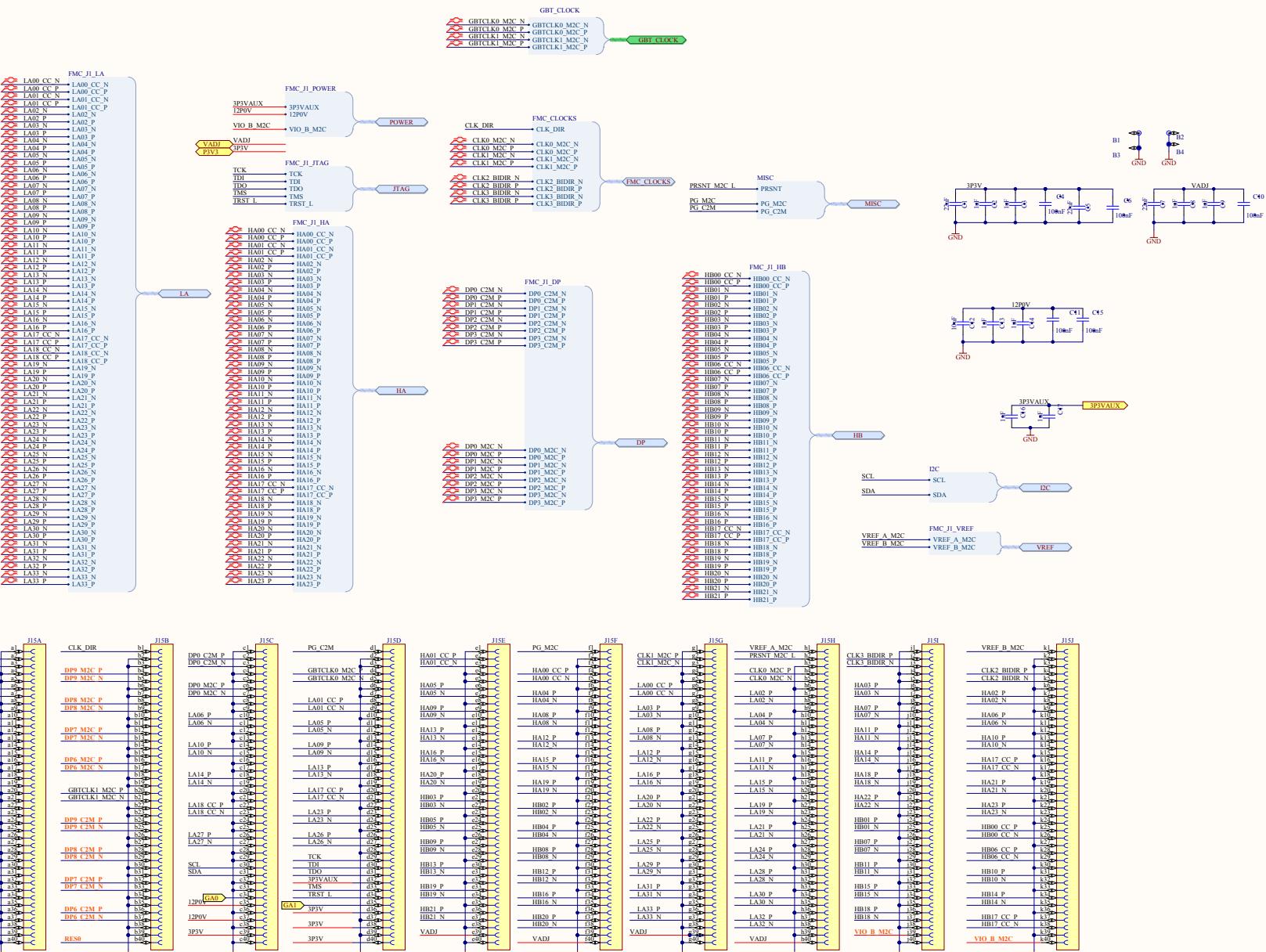
1 2 3 4

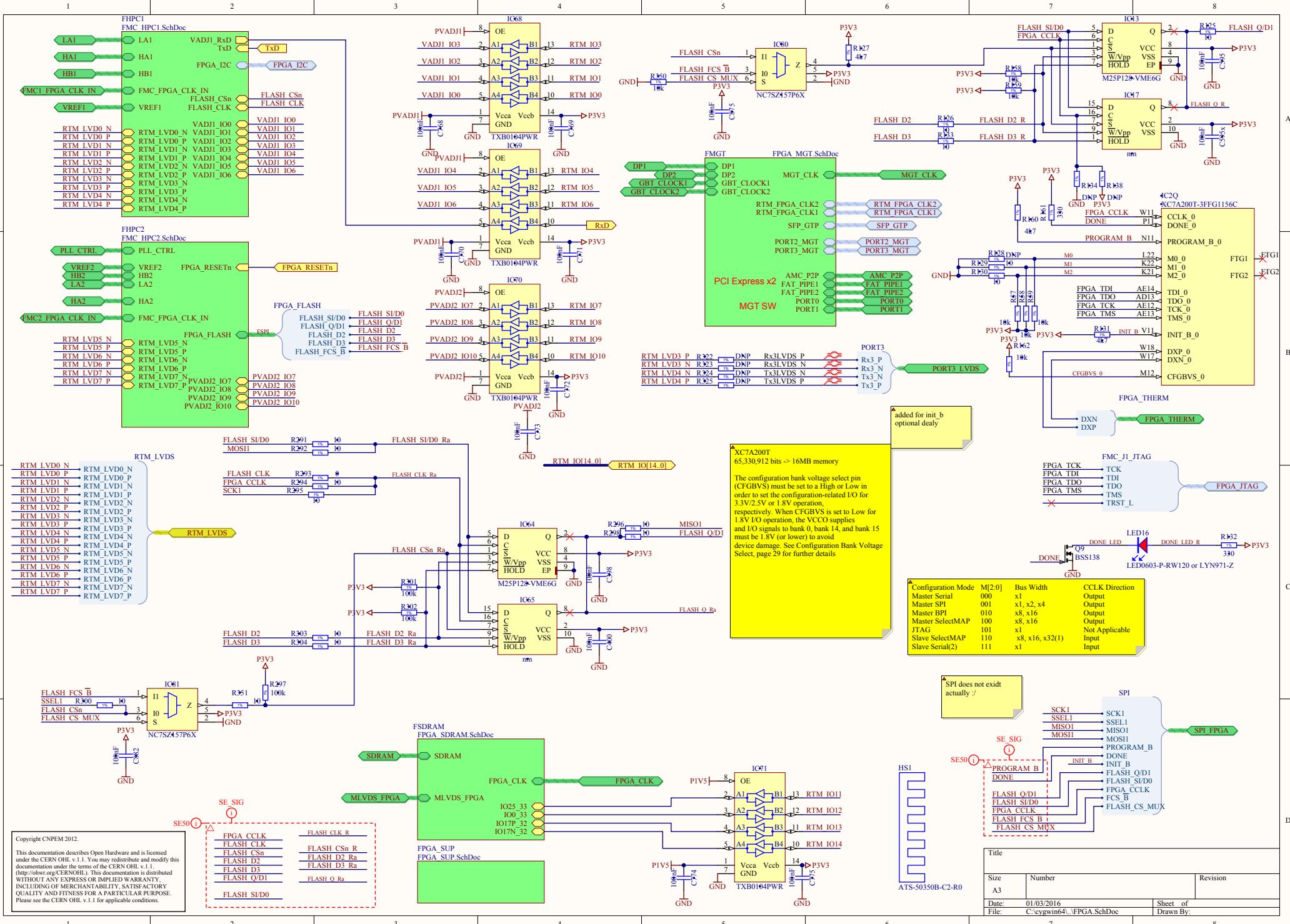


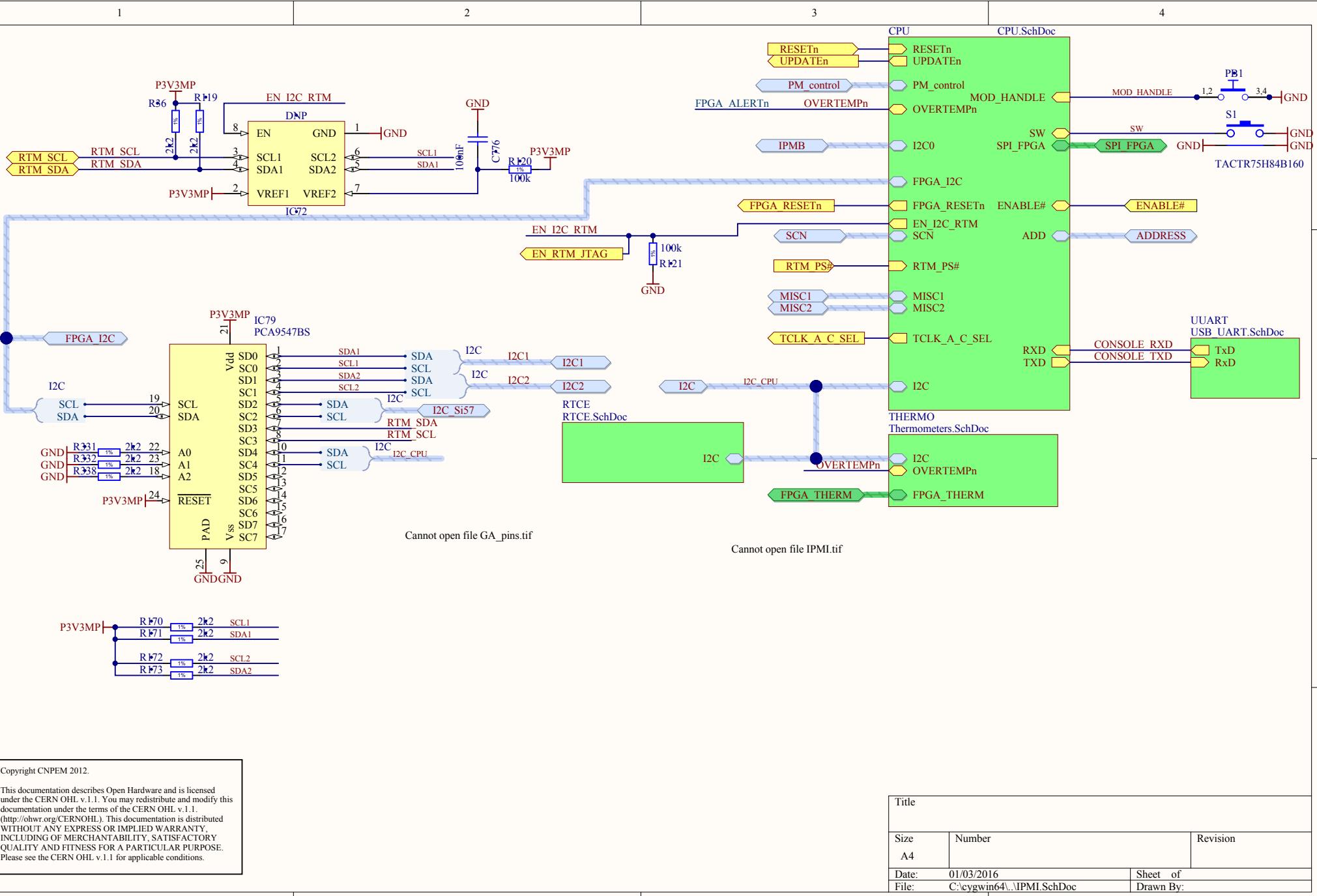
Title		
Size	Number	Revision
A4		
Date: 01/03/2016		Sheet of
File: C:\cygwin64\AMC FMC Carrier block SchDoc		1

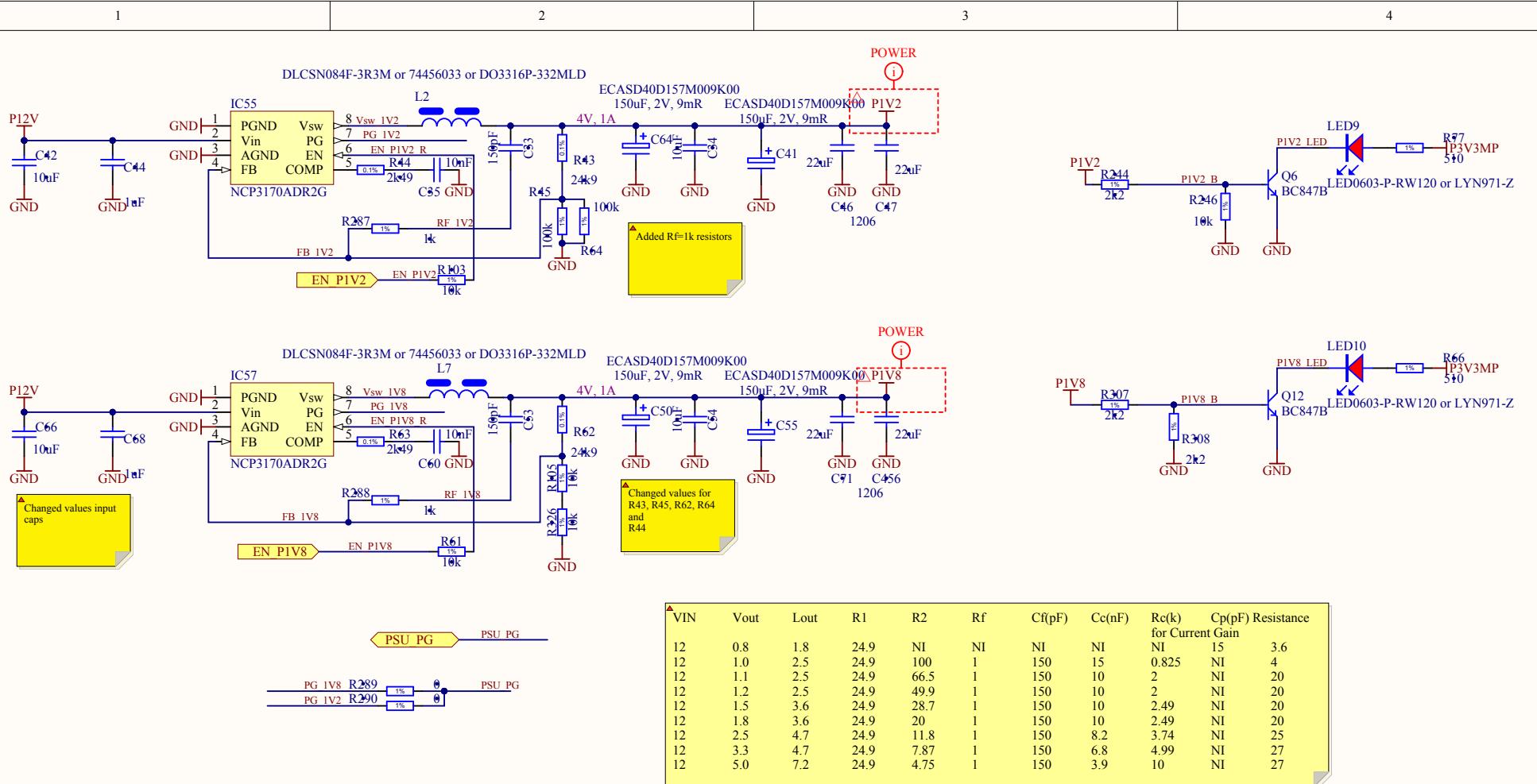
1 2 3 4







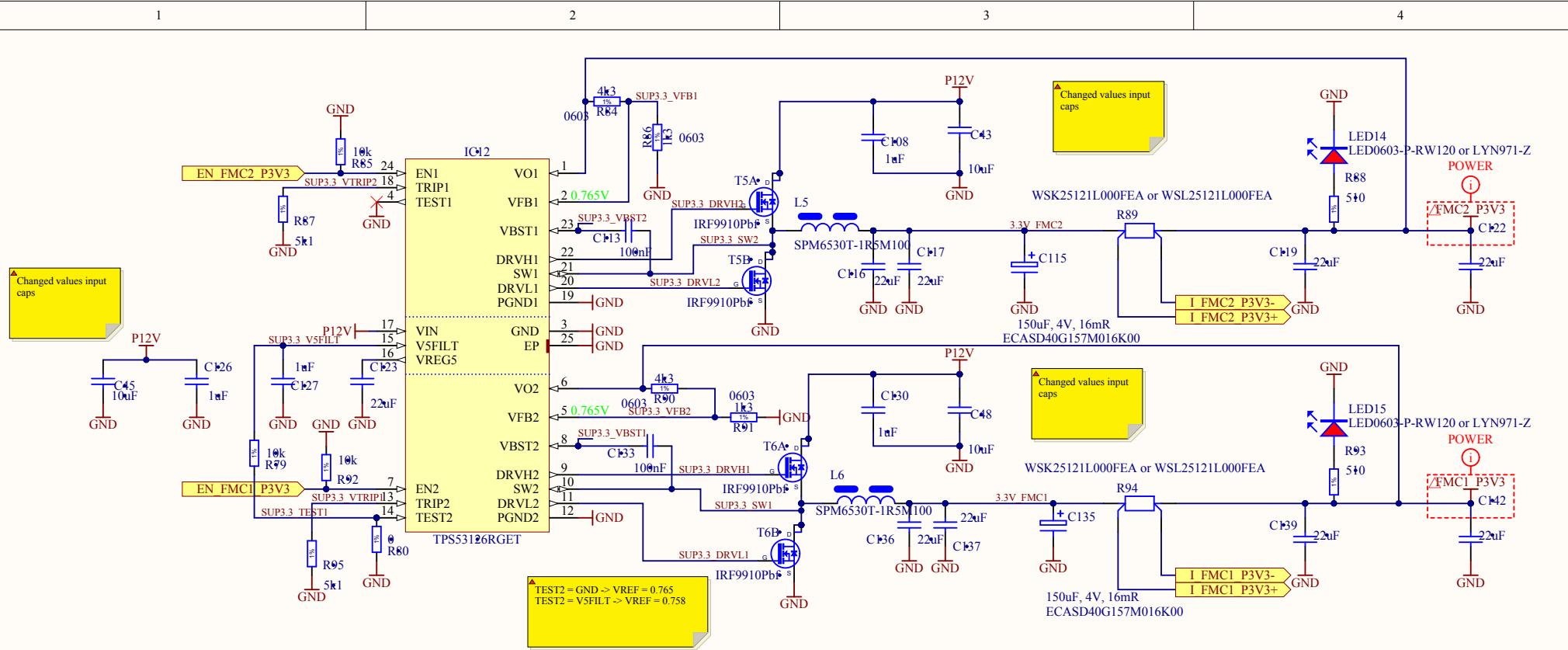




Copyright CNPEM 2012.

This documentation describes Open Hardware and is licensed under the CERN OHL v.1.1. You may redistribute and modify this documentation under the terms of the CERN OHL v.1.1.
(<http://ohwr.org/CERNOHL>). This documentation is distributed WITHOUT ANY EXPRESS OR IMPLIED WARRANTY, INCLUDING OF MERCHANTABILITY, SATISFACTORY QUALITY AND FITNESS FOR A PARTICULAR PURPOSE. Please see the CERN OHL v.1.1 for applicable conditions.

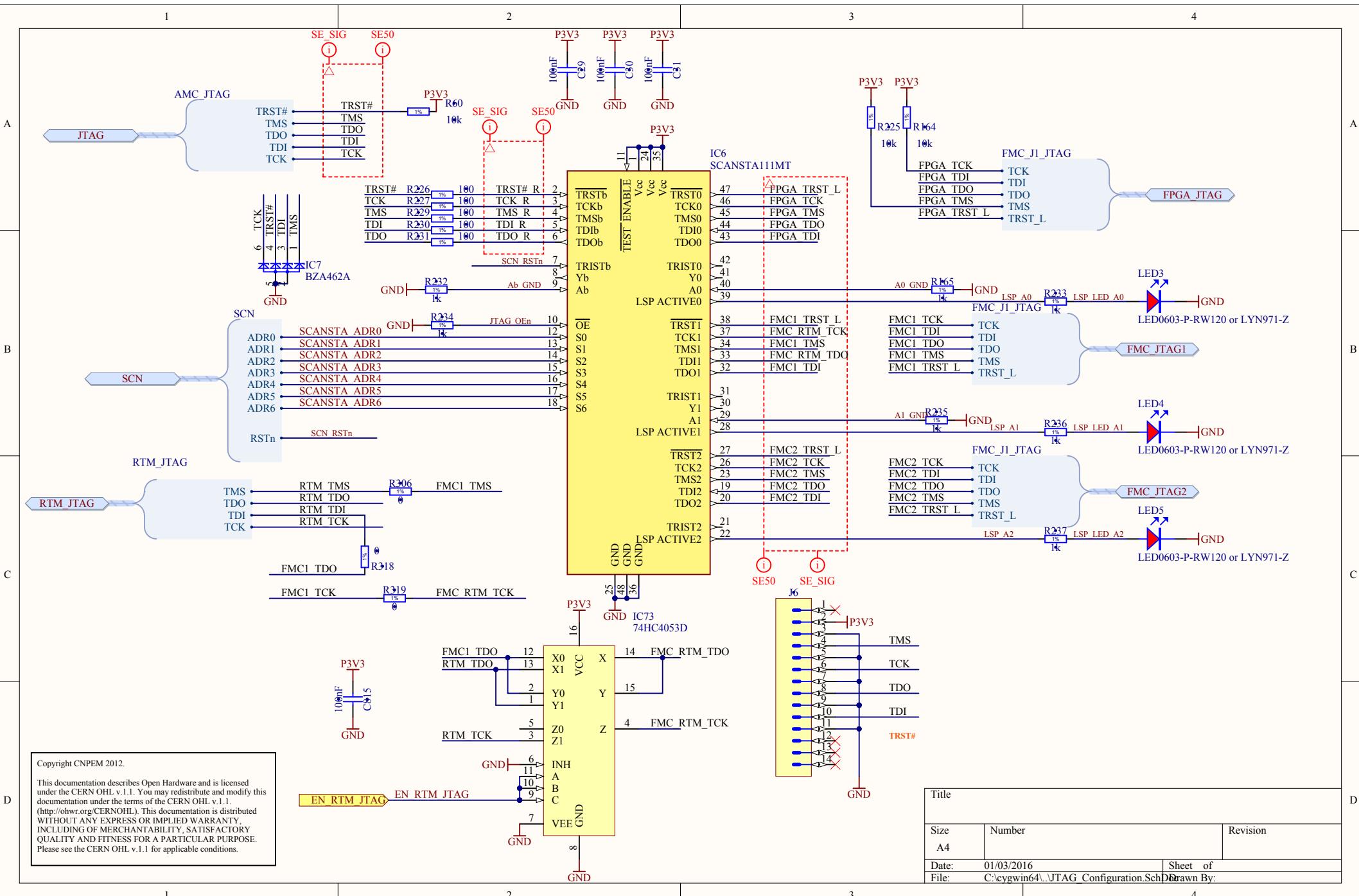
Title		
Size A4	Number	Revision
Date:	01/03/2016	Sheet of
File:	C:\cygwin64\..\SUP 1.2 1.8.SchDoc	Drawn By:

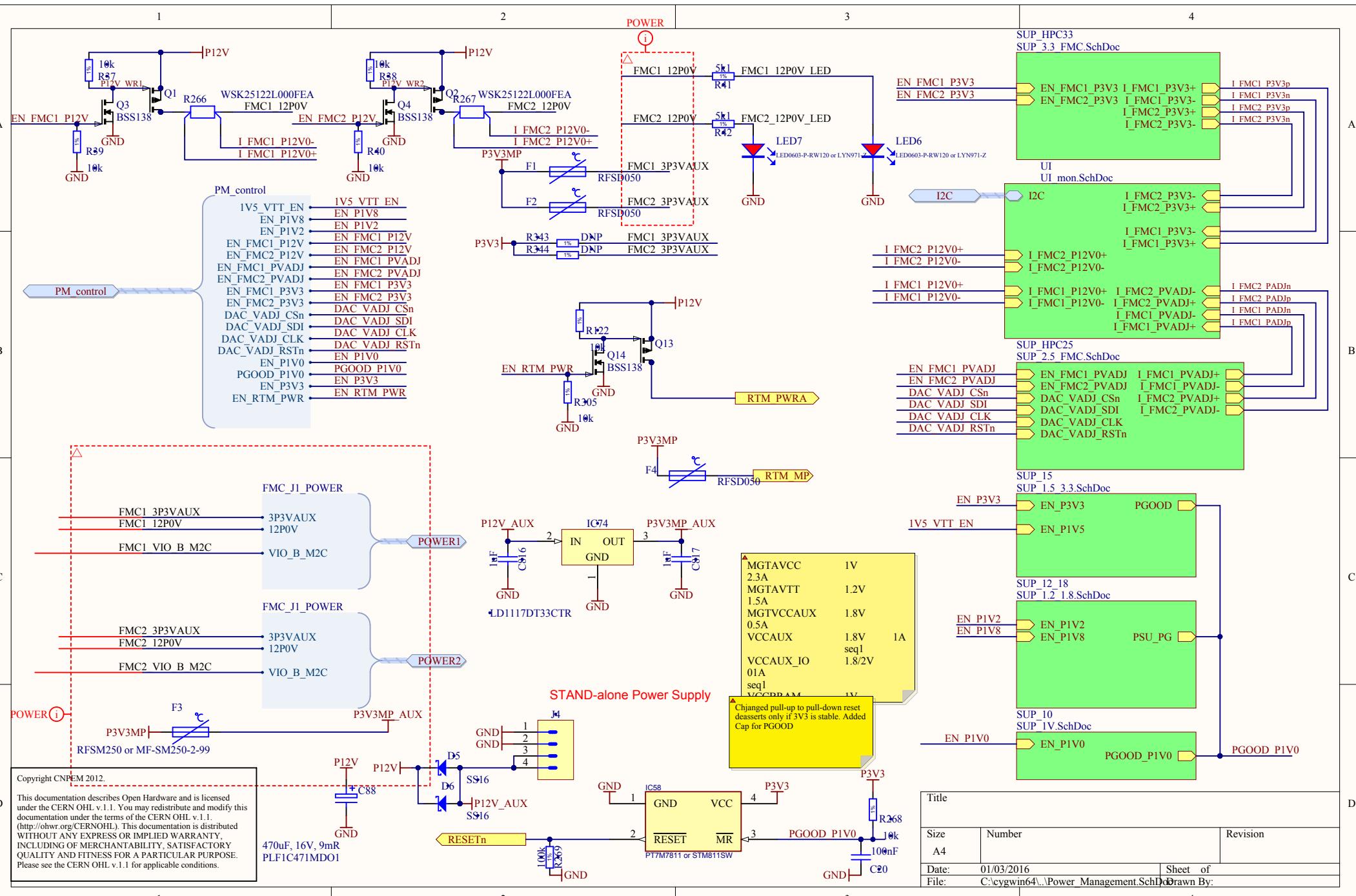


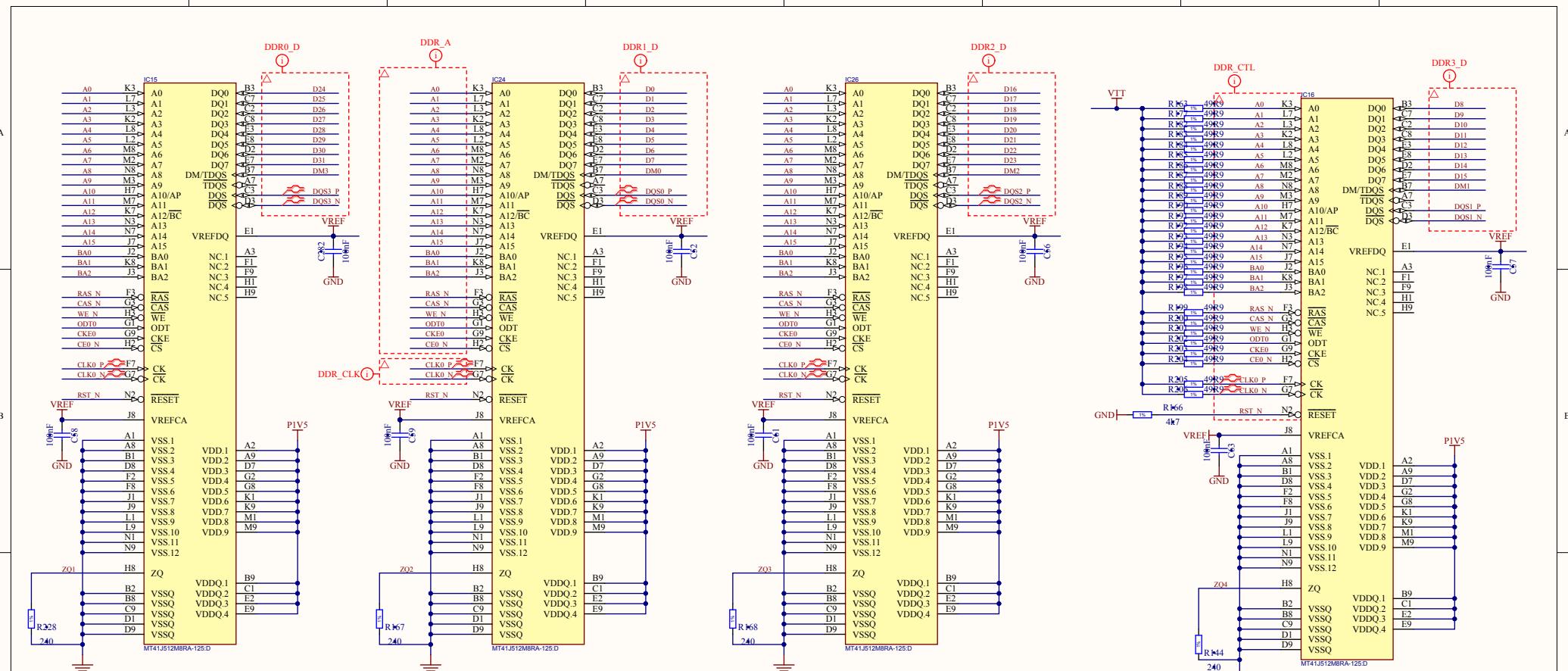
Copyright CNPEM 2012.

This documentation describes Open Hardware and is licensed under the CERN OHL v.1.1. You may redistribute and modify this documentation under the terms of the CERN OHL v.1.1 (<http://ohwr.org/CERNOHL>). This documentation is distributed WITHOUT ANY EXPRESS OR IMPLIED WARRANTY, INCLUDING OF MERCHANTABILITY, SATISFACTORY QUALITY AND FITNESS FOR A PARTICULAR PURPOSE. Please see the CERN OHL v.1.1 for applicable conditions.

Title		
Size	Number	Revision
A4		
Date: 01/03/2016	Sheet of	
File: C:\cygwin64\...\SUP_3.3_FMC.SchDoc	Drawn By:	



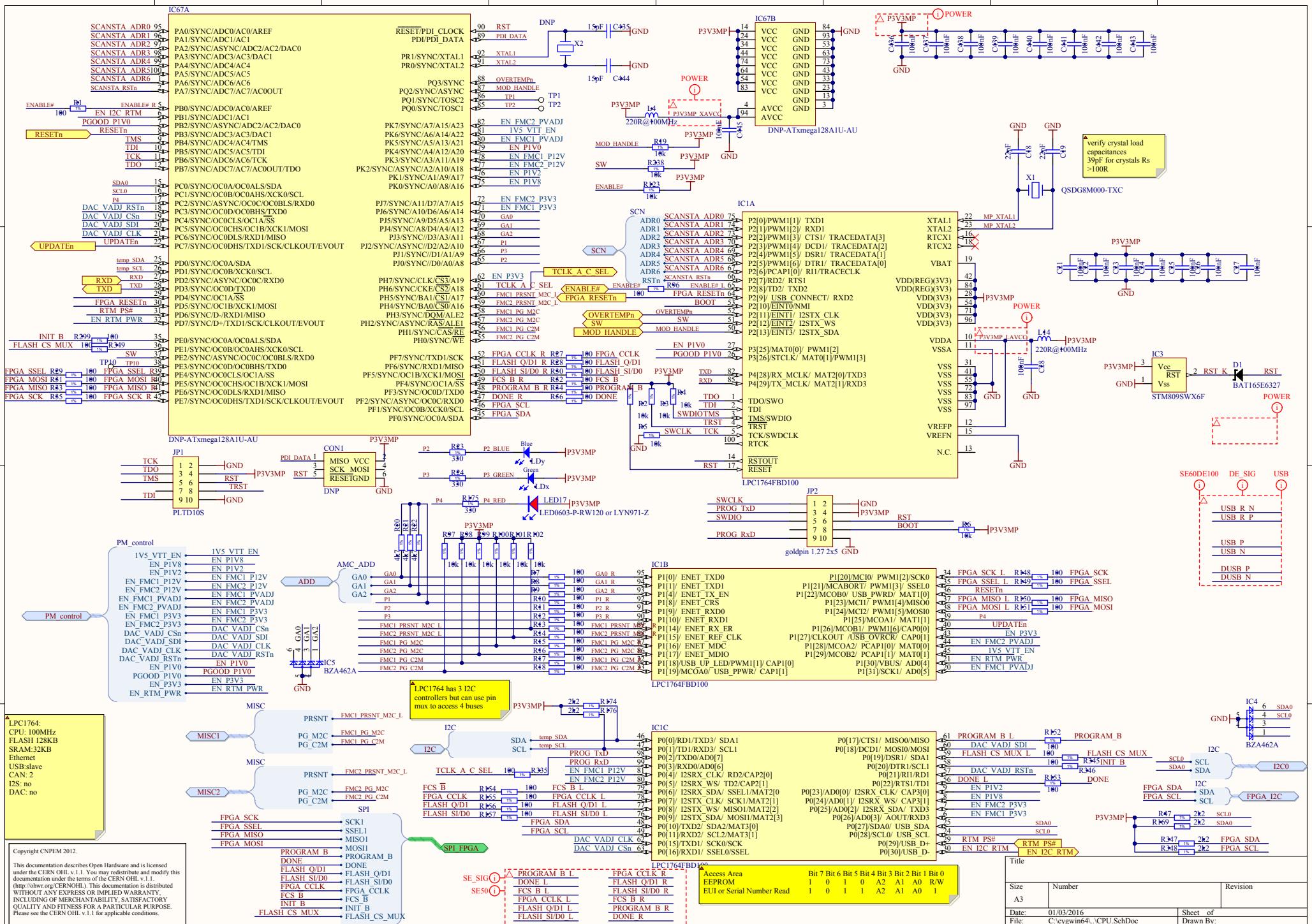




All capacitors without values are 100nF 0201 by default

Copyright CNPEM 2012.
This documentation describes Open Hardware and is licensed
under the terms of the CERN OHL v.1 license (<http://ohwr.org/CERN-OHL>). This documentation is distributed
WITHOUT ANY EXPRESS OR IMPLIED WARRANTY,
INCLUDING MERCHANTABILITY, SATISFACTORY
QUALITY AND FITNESS FOR A PARTICULAR PURPOSE.
Please see the CERN OHL v.1.1 for applicable conditions.

Title		Revision
Size	Number	
A3		
Date:	01/03/2016	Sheet of
File:	C:\cygwin64\SDRAM.SchDoc	Drawn By:



1

1

1

1

A

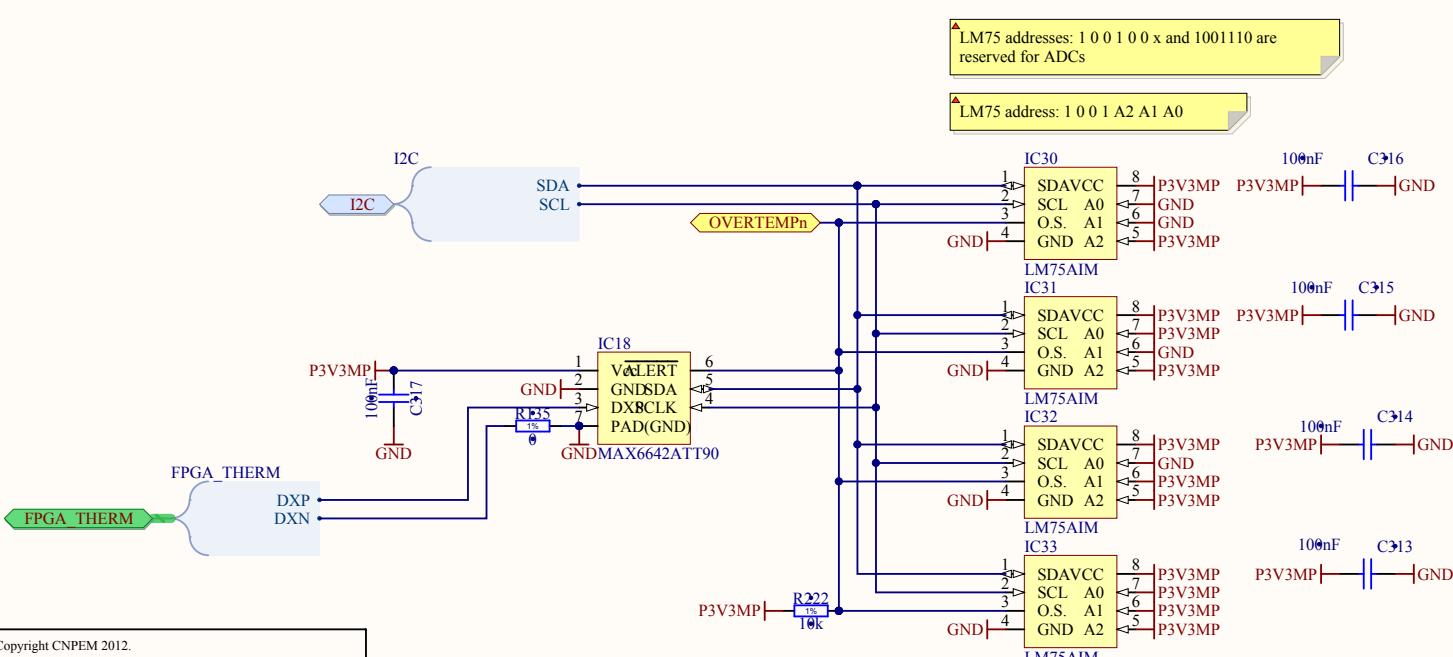
1

B

1

1

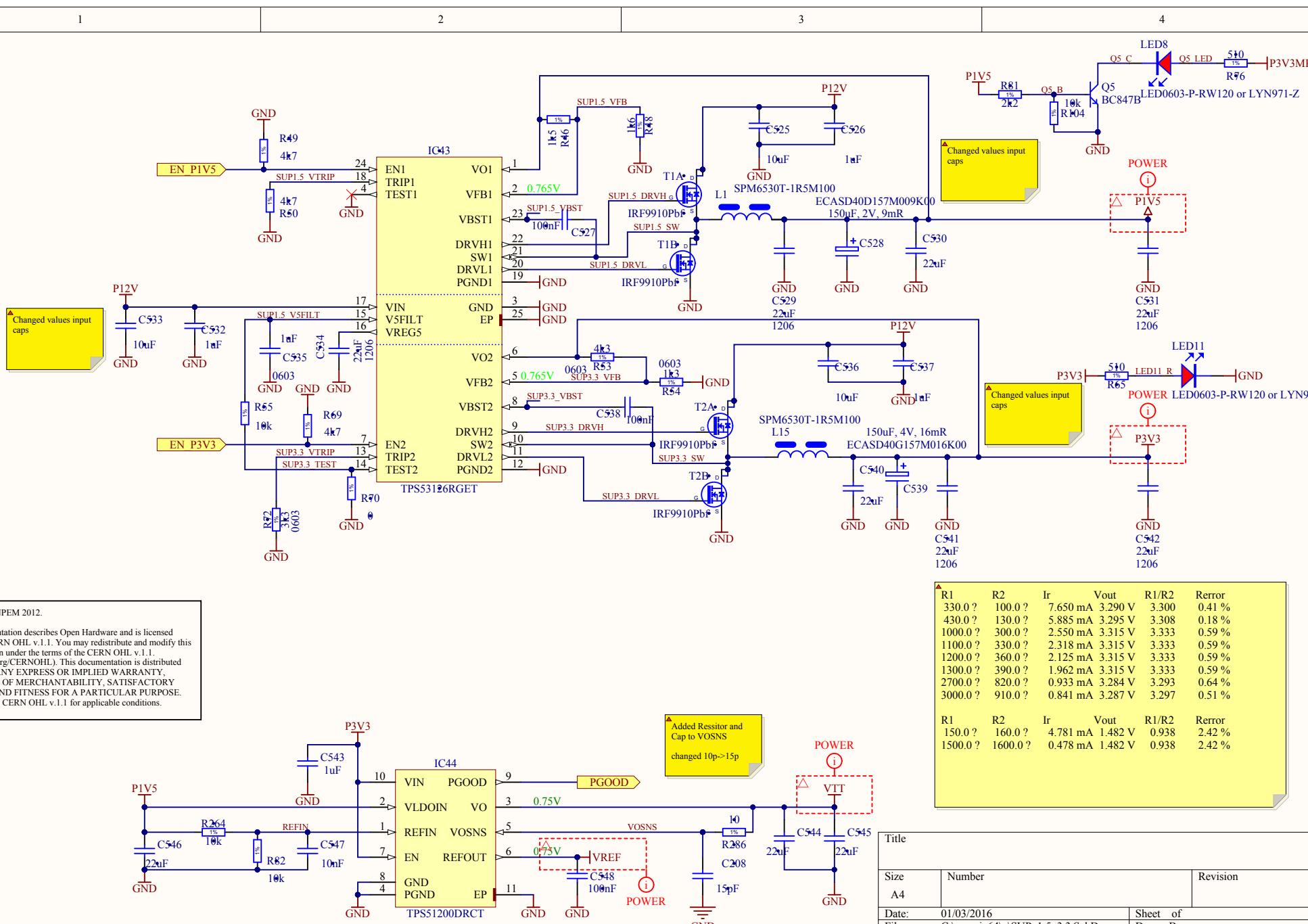
1



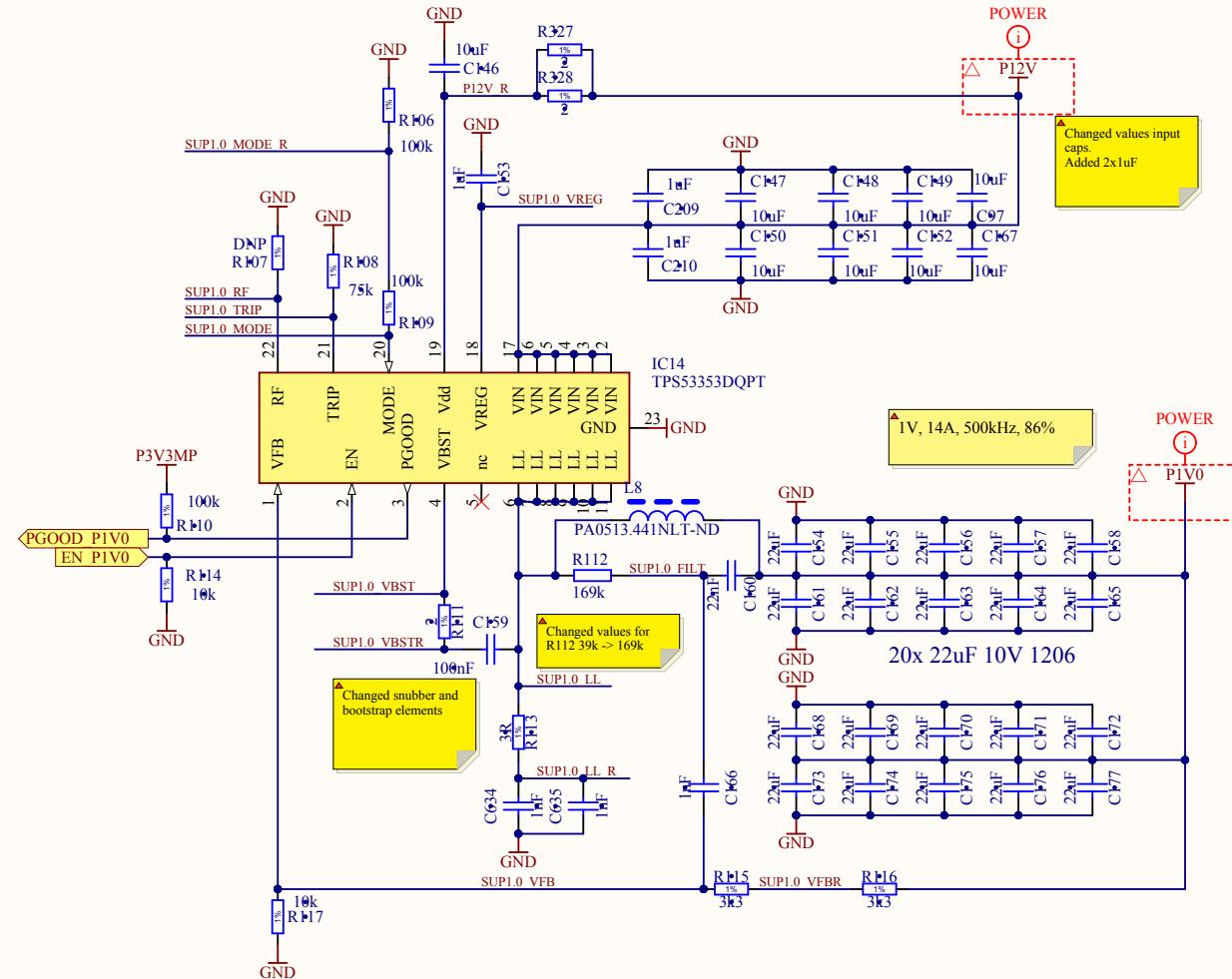
Copyright CNPEM 2012.

This documentation describes Open Hardware and is licensed under the CERN OHL v.1.1. You may redistribute and modify this documentation under the terms of the CERN OHL v.1.1. (<http://ohwr.org/CERNOHL>). This documentation is distributed WITHOUT ANY EXPRESS OR IMPLIED WARRANTY, INCLUDING OF MERCHANTABILITY, SATISFACTORY QUALITY AND FITNESS FOR A PARTICULAR PURPOSE. Please see the CERN OHL v.1.1 for applicable conditions.

Title		
Size A4	Number	Revision
Date:	01/03/2016	Sheet of
File:	C:\cygwin64\...\Thermometers.SchDoc	Drawn By:



Cannot open file
C:\Users\Greg\Documents\DESIGNS\BPM-DBE\PCB_uTCA_FMC_Carrier\TPS53353.tif



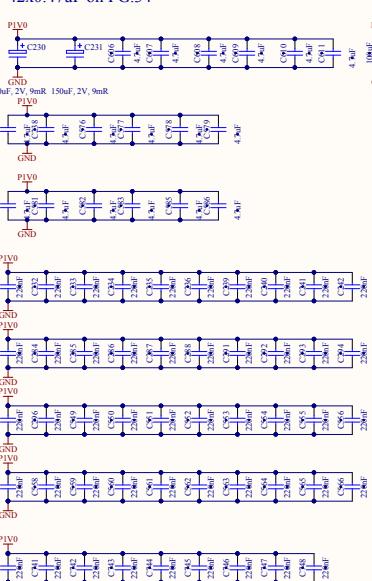
Copyright CNPEM 2012.

This documentation describes Open Hardware and is licensed under the CERN OHL v.1.1. You may redistribute and modify this documentation under the terms of the CERN OHL v.1.1. (<http://ohwr.org/CERNOHL>). This documentation is distributed WITHOUT ANY EXPRESS OR IMPLIED WARRANTY, INCLUDING OF MERCHANTABILITY, SATISFACTORY QUALITY AND FITNESS FOR A PARTICULAR PURPOSE. Please see the CERN OHL v.1.1 for applicable conditions.

Title		
Size A4	Number	Revision
Date:	01/03/2016	Sheet of
File:	C:\vgwin64\ SUP 1V.SchDoc	Drawn By:

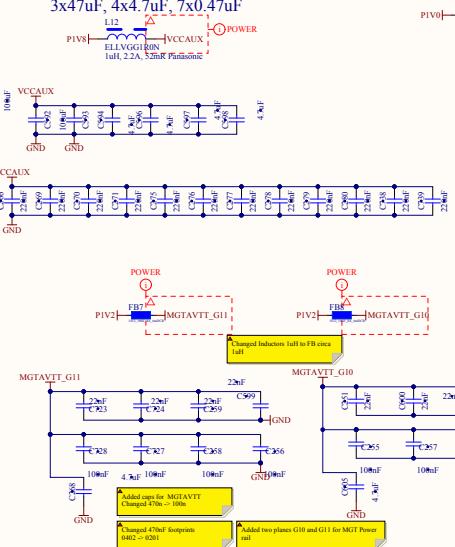
1x680uF, 2x100uF, 28x4.7uF

42x0.47uF on PG.34



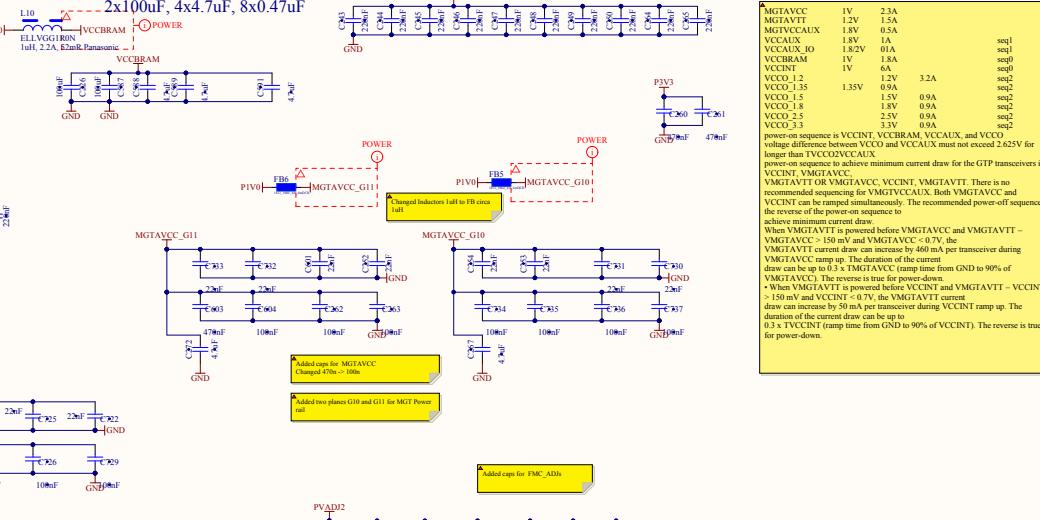
VCCAUX

3x47uF, 4x4.7uF, 7x0.47uF



VCCBRAM

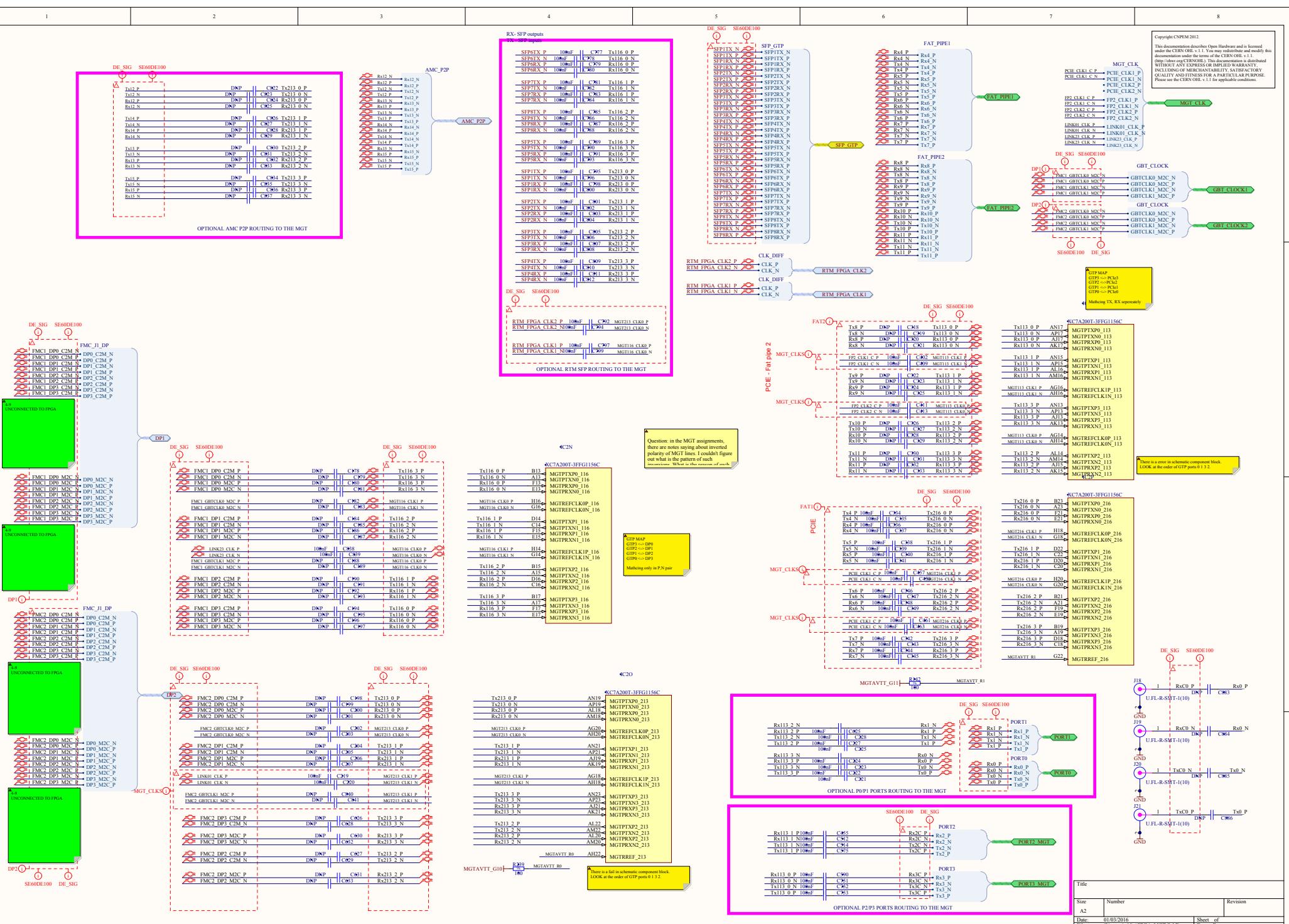
2x100uF, 4x4.7uF, 8x0.47uF

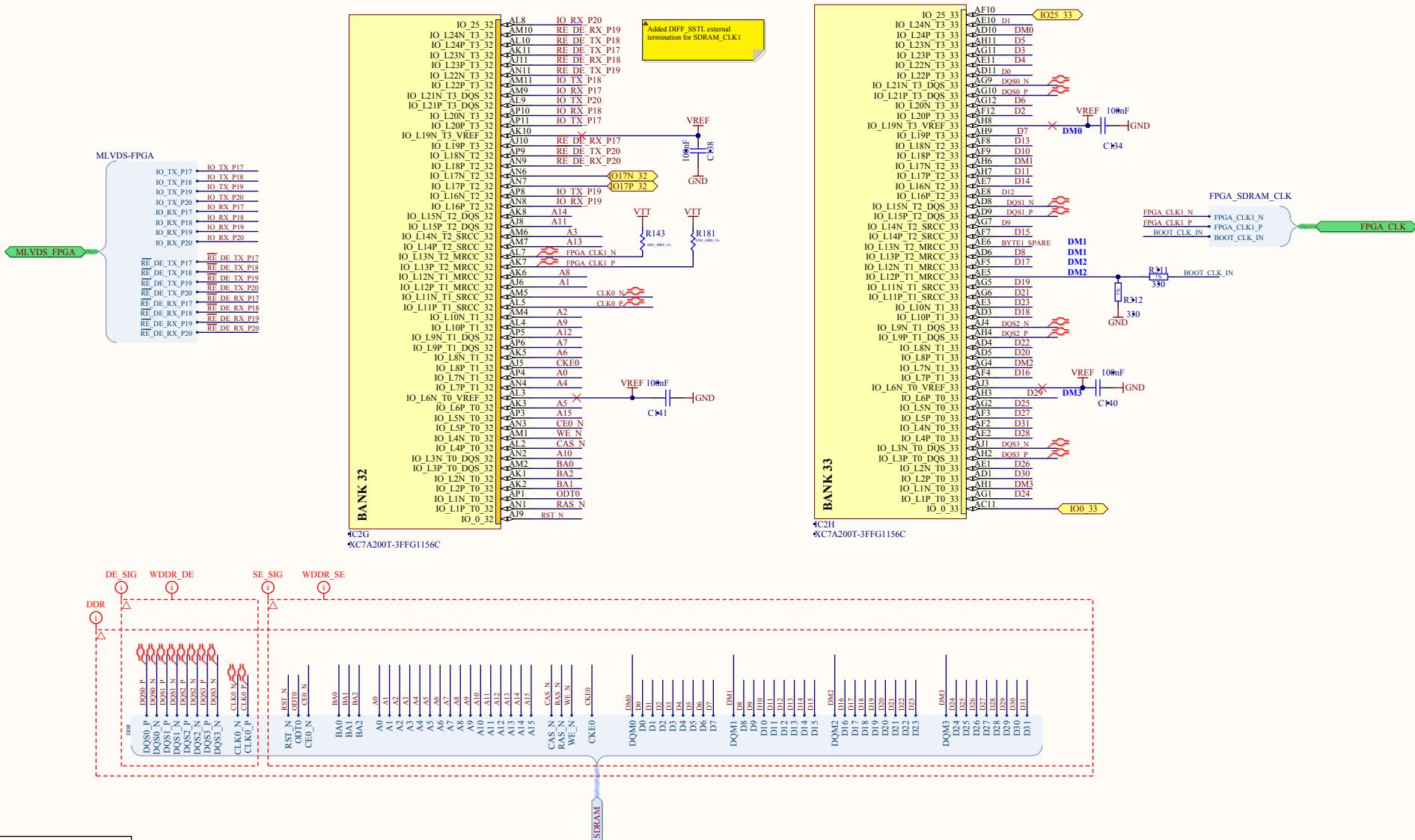


VCCINT, VCCBRAM, VCCAUX, and VCCO voltage levels are VCCINT, VCCBRAM, VCCAUX, and VCCO respectively. The power-on sequence is VCCINT -> VCCBRAM -> VCCAUX -> VCCO. Both VMGTAVCC and VMGTAVT must be powered up before VMGTVCAUX. Both VMGTAVCC and VMGTAVT must be powered up before VMGTVCAUX. The recommended power-on sequence is the reverse of the power-on sequence to achieve minimum current draw. When VMGTAVCC is powered up before VMGTAVCC and VMGTAVT, the VMGTAVCC current draw can increase by 460 mA per transceiver during VMGTAVCC ramp up. The duration of the current draw from VMGTAVCC to VMGTAVCC (from GND to 90% of VMGTAVCC). The reverse is true for power-down. When VMGTAVT is powered up before VMGTAVCC and VMGTAVT - VCCINT -> VMGTAVT -> VMGTAVCC. The current draw can increase by 50 mA per transceiver during VMGTAVT ramp up. The duration of the current draw can be up to 0.3 μ s. The recommended power-on sequence is VMGTAVCC -> VMGTAVCC and VMGTAVT -> VMGTAVT. The current draw can increase by 460 mA per transceiver during VMGTAVCC ramp up. The duration of the current draw from VMGTAVCC to VMGTAVCC (from GND to 90% of VMGTAVCC). The reverse is true for power-down.

A1

A1	GND	GND	J20	V13	GND	GND	AF17
A11	GND	GND	J21	V15	GND	GND	AF18
A12	GND	GND	J22	V16	GND	GND	AF19
A13	GND	GND	J23	V17	GND	GND	AF20
A14	GND	GND	J24	V18	GND	GND	AF21
A15	GND	GND	J25	V19	GND	GND	AF22
A16	GND	GND	J26	V20	GND	GND	AF23
A17	GND	GND	J27	V21	GND	GND	AF24
A18	GND	GND	J28	V22	GND	GND	AF25
A19	GND	GND	J29	V23	GND	GND	AF26
A20	GND	GND	J30	V24	GND	GND	AF27
A21	GND	GND	J31	V25	GND	GND	AF28
A22	GND	GND	J32	V26	GND	GND	AF29
A23	GND	GND	J33	V27	GND	GND	AF30
A24	GND	GND	J34	V28	GND	GND	AF31
A25	GND	GND	J35	V29	GND	GND	AF32
A26	GND	GND	J36	V30	GND	GND	AF33
A27	GND	GND	J37	V31	GND	GND	AF34
A28	GND	GND	J38	V32	GND	GND	AF35
A29	GND	GND	J39	V33	GND	GND	AF36
A30	GND	GND	J40	V34	GND	GND	AF37
A31	GND	GND	J41	V35	GND	GND	AF38
A32	GND	GND	J42	V36	GND	GND	AF39
A33	GND	GND	J43	V37	GND	GND	AF40
A34	GND	GND	J44	V38	GND	GND	AF41
A35	GND	GND	J45	V39	GND	GND	AF42
A36	GND	GND	J46	V40	GND	GND	AF43
A37	GND	GND	J47	V41	GND	GND	AF44
A38	GND	GND	J48	V42	GND	GND	AF45
A39	GND	GND	J49	V43	GND	GND	AF46
A40	GND	GND	J50	V44	GND	GND	AF47
A41	GND	GND	J51	V45	GND	GND	AF48
A42	GND	GND	J52	V46	GND	GND	AF49
A43	GND	GND	J53	V47	GND	GND	AF50
A44	GND	GND	J54	V48	GND	GND	AF51
A45	GND	GND	J55	V49	GND	GND	AF52
A46	GND	GND	J56	V50	GND	GND	AF53
A47	GND	GND	J57	V51	GND	GND	AF54
A48	GND	GND	J58	V52	GND	GND	AF55
A49	GND	GND	J59	V53	GND	GND	AF56
A50	GND	GND	J60	V54	GND	GND	AF57
A51	GND	GND	J61	V55	GND	GND	AF58
A52	GND	GND	J62	V56	GND	GND	AF59
A53	GND	GND	J63	V57	GND	GND	AF60
A54	GND	GND	J64	V58	GND	GND	AF61
A55	GND	GND	J65	V59	GND	GND	AF62
A56	GND	GND	J66	V60	GND	GND	AF63
A57	GND	GND	J67	V61	GND	GND	AF64
A58	GND	GND	J68	V62	GND	GND	AF65
A59	GND	GND	J69	V63	GND	GND	AF66
A60	GND	GND	J70	V64	GND	GND	AF67
A61	GND	GND	J71	V65	GND	GND	AF68
A62	GND	GND	J72	V66	GND	GND	AF69
A63	GND	GND	J73	V67	GND	GND	AF70
A64	GND	GND	J74	V68	GND	GND	AF71
A65	GND	GND	J75	V69	GND	GND	AF72
A66	GND	GND	J76	V70	GND	GND	AF73
A67	GND	GND	J77	V71	GND	GND	AF74
A68	GND	GND	J78	V72	GND	GND	AF75
A69	GND	GND	J79	V73	GND	GND	AF76
A70	GND	GND	J80	V74	GND	GND	AF77
A71	GND	GND	J81	V75	GND	GND	AF78
A72	GND	GND	J82	V76	GND	GND	AF79
A73	GND	GND	J83	V77	GND	GND	AF80
A74	GND	GND	J84	V78	GND	GND	AF81
A75	GND	GND	J85	V79	GND	GND	AF82
A76	GND	GND	J86	V80	GND	GND	AF83
A77	GND	GND	J87	V81	GND	GND	AF84
A78	GND	GND	J88	V82	GND	GND	AF85
A79	GND	GND	J89	V83	GND	GND	AF86
A80	GND	GND	J90	V84	GND	GND	AF87
A81	GND	GND	J91	V85	GND	GND	AF88
A82	GND	GND	J92	V86	GND	GND	AF89
A83	GND	GND	J93	V87	GND	GND	AF90
A84	GND	GND	J94	V88	GND	GND	AF91
A85	GND	GND	J95	V89	GND	GND	AF92
A86	GND	GND	J96	V90	GND	GND	AF93
A87	GND	GND	J97	V91	GND	GND	AF94
A88	GND	GND	J98	V92	GND	GND	AF95
A89	GND	GND	J99	V93	GND	GND	AF96
A90	GND	GND	J100	V94	GND	GND	AF97
A91	GND	GND	J101	V95	GND	GND	AF98
A92	GND	GND	J102	V96	GND	GND	AF99
A93	GND	GND	J103	V97	GND	GND	AF100
A94	GND	GND	J104	V98	GND	GND	AF101
A95	GND	GND	J105	V99	GND	GND	AF102
A96	GND	GND	J106	V100	GND	GND	AF103
A97	GND	GND	J107	V101	GND	GND	AF104
A98	GND	GND	J108	V102	GND	GND	AF105
A99	GND	GND	J109	V103	GND	GND	AF106
A100	GND	GND	J110	V104	GND	GND	AF107
A101	GND	GND	J111	V105	GND	GND	AF108
A102	GND	GND	J112	V106	GND	GND	AF109
A103	GND	GND	J113	V107	GND	GND	AF110
A104	GND	GND	J114	V108	GND	GND	AF111
A105	GND	GND	J115	V109	GND	GND	AF112
A106	GND	GND	J116	V110	GND	GND	AF113
A107	GND	GND	J117	V111	GND	GND	AF114
A108	GND	GND	J118	V112	GND	GND	AF115
A109	GND	GND	J119	V113	GND	GND	AF116
A110	GND	GND	J120	V114	GND	GND	AF117
A111	GND	GND	J121	V115	GND	GND	AF118
A112	GND	GND	J122	V116	GND	GND	AF119
A113	GND	GND	J123	V117	GND	GND	AF120
A114	GND	GND	J124	V118	GND	GND	AF121
A115	GND	GND	J125	V119	GND	GND	AF122
A116	GND	GND	J126	V120	GND	GND	AF123
A117	GND	GND	J127	V121	GND	GND	AF124
A118	GND	GND	J128	V122	GND	GND	AF125
A119	GND	GND	J129	V123	GND	GND	AF126
A120	GND	GND	J130	V124	GND	GND	AF127
A121	GND	GND	J131	V125	GND	GND	AF128
A122	GND	GND	J132	V126	GND	GND	AF129
A123	GND	GND	J133	V127	GND	GND	AF130
A124	GND	GND	J134	V128	GND	GND	AF131
A125	GND	GND	J135	V129	GND	GND	AF132
A126	GND	GND	J136	V130	GND	GND	AF133
A127	GND	GND	J137	V131	GND	GND	AF134
A128	GND	GND	J138	V132	GND	GND	AF135
A129	GND	GND	J139	V133	GND	GND	AF136
A130	GND	GND	J140	V134	GND	GND	AF137
A131	GND	GND	J141	V135	GND	GND	AF138
A132	GND	GND	J142	V136	GND	GND	AF139
A133	GND	GND	J143	V137	GND	GND	AF140
A134	GND	GND	J144	V138	GND	GND	AF141
A135	GND	GND	J145	V139	GND	GND	AF142
A136	GND	GND	J146	V140	GND	GND	AF143
A137	GND	GND	J147	V141	GND	GND	AF144
A138	GND	GND	J148	V142	GND	GND	AF145
A139	GND	GND	J149	V143	GND	GND	AF146
A140	GND	GND	J150	V144	GND	GND	AF147
A141	GND	GND	J151	V145	GND	GND	AF148
A142	GND	GND	J152	V146	GND	GND	AF149
A143	GND	GND	J153	V147	GND	GND	AF150
A144	GND	GND	J154	V148	GND	GND	AF151
A145	GND	GND	J155	V149	GND	GND	AF152
A146	GND	GND	J156	V150	GND	GND	AF153
A147	GND	GND	J157	V151	GND	GND	AF154
A148	GND	GND	J158	V152	GND	GND	AF155
A149	GND	GND	J159	V153	GND	GND	AF156
A150	GND	GND	J160	V154	GND	GND	AF157
A151	GND	GND	J161	V155	GND	GND	AF158
A152	GND	GND	J162	V156	GND	GND	AF159
A153	GND	GND	J163	V157	GND	GND	AF160
A154	GND	GND	J164	V158	GND	GND	AF161
A155	GND	GND	J165	V159	GND	GND	AF162
A156	GND	GND	J166	V160	GND	GND	AF163
A157	GND	GND	J167	V161	GND	GND	AF164
A158	GND	GND	J168	V162	GND	GND	AF165
A159	GND	GND	J169	V163	GND	GND	AF166
A160	GND	GND	J170	V164	GND	GND	AF167
A161	GND	GND	J171	V165	GND	GND	AF168
A162	GND	GND	J172	V166	GND	GND	AF169
A163	GND	GND	J173	V167	GND	GND	AF170
A164	GND	GND	J174	V168	GND	GND	AF171
A165	GND	GND	J175	V169	GND	GND	AF172
A166	GND	GND	J176	V170	GND	GND	AF173
A167	GND	GND	J177	V171	GND	GND	AF174
A168	GND	GND	J178	V172	GND	GND	AF175
A169	GND	GND	J179	V173	GND	GND	AF176
A170	GND	GND	J180	V174	GND	GND	AF177
A171	GND	GND	J181	V175	GND	GND	AF178
A172	GND	GND	J182	V176	GND	GND	AF179
A173	GND	GND	J183	V177	GND	GND	AF180
A174	GND	GND	J184	V178	GND	GND	AF181
A175	GND	GND	J185	V179	GND	GND	AF182
A176	GND	GND	J186	V180	GND	GND	AF183
A177	GND	GND	J187	V181	GND	GND	AF184
A178	GND	GND	J188	V182	GND	GND	AF185
A179	GND	GND	J189	V183	GND	GND	AF186
A180	GND	GND					





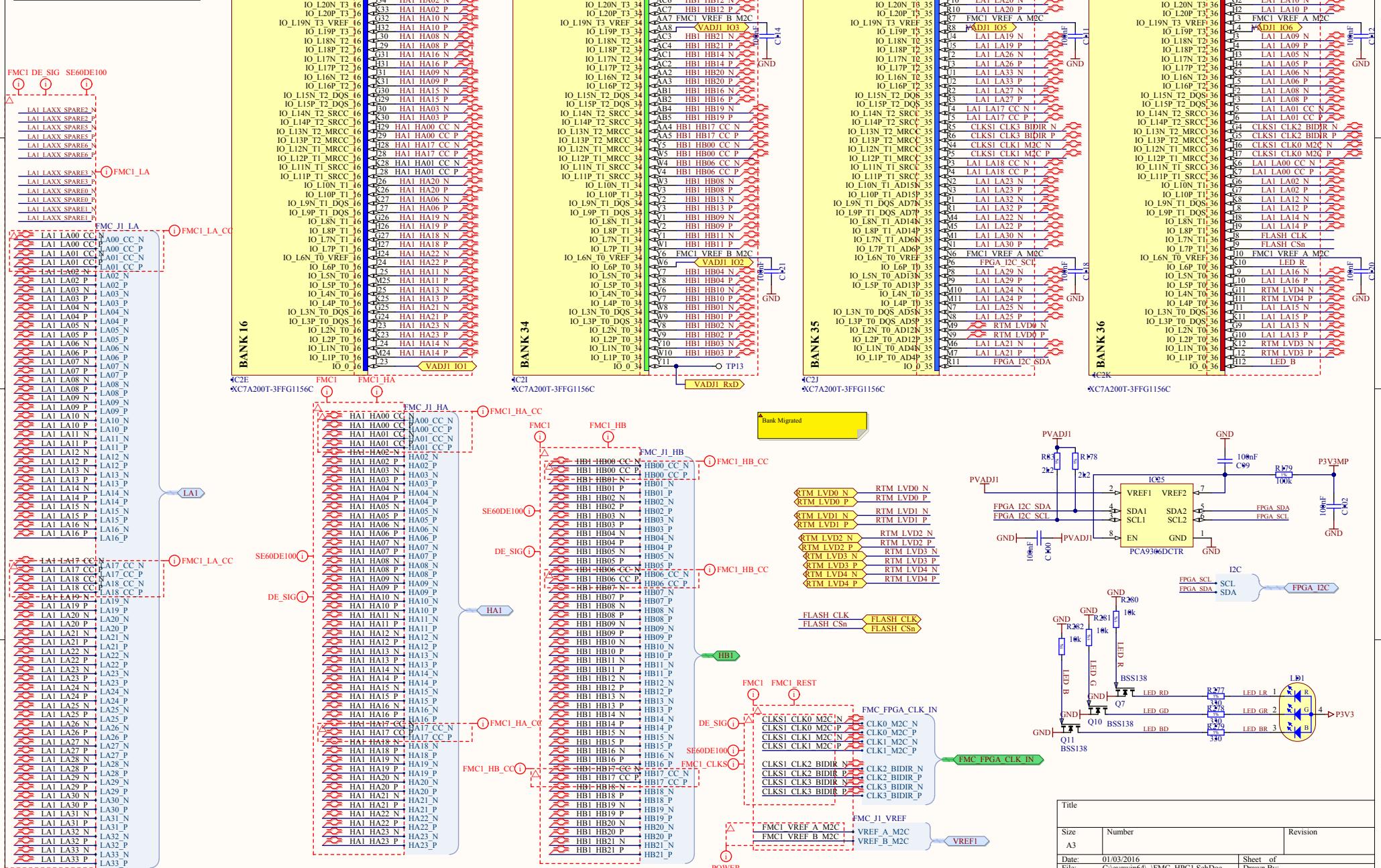
Copyright CNPEM 2012.

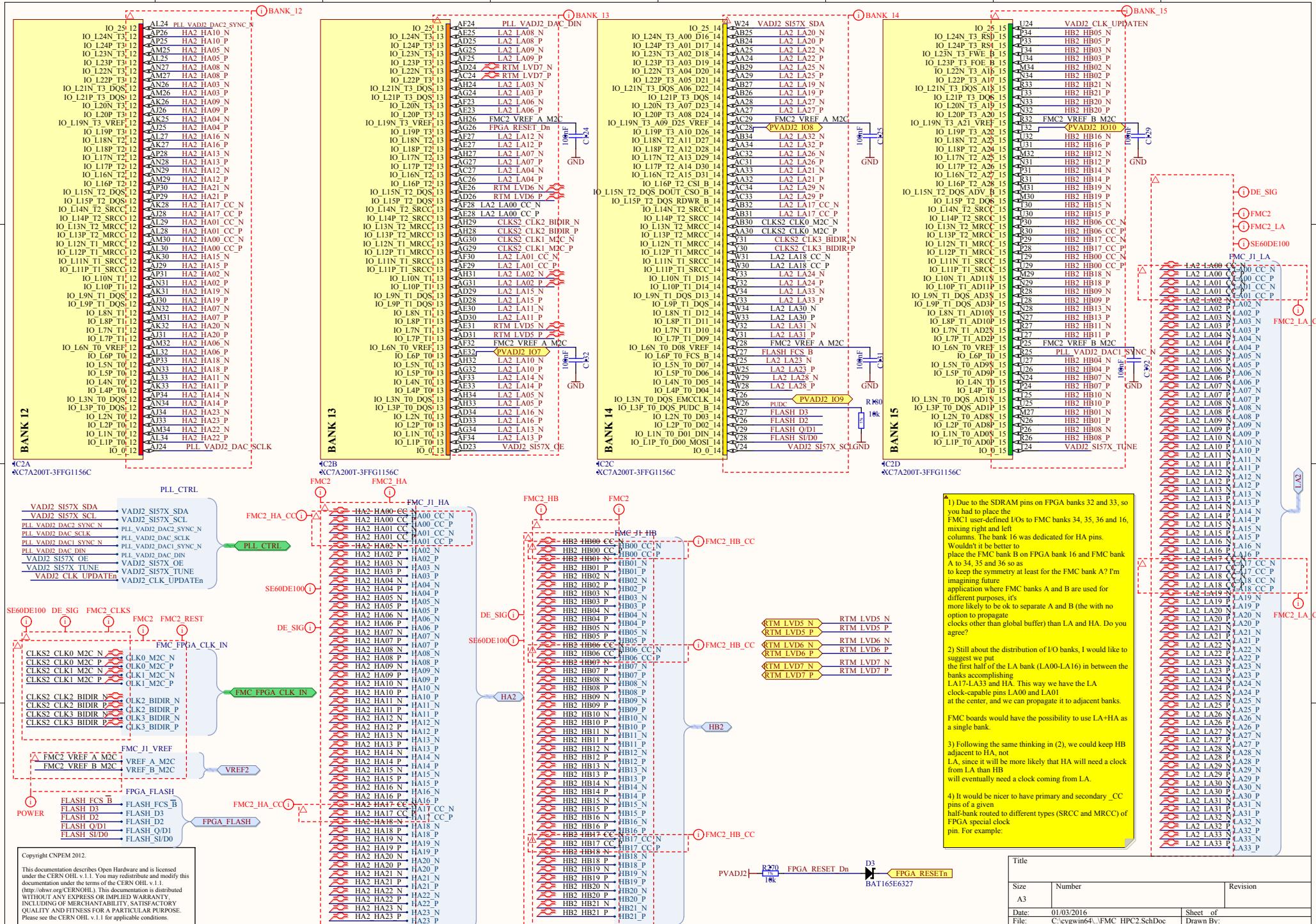
This documentation describes Open Hardware and is licensed under the CERN OHL v.1.1. You may redistribute and modify this documentation under the terms of the CERN OHL v.1.1. (<http://ohwr.org/CERNOHL>). This documentation is distributed WITHOUT ANY EXPRESS OR IMPLIED WARRANTY, INCLUDING MERCHANTABILITY, SATISFACTORY QUALITY AND FITNESS FOR A PARTICULAR PURPOSE. Please see the CERN OHL v.1.1 for applicable conditions.

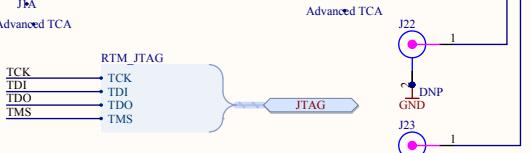
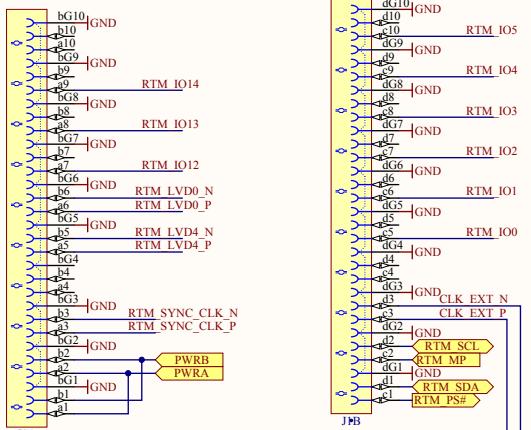
Title		
Size	Number	Revision
A3		
Date: 01/03/2016	Sheet of	
File: C:\cyview\64\1\FPGA_SDRAM.SchDoc	Drawn By:	

Copyright CNPEM 2012.

This documentation describes Open Hardware and is licensed under the CERN OHL v.1.1. You may redistribute and modify this documentation under the terms of the CERN OHL v.1.1. (<http://ohwr.org/CERNOHL>). This documentation is distributed WITHOUT ANY EXPRESS OR IMPLIED WARRANTY, INCLUDING MERCHANTABILITY, SATISFACTORY QUALITY AND FITNESS FOR A PARTICULAR PURPOSE. Please see the CERN OHL v.1.1 for applicable conditions.





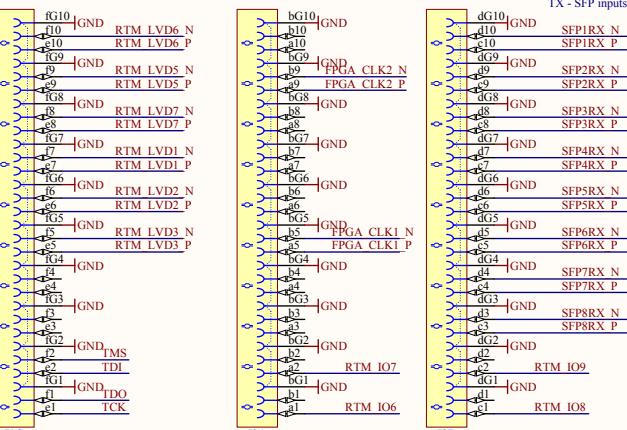


not present in XC7A200T

IO_25	31	E7
IO_124N	T3	37
IO_124P	T3	37
IO_123N	T3	37
IO_123P	T3	37
IO_122N	T3	37
IO_122P	T3	37
O_L21N	T3	DQ5
O_L21P	T3	DQ5
IO_120N	T3	37
IO_120P	T3	37
I_L19N	T3	VREF
I_L19P	T3	VREF
IO_117N	T3	37
IO_117P	T3	37
IO_116N	T3	37
IO_116P	T2	37
O_L15N	T2	DQ5
O_L15P	T2	DQ5
I_L14N	T2	SRCC
D_L14P	T2	SRCC
I_L13N	T2	MRCC
I_L13P	T2	MRCC
I_L12N	T1	MRCC
I_L12P	T1	MRCC
I_L11N	T1	SRCC
D_L11P	T1	SRCC
IO_110N	T1	37
IO_110P	T1	37
I_O_9N	T1	DQ5
IO_109P	T1	DQ5
IO_108	T1	37
IO_108P	T1	37
IO_107N	T1	37
IO_107P	T1	37
O_L6N	T0	VREF

BANK 37

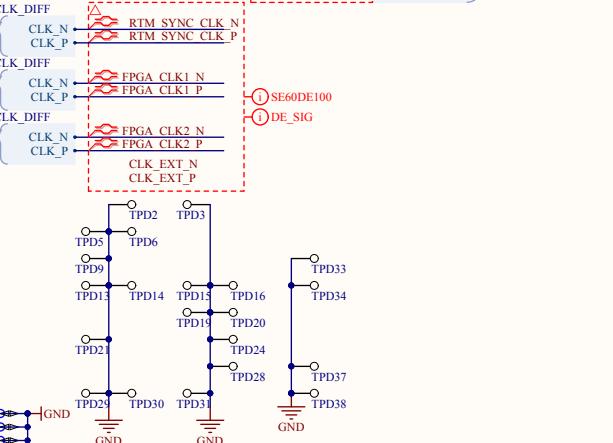
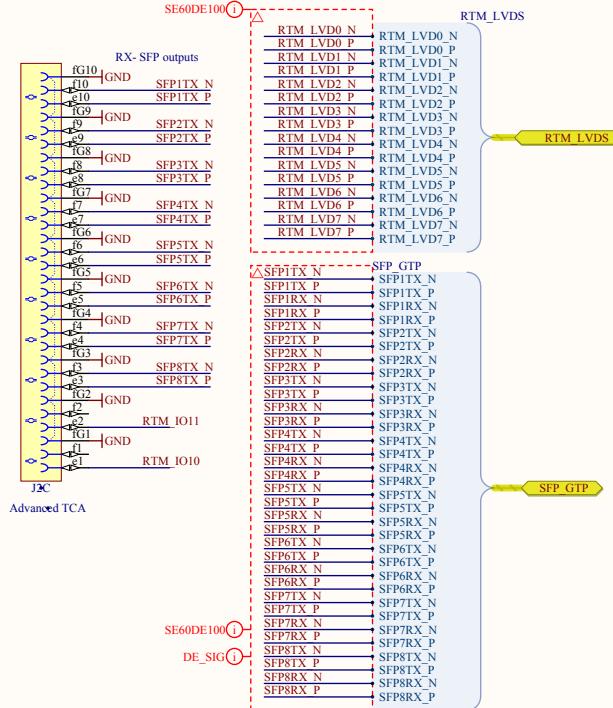
2L
C7A200T-3EEG1156C



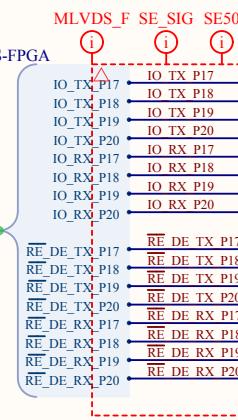
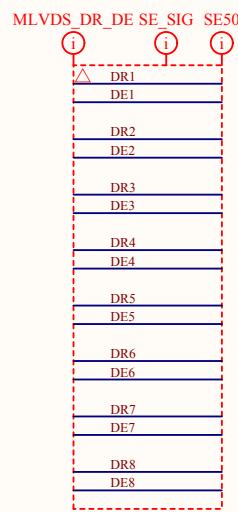
in XC7A200T	
I0	15_7
I0_L24N	T3_17
I0_L24P	T3_17
I0_L23N	T3_17
I0_L23P	T3_17
I0_L22N	T3_17
I0_L22P	T3_17
I0_L21N	T3_DQS_17
I0_L21P	T3_DQS_17
I0_L20N	T3_17
I0_L20P	T3_17
I0_L19N	T3_VREF_17
I0_L19P	T3_VREF_17
I0_L18N	T2_17
I0_L18P	T2_17
I0_L17N	T2_17
I0_L17P	T2_17
I0_L16N	T2_17
I0_L16P	T2_17
I0_L15N	T2_DQS_17
I0_L15P	T2_DQS_17
I0_L14N	T2_SRCC_17
I0_L14P	T2_SRCC_17
I0_L13N	T2_MRCC_17
I0_L13P	T2_MRCC_17
I0_L12N	T1_MRCC_17
I0_L12P	T1_MRCC_17
I0_L11N	T1_SRCC_17
I0_L11P	T1_SRCC_17
I0_L10N	T1_17
I0_L10P	T1_17
I0_L9N	T1_DQS_17
I0_L9P	T1_DQS_17
I0_L8N	T1_17
I0_L8P	T1_17
I0_L7N	T1_17
I0_L7P	T1_17
I0_L6N	T0_VREF_17
I0_L6P	T0_VREF_17
I0_L5N	T0_17
I0_L5P	T0_17
I0_L4N	T0_17
I0_L4P	T0_17
I0_L3N	T0_DQS_17
I0_L3P	T0_DQS_17
I0_L2N	T0_17
I0_L2P	T0_17
I0_L1N	T0_17
I0_L1P	T0_17
I0_L0N	T0_17

BANK 17

A200T-3FFG1156C



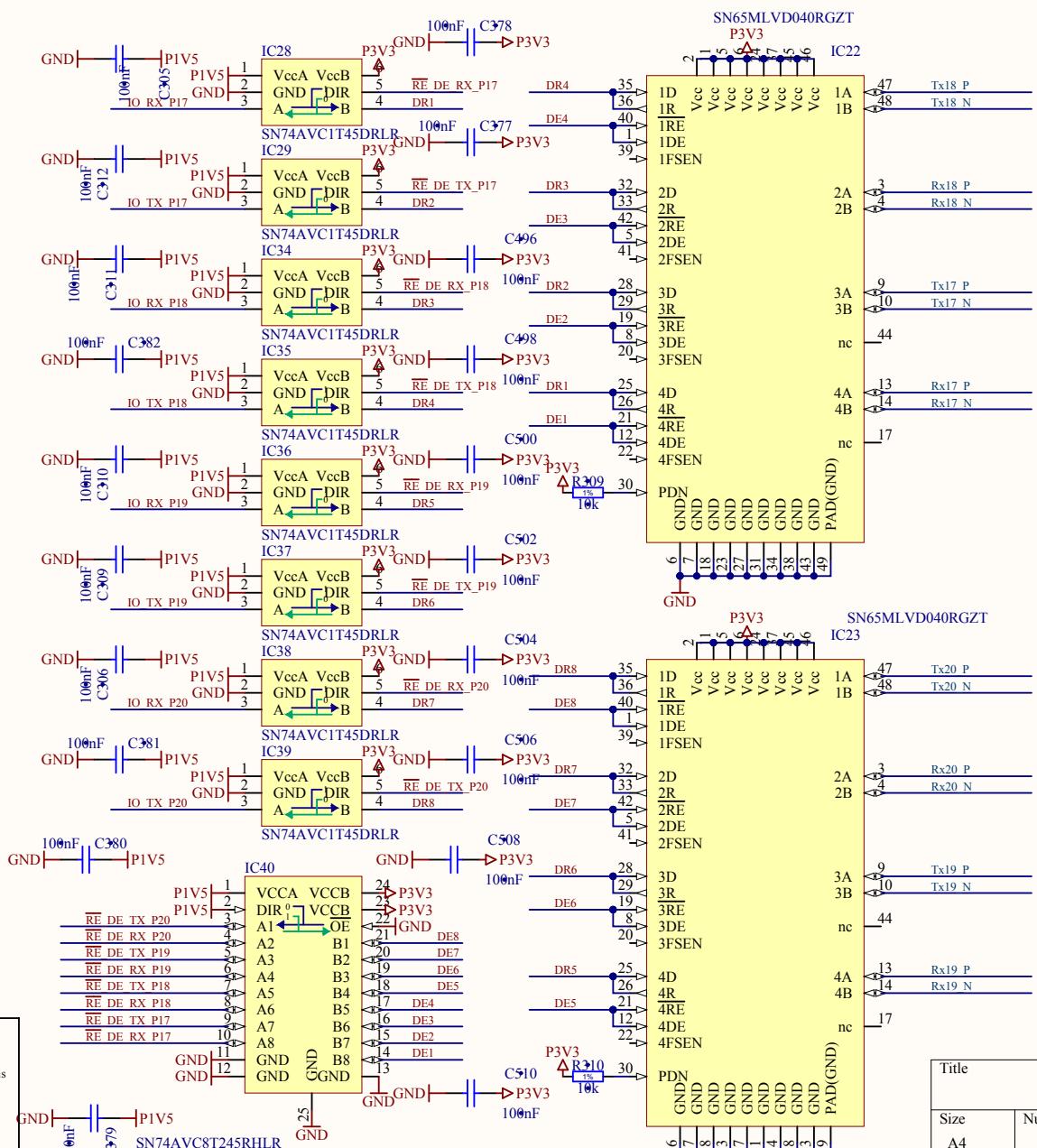
Title		Revision
Size	Number	
A3		
Date:	01/03/2016	Sheet of
File:	C:\cygwin64\RTM.CON.SchDoc	Drawn By:



D

Copyright CNPEM 2012.

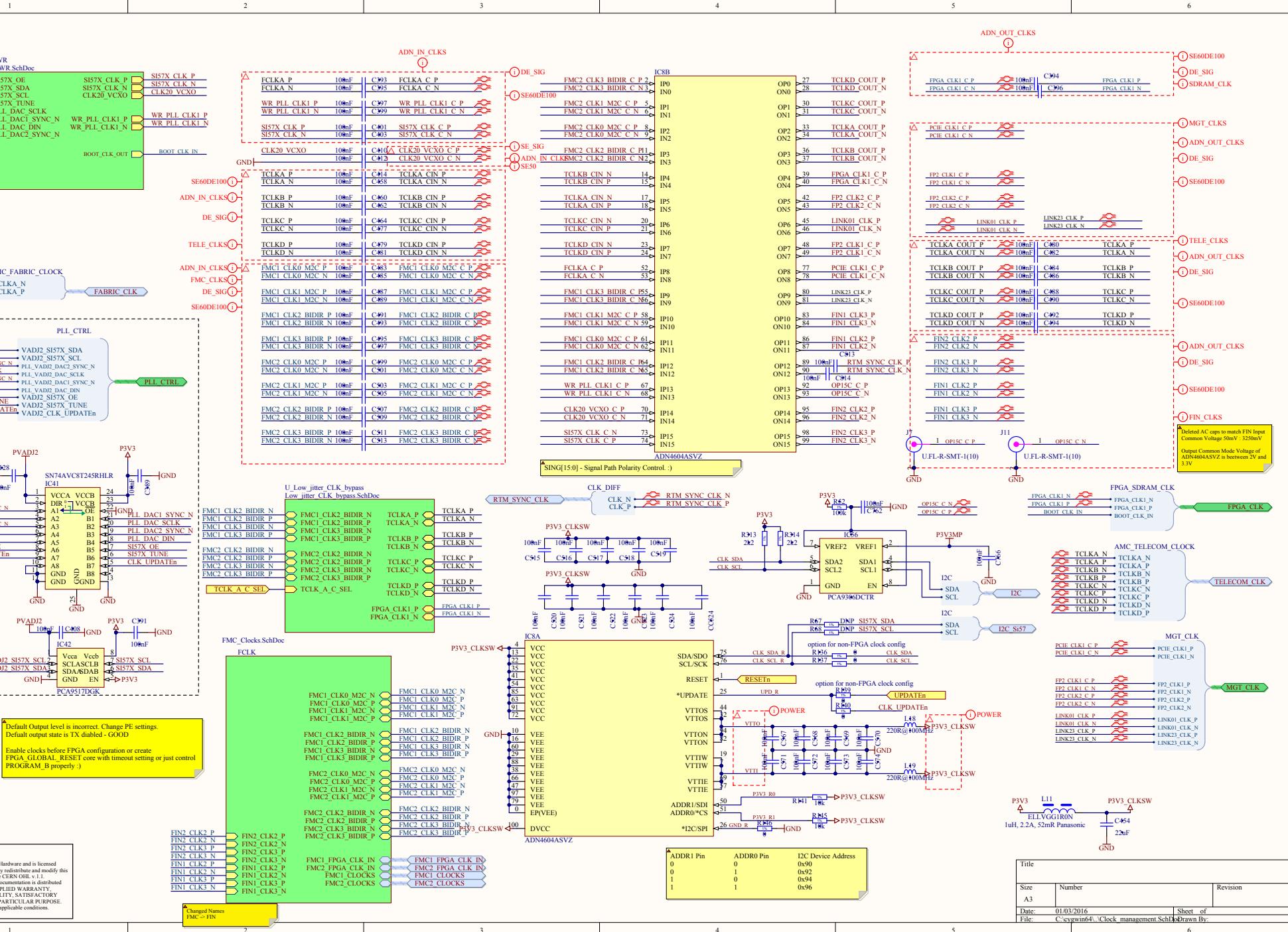
This documentation describes Open Hardware and is licensed under the CERN OHL v.1.1. You may redistribute and modify this documentation under the terms of the CERN OHL v.1.1 (<http://ohl.cern.org/CERNohl.html>). This documentation is distributed WITHOUT ANY EXPRESS OR IMPLIED WARRANTY, INCLUDING MERCHANTABILITY, SATISFACTORY QUALITY AND FITNESS FOR A PARTICULAR PURPOSE. Please see the CERN OHL v.1.1 for applicable conditions.



D

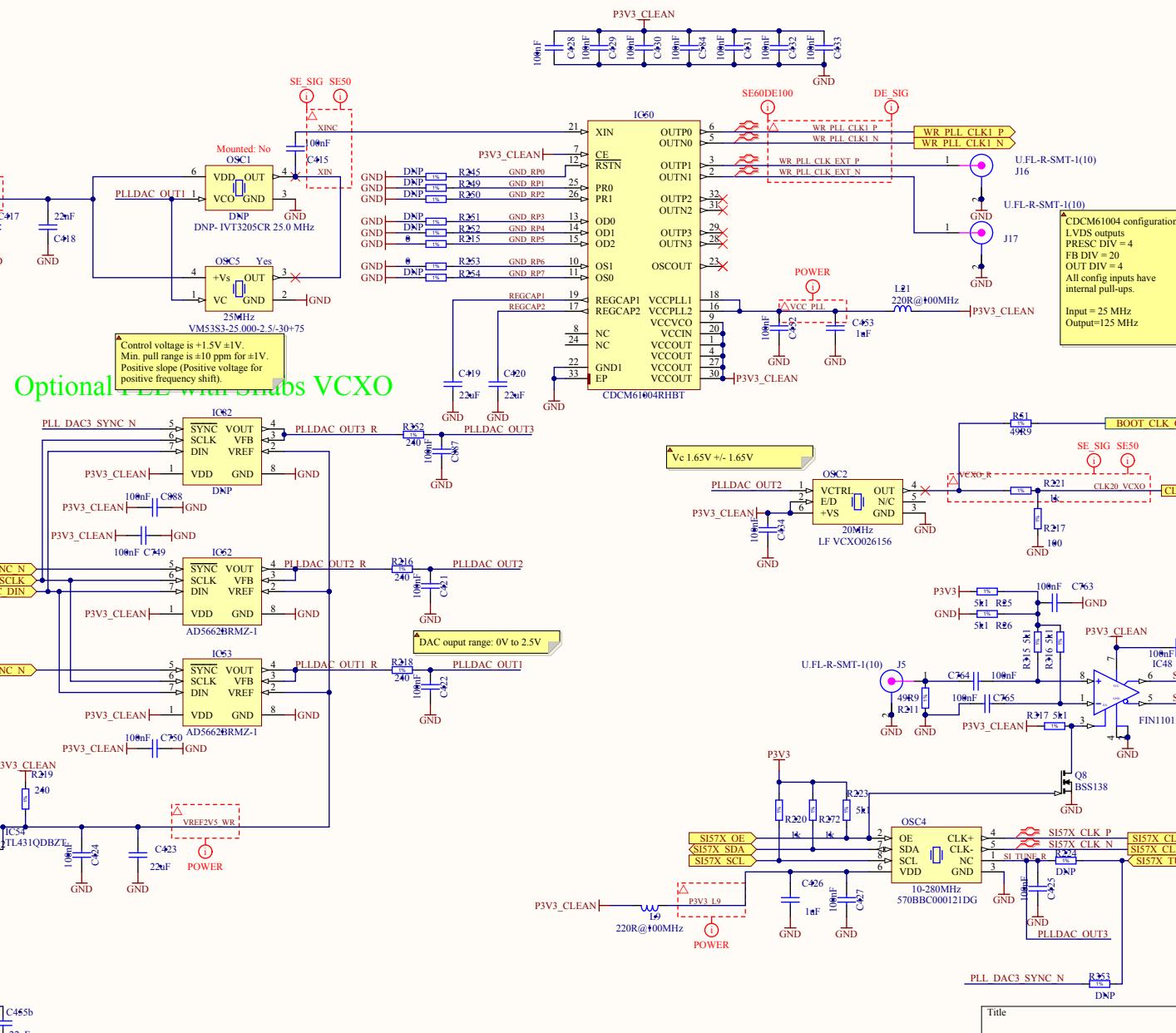
Title _____

Size	Number	Revision
A4	_____	_____
Date:	01/03/2016	Sheet of _____
File:	C:\cygwin64\...\M-LVDS PHY.SchDoc	Drawn By: _____



Copyright CNPME 2012.

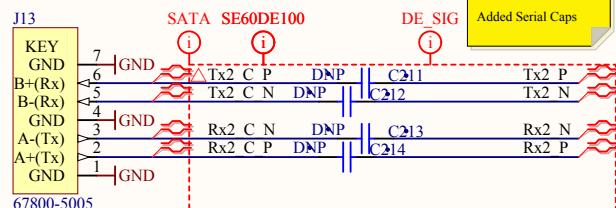
This documentation describes Open Hardware and is licensed under the terms of the CERN OHL v.1.1. You may redistribute and modify this documentation under the terms of the CERN OHL v.1.1. (<http://ohwr.org/CERNOHL>). This documentation is distributed WITHOUT ANY WARRANTY, without even the implied warranty of MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, or NON-INFRINGEMENT. Please see the CERN OHL v.1.1 for applicable conditions.



Title		
Size	Number	Revision
A3		
Date:	01/03/2016	Sheet of
File:	C:\cygwin64\Clock WR.SchDoc	Drawn By:

SATA naming is relative to HOST

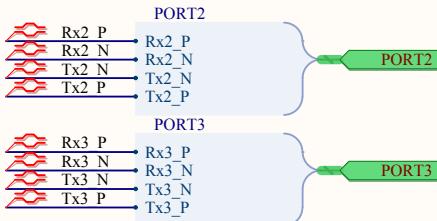
For normal SATA cables apply:
B = HOST SATA RX
A = HOST SATA TX



Apply to all AMC ports: see table 6-1 PICMG AMC.0 R2.0 1.5.11.2006

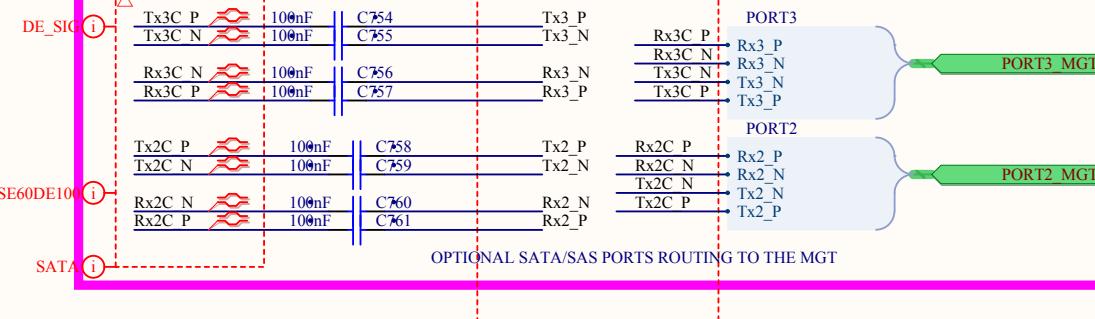
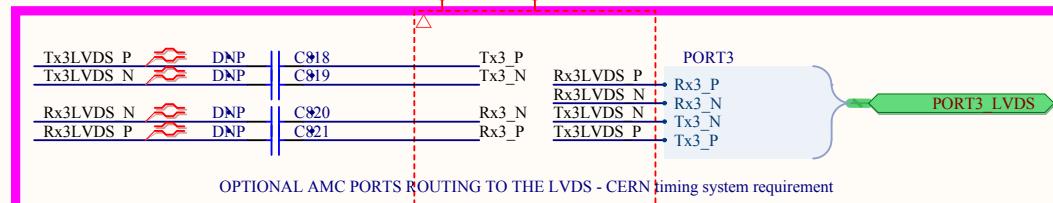
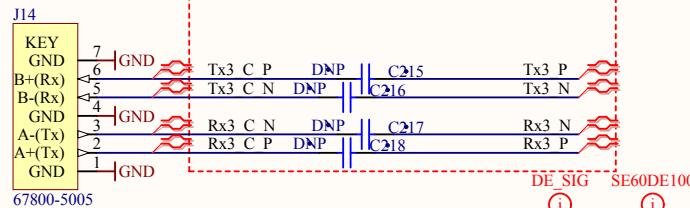
RXes are CARRIER-OUTPUT

TXes are CARRIER-INPUT



Carrier is a HOST

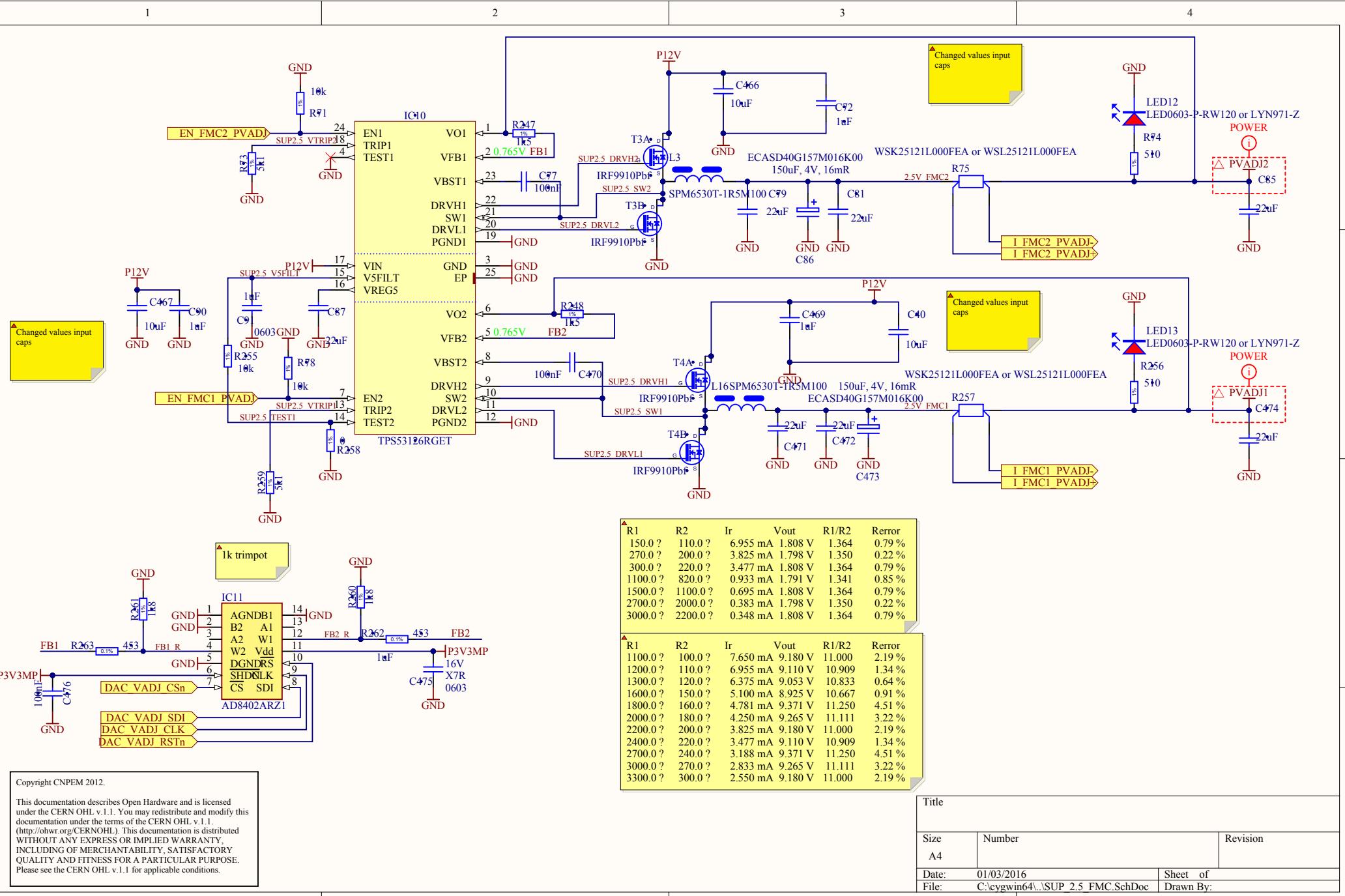
There also Exist a Cross-Over SATA Cable so always there is a possibility to change that

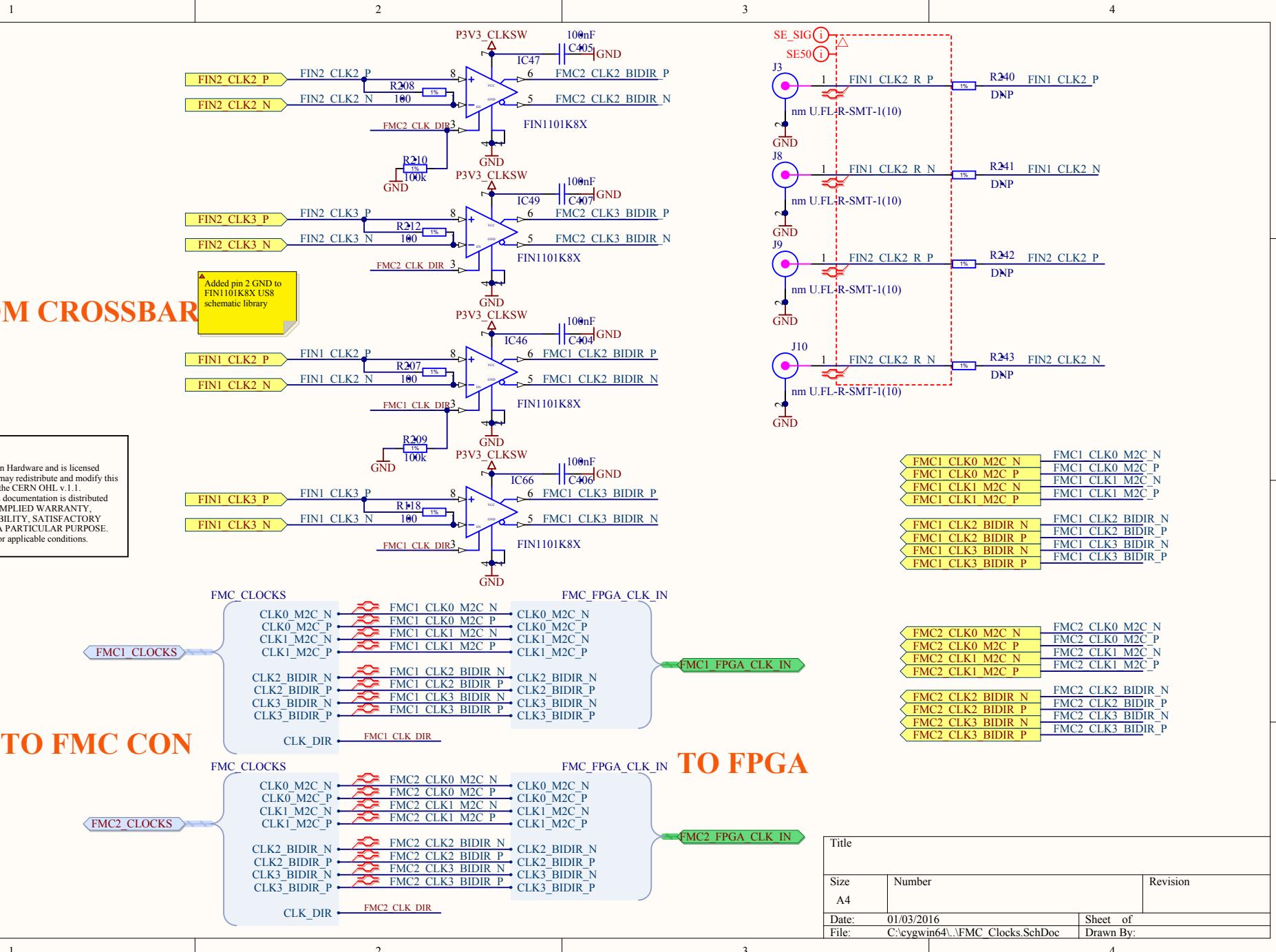


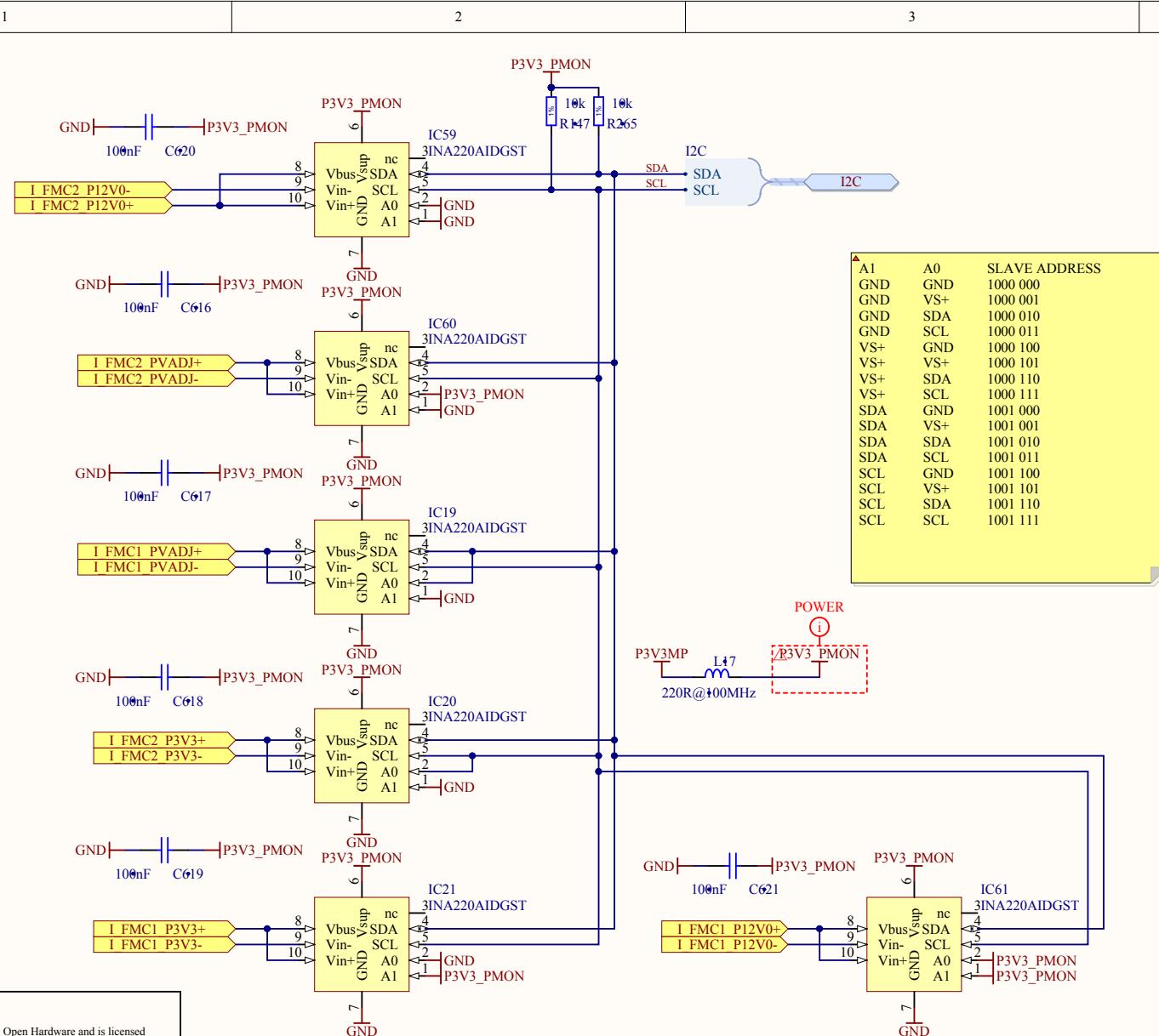
Copyright CNPEM 2012.

This documentation describes Open Hardware and is licensed under the terms of the CERN OHL v.1.1. You may redistribute and modify this documentation under the terms of the CERN OHL v.1.1. (<http://ohwr.org/CERNOHL>). This documentation is distributed WITHOUT ANY EXPRESS OR IMPLIED WARRANTY, INCLUDING MERCHANTABILITY, SATISFACTORY QUALITY AND FITNESS FOR A PARTICULAR PURPOSE. Please see the CERN OHL v.1.1 for applicable conditions.

Title		
Size	Number	Revision
A4		
Date: 01/03/2016	Sheet of	
File: C:\cygwin64\AMC-SATA.SchDoc	Drawn By:	



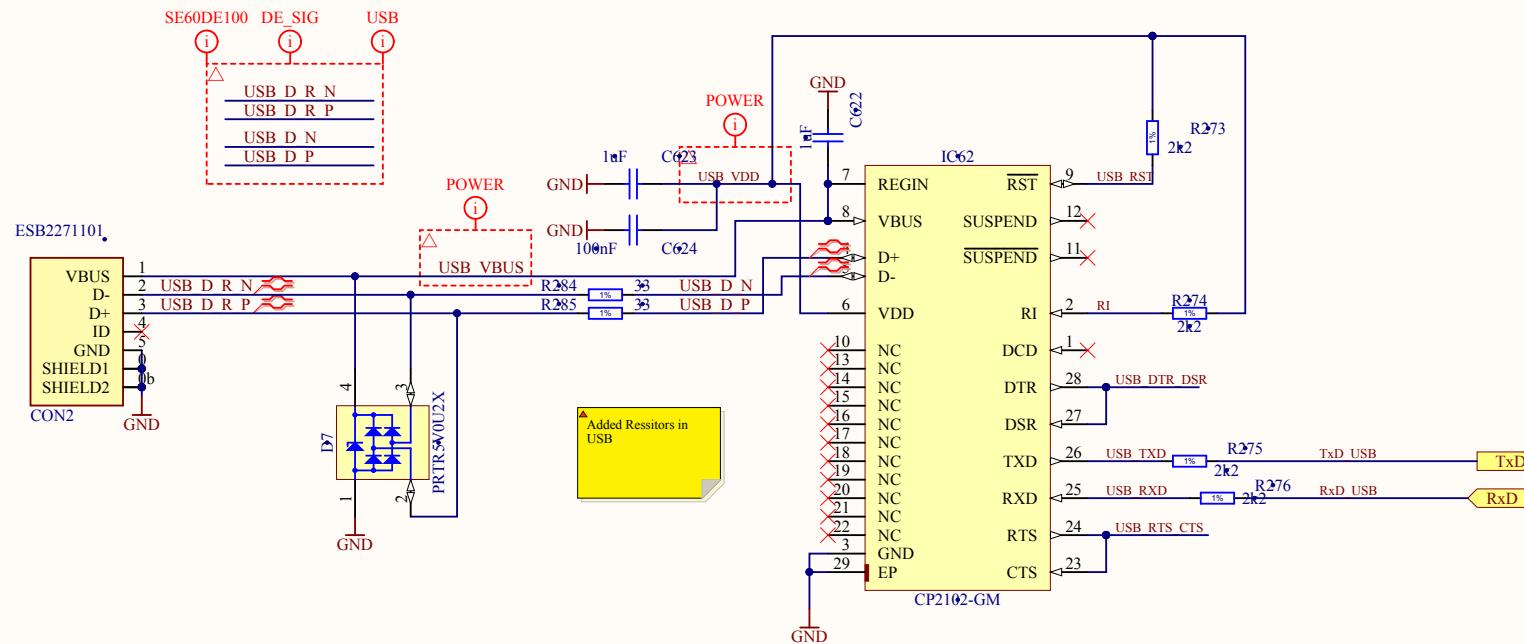




Copyright CNPEM 2012.

This documentation describes Open Hardware and is licensed under the CERN OHL v.1.1. You may redistribute and modify this documentation under the terms of the CERN OHL v.1.1.
(<http://ohwr.org/CERNOHL>). This documentation is distributed WITHOUT ANY EXPRESS OR IMPLIED WARRANTY,
INCLUDING OF MERCHANTABILITY, SATISFACTORY
QUALITY AND FITNESS FOR A PARTICULAR PURPOSE.
Please see the CERN OHL v.1.1 for applicable conditions.

Title		
Size A4	Number	Revision
Date:	01/03/2016	Sheet of
File:	C:\cygwin64\UI_mon.SchDoc	Drawn By:

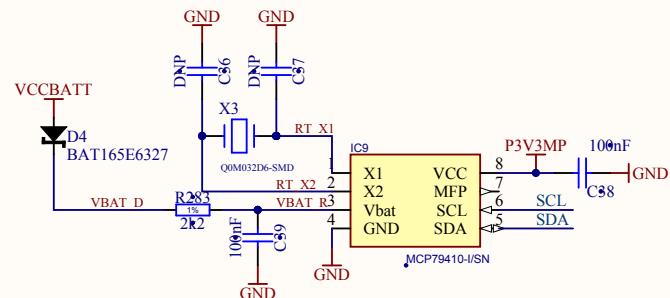


Copyright CNPEM 2012.

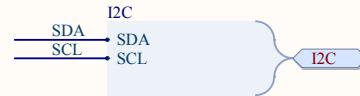
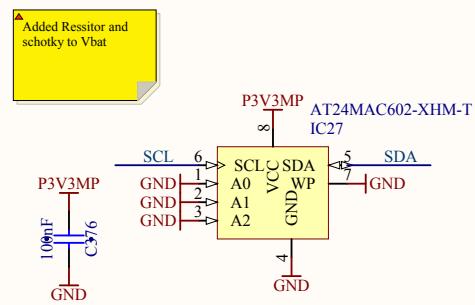
This documentation describes Open Hardware and is licensed under the CERN OHL v.1.1. You may redistribute and modify this documentation under the terms of the CERN OHL v.1.1. (<http://ohwr.org/CERNOHL>). This documentation is distributed WITHOUT ANY EXPRESS OR IMPLIED WARRANTY, INCLUDING MERCHANTABILITY, SATISFACTORY QUALITY AND FITNESS FOR A PARTICULAR PURPOSE. Please see the CERN OHL v.1.1 for applicable conditions.

Title		
Size	Number	Revision
A4		
Date: 01/03/2016	Sheet of	
File: C:\cygwin64\.\USB_UART.SchDoc	Drawn By:	

A



B



C

Copyright CNPEM 2012.

This documentation describes Open Hardware and is licensed under the CERN OHL v.1.1. You may redistribute and modify this documentation under the terms of the CERN OHL v.1.1. (<http://ohwr.org/CERNOHL>). This documentation is distributed WITHOUT ANY EXPRESS OR IMPLIED WARRANTY, INCLUDING OF MERCHANTABILITY, SATISFACTORY QUALITY AND FITNESS FOR A PARTICULAR PURPOSE. Please see the CERN OHL v.1.1 for applicable conditions.

Title

Size

A4

Number

Revision

Date:

01/03/2016

Sheet of

File:

C:\cygwin64\RTCE.SchDoc

Drawn By:

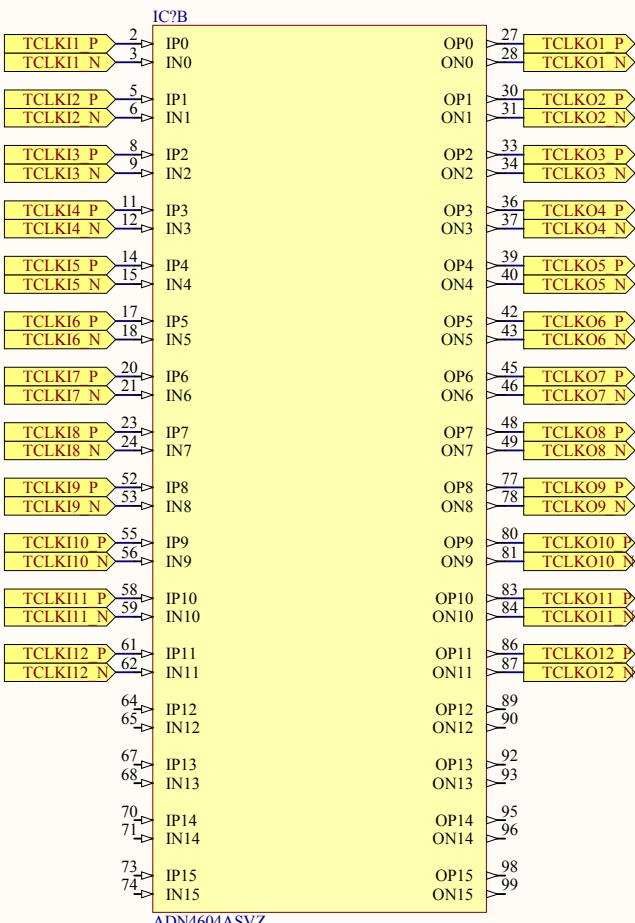
1

2

3

4

A

**IC?A**

4	VCC	75 SDA/SDO
13	VCC	76 SCL/SCK
22	VCC	
35	VCC	
41	VCC	RESET 1
54	VCC	*UPDATE 25
85	VCC	44 VTTOS
63	VCC	32 VTTOS
91	VCC	
72	VCC	
10	VEE	94 VTTON
16	VEE	82 VTTON
60	VEE	
29	VEE	19 VTTIW
88	VEE	7 VTTIW
38	VEE	
66	VEE	69 VTTIE
47	VEE	57 VTTIE
97	VEE	
79	VEE	
101	EP(VEE)	50 ADDR1/SDI
		51 ADDR0/*CS
100	DVCC	26 *I2C/SPI

ADN4604ASVZ

SDA/SDO
SCL/SCK
RESET
*UPDATE
VTTOS
VTTOS
VTTON
VTTON
VTTIW
VTTIW
VTTIE
VTTIE
ADDR1/SDI
ADDR0/*CS
*I2C/SPI

- SDA
- SCL
- SYNC
- CLK
- DATA
- LE1
- LE2
- OE
- GOE1
- GOE2

C

MUX1 SEL
MUX1 SEL
MUX1 SEL
MUX2 SEL
MUX2 SEL
MUX2 SEL

1

2

3

4

D

1

2

3

4

A

A

B

B

C

C

D

D



0805_0.1μF_50V_±25% X7R

1

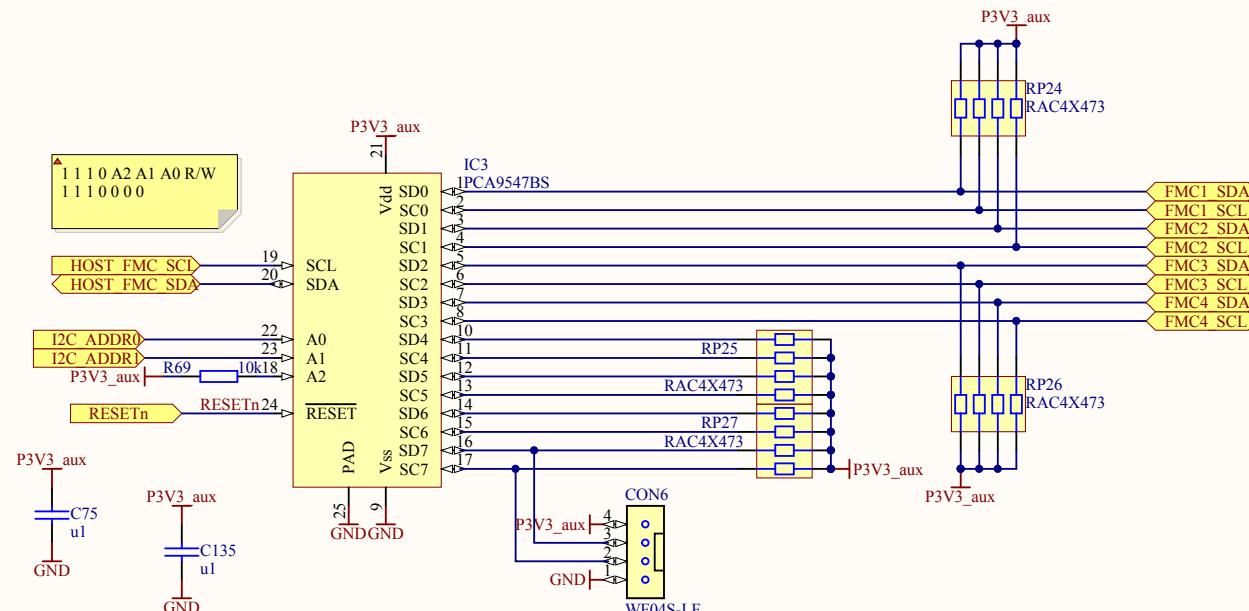
2

3

4

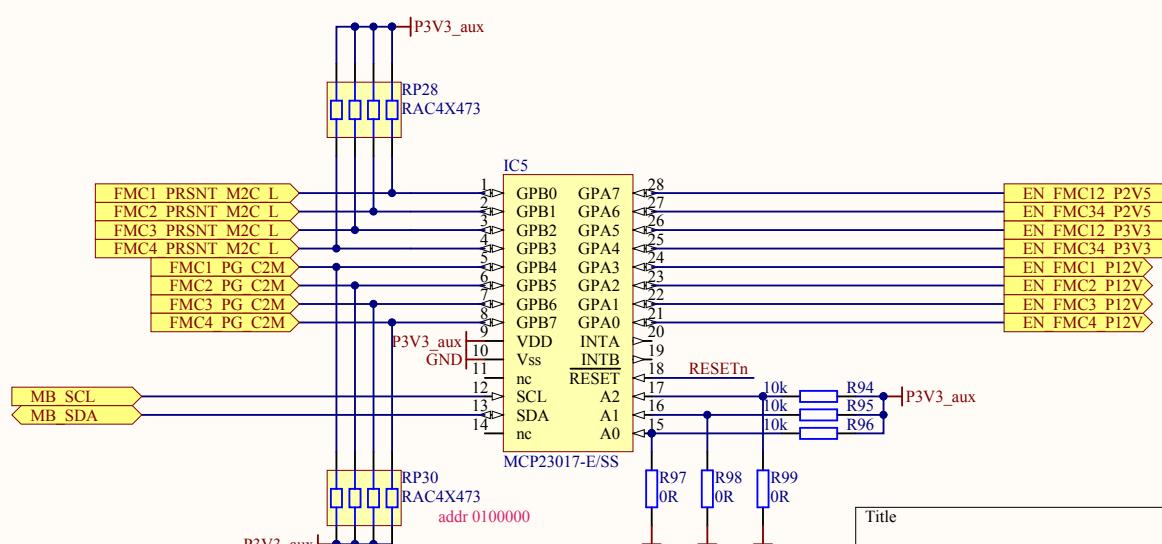
Title		
Size A4	Number	Revision
Date: 01/03/2016		Sheet of
File: C:\cygwin64\.\HeightRuleRoom1.9mm.SchDrawn By:		

A



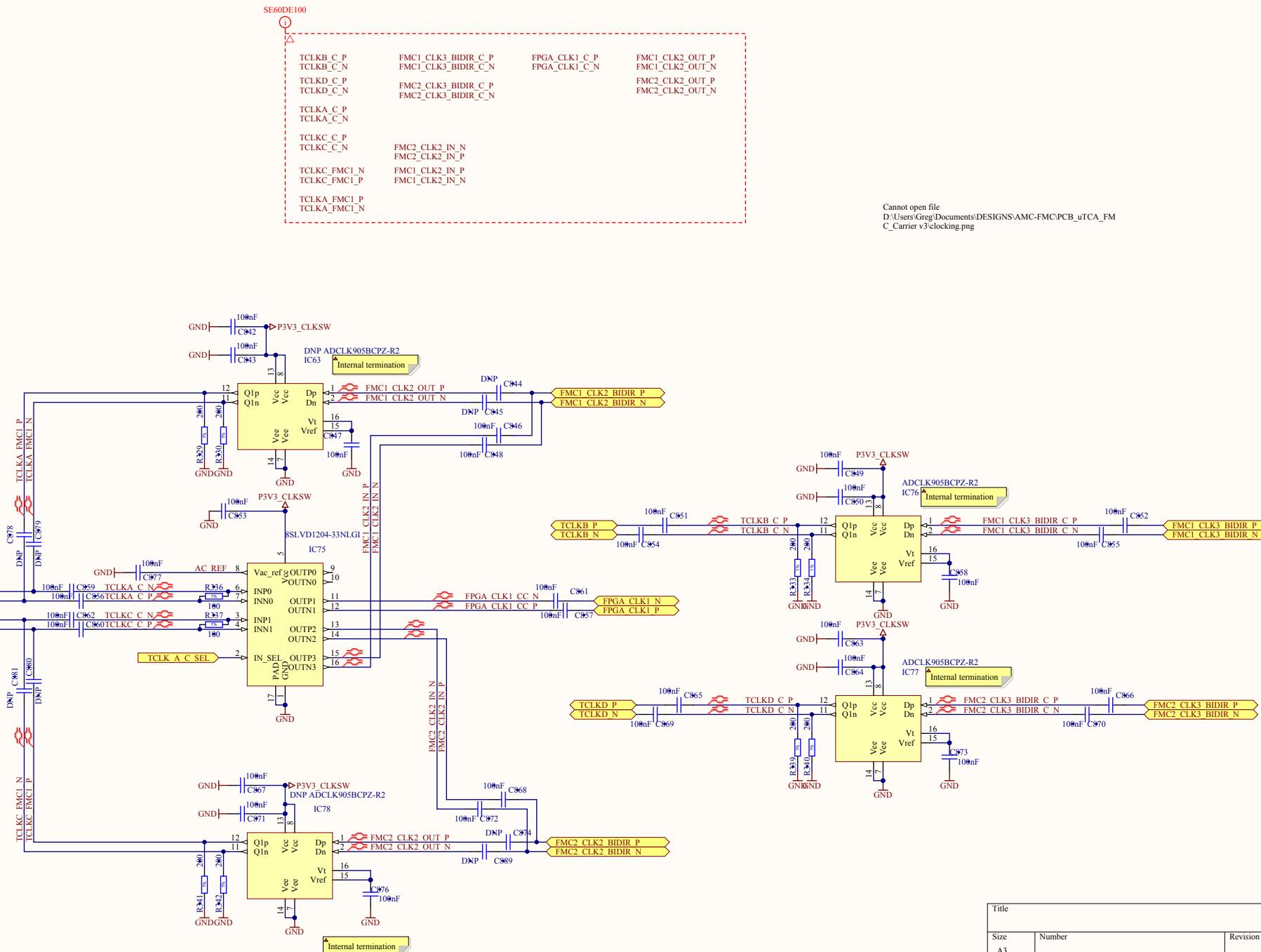
B

C

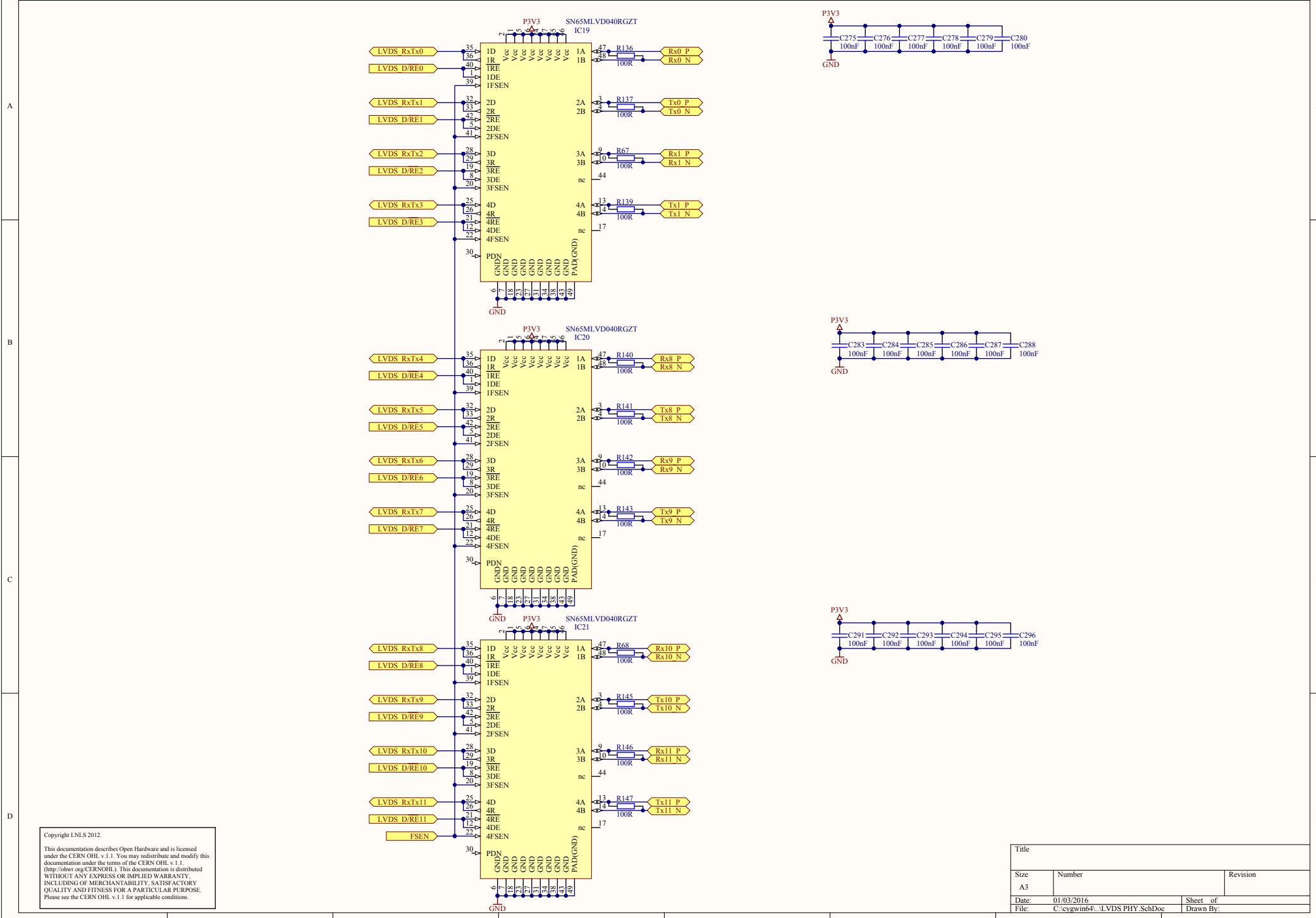


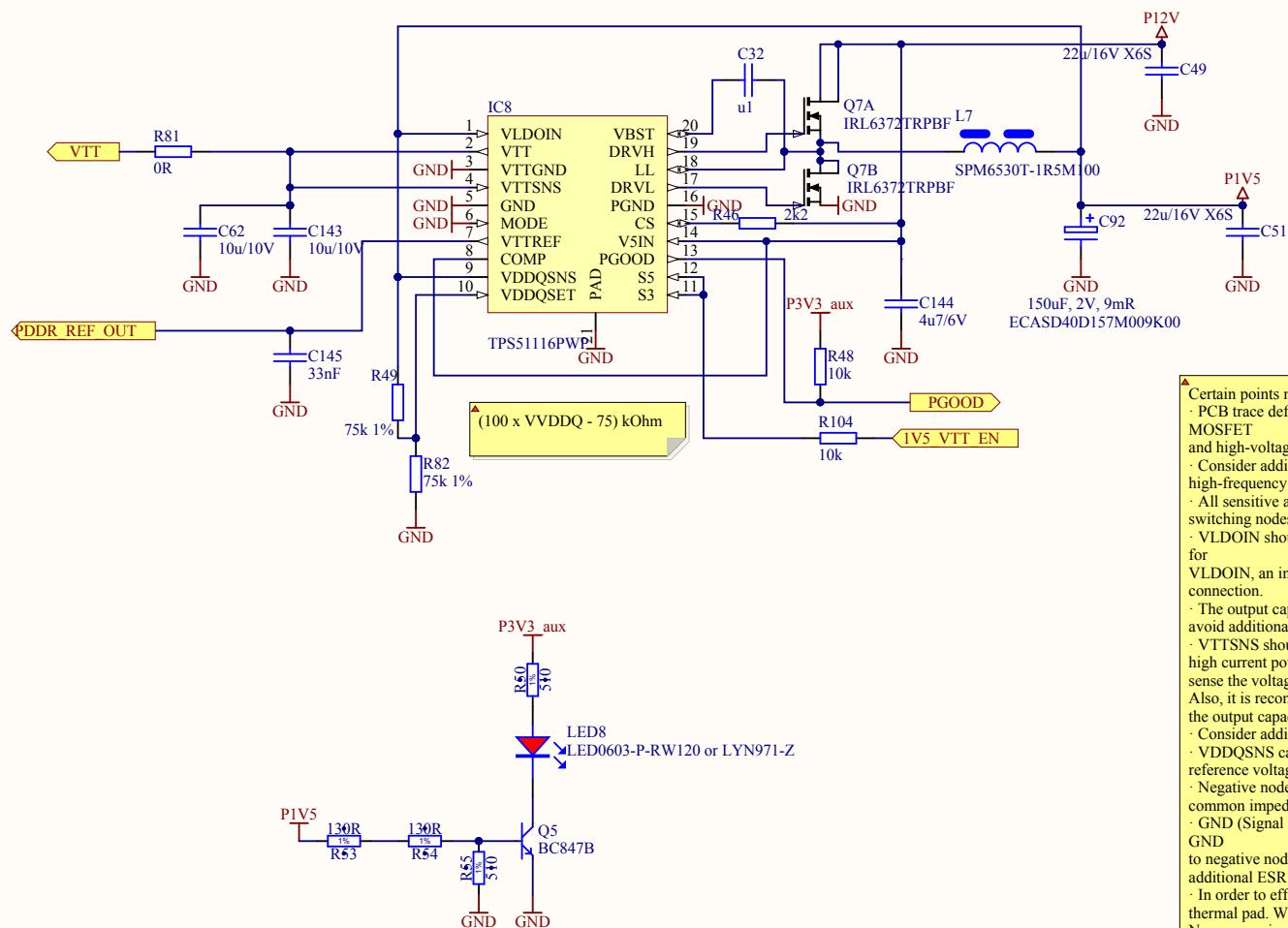
D

Title		
Size	Number	Revision
A4		
Date: 01/03/2016	Sheet of	
File: C:\cygwin64\I2C switch.SchDoc	Drawn By:	



Cannot open file
D:\Users\Greg\Documents\DESIGNS\AMC-FMC\PCB_uTCA_FM
C Carrier v3\clocking.png





P1V5 current output: 10mR -> 10mV per Amp, with 100x gain gives 2A range with 2.048V

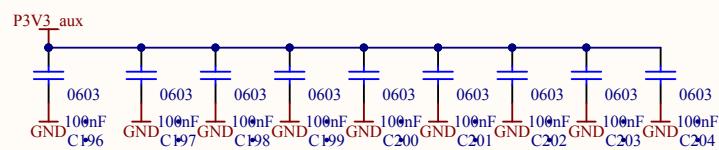
▲ Certain points must be considered before designing a layout using the TPS51116.
 - PCB trace defined as LL node, which connects to source of switching MOSFET, drain of rectifying MOSFET and high-voltage side of the inductor, should be as short and wide as possible.
 - Consider adding a small snubber circuit, consists of 3 W and 1 nF, between LL and PGND in case a high-frequency surge is observed on the LL voltage waveform.
 - All sensitive analog traces such as VDDQSNS, VTTNS and CS should placed away from high-voltage switching nodes such as LL, DRVL or DRVH nodes to avoid coupling.
 - VLDOIN should be connected to VDDQ output with short and wide trace. If different power source is used for VLDOIN, an input bypass capacitor should be placed to the pin as close as possible with short and wide connection.
 - The output capacitor for VTT should be placed close to the pin with short and wide connection in order to avoid additional ESR and/or ESL of the trace.
 - VTTNS should be connected to the positive node of VTT output capacitor(s) as a separate trace from the high current power line and is strongly recommended to avoid additional ESR and/or ESL. If it is needed to sense the voltage of the point of the load, it is recommended to attach the output capacitor(s) at that point. Also, it is recommended to minimize any additional ESR and/or ESL of ground trace between GND pin and the output capacitor(s).
 - Consider adding LPF at VTTNS in case ESR of the VTT output capacitor(s) is larger than 2 mW.
 - VDDQSNS can be connected separately from VLDOIN. Remember that this sensing potential is the reference voltage of VTREF. Avoid any noise generative lines.
 - Negative node of VTT output capacitor(s) and VTREF capacitor should be tied together by avoiding common impedance to the high current path of the VTT source/sink current.
 - GND (Signal GND) pin node represents the reference potential for VTREF and VTT outputs. Connect GND to negative nodes of VTT capacitor(s), VTREF capacitor and VDDQ capacitor(s) with care to avoid additional ESR and/or ESL. GND and PGND (power ground) should be connected together at a single point.
 - In order to effectively remove heat from the package, prepare thermal land and solder to the package's thermal pad. Wide trace of the component-side copper, connected to this thermal land, helps heat spreading. Numerous vias with a 0.33-mm diameter connected from the thermal land to the internal/solder-side ground plane(s) should be used to help dissipation. Do NOT connect PGND to this thermal land underneath the package.

Copyright LNLs 2012.

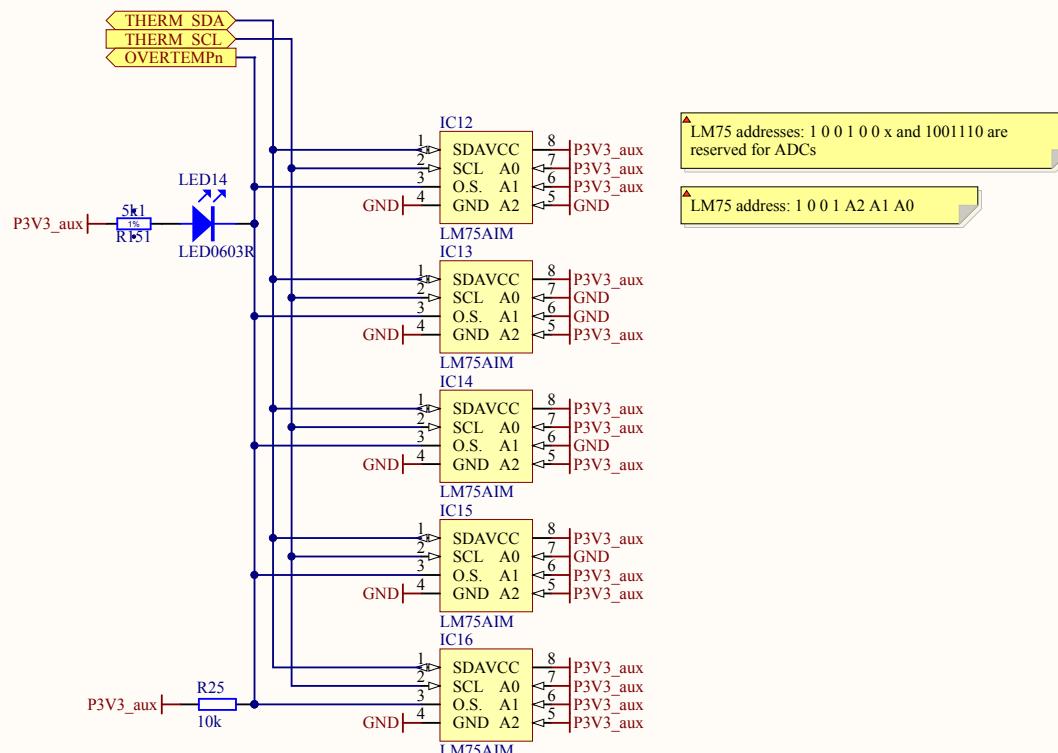
This documentation describes Open Hardware and is licensed under the terms of the CERN OHL v.1.1. You may redistribute and modify this documentation under the terms of the CERN OHL v.1.1. (<http://ohwr.org/CERNOHL>). This documentation is distributed WITHOUT ANY EXPRESS OR IMPLIED WARRANTY, INCLUDING MERCHANTABILITY, SATISFACTORY QUALITY AND FITNESS FOR A PARTICULAR PURPOSE. Please see the CERN OHL v.1.1 for applicable conditions.

Title		
Size	Number	Revision
A4		
Date: 01/03/2016	Sheet of	
File: C:\cygwin64\...\SUP_1.5_VTT.SchDoc	Drawn By:	

A



B



C

D

Title		
Size	Number	Revision
A4		
Date: 01/03/2016	Sheet of	
File: C:\cygwin64\.\THERMAL MANAGEMENT.Dwg	16	Doc