Assignment 4:

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Question 1:

Virtual address bit: $\log_2 2^{32} = 32$ bit

Physical address bit: $\log_2 2^{18} = 18$ bit

Number of entries (Page table length registers): $2^{32} / 2^{11} = 2^{21}$ entries

Page size: 4096 bytes = 2^{11} bytes => Page offset: $\log_2 2^{11} = 11$ bit

Virtual address:

0x11123456 = 0 0001 0001 0001 0010 0011 0**100 0101 0110** (binary)

MMU are responsible for translating Virtual address to Physical address:

1. Determine page number and offset:

- Page Offset: 100 0101 0110 = 0x456

- Virtual Page number: 00 0010 0010 0010 0100 0110 = 0x22246

2. MMU check if page number is larger than the page length registers to see if need to raise an exception:

- In this case no, therefore, not need for raise an exception.

3. MMU use page table to determine frame number at location 0x22246

- After getting the frame number (physical page number), the MMU combine with the page offset (0x456) to get the physical address

Question 2:

(1 millisecond = 10^6 nanoseconds (ns))

Memory access time: ma = 100 ns

Page fault service time:

- If available empty page: TLB access time = 8 milliseconds = $8x10^6$ ns
- If the replace paged was modified: Page table access time = 20 millisec = $20x10^6$ ns

Effective access time (EAT): no more than 200 ns

Page replaces frequency: Modified rate = 70%

Find Page fault frequency P:

EAT = P * (ma+ ($8x10^6$ns)* (1-Modified rate) + ($20x10^6$ns)* Modified rate) + (1- P) * ma

EAT = P (100 + ((8*0.3+20*0.7) $x10^6$)) +(1-P) (100)

EAT = P (16.4) $x10^6$ + 100P + 100 – 100P

200 = 16.4 $x10^6$P + 100 = 16.4 $x10^6$P +100

P = (200 – 100)/ 16.4 $x10^6$ = **$6.09756098 x10^{-6}$**