BUE
The British University In Egypt
الجامعة البريطانية في مصر

Exercise Sheet 1

Revision

Problem 1:

Conversions:

a. Convert the following hexadecimal numbers to their representation in binary:
   i. FACD
   ii. A39B
   iii. 821F
   iv. 7065
   v. F1C4

b. Convert the following binary numbers to their representation in hexadecimal:
   i. 1010000000111011
   ii. 0101101110100101
   iii. 1011010011110100
   iv. 1111010100100111
   v. 0011010110011010

Problem 2:

Given an architecture with a register size of 16 bits. State each of the numbers from exercise 1 as positive or negative if stored in registers of this size.

Problem 3:

Convert the following negative numbers to their representation in binary in an 8-bit register using 2's complement:

i. -5
ii. -6
iii. -2
iv. -1 (Remember this representation!)
v. -8 (Could 4-bit register +8?)

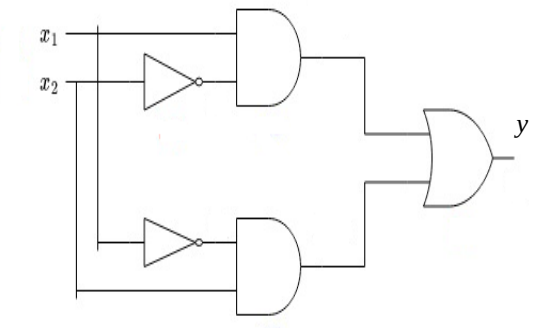
Problem 4:

Given an architecture with a register size of 4 bits. Perform the following mathematical operations in binary. State when an overflow occurs.

i. 2+5
ii. 5+3
iii. 3+(-2)
iv. 5+(-3)
v. 4+(-1)
vi. -3+(-2)
vii. -5+(-3)

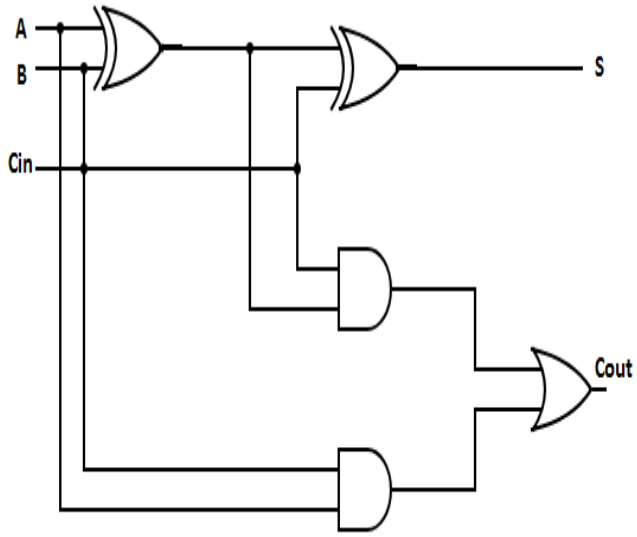
Problem 5:

a. Given the below simple digital circuit, fill the below table with the value of output y given the inputs x1, and x2 as stated in the table.



x1	x2	y
0	0	
0	1	
1	0	
1	1	

b. Given the below simple digital circuit, fill the below table with the values of the outputs S and Cout given the inputs A, B, and Cin as stated in the table.



A	B	Cin	S	Cout
0	0	0		
0	0	1		
0	1	0		
0	1	1		
1	0	0		
1	0	1		
1	1	0		
1	1	1		

Problem 6:

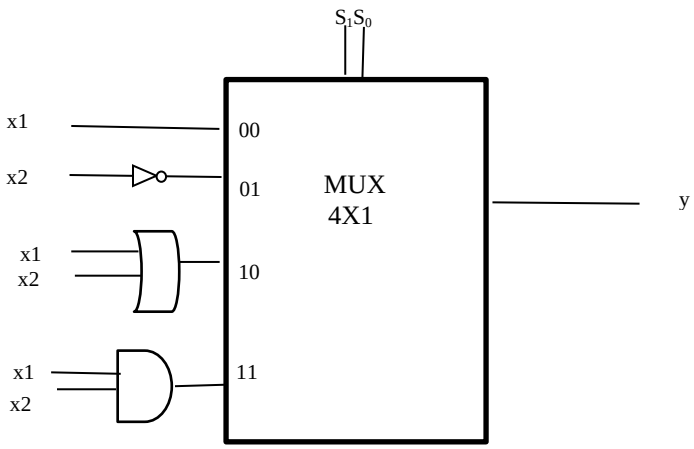
For each of the following multiplexers, state the number of selection lines:

i. 16 × 1 multiplexer.
ii. 32× 1 multiplexer.

iii. 128× 1 multiplexer.
iv. 256× 1 multiplexer.

Problem 7:

Given the below design, fill the below table with the values of the output y given the inputs x1, x2, and the selection lines as stated in the table.



x1	x2	S1	S0	y
0	0	0	0	
0	1	0	1	
1	0	1	0	
1	1	1	1	