Problems covering Part 1 in the Lecture:

Problem 1:

Represent the following conditional control statement by *two* register transfer statements with control functions:

If (X = 1) then (R1 ← R3) else if (Y=0 and Z = 1) then (R1 ← R4+R2)

Problem 2:

Explain the memory operation in each of the following transfer statements.

a. M[AR]← R2
b. R3 ← M[AR]

Problem 3:

If the values in AR = 500, DR = 80, R2 = 50 and R3 = 70, the content of Memory address 500 is 100 and the content of Memory address 501 is 101. Show the content of the 4 registers and the content of the memory addresses 500 and 501 after the following RTL statements.

M[AR]← DR
R2 ← M[AR]
DR ← R3
AR ← AR+1
M[AR] ← R3

Problem 4:

Assume an accumulator-based architecture has a byte-addressable memory, a word size of 32 bits, and each instruction is 32 bits. If the instruction in execution now was at address 400 in decimal. If the instruction in execution is adding R1 and R2, R1 has a value of 50, whereas R2 has a value of 30. What is the value of register PC while executing the instruction? What is the value of register AC after the execution of the instruction?

Problems covering Part 2 in the Lecture:

Problem 5:

A digital computer has a common bus system for 16 registers of 32 bits each. The bus is constructed with multiplexers.

a. How many multiplexers are in the bus?
b. What size of multiplexers is needed?
c. How many selection inputs are there in each multiplexer?

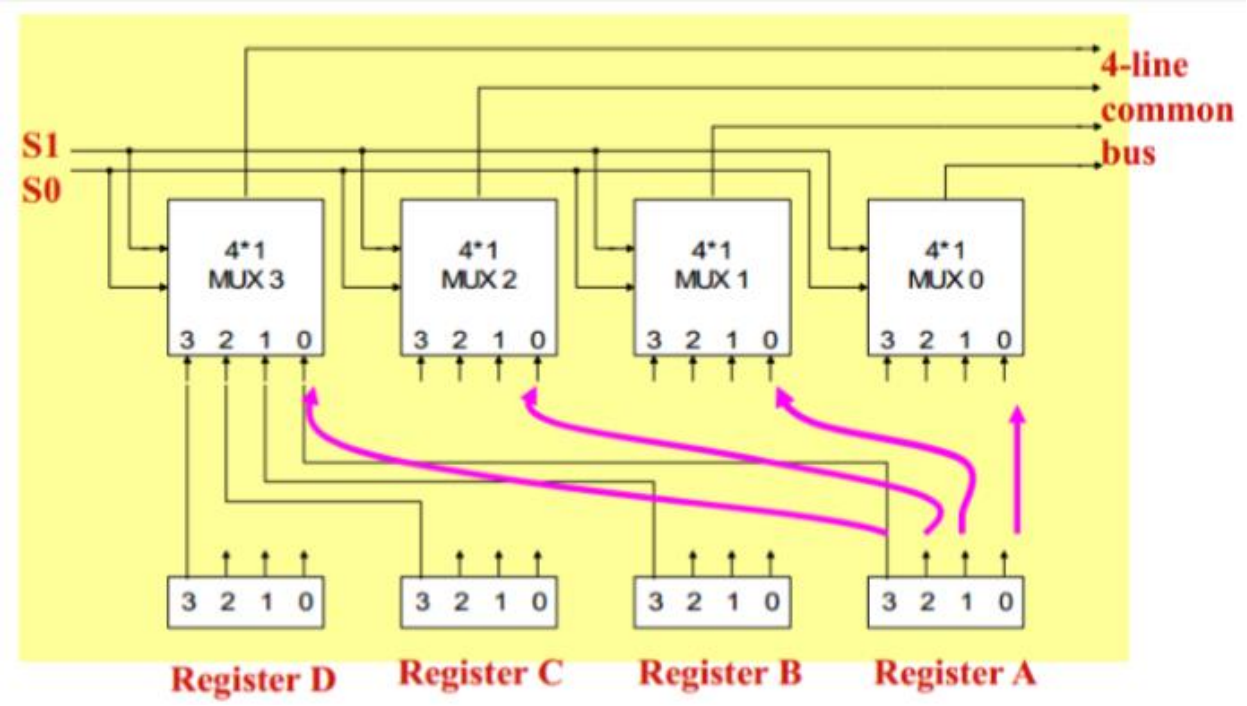
Problem 6:

Design the common bus for the system in problem 5 showing only the first two multiplexers and focusing on the first four inputs for each of these multiplexers.

Problem 7:

Given the common bus system for 4 registers where each register is 4-bits. State for each of the following Register transfer language statements, the selection lines values, and the load of which register should be set to 1.

a) D ← A
b) C ← B
c) B ←D
d) B ←C, A←C



Problems covering Part 3 in the Lecture:

Problem 8:

Design a 4-bit arithmetic circuit for decrementing the value of register A using 4 full-adder circuits.

Problem 9:

Design a 2-bit arithmetic circuit for incrementing the value of register A using 2 full-adder circuits. Assume the C_{in} for the least significant bit to the circuit is 1.

Problem 10:

Design a 2-bit arithmetic circuit for subtracting the value of register B from register A using 2 full-adder circuits. Assume the C_{in} for the least significant bit to the circuit is 1.