Informatics and Computer Science	**23CSCI10I** **Assessment One** **2023-2024**
Module Title **Computer Architecture**	
Module Leader **Dr. Noura El Maghawry**	Semester **One**
Assessment Weight **20% of the total course mark**	Time: **60 minutes**

Instructions to students:

1. The assignment is 4 pages including the cover page.
2. All questions are Mandatory.
3. Feedback: Assessment model answers will be posted on the e-learning

Marking Schema:

Question	Q1	Q2	Q3	Q4	Q5	Total
Marks	10	10	10	10	10	50
Earned marks						

Problem 1

a. A compiler designer is trying to decide between two code sequences for a specific computer. The code sequences are composed of three categories of instructions A, B, and C. The hardware designers have supplied the following facts for the clock cycles needed for one instruction of category A as 3 clock cycles, for category B as 2 clock cycles, and for category C as 4 clock cycles.

The compiler writer is considering two code sequences that require the following instruction counts:

Code Sequence	A	B	C
1	2	5	3
2	4	4	2

Which code sequence will execute faster if CPI is considered? Show your work.

[6 marks]

b. The following memory units are specified by the number of memory cells times the number of bits per memory cell. How many address lines are needed in each case, given that the memory is byte-addressable, and the word is 4 bytes?

i. 16Kw×8

ii. 512Mw×8

[4 marks]

[Q1 Total: 10 marks]

Solution:

a.

$$CPI = \frac{Total\ clock\ cycles}{Instruction\ count}$$

$$CPI1 = \frac{(2 \times 3) + (5 \times 2) + (3 \times 4)}{(2 + 5 + 3)} = 2.8$$

$$CPI2 = \frac{(4 \times 3) + (4 \times 2) + (2 \times 4)}{(4 + 4 + 2)} = 2.8$$

Both code sequences has the same CPI.

b.

	Memory	Address lines
16Kw×8	$2^4 \times 2^{10} = 2^{14}$ words $= 2^{16}$ cells	16
512Mw×8	$2^9 \times 2^{20} = 2^{29}$ words $= 2^{31}$ cells	31

Problem 2:

a. A digital computer has a common bus system for 32 registers of 16 bits each. If the bus is constructed with multiplexers.

i. How many multiplexers are there in the bus?

ii. What size of multiplexers is needed?

iii. How many selection lines needed for any multiplexer?

[3 marks]

b. Two enhancements with the following speedups are proposed for a new machine: Speedup (a) = 20, Speedup (b) = 30. Assume that for some set of programs, the fraction of use is 15% for enhancement (a), 10% for enhancement (b). If only one enhancement can be implemented, which should be chosen to maximize the speedup? Show your workout.

[7 marks]

[Q2 Total: 10 marks]

Solution:

a.

i. 16 multiplexers, one for each bit of the registers.

ii. 32 × 1 multiplexers.

iii. 5 selection lines to select one of 32 registers.

b.

$$SU_a = \frac{1}{(1-Frac\ used a)+\frac{Frac\ used\ a}{SU1}} = \frac{1}{(1-0.15)+\frac{0.15}{20}} = 1.16$$

$$SU_b = \frac{1}{(1-Frac\ used\ b)+\frac{Frac\ used\ b}{SU2}} = \frac{1}{(1-0.1)+\frac{0.1}{30}} = 1.10$$

The first enhancement should be chosen.

Problem 3:

Write an assembly program that is equivalent to the following code:

```
        int product =1;
        int i = 5;
        for (int j =1; j<=20; j++)
           {
               product+= i*j;
               i= i+5;
            }
```

[Q3 Total: 10 marks]

Solution:

```
        move $s0, 1
        move $s1, 5
        move $s2, 1

Loop:
        slti $t0, $s2, 21
        beq $t0, $zero, done

        mul $t1, $s1, $s2
        add $s3, $s3, $t1

        addi $s1, $s1, 5
        addi $s2, $s2, 1
        j Loop
done:
```

Problem 4:

a. Starting from an initial value of R = 01101001, determine the sequence of binary values of R after a logical shift left, followed by a circular shift right, followed by an arithmetic shift right, followed by a circular shift left, followed by an arithmetic shift left. State whether there is an overflow.

[6 marks]

b. Starting from an initial value of $s1 = 0xABCD, determine the value of register $s1 in hexadecimal after each instruction causing a change in $s1 is executed:

```
move $s0, 0xACAB
and $s1, $s1, $s0
addi $s1, $s0, 1
ori $s1, $s1, 0xFAAA
```

[4 marks]
[Q4 Total: 10 marks]

Solution:

a. R = 01101001

After logical Shift left: 11010010

After circular shift right: 01101001

After arithmetic shift right: 00110100

After circular shift left: 01101000

After Arithmetic shift left: 11010000

After arithmetic shift left, an overflow occurred.

b.

```
move $s0, 0xACAB                    # no change in $s1
and $s1, $s1, $s0                   # $s1 = 0xA889
addi $s1, $s0, 1                    # $s1 = 0xACAC
ori $s1, $s1, 0xFAAA                  # $s1 = 0xFEAE
```

Problem 5:

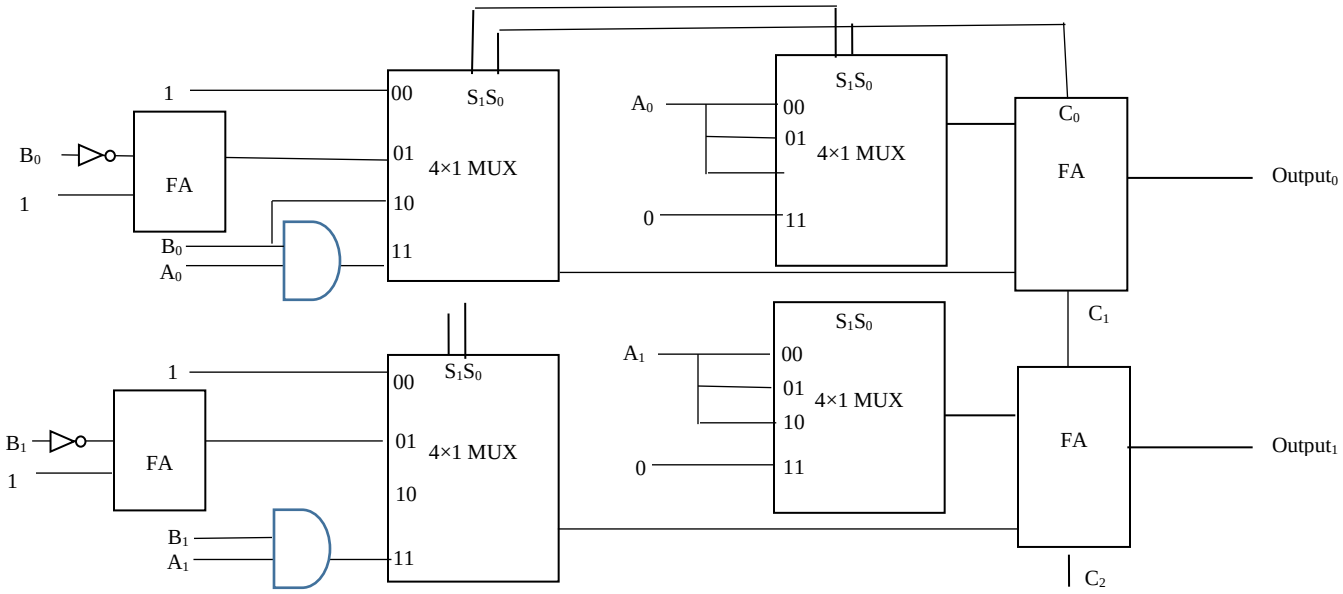
Design a circuit for two n-bit data inputs A and B. The circuit generates the following arithmetic operations based on the selection specified, **assuming that the C_{in} of the full adder for the least significant bit is designed to be one of the selection inputs to the Multiplexers (S0):**

S_1 C_{in}	Operation
0 0	Output = A-1
0 1	Output = A+B’
1 0	Output = A+B
1 1	Output = A^B + 1

Draw the logic diagram for the first two stages.

[Q5 Total: 10 marks]

Solution:


1
B0
1
FA
00
01
10
11
S1S0
4×1 MUX
B0
A0
A0
0
S1S0
00
01
10
11
4×1 MUX
C0
FA
Output0
C1
1
B1
1
FA
00
01
10
11
S1S0
4×1 MUX
B1
A1
A1
0
S1S0
00
01
10
11
4×1 MUX
FA
Output1
C2