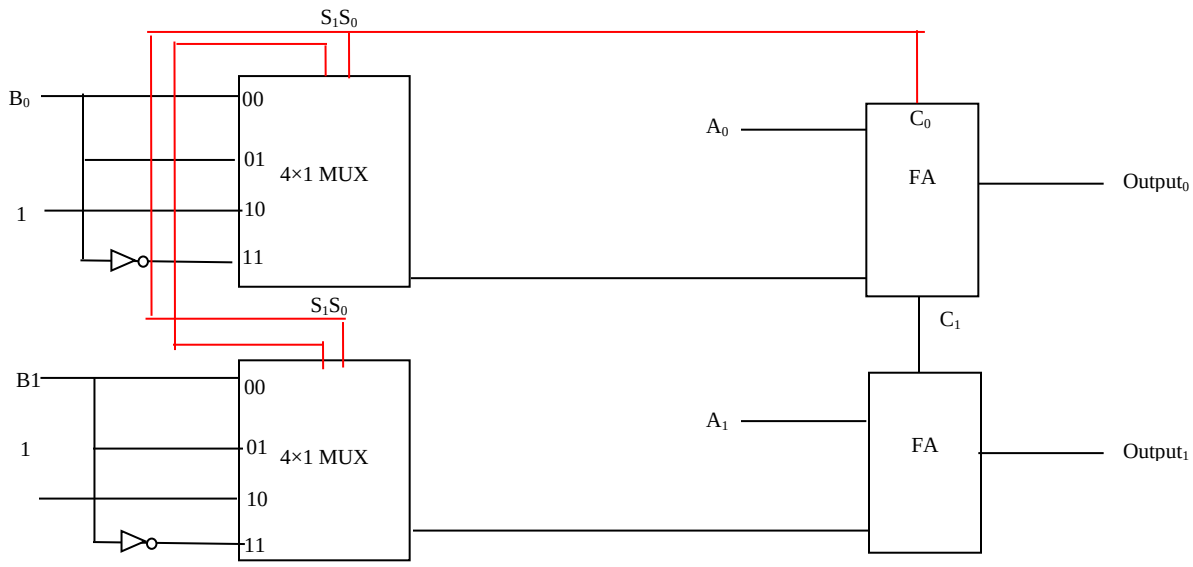
Problem 1:

Design an arithmetic circuit that given two n-bit data inputs A and B. The circuit generates the following four arithmetic operations in conjunction with the input carry **C_{in} connected as S0**. Draw the logic diagram for the first two stages.

S1	S0	Operation
0	0	D= A+B (add)
0	1	D= A+B+1 (Add with carry)
1	0	D= A-1 (decrement)
1	1	D= A+B′+1 (subtract)

Solution:

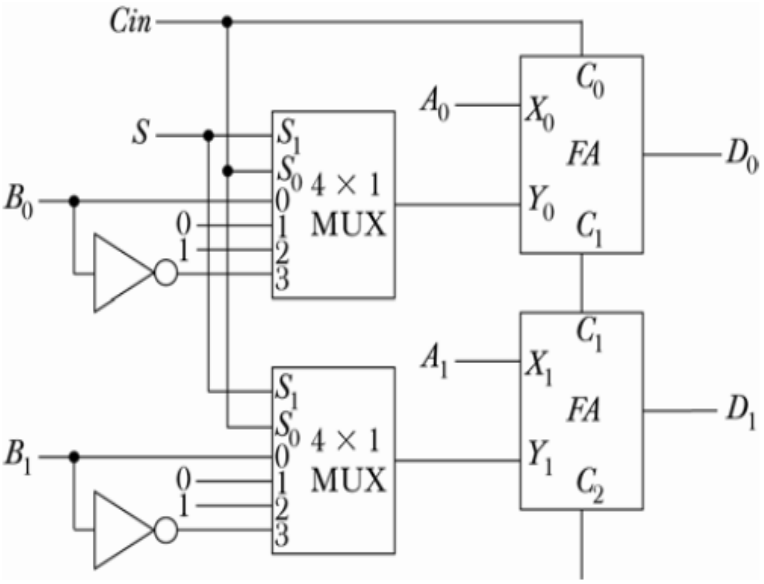


Problem 2:

Design an arithmetic circuit with one selection variable S and two n-bit data inputs A and B. The circuit generates the following four arithmetic operations in conjunction with the input carry C_{in}. Draw the logic diagram for the first two stages.

S	C_{in} = 0	C_{in} = 1
0	D= A+B (add)	D= A+1 (increment)
1	D= A-1 (decrement)	D= A+B′+1 (subtract)

Solution:



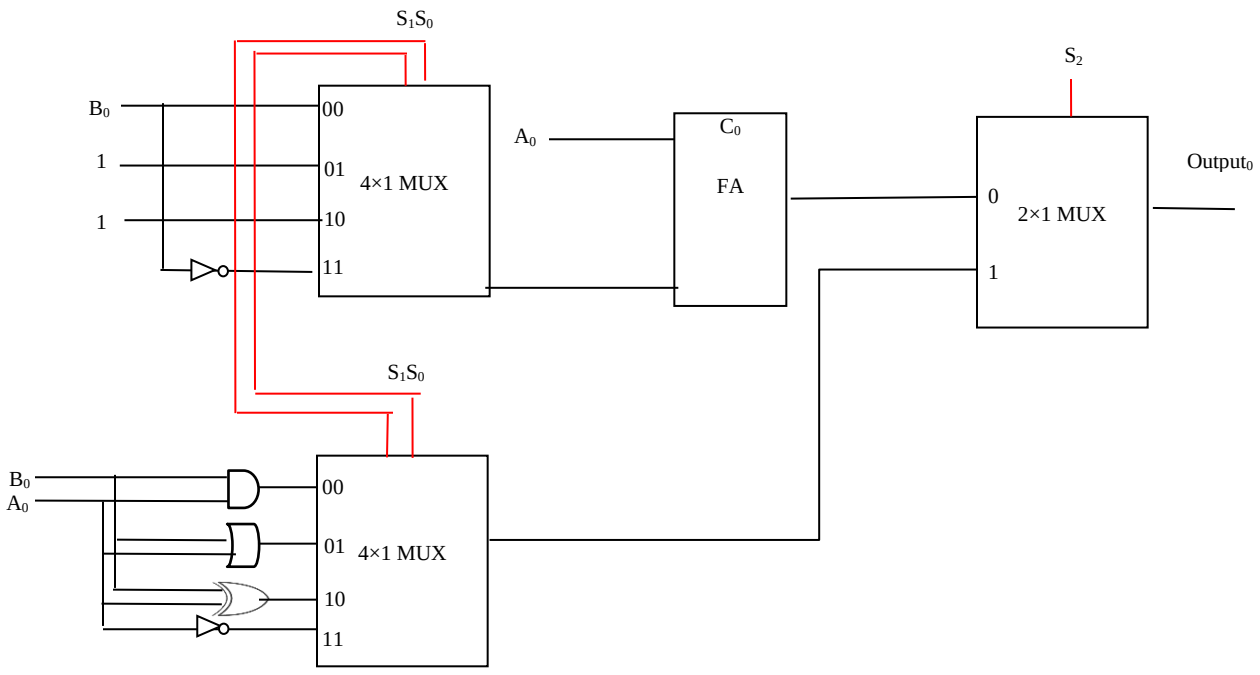
S	C_{in}	X	Y	
0	0	A	B	(A+B)
0	1	A	0	(A+1)
1	0	A	1	(A-1)
1	1	A	B′	(A-B)

Problem 3:

Design an arithmetic and logic circuit with three Selection lines and two n-bit data inputs A and B. The circuit generates four arithmetic operations when selection S2 is equal to zero and generates logic operations when selection S2 is equal to 1. The operations are stated in the table below. Draw the logic diagram for the first stage.

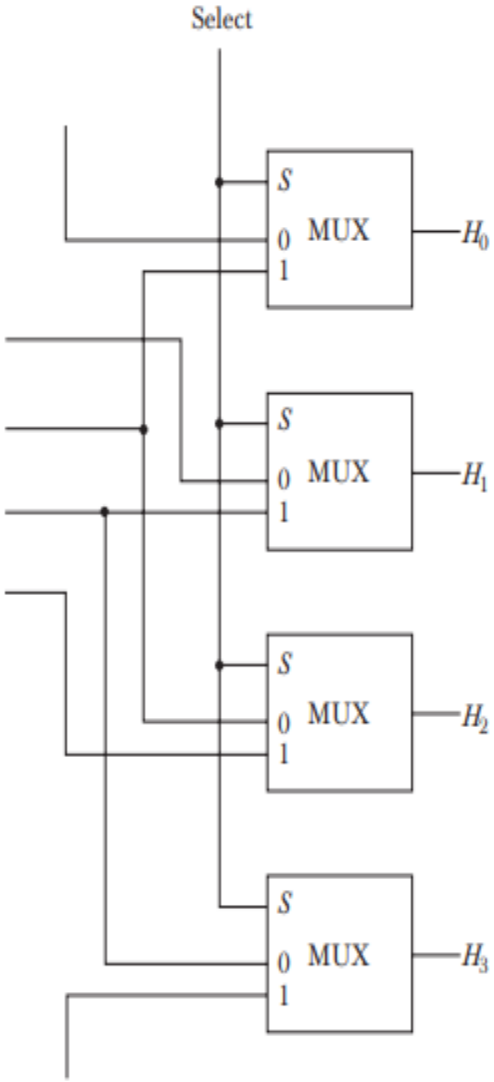
S2	S1	S0	Operation
0	0	0	A+B
0	0	1	A+1
0	1	0	A-1
0	1	1	A+B' (Subtract with borrow)
1	0	0	$A \wedge B$
1	0	1	$A \vee B$
1	1	0	$A \oplus B$
1	1	1	A'

Solution:

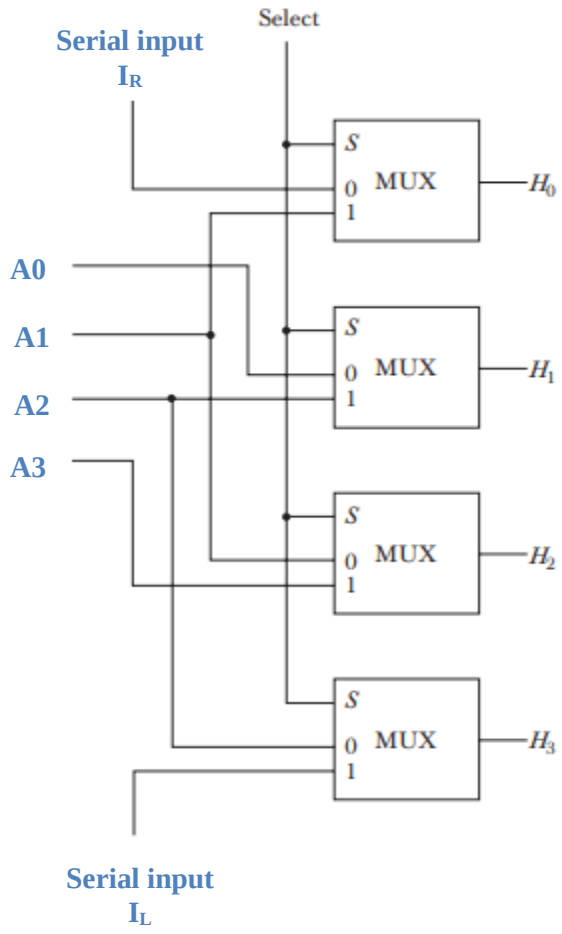


Problem 4:

Given the below diagram for a 4-bit shifter circuit for register A. State the inputs to the multiplexers, so that the circuit performs both shifting right and shifting left microoperations. Assume H0 is the least significant bit for the output and H3 is the most significant bit.



Solution:



S	H3	H2	H1	H0	Micro-operation
0	A3	A1	A0	I_R	Shift left
1	I_L	A3	A2	A1	Shift right

Problem 5:

Starting from an initial value of R = 11010111, determine the sequence of binary values of R after a logical shift left, followed by a circular shift-right, followed by a logical shift right and a circular shift right.

Solution:

R = 11010111
Logical shift left: 10101110
Circular shift-right: 01010111
Logical shift right: 00101011
Circular shift right: 10010101

Problem 6:

An 8-bit register contains the binary value 10011100. What is the register value after arithmetic shift right? Starting from the initial number 10011100, determine the register value after an arithmetic shift left, and state whether there is an overflow.

Solution:

R = 10011100
Arithmetic shift right: 11001110
Arithmetic shift left: 00111000 overflow because a negative number changed to positive.