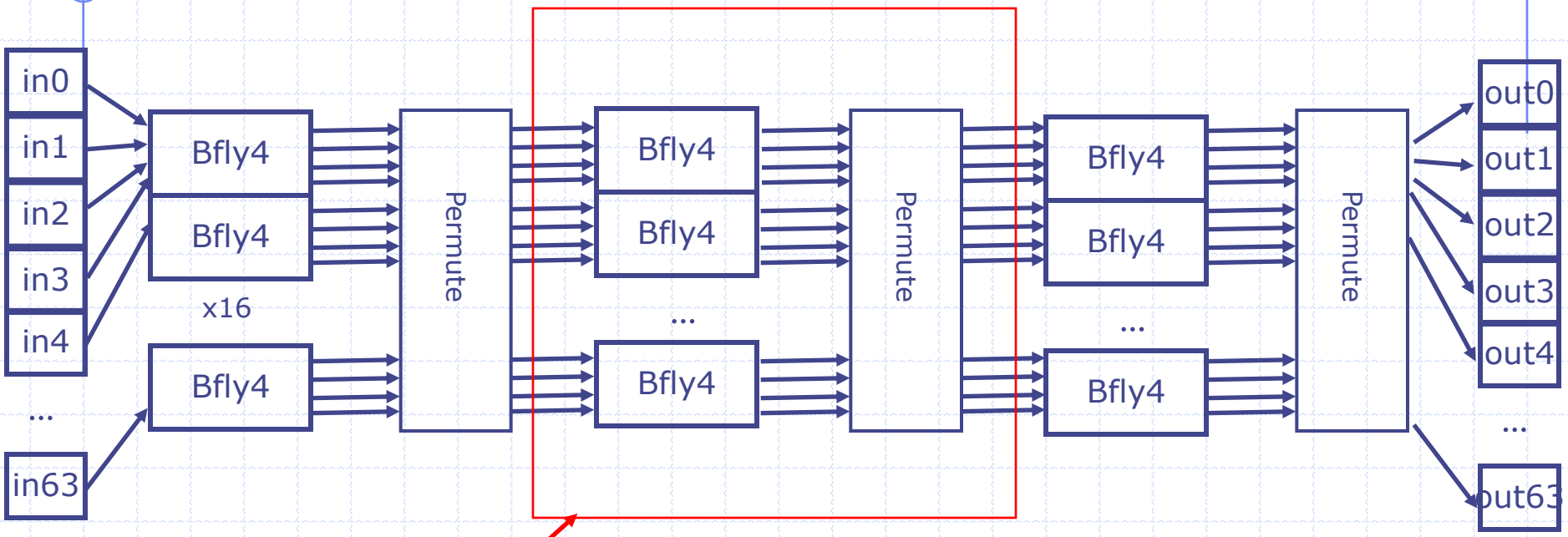
Folding and Pipelining complex combinational circuits

Arvind
Computer Science & Artificial Intelligence Lab
Massachusetts Institute of Technology

Combinational IFFT:

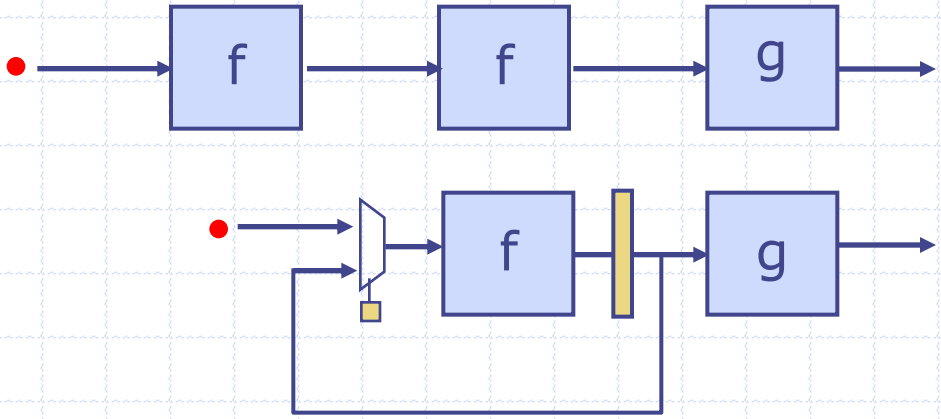
Suppose we want to reduce the area of the circuit



Reuse the same circuit three times to reduce area

Folding

Reusing a combinational block



Introduce state elements to hold intermediate values

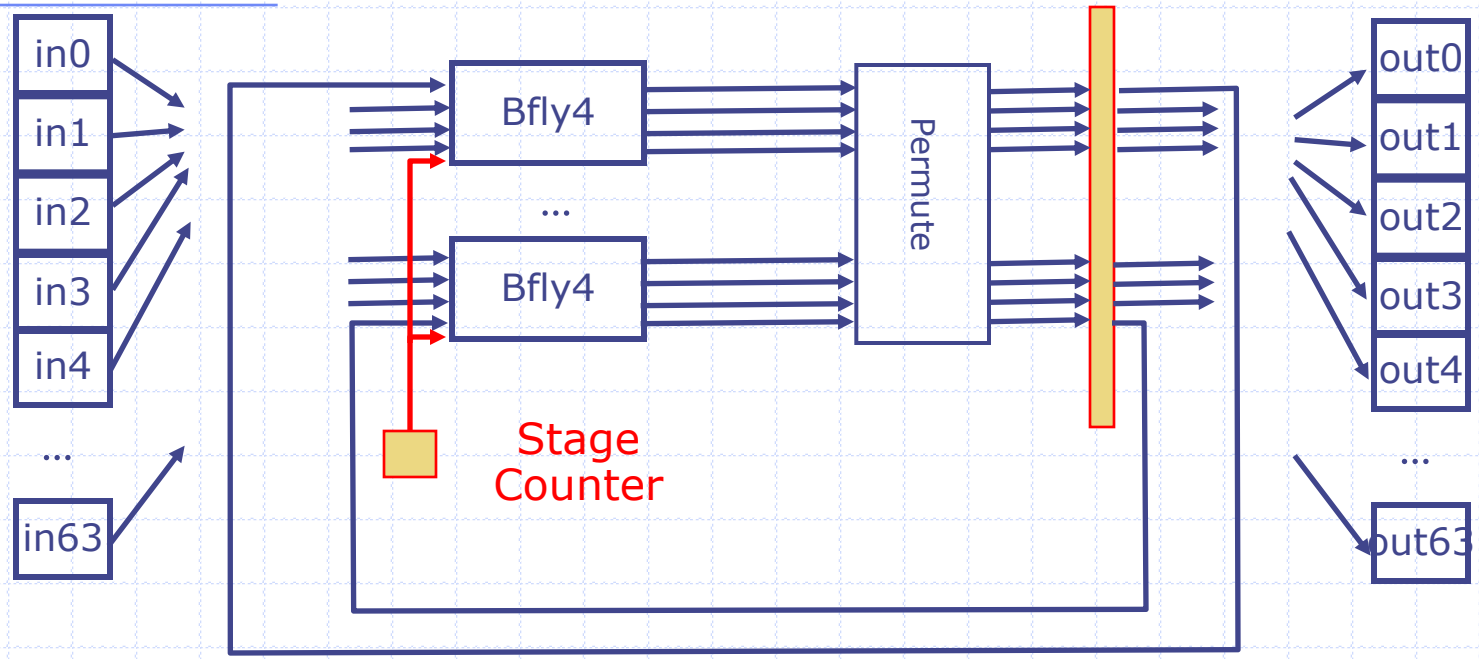
we expect:

Throughput to decrease – less parallelism

Area to decrease – reusing a block

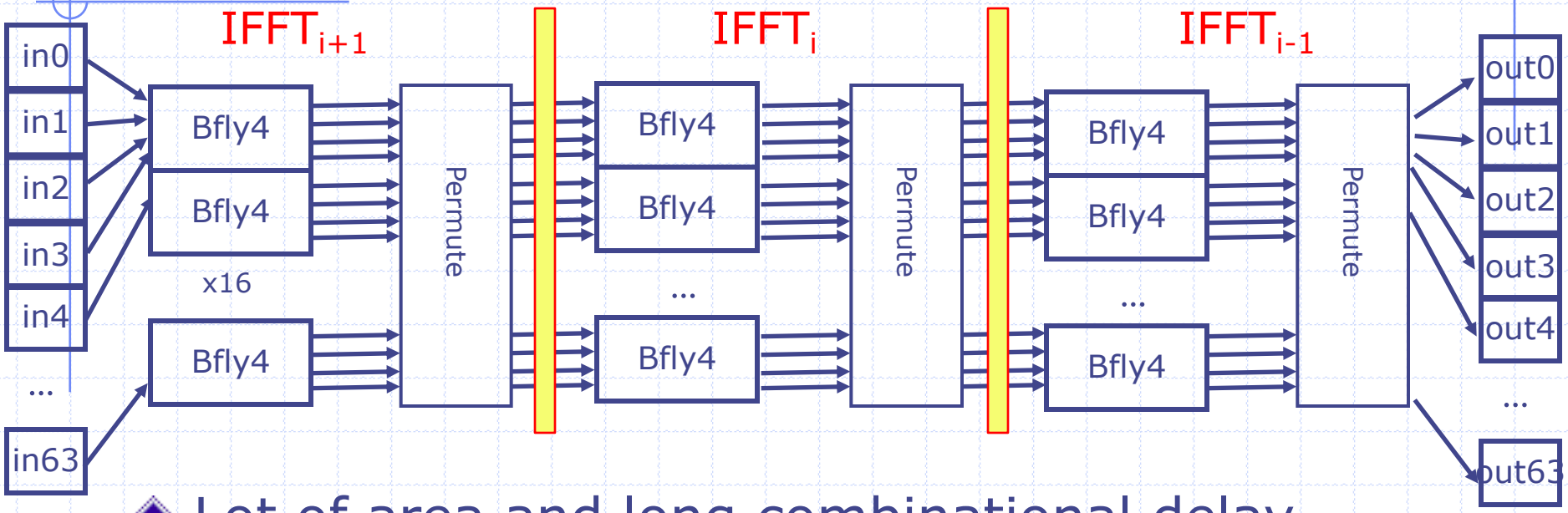
The clock needs to run faster for the same throughput ⇒ hyper-linear increase in energy

Circular or folded pipeline: Reusing the Pipeline Stage



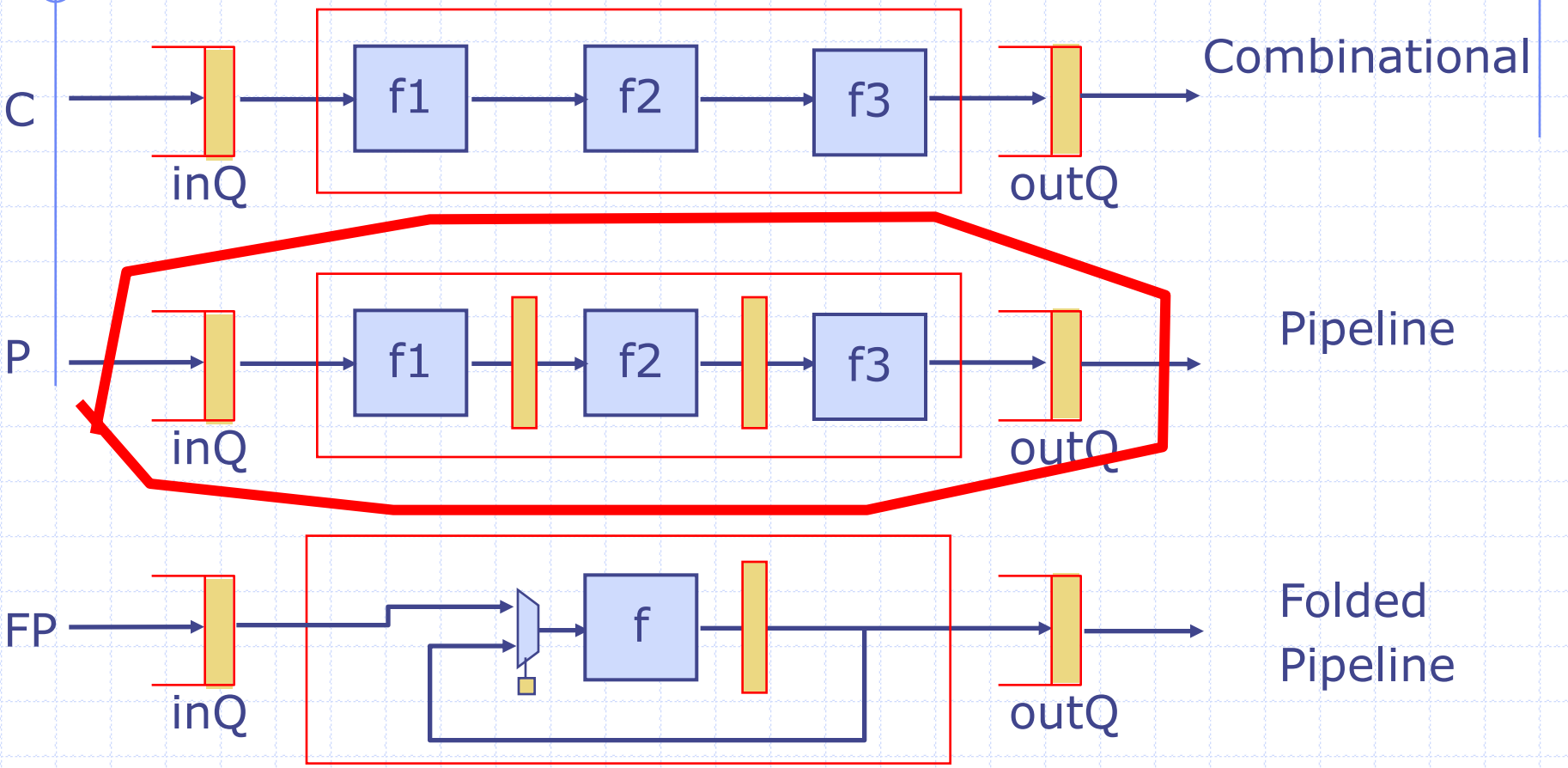
Combinational IFFT

3 different datasets in the pipeline



- Lot of area and long combinational delay
- Folded or multi-cycle version can save area and reduce the combinational delay but throughput per clock cycle gets worse
- Pipelining: a method to increase the circuit throughput to evaluate multiple IFFTs

Pipelining a block



Clock: C < P ≈ FP

Area: FP < C < P

Throughput: FP < C < P