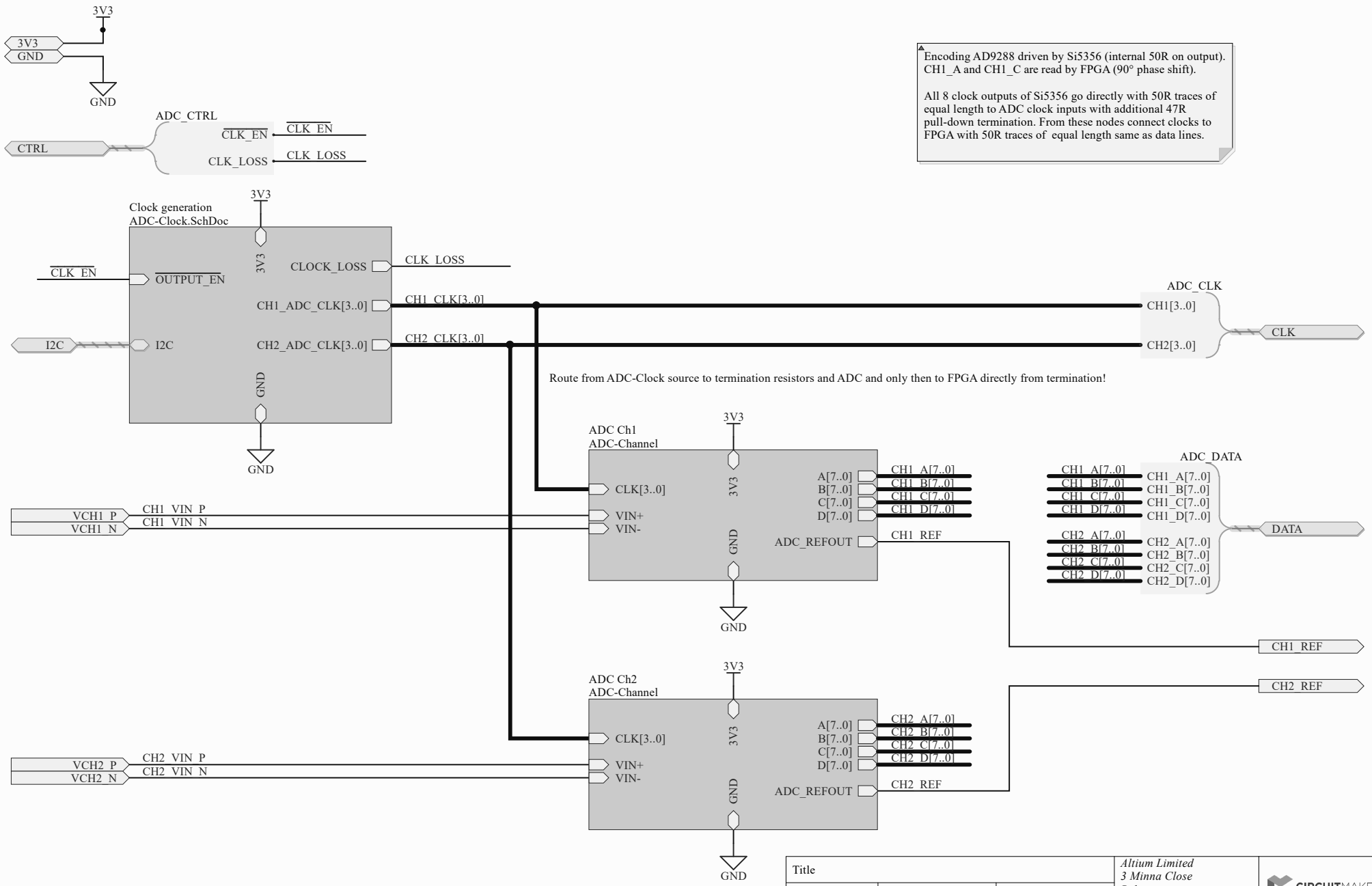
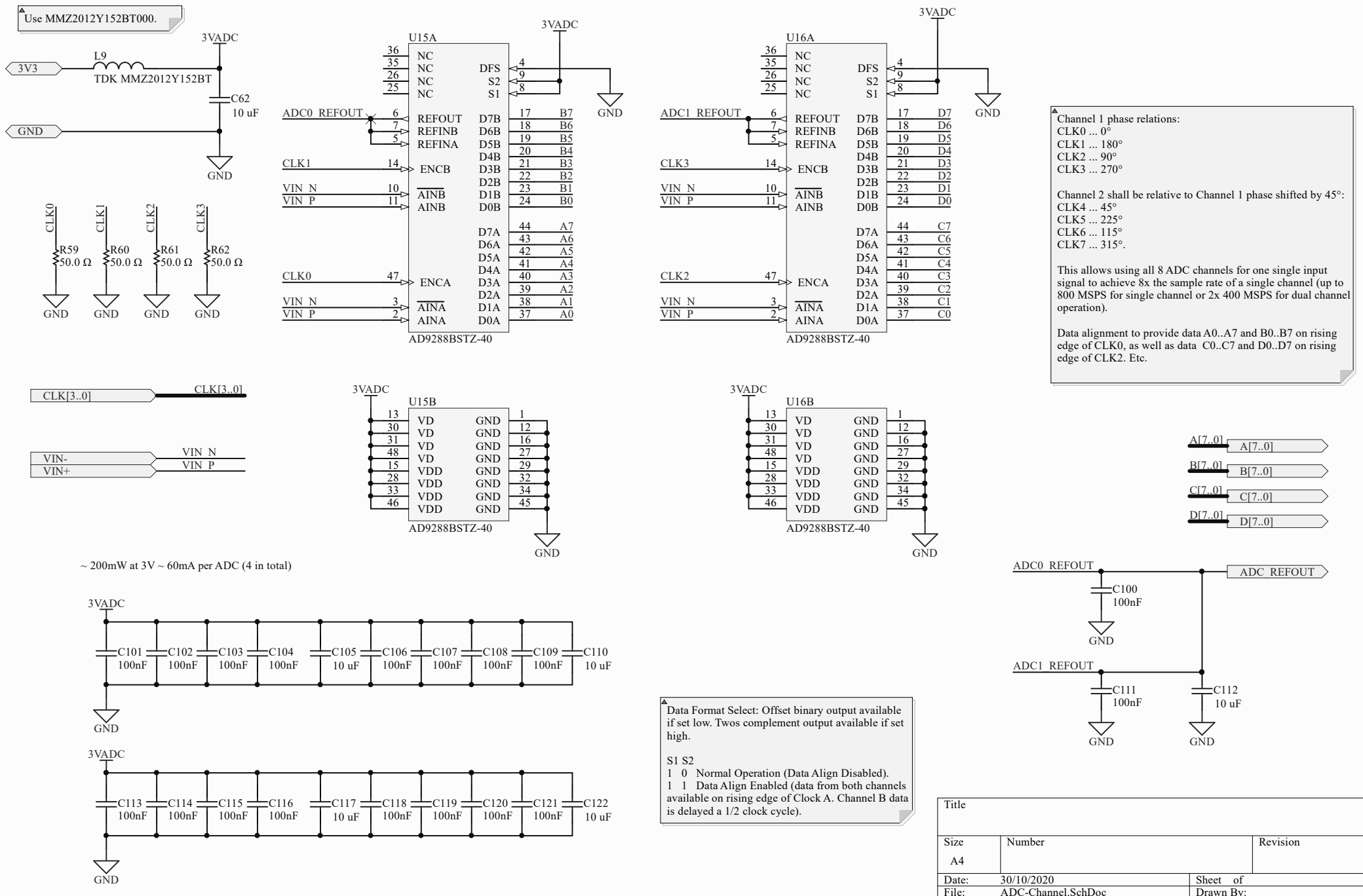
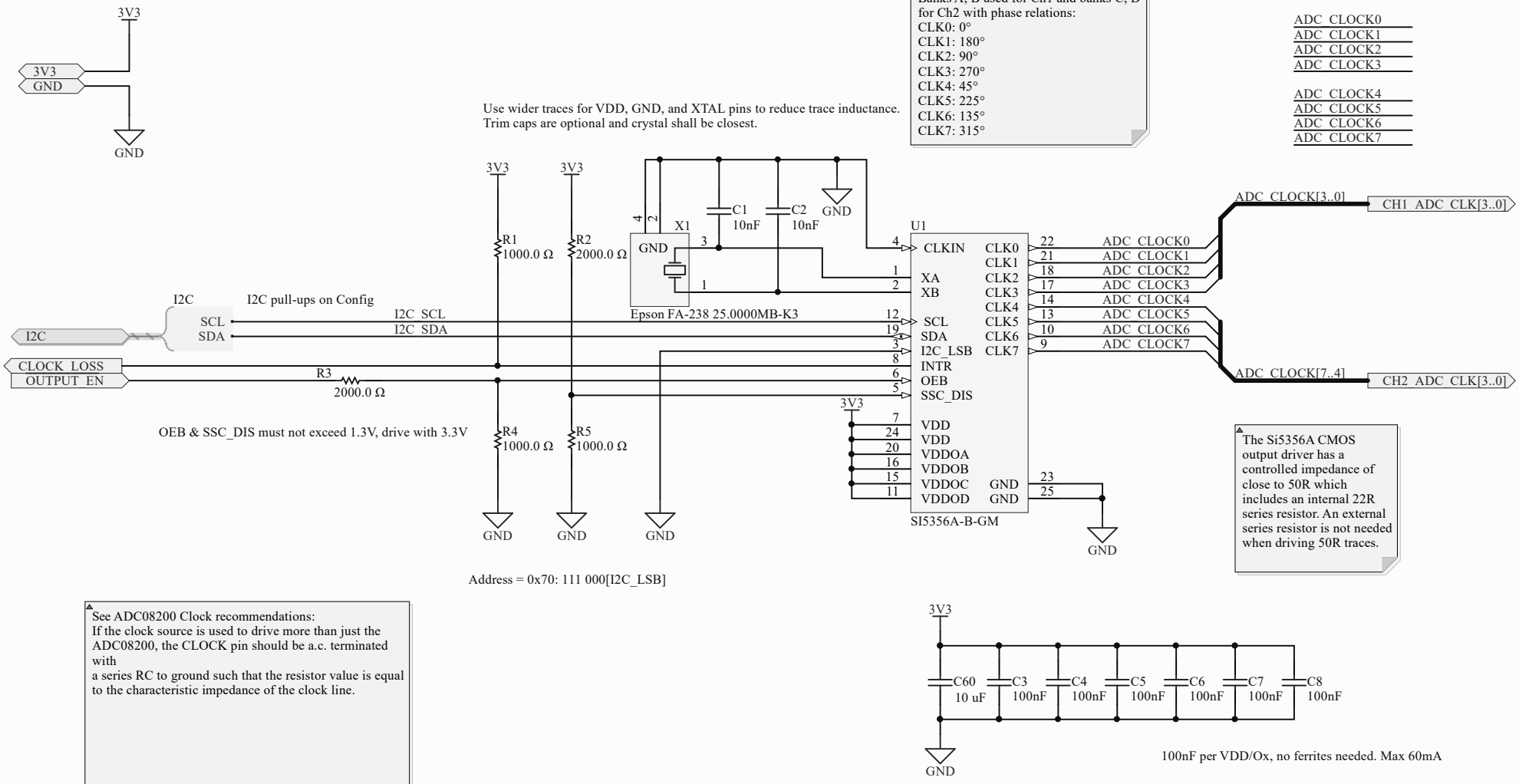
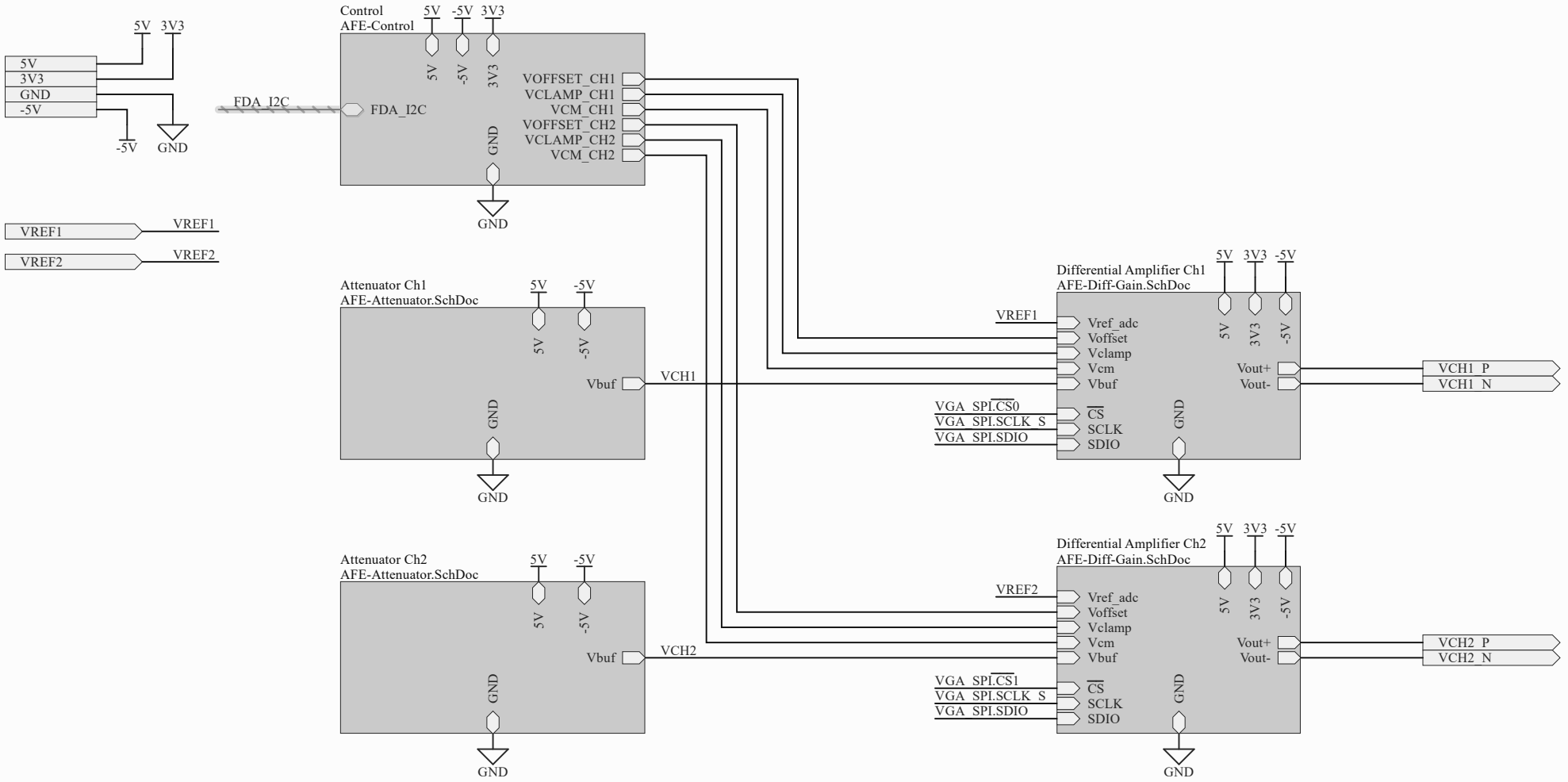

3V3
3V3
GND
GND
ADC_CTRL
CTRL
CLK_EN
CLK_EN
CLK_LOSS
CLK_LOSS
Encoding AD9288 driven by Si5356 (internal 50R on output).
CH1_A and CH1_C are read by FPGA (90° phase shift).
All 8 clock outputs of Si5356 go directly with 50R traces of equal length to ADC clock inputs with additional 47R pull-down termination. From these nodes connect clocks to FPGA with 50R traces of equal length same as data lines.
Clock generation
ADC-Clock.SchDoc
3V3
CLK_EN
OUTPUT_EN
I2C
I2C
3V3
GND
CLOCK_LOSS
CH1_ADC_CLK[3..0]
CH2_ADC_CLK[3..0]
CLK_LOSS
CH1_CLK[3..0]
CH2_CLK[3..0]
GND
ADC_CLK
CH1[3..0]
CH2[3..0]
CLK
Route from ADC-Clock source to termination resistors and ADC and only then to FPGA directly from termination!
ADC Ch1
ADC-Channel
3V3
CLK[3..0]
VIN+
VIN-
3V3
GND
A[7..0]
B[7..0]
C[7..0]
D[7..0]
ADC_REFOUT
CH1_A[7..0]
CH1_B[7..0]
CH1_C[7..0]
CH1_D[7..0]
CH1_REF
GND
VCH1_P
VCH1_N
CH1_VIN_P
CH1_VIN_N
ADC_DATA
CH1_A[7..0]
CH1_B[7..0]
CH1_C[7..0]
CH1_D[7..0]
CH2_A[7..0]
CH2_B[7..0]
CH2_C[7..0]
CH2_D[7..0]
DATA
CH1_REF
CH2_REF
ADC Ch2
ADC-Channel
3V3
CLK[3..0]
VIN+
VIN-
3V3
GND
A[7..0]
B[7..0]
C[7..0]
D[7..0]
ADC_REFOUT
CH2_A[7..0]
CH2_B[7..0]
CH2_C[7..0]
CH2_D[7..0]
CH2_REF
GND
VCH2_P
VCH2_N
CH2_VIN_P
CH2_VIN_N
Title
Size: A4
Number:
Revision:
Date: 30/10/2020
Time: 21:26:04
Sheet of
File: ADC.SchDoc
Altium Limited
3 Minna Close
Belrose
NSW 2085
Australia
CIRCUITMAKER


Use MMZ2012Y152BT000.
3V3
L9
TDK MMZ2012Y152BT
3VADC
C62
10 uF
GND
CLK0
CLK1
CLK2
CLK3
R59 50.0 Ω
R60 50.0 Ω
R61 50.0 Ω
R62 50.0 Ω
U15A
U16A
NC
DFS
S2
S1
REFOUT
REFINB
REFINA
ENCB
AINB
AINA
D7B
D6B
D5B
D4B
D3B
D2B
D1B
D0B
D7A
D6A
D5A
D4A
D3A
D2A
D1A
D0A
ADC0_REFOUT
ADC1_REFOUT
CLK1
CLK3
CLK0
CLK2
VIN_N
VIN_P
AD9288BSTZ-40
Channel 1 phase relations:
CLK0 ... 0°
CLK1 ... 180°
CLK2 ... 90°
CLK3 ... 270°
Channel 2 shall be relative to Channel 1 phase shifted by 45°:
CLK4 ... 45°
CLK5 ... 225°
CLK6 ... 115°
CLK7 ... 315°.
This allows using all 8 ADC channels for one single input signal to achieve 8x the sample rate of a single channel (up to 800 MSPS for single channel or 2x 400 MSPS for dual channel operation).
Data alignment to provide data A0..A7 and B0..B7 on rising edge of CLK0, as well as data C0..C7 and D0..D7 on rising edge of CLK2. Etc.
CLK[3..0]
VIN-
VIN+
U15B
U16B
VD
VDD
A[7..0]
B[7..0]
C[7..0]
D[7..0]
~ 200mW at 3V ~ 60mA per ADC (4 in total)
C101 100nF
C102 100nF
C103 100nF
C104 100nF
C105 10 uF
C106 100nF
C107 100nF
C108 100nF
C109 100nF
C110 10 uF
C113 100nF
C114 100nF
C115 100nF
C116 100nF
C117 10 uF
C118 100nF
C119 100nF
C120 100nF
C121 100nF
C122 10 uF
C100 100nF
C111 100nF
C112 10 uF
ADC_REFOUT
Data Format Select: Offset binary output available if set low. Twos complement output available if set high.
S1 S2
1 0 Normal Operation (Data Align Disabled).
1 1 Data Align Enabled (data from both channels available on rising edge of Clock A. Channel B data is delayed a 1/2 clock cycle).
Title
Size A4
Number
Revision
Date: 30/10/2020
Sheet of
File: ADC-Channel.SchDoc
Drawn By:

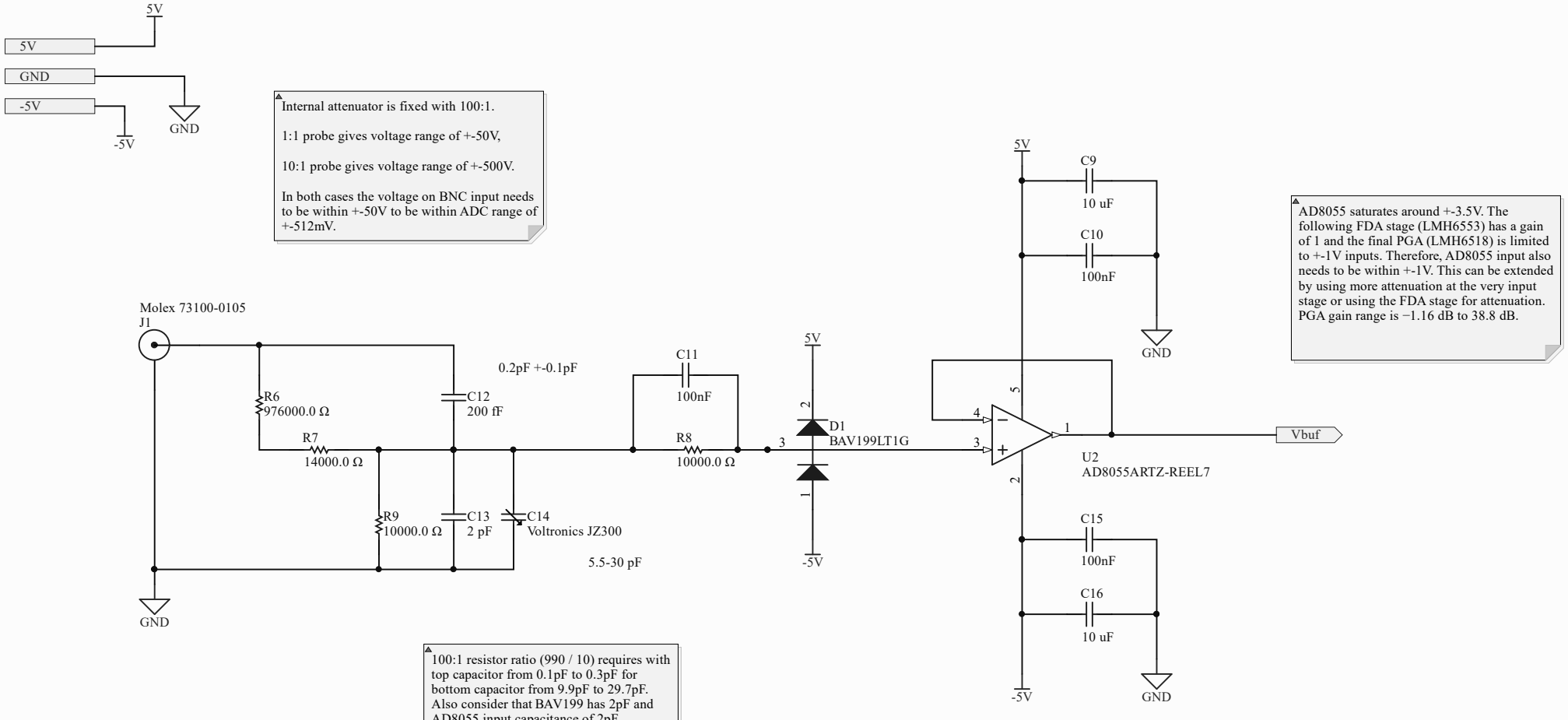


Title *Vienna-Scope*			*Altium Limited* *3 Minna Close* *Belrose* *NSW 2085* *Australia*
Size: A4	Number:	Revision:	
Date: 30/10/2020 Time: 21:26:05		Sheet of	
File: ADC-Clock.SchDoc			

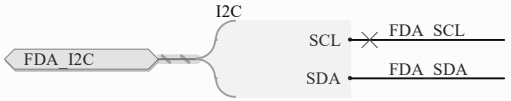
CIRCUITMAKER



Title			*Altium Limited* *3 Minna Close* *Belrose* *NSW 2085* *Australia*
Size: A4	Number:	Revision:	
Date: 30/10/2020 Time: 21:26:05		Sheet of	
File: AFE.SchDoc			



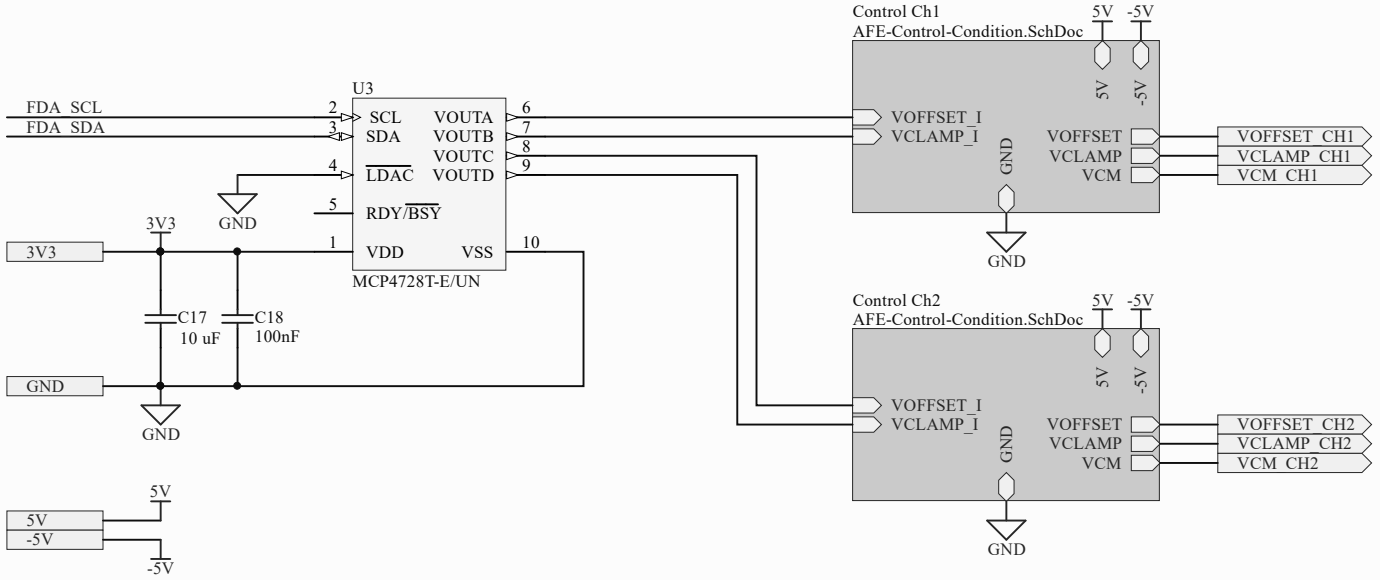
Title			*Altium Limited* *3 Minna Close* *Belrose* *NSW 2085* *Australia*
Size: A4	Number:	Revision:	
Date: 30/10/2020 Time: 21:26:06		Sheet of	
File: AFE-Attenuator.SchDoc			



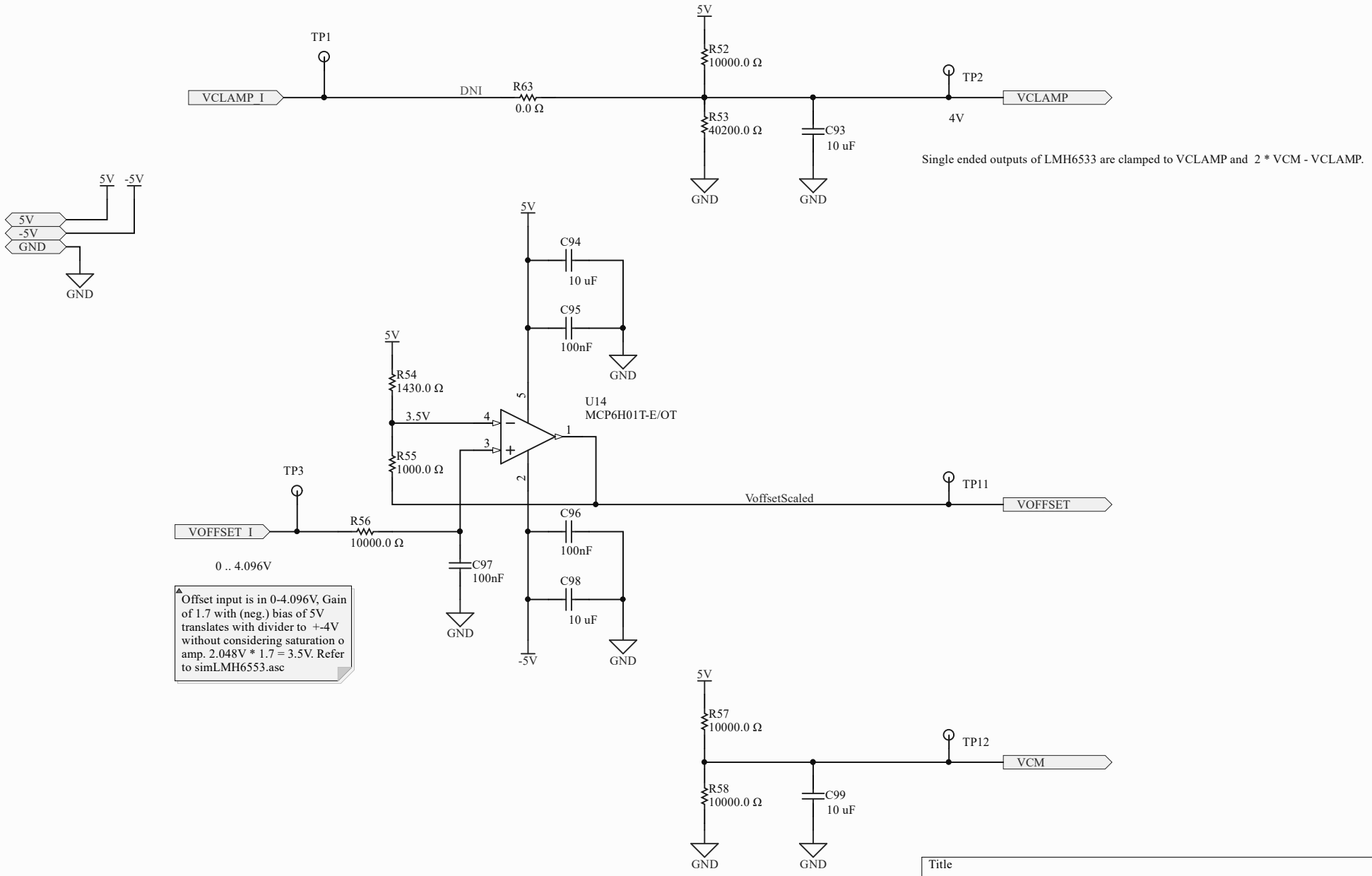
I2C address: 1100 A2 A1 A0, with A2..A0 programmable to EEPROM. Default is 000.

Internal reference shall be used (default), choose gain of 2 to provide UFS = 4.096V (default gain is 1).

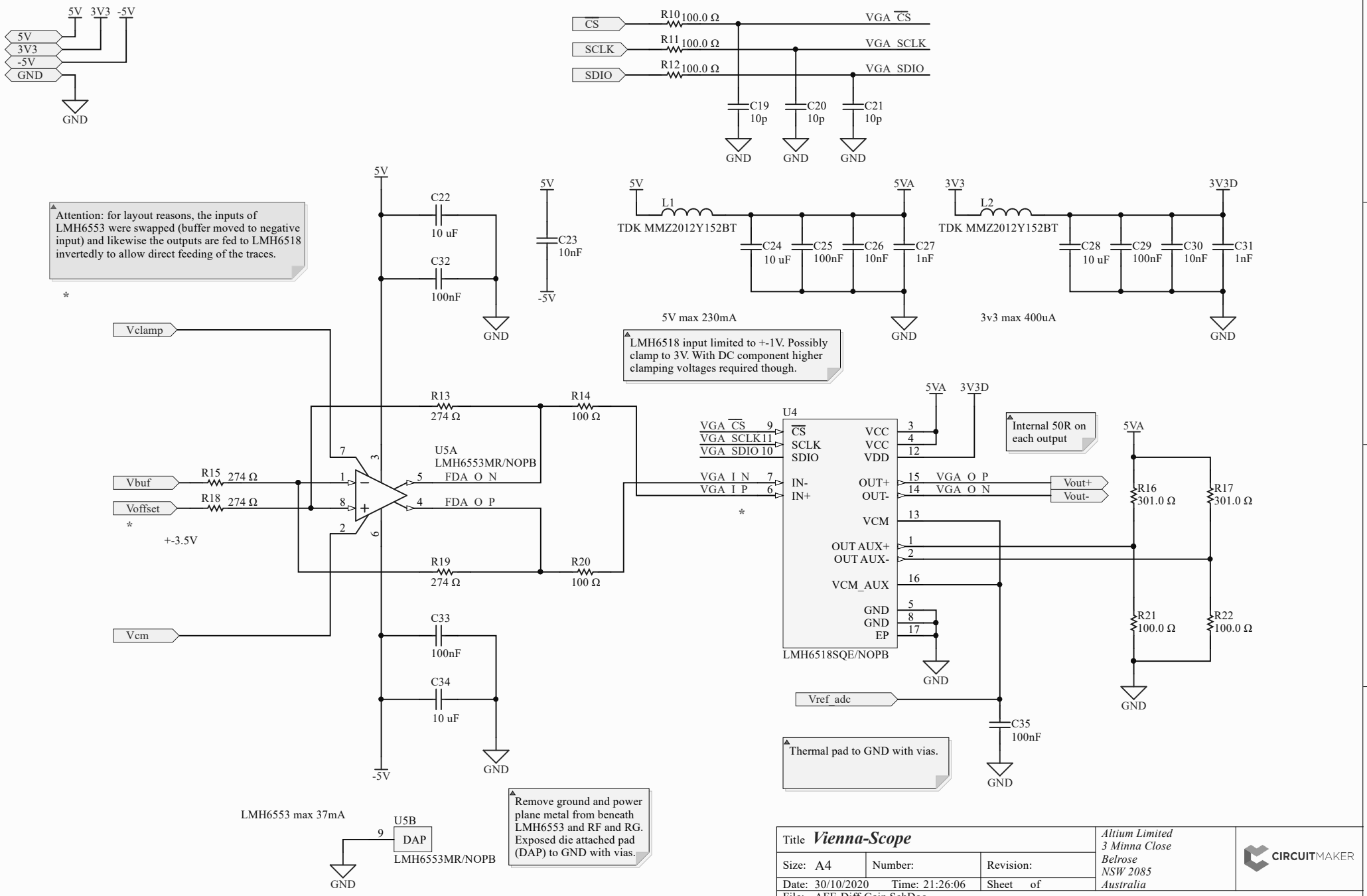
Fully Differential Amplifier voltage input generation

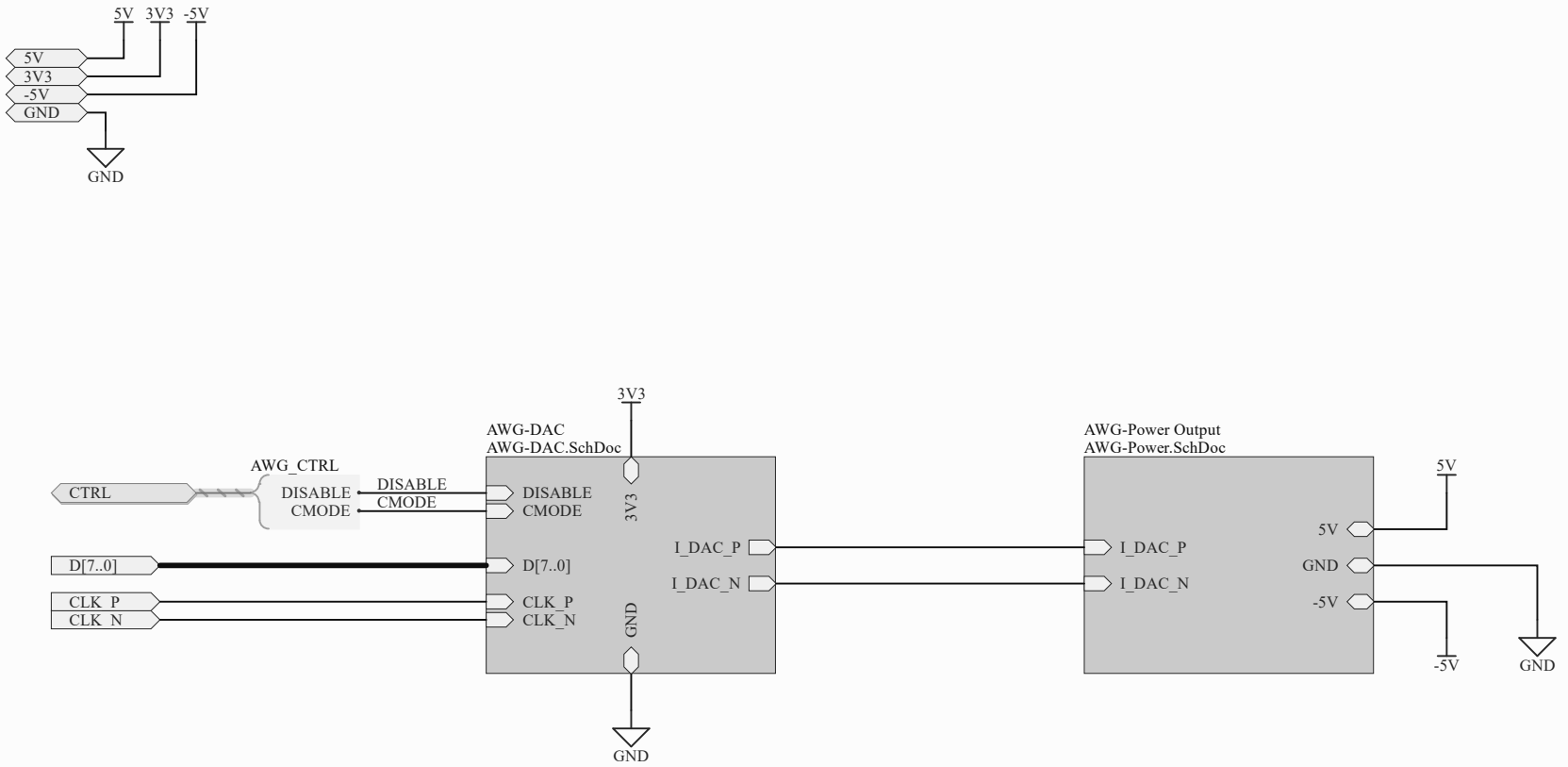


Title			*Altium Limited* *3 Minna Close* *Belrose* *NSW 2085* *Australia*
Size: A4	Number:	Revision:	
Date: 30/10/2020 Time: 21:26:06		Sheet of	
File: AFE-Control.SchDoc			



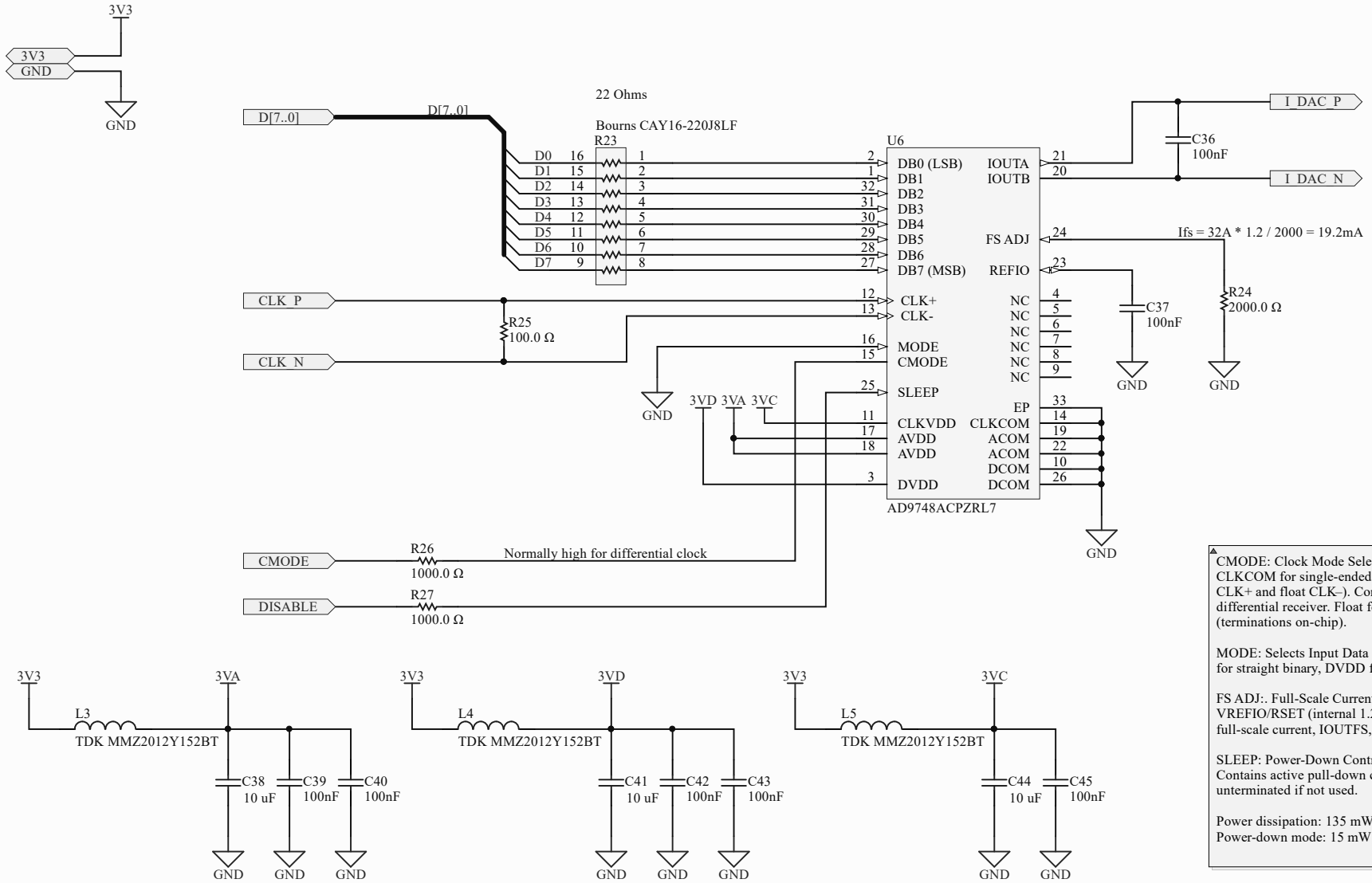
Title		
Size: A4	Number	Revision
Date: 30/10/2020		Sheet of
File: AFE-Control-Condition.SchDoc		Drawn By:


5V
3V3
-5V
GND
CS
SCLK
SDIO
R10 100.0 Ω
R11 100.0 Ω
R12 100.0 Ω
VGA_CS
VGA_SCLK
VGA_SDIO
C19 10p
C20 10p
C21 10p
Attention: for layout reasons, the inputs of LMH6553 were swapped (buffer moved to negative input) and likewise the outputs are fed to LMH6518 invertedly to allow direct feeding of the traces.
C22 10 uF
C32 100nF
C23 10nF
L1
TDK MMZ2012Y152BT
C24 10 uF
C25 100nF
C26 10nF
C27 1nF
5VA
5V max 230mA
L2
TDK MMZ2012Y152BT
C28 10 uF
C29 100nF
C30 10nF
C31 1nF
3V3D
3v3 max 400uA
LMH6518 input limited to +-1V. Possibly clamp to 3V. With DC component higher clamping voltages required though.
Vclamp
Vbuf
Voffset
+-3.5V
R15 274 Ω
R18 274 Ω
R13 274 Ω
R14 100 Ω
R19 274 Ω
R20 100 Ω
U5A
LMH6553MR/NOPB
FDA_O_N
FDA_O_P
Vcm
C33 100nF
C34 10 uF
U4
VGA_I_N
VGA_I_P
IN-
IN+
OUT+
OUT-
VCC
VDD
VCM
OUT AUX+
OUT AUX-
VCM_AUX
GND
EP
LMH6518SQE/NOPB
Internal 50R on each output
Vout+
Vout-
R16 301.0 Ω
R17 301.0 Ω
R21 100.0 Ω
R22 100.0 Ω
Vref_adc
C35 100nF
Thermal pad to GND with vias.
LMH6553 max 37mA
U5B
DAP
LMH6553MR/NOPB
Remove ground and power plane metal from beneath LMH6553 and RF and RG. Exposed die attached pad (DAP) to GND with vias.
Title Vienna-Scope
Size: A4
Number:
Revision:
Date: 30/10/2020 Time: 21:26:06
Sheet of
File: AFE-Diff-Gain.SchDoc
Altium Limited
3 Minna Close
Belrose
NSW 2085
Australia
CIRCUITMAKER



Title			*Altium Limited* *3 Minna Close* *Belrose* *NSW 2085* *Australia*
Size: A4	Number:	Revision:	
Date: 30/10/2020 Time: 21:26:07		Sheet of	
File: AWG.SchDoc			

CIRCUITMAKER



CMODE: Clock Mode Selection. Connect to CLKCOM for single-ended clock receiver (drive CLK+ and float CLK–). Connect to CLKVDD for differential receiver. Float for PECL receiver (terminations on-chip).

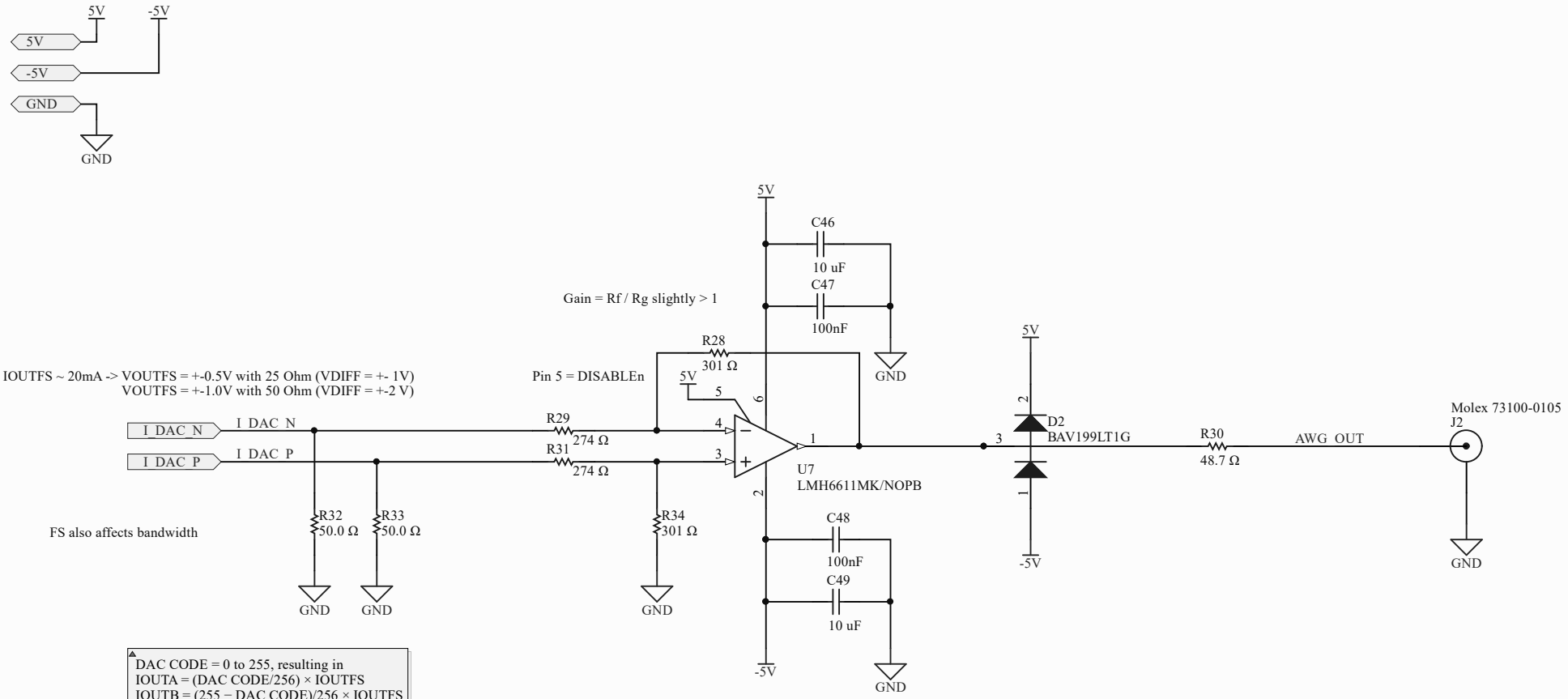
MODE: Selects Input Data Format. Connect to DCOM for straight binary, DVDD for twos complement.

FS ADJ:. Full-Scale Current Output Adjust: IREF = VREFIO/RSET (internal 1.2V reference). The full-scale current, IOUTFS, is 32 times IREF.

SLEEP: Power-Down Control Input. Active high. Contains active pull-down circuit; it can be left unterminated if not used.

Power dissipation: 135 mW @ 3.3 V
Power-down mode: 15 mW @ 3.3 V

Title			*Altium Limited* *3 Minna Close* *Belrose* *NSW 2085* *Australia*
Size: A4	Number:	Revision:	
Date: 30/10/2020 Time: 21:26:07		Sheet of	
File: AWG-DAC.SchDoc			



DAC CODE = 0 to 255, resulting in
IOUTA = (DAC CODE/256) × IOUTFS
IOUTB = (255 − DAC CODE)/256 × IOUTFS

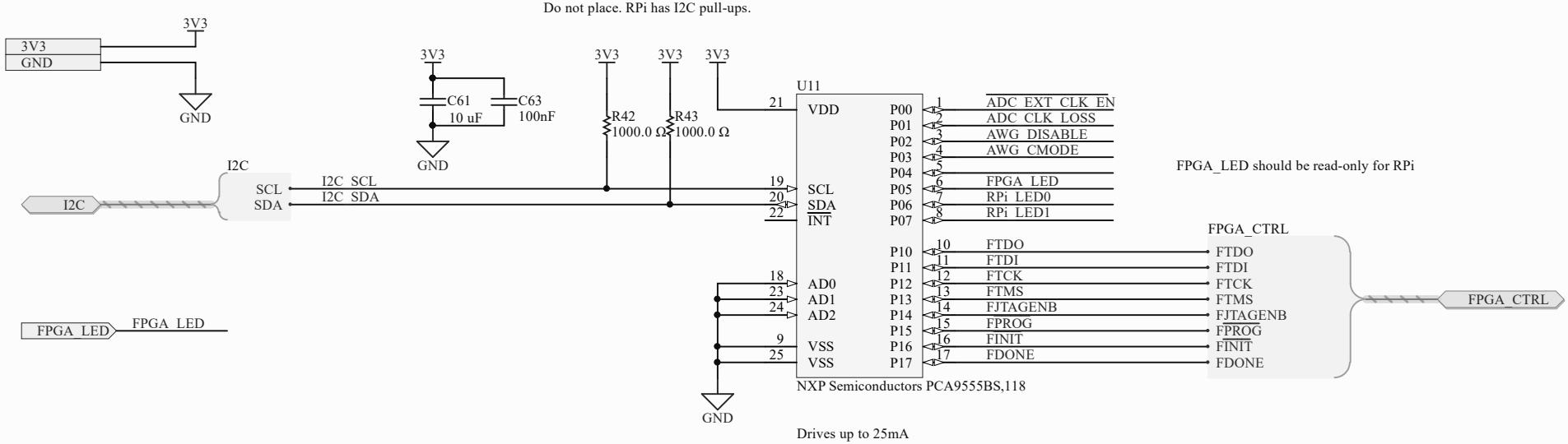
VOUTA = IOUTA × RLOAD,
VOUTB = IOUTB × RLOAD

VDIFF = (IOUTA − IOUTB) × RLOAD

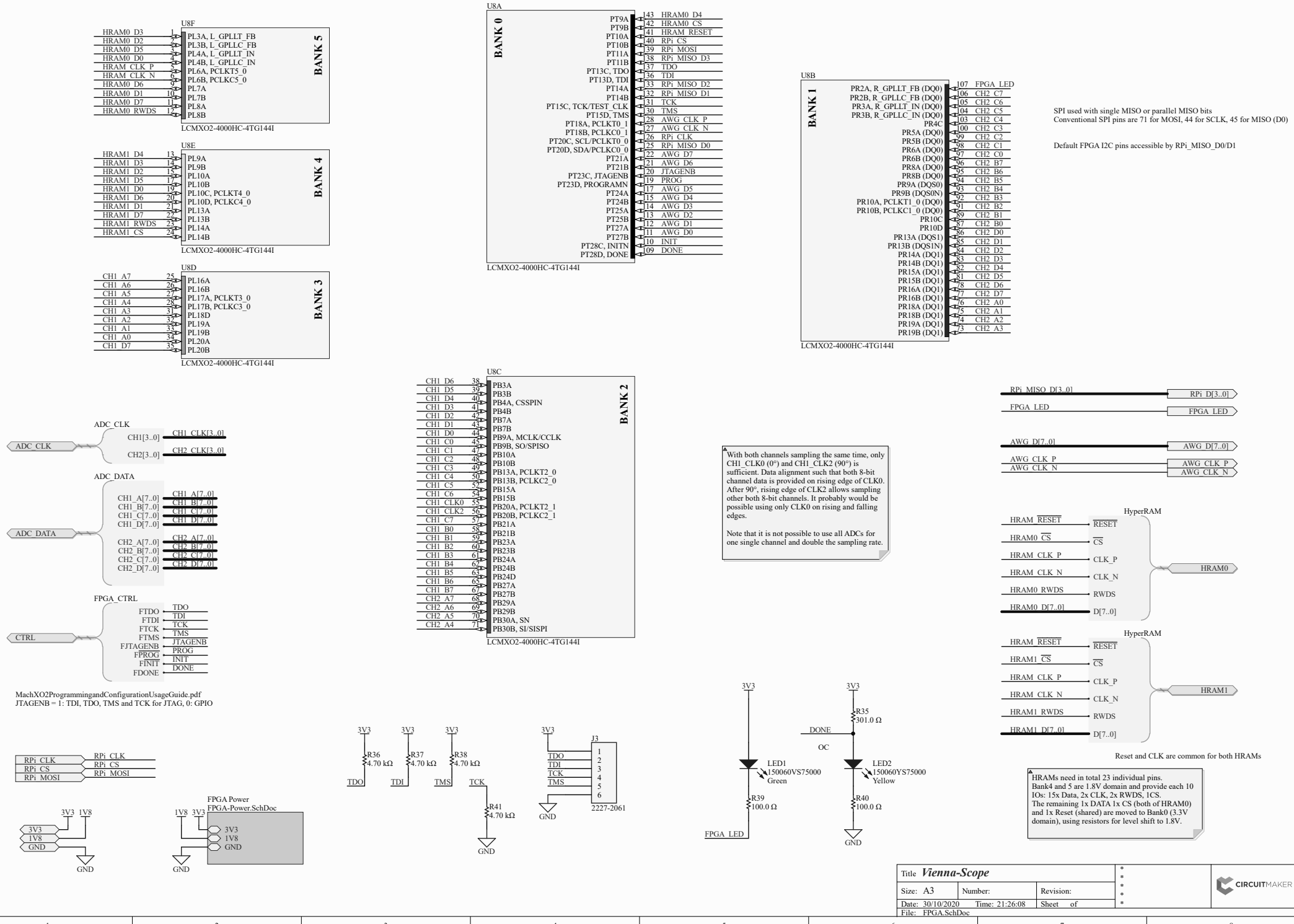
For optimal performance limit voltage swing at IOUTA and IOUTB to ±0.5 V.

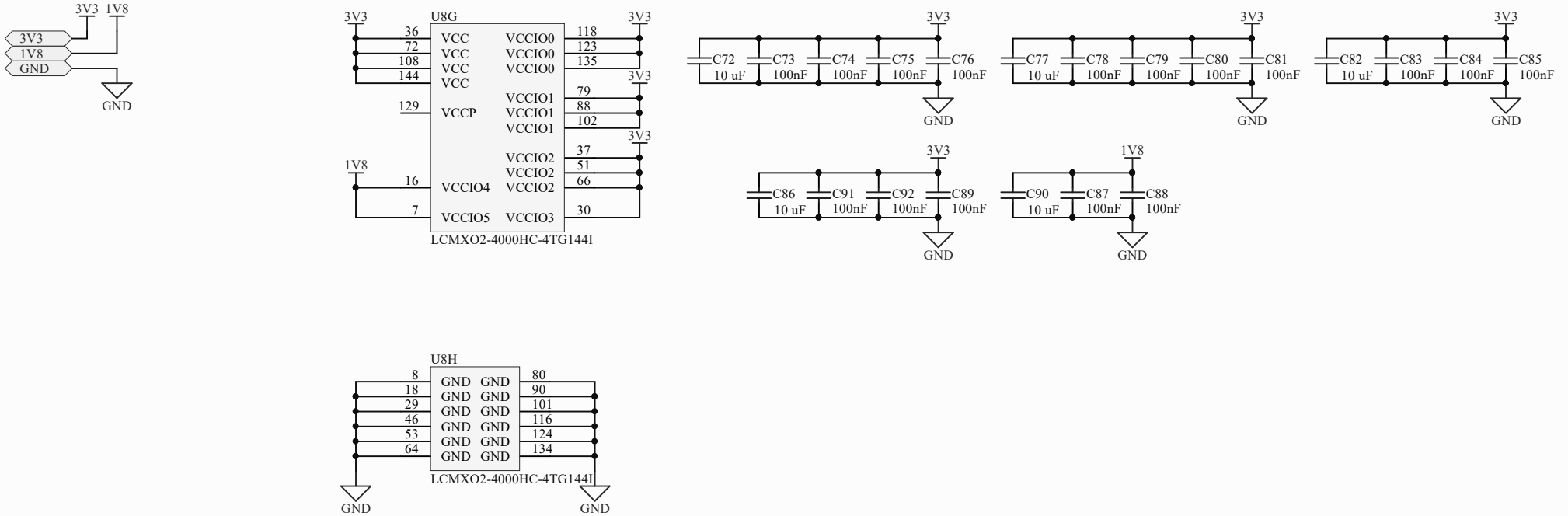
Title			*Altium Limited* *3 Minna Close* *Belrose* *NSW 2085* *Australia*
Size: A4	Number:	Revision:	
Date: 30/10/2020 Time: 21:26:07		Sheet of	
File: AWG-Power.SchDoc			

CIRCUITMAKER

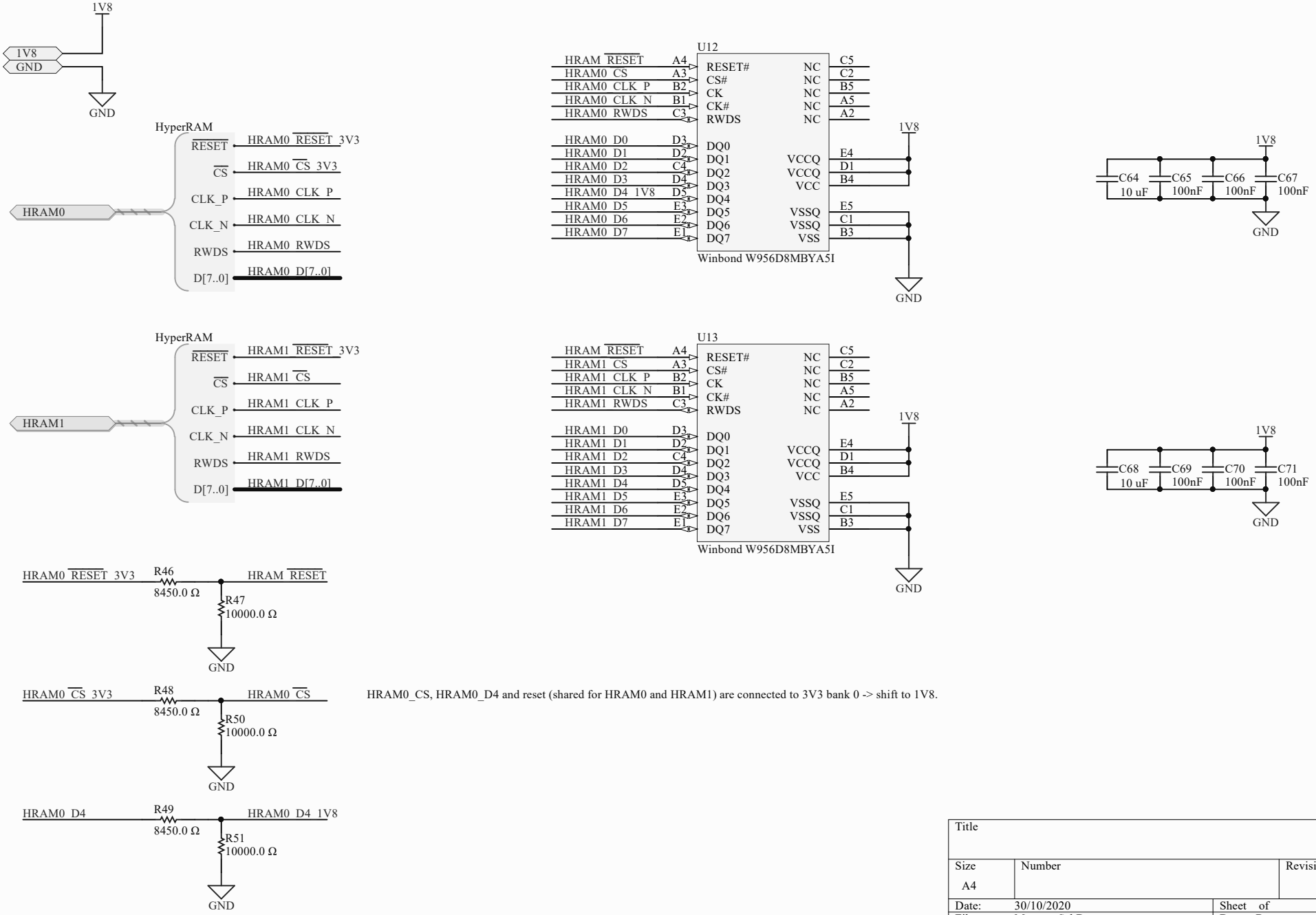


Title			*Altium Limited* *3 Minna Close* *Belrose* *NSW 2085* *Australia*
Size: A4	Number:	Revision:	
Date: 30/10/2020 Time: 21:26:07		Sheet of	
File: Control.SchDoc			


U8F
BANK 5
HRAM0_D3 1 PL3A, L_GPLLT_FB
HRAM0_D2 2 PL3B, L_GPLLC_FB
HRAM0_D5 3 PL4A, L_GPLLT_IN
HRAM0_D0 4 PL4B, L_GPLLC_IN
HRAM_CLK_P 5 PL6A, PCLKT5_0
HRAM_CLK_N 6 PL6B, PCLKC5_0
HRAM0_D6 9 PL7A
HRAM0_D1 10 PL7B
HRAM0_D7 11 PL8A
HRAM0_RWDS 12 PL8B
LCMXO2-4000HC-4TG144I
U8E
BANK 4
HRAM1_D4 13 PL9A
HRAM1_D3 14 PL9B
HRAM1_D2 15 PL10A
HRAM1_D5 17 PL10B
HRAM1_D0 19 PL10C, PCLKT4_0
HRAM1_D6 20 PL10D, PCLKC4_0
HRAM1_D1 21 PL13A
HRAM1_D7 22 PL13B
HRAM1_RWDS 23 PL14A
HRAM1_CS 24 PL14B
LCMXO2-4000HC-4TG144I
U8D
BANK 3
CH1_A7 25 PL16A
CH1_A6 26 PL16B
CH1_A5 27 PL17A, PCLKT3_0
CH1_A4 28 PL17B, PCLKC3_0
CH1_A3 31 PL18D
CH1_A2 32 PL19A
CH1_A1 33 PL19B
CH1_A0 34 PL20A
CH1_D7 35 PL20B
LCMXO2-4000HC-4TG144I
U8A
BANK 0
PT9A 143 HRAM0_D4
PT9B 142 HRAM0_CS
PT10A 141 HRAM_RESET
PT10B 140 RPi_CS
PT11A 139 RPi_MOSI
PT11B 138 RPi_MISO_D3
PT13C, TDO 137 TDO
PT13D, TDI 136 TDI
PT14A 133 RPi_MISO_D2
PT14B 132 RPi_MISO_D1
PT15C, TCK/TEST_CLK 131 TCK
PT15D, TMS 130 TMS
PT18A, PCLKT0_1 128 AWG_CLK_P
PT18B, PCLKC0_1 127 AWG_CLK_N
PT20C, SCL/PCLKT0_0 126 RPi_CLK
PT20D, SDA/PCLKC0_0 125 RPi_MISO_D0
PT21A 122 AWG_D7
PT21B 121 AWG_D6
PT23C, JTAGENB 120 JTAGENB
PT23D, PROGRAMN 119 PROG
PT24A 117 AWG_D5
PT24B 115 AWG_D4
PT25A 114 AWG_D3
PT25B 113 AWG_D2
PT27A 112 AWG_D1
PT27B 111 AWG_D0
PT28C, INITN 110 INIT
PT28D, DONE 109 DONE
LCMXO2-4000HC-4TG144I
U8B
BANK 1
PR2A, R_GPLLT_FB (DQ0) 107 FPGA_LED
PR2B, R_GPLLC_FB (DQ0) 106 CH2_C7
PR3A, R_GPLLT_IN (DQ0) 105 CH2_C6
PR3B, R_GPLLC_IN (DQ0) 104 CH2_C5
PR4C 103 CH2_C4
PR5A (DQ0) 100 CH2_C3
PR5B (DQ0) 99 CH2_C2
PR6A (DQ0) 98 CH2_C1
PR6B (DQ0) 97 CH2_C0
PR8A (DQ0) 96 CH2_B7
PR8B (DQ0) 95 CH2_B6
PR9A (DQS0) 94 CH2_B5
PR9B (DQS0N) 93 CH2_B4
PR10A, PCLKT1_0 (DQ0) 92 CH2_B3
PR10B, PCLKC1_0 (DQ0) 91 CH2_B2
PR10C 89 CH2_B1
PR10D 87 CH2_B0
PR13A (DQS1) 86 CH2_D0
PR13B (DQS1N) 85 CH2_D1
PR14A (DQ1) 84 CH2_D2
PR14B (DQ1) 83 CH2_D3
PR15A (DQ1) 82 CH2_D4
PR15B (DQ1) 81 CH2_D5
PR16A (DQ1) 78 CH2_D6
PR16B (DQ1) 77 CH2_D7
PR18A (DQ1) 76 CH2_A0
PR18B (DQ1) 75 CH2_A1
PR19A (DQ1) 74 CH2_A2
PR19B (DQ1) 73 CH2_A3
LCMXO2-4000HC-4TG144I
SPI used with single MISO or parallel MISO bits
Conventional SPI pins are 71 for MOSI, 44 for SCLK, 45 for MISO (D0)
Default FPGA I2C pins accessible by RPi_MISO_D0/D1
U8C
BANK 2
CH1_D6 38 PB3A
CH1_D5 39 PB3B
CH1_D4 40 PB4A, CSSPIN
CH1_D3 41 PB4B
CH1_D2 42 PB7A
CH1_D1 43 PB7B
CH1_D0 44 PB9A, MCLK/CCLK
CH1_C0 45 PB9B, SO/SPISO
CH1_C1 47 PB10A
CH1_C2 48 PB10B
CH1_C3 49 PB13A, PCLKT2_0
CH1_C4 50 PB13B, PCLKC2_0
CH1_C5 52 PB15A
CH1_C6 54 PB15B
CH1_CLK0 55 PB20A, PCLKT2_1
CH1_CLK2 56 PB20B, PCLKC2_1
CH1_C7 57 PB21A
CH1_B0 58 PB21B
CH1_B1 59 PB23A
CH1_B2 60 PB23B
CH1_B3 61 PB24A
CH1_B4 62 PB24B
CH1_B5 63 PB24D
CH1_B6 65 PB27A
CH1_B7 67 PB27B
CH2_A7 68 PB29A
CH2_A6 69 PB29B
CH2_A5 70 PB30A, SN
CH2_A4 71 PB30B, SI/SISPI
LCMXO2-4000HC-4TG144I
RPi_MISO_D[3..0]
RPi_D[3..0]
FPGA_LED
AWG_D[7..0]
AWG_CLK_P
AWG_CLK_N
ADC_CLK
CH1[3..0]
CH1_CLK[3..0]
CH2[3..0]
CH2_CLK[3..0]
ADC_DATA
CH1_A[7..0]
CH1_B[7..0]
CH1_C[7..0]
CH1_D[7..0]
CH2_A[7..0]
CH2_B[7..0]
CH2_C[7..0]
CH2_D[7..0]
With both channels sampling the same time, only CH1_CLK0 (0°) and CH1_CLK2 (90°) is sufficient. Data alignment such that both 8-bit channel data is provided on rising edge of CLK0. After 90°, rising edge of CLK2 allows sampling other both 8-bit channels. It probably would be possible using only CLK0 on rising and falling edges.
Note that it is not possible to use all ADCs for one single channel and double the sampling rate.
HyperRAM
HRAM_RESET
HRAM0_CS
HRAM_CLK_P
HRAM_CLK_N
HRAM0_RWDS
HRAM0_D[7..0]
RESET
CS
CLK_P
CLK_N
RWDS
D[7..0]
HRAM0
HyperRAM
HRAM1_CS
HRAM1_RWDS
HRAM1_D[7..0]
HRAM1
Reset and CLK are common for both HRAMs
FPGA_CTRL
FTDO
FTDI
FTCK
FTMS
FJTAGENB
FPROG
FINIT
FDONE
TDO
TDI
TCK
TMS
JTAGENB
PROG
INIT
DONE
CTRL
MachXO2ProgrammingandConfigurationUsageGuide.pdf
JTAGENB = 1: TDI, TDO, TMS and TCK for JTAG, 0: GPIO
HRAMs need in total 23 individual pins.
Bank4 and 5 are 1.8V domain and provide each 10 IOs: 15x Data, 2x CLK, 2x RWDS, 1CS.
The remaining 1x DATA 1x CS (both of HRAM0) and 1x Reset (shared) are moved to Bank0 (3.3V domain), using resistors for level shift to 1.8V.
RPi_CLK
RPi_CS
RPi_MOSI
3V3
1V8
GND
FPGA Power
FPGA-Power.SchDoc
R36 4.70 kΩ
R37 4.70 kΩ
R38 4.70 kΩ
R41 4.70 kΩ
J3
2227-2061
R35 301.0 Ω
DONE
OC
LED1 150060VS75000 Green
LED2 150060VS75000 Yellow
R39 100.0 Ω
R40 100.0 Ω
Title Vienna-Scope
Size: A3
Number:
Revision:
Date: 30/10/2020
Time: 21:26:08
Sheet of
File: FPGA.SchDoc
CIRCUITMAKER



Title		
Size: A4	Number	Revision
Date: 30/10/2020		Sheet of
File: FPGA-Power.SchDoc		Drawn By:



HRAM0_CS, HRAM0_D4 and reset (shared for HRAM0 and HRAM1) are connected to 3V3 bank 0 -> shift to 1V8.

Title		
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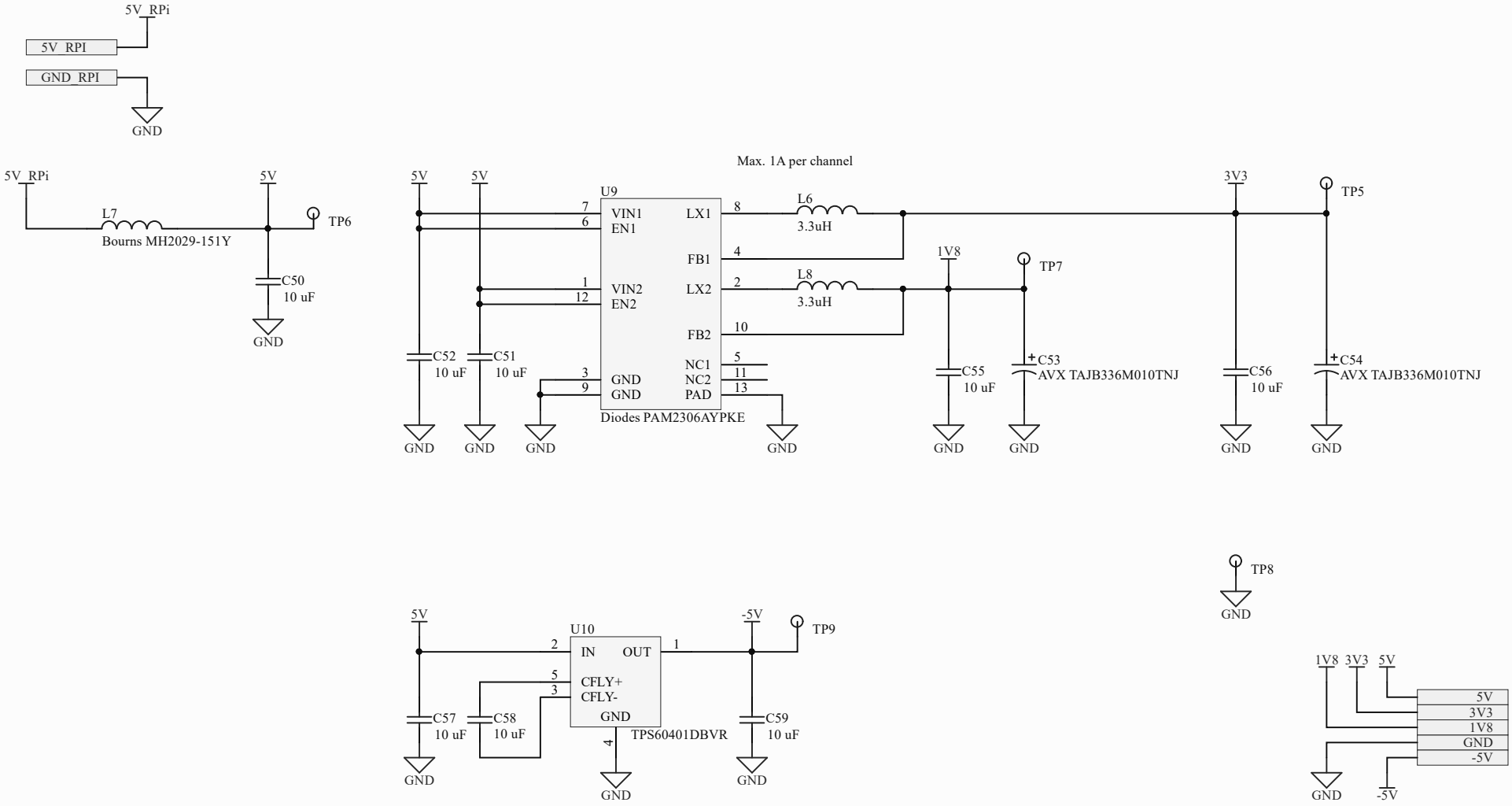
Date: 30/10/2020		Sheet of
File: Memory.SchDoc		Drawn By:



Title			*Altium Limited* *3 Minna Close* *Belrose* *NSW 2085* *Australia*
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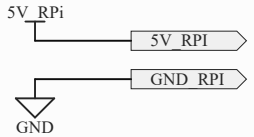
Even though 3.3V from RPi would be availabe, it is ignored and not used. Instead, VS generates onboard 3.3V and 1.8V from USB-5V to allow using a different control board.

I2C 7-bit addresses:

PCA9555: 0100 000
Si5365A: 1110 000
MCP4728A0: 1100 000
MachOX2: 1000000 (7-bit mode) or 1111000000 (10-bit mode).

LSB (R/W\) determines read = 1 or write = 0



Top view with components placed this side.

Stackup shall be VS (female) on bottom and RPi Zero W on top of it (male).

Thus, RPi connector should be placed towards right side edge of VS.

RPi Zero W dimensions: 66.0mm x 30.5mm x 5.0mm.

SPI uses RPi as master and has three functions:
-VGA configuration using three wires: SCLK_S, CS, SDIO, that is MOSI,
-FPGA configuration using four wires: SCLK_M, CS, MOSI, MISO0,
-Parallel high speed bus from FPGA to RPi using extended SPI: SCLK_M, CS, 4-6x MISO or one MOSI/SDIO.

SCLK_M is the default clock source and is not connected to VGA clock SCLK_S to avoid undesired coupling.

Title			*Altium Limited* *3 Minna Close* *Belrose* *NSW 2085* *Australia*
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File: RPi.SchDoc			

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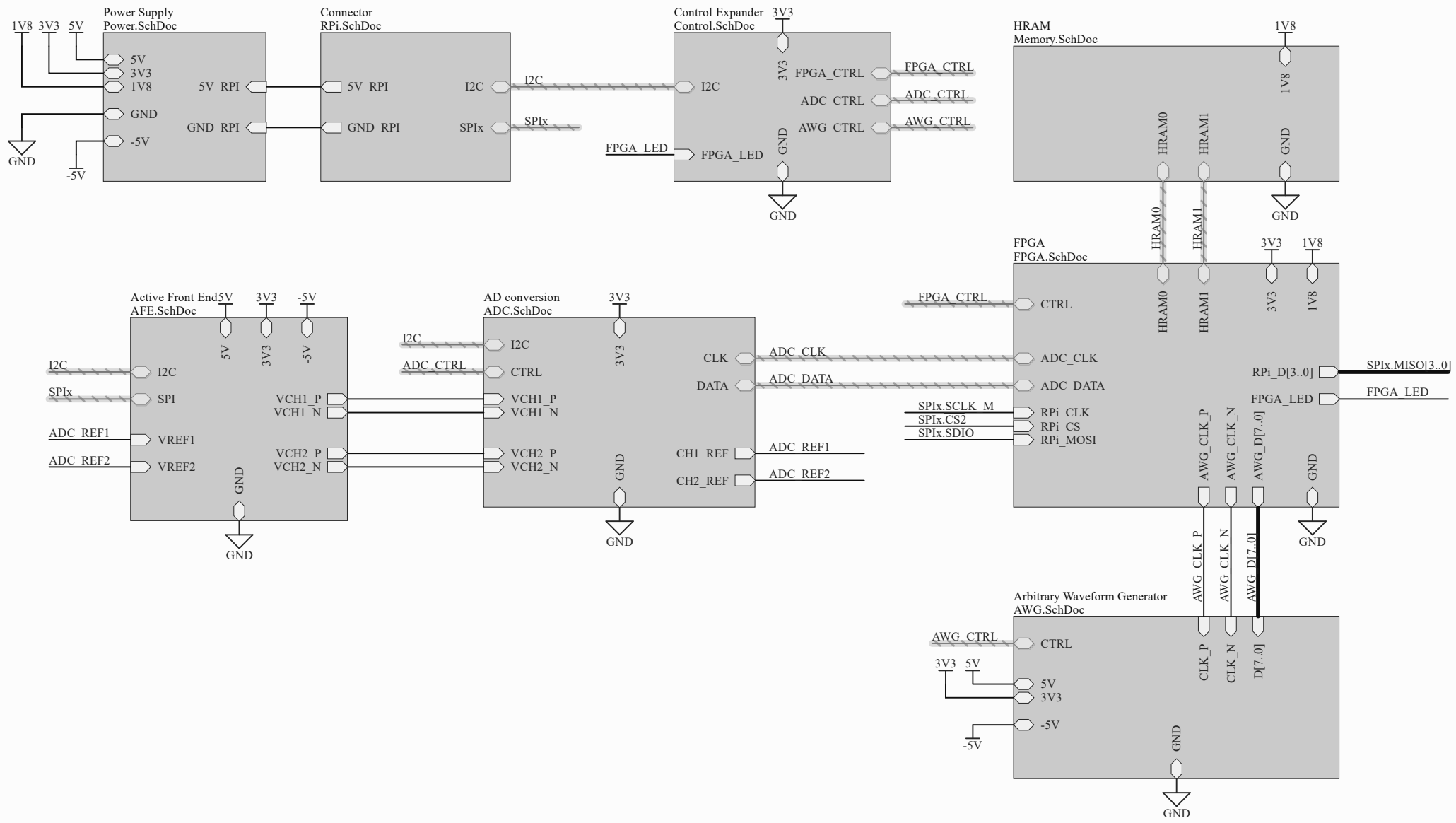
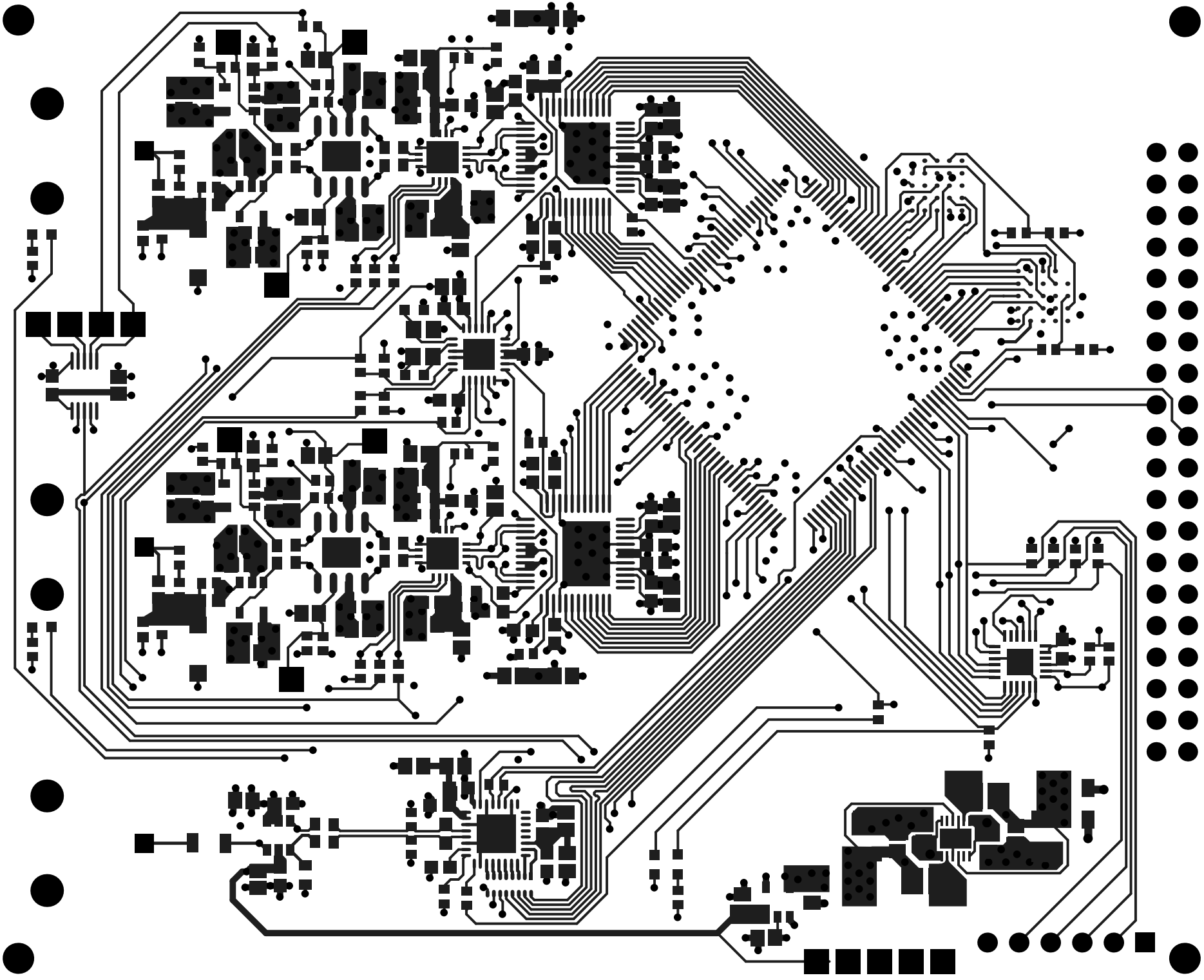
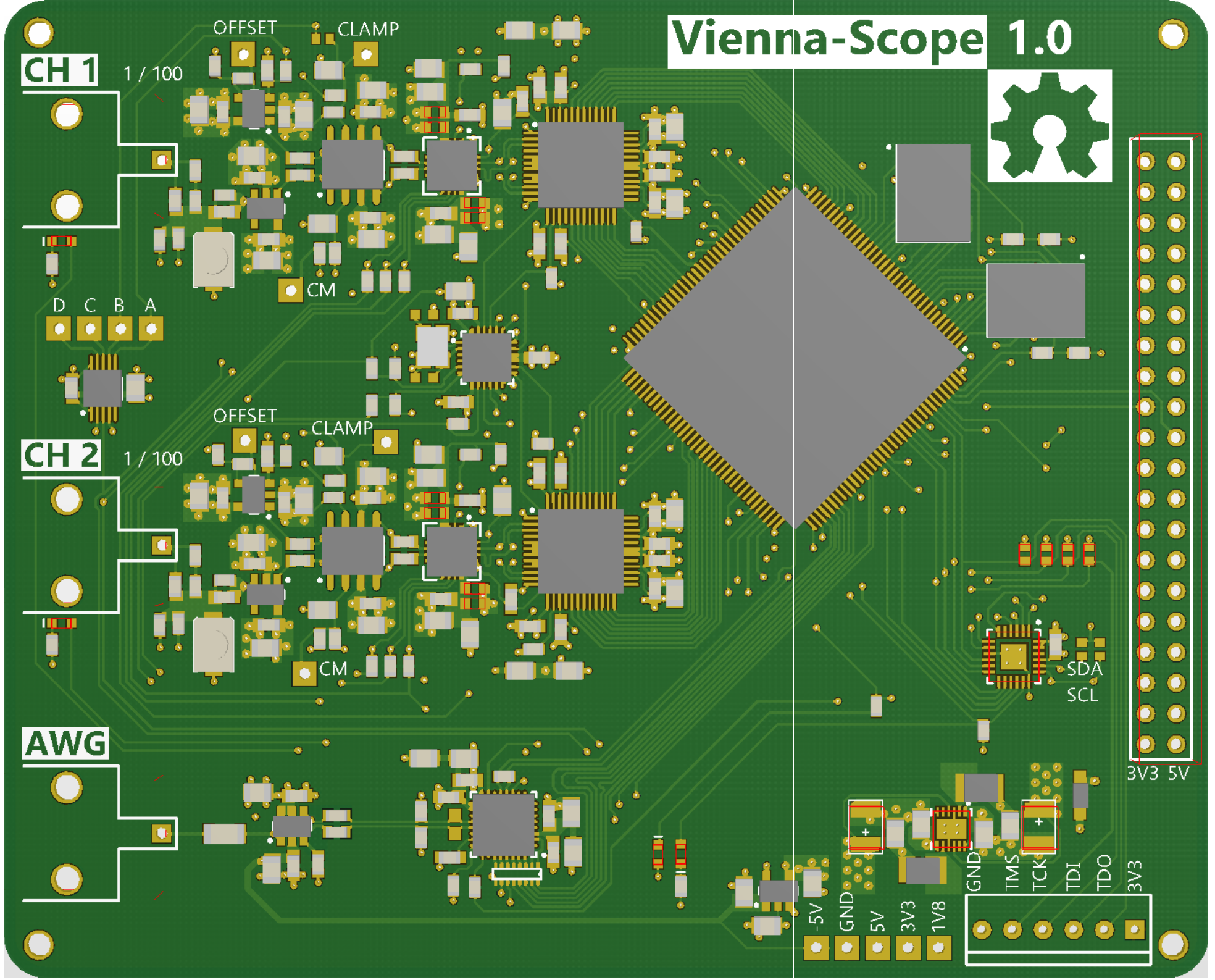

Power Supply
Power.SchDoc
1V8 3V3 5V
5V
3V3
1V8
GND
-5V
5V_RPI
GND_RPI
GND
-5V
Connector
RPi.SchDoc
5V_RPI
GND_RPI
I2C
SPIx
I2C
SPIx
Control Expander
Control.SchDoc
3V3
I2C
FPGA_LED
3V3
FPGA_CTRL
ADC_CTRL
AWG_CTRL
GND
FPGA_CTRL
ADC_CTRL
AWG_CTRL
FPGA_LED
GND
HRAM
Memory.SchDoc
1V8
HRAM0
HRAM1
GND
1V8
HRAM0
HRAM1
GND
FPGA
FPGA.SchDoc
FPGA_CTRL
CTRL
HRAM0
HRAM1
3V3
1V8
ADC_CLK
ADC_DATA
RPi_CLK
RPi_CS
RPi_MOSI
RPi_D[3..0]
FPGA_LED
SPIx.SCLK_M
SPIx.CS2
SPIx.SDIO
SPIx.MISO[3..0]
FPGA_LED
AWG_CLK_P
AWG_CLK_N
AWG_D[7..0]
GND
Active Front End
AFE.SchDoc
5V
3V3
-5V
I2C
SPIx
ADC_REF1
ADC_REF2
I2C
SPI
VREF1
VREF2
VCH1_P
VCH1_N
VCH2_P
VCH2_N
GND
AD conversion
ADC.SchDoc
3V3
I2C
ADC_CTRL
I2C
CTRL
3V3
CLK
DATA
CH1_REF
CH2_REF
ADC_CLK
ADC_DATA
ADC_REF1
ADC_REF2
VCH1_P
VCH1_N
VCH2_P
VCH2_N
GND
Arbitrary Waveform Generator
AWG.SchDoc
AWG_CTRL
CTRL
3V3
5V
5V
3V3
-5V
-5V
GND
CLK_P
CLK_N
D[7..0]
AWG_CLK_P
AWG_CLK_N
AWG_D[7..0]
GND
Title Vienna-Scope
Size: A4
Number:
Revision:
Date: 30/10/2020
Time: 21:26:09
Sheet of
File: Top.SchDoc
3 Minna Close
Belrose
NSW 2085
Australia
CIRCUITMAKER




Vienna-Scope 1.0
CH 1
1 / 100
OFFSET
CLAMP
CM
D C B A
CH 2
1 / 100
OFFSET
CLAMP
CM
AWG
SDA
SCL
3V3 5V
-5V GND 5V 3V3 1V8
GND TMS TCK TDI TDO 3V3