**MINISTRY OF EDUCATION AND TRAINING**

**HCMC UNIVERSITY OF TECHNOLOGY AND EDUCATION**

**FACULTY OF INTERNATIONAL EDUCATION**



**SENIOR PROJECT 2 REPORT**

**TOPIC: DESIGN AND EVALUATION OF LOW POWER SRAM**

|  |  |  |
| --- | --- | --- |
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**ABSTRACT**

Memory caches made from Static Random Access Memory (SRAM) cells are one of the most essential components on modern computers in order to minimize operation delay due to the separation between the Central Processing Unit and the Memory Cache. All SRAM designs have to be stable in their Write, Read and Hold operations so that the data stored inside them does not get corrupted by noise. Due to SRAM working at a very high frequency, it tends to dissipates a lot of power, which gives the need to also lessen the power consumption. This project has analyzed and compared the characteristics of the common 6-Transistor (6T) design with the 8-Transistor (8T) design, and also proposed a Low-power variant of each design using various power-reducing techniques, namely Power Gating and Voltage Scaling. The operation of the SRAM cells is simulated with the CADENCE Virtuoso Design Suite using the Complementary Metal Oxide Semiconductor (aka CMOS) on the 90nm TSMC Process. Finally, this project presents the analysis of various characteristics of the SRAM designs, including power consumption and delay under different simulated scenarios.

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# Overview

## Trends in Microchip and Integrated Circuits design today

Digital designs have taken the world by storm over the past decades and computer systems continue to develop every day. On the other hand, faster and more complicated computers also result in higher power consumption, higher cost, etc. Thus came the following trends in IC designs:

* Power optimization and leakage reduction
* Timing optimization
* AI-driven floorplanning and placement
* etc…

## Rationale of Project

The CMOS technology has been integral in the development of the semiconductor memory system design and manufacture industry. In any computer, the cache memory directly influences the performance and operation of the whole system due to it being closely connected to the CPU. One of the most commonly used computer architecture is the Von-Neumann architecture. The Von-Neumann architecture can have bottlenecks [1] from too much information that couldn’t be processed in time, which gave the need for high-speed cache memories, usually made from Static Random Access Memory (SRAM) cells in order to store immediate instructions and data which are waiting for their turn to be processed, thus minimizes said bottlenecking from happening.

The rise of embedded systems in general and microcontrollers in particular has put up new challenges in optimizing design area, power consumption, stability and performance. Nowadays, cache memory systems with smaller CMOS process nodes such as 45nm or smaller that are fast but also expensive are mostly used in modern high-performance computer systems. That said, common microcontrollers like the Arduino or STM32 boards all utilize SRAM cache memories to store programs and process data, albeit with larger node processes. Larger node processes like the 90nm TSMC process are still being used in low-performance embedded systems and Internet of Things (IoT) applications [3] due to their low cost and power consumption.

After assessing the trends and problems stated above, we reached the decision that we will be taking on the “Design and Evaluation of Low Power SRAM” project.

## Research Subjects

The 6T and 8T SRAM low-power project encompasses a wide range of topics, including low-power circuit design, stability and reliability analysis, technology scaling, optimization for low voltage operation, and performance enhancement. Evaluation of the performance of 6T and 8T SRAM involves analyzing read and write access times, power consumption, stability under low-voltage operation, and reliability metrics.

## Project Goals and Objectives

In this project, we are focused on achieving improved performance, reduced power consumption, enhanced stability in memory design, and evaluating performance. This includes reducing power leakage, optimizing circuitry for power efficiency, improving data retrieval and storage speed, enhancing stability and reliability in low-power modes, enabling low-voltage operation, ensuring compatibility with semiconductor manufacturing processes, minimizing standby power consumption, and improving noise immunity, evaluating power consumption, delay and SMN (Static Noise Margin) between 6T and 8T designs. These objectives collectively aim to address the challenges of designing low-power SRAM, ultimately striving to create efficient, reliable, and compact memory solutions for modern electronic devices.

## Cadence Virtuoso

Cadence Virtuoso is a widely used Electronic Design Automation (EDA) tool suite that provides a platform for designing integrated circuits (ICs) and semiconductor devices. It offers a user-friendly environment for schematic capture, layout, simulation, and verification of complex analog, digital, and mixed-signal designs. In conjunction with the 90nm Process Design Kit (PDK) provided by TSMC, Virtuoso enables engineers to create circuit layouts, perform simulations, and verify designs according to the specific manufacturing process requirements.

# Theoretical Basis

## CMOS Theory

The majority of integrated circuits are built using silicon (Si), a semiconductor. Atoms are arranged in a three-dimensional lattice in pure silicon. Since silicon is a Group IV element, as Figure 2.1(a) illustrates, it can form covalent connections with four neighboring atoms. For drawing convenience, the lattice is depicted in the plane, although in reality, it forms a cubic crystal.

Pure silicon is not a good conductor because all of its valence electrons are bound together in chemical compounds. Dopants, or minute quantities of impurities, can be added to the silicon lattice to increase conductivity. Group V dopants (like arsenic) have five valence electrons in their structure. As seen in Figure 2.1(b), it substitutes a silicon atom in the lattice while still forming connections with four neighbors, leaving the fifth valence electron freely attached to the arsenic atom. At ambient temperature, the lattice's thermal vibrations are sufficient to release the electron, leaving behind a free electron and a positively charged As+ ion. Since a free electron can transport current, conductivity is increased. Because the free carriers are electrons with a negative charge, we refer to this semiconductor as an n-type. Similarly, as seen in Figure 2.1(c), a Group III dopant like boron has three valence electrons. An electron can be borrowed by the dopant atom from a nearby silicon atom, causing the latter to become one electron shorter. The hole, or missing electron, can move around the lattice by being borrowed by that atom, and so on. We refer to this as a p-type semiconductor since the hole functions as a positive carrier.

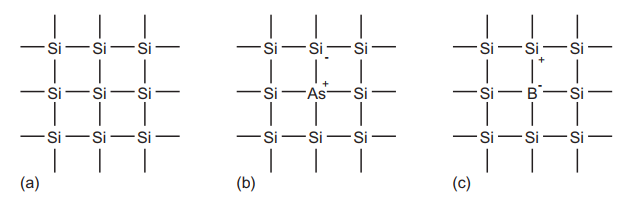
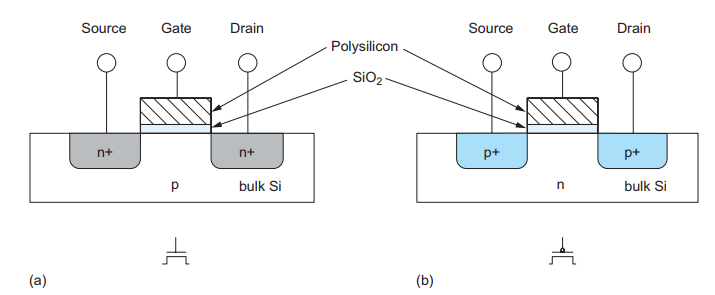


Figure 2. 1. Silicon lattice and dopant atoms.

A Metal-Oxide-Semiconductor (MOS) structure is a sandwich-like structure made of conducting and insulating layers layered on top of one another. A sequence of chemical processing procedures, including silicon oxidation, selective dopant introduction, and the deposition and etching of metal wires and contacts, are used to create these structures. The virtually faultless single crystals of silicon used to build transistors are sold as thin, flat, round wafers with a diameter of 15 to 30 cm. Two types of transistors (sometimes referred to as devices) are available with CMOS technology: n-type transistors (nMOS) and p-type transistors (pMOS). Since electric fields regulate transistor function, the devices are often referred to as Metal Oxide Semiconductor Field Effect Transistors, or MOSFETs for short.

Figure 2.2 displays the transistors' cross-sections and symbols. Heavily doped n- or p-type silicon is shown by the n+ and p+ areas.



*Figure 2. 2. (a) nMOS transistor and (b) pMOS transistor.*

**nMOS Transistor:** The source and drain of a nMOS transistor are n-type semiconductor areas that are located next to the gate and are constructed with a p-type body. Since they are physically identical, we will treat them as such for the time being. Usually, the body is grounded.

**pMOS Transistor:** The exact opposite is a pMOS transistor, which has an n-type body and p-type source and drain regions. The substrate can be either n-type or p-type in CMOS technology that uses both types of transistors. To create the other type of transistor's body, dopant atoms must be put to a specific well where the other flavor of transistor is to be constructed.

The gate is the control input which modifies the direction of electrical current flow between the source and drain. Consider a nMOS transistor. The p-n junctions of the source and drain to the body are reverse-biased because the body is typically grounded. There is no current flowing through the reverse-biased junctions if the gate is also grounded. As a result, we declare the transistor off. Raising the gate voltage produces an electric field that begins to draw free electrons to the Si–SiO2 interface's bottom. When the voltage is sufficiently increased, the electrons begin to outweigh the holes, causing the channel—a small area beneath the gate—to invert and function as an n-type semiconductor. As a result, current can flow and an electron carrier conducting route forms from source to drain. The transistor is said to be ON.

Once more, the situation is the opposite for a pMOS transistor. The voltage applied to the body is positive. The transistor is off when the gate is likewise positive since this causes the source and drain junctions to become reverse-biased and prevent current flow. Positive charges are drawn to the underside of the Si–SiO2 contact when the gate voltage is reduced. The transistor turns on when the gate voltage is low enough to invert the channel and create a conducting path for positive carriers from the source to the drain. Observe that the pMOS transistor's symbol has a bubble on the gate, signifying that its behavior differs from that of the nMOS.

## 6-Transistor (6T) SRAM

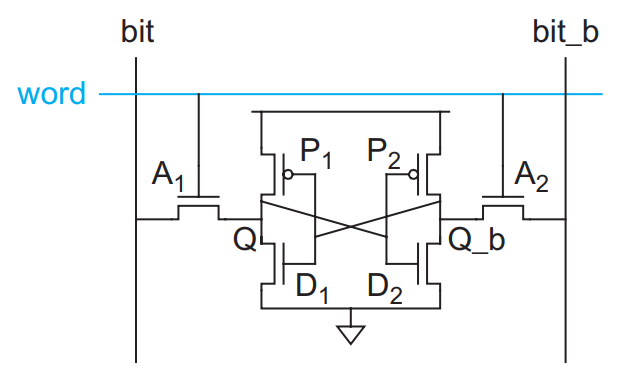


Figure 2. 3. Diagram of 6T SRAM Cell.

The 6-Transistor SRAM Cell essentially comprises of 2 Inverters (P1 + D1 and P2 + D2), each with their output connected to the other’s input, and 2 nMOS acting as Access ports for the SRAM Cell. The Bitlines bit and bit\_b are the data to be written (by a Data Write Circuit) into the SRAM Cell, which is allowed to do so by having the Wordline word activated.

### Operation Principle

**Read operation:**

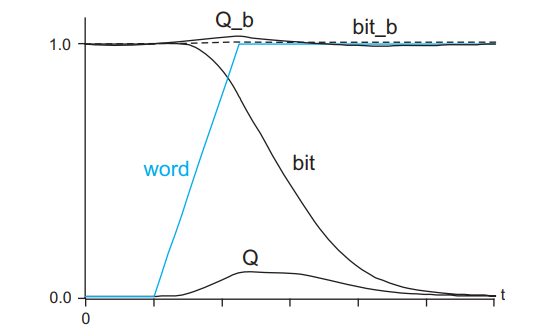
* Initially, the Bitlines bit and bit\_b will be floating high, then Wordline word is raised, activating the two Access transistors.
* Assume Q is initially 0 (and Q\_b is initially 1). Both bitlines are floating at high, and with Q = 0, the voltage at Q will be raised due to bit being pulled to GND with the current flowing through Q.
* However, if Q, which is the input to the right Inverter, is raised above the threshold voltage of the nMOS, the Inverter will output logic 0 at Q\_b and bit\_b will be pulled to GND, causing an error in the Read operation.
* To counter this, the transistors D1 and D2 must be stronger (that is to say it can allow the current to pass through it more easily) than their respective Access transistors in order to have bit or bit\_b being pulled to GND immediately without raising Q or Q\_b which might cause bit-flippings that can lead to Read errors. This is called Read stability.

Figure 2. 4. Read waveform.

* Finally, when one of the two bitlines have a voltage drop (means there are a difference in voltage between them), the bitlines will go through a Sense Amplifier which will sense the voltage difference and essentially “reads” the data stored inside individual SRAM Cells.

**Write operation:**

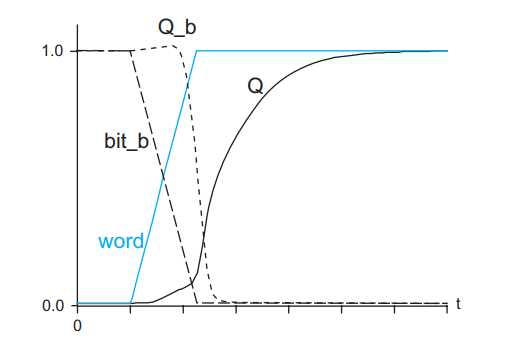
* Assume that Q is initially 0 and a logic 1 is needed to be written into Q, meaning Q\_b is at logic 1 and is needed to be pulled down to 0. Bitlines are not at floating high. Instead, the bitlines are charged by a Write Driver. Wordline is also raised.
* ****However, we know that Q\_b cannot be pulled to 0 through D2 (established in Read operation). Instead, Q\_b will be pulled down to 0 through A2 to bit\_b.

Figure 2. 5. Write waveform.

* When Q\_b is pulled down to 0, it will turn on P1, which will raise Q to 1. In order for Q\_b to be pulled down without causing errors, P2 will need to be much weaker than A2 (same to P1 and A1). This is called Write stability.

**SRAM Architecture:**

A complete SRAM memory circuit comprises of a memory cell with other devices such as row and column decoders, sense amplifiers, write drivers and prechargers [1-2]. The accompanying blocks allow for read and write operation on the memory cell. The following figure presents the block diagram of a typical SRAM circuit.

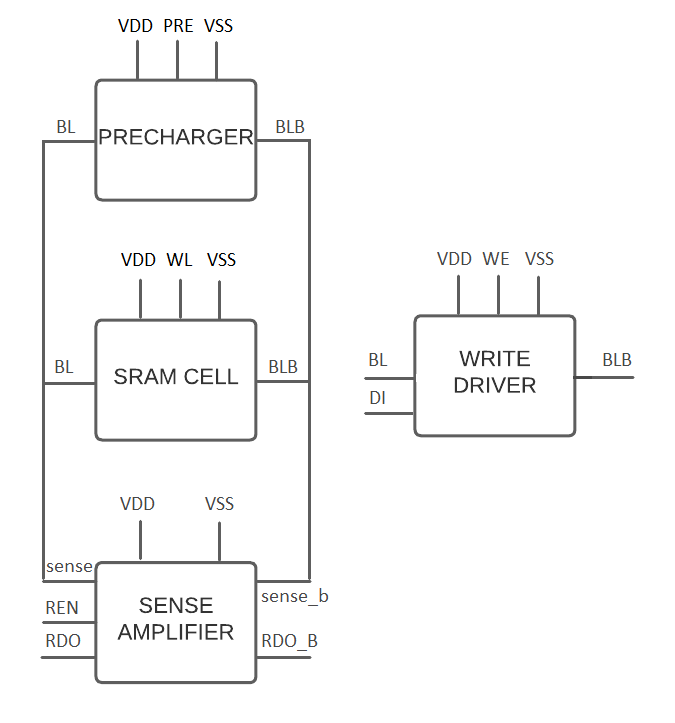


Figure 2. 6. Block diagram of SRAM circuit.

The typical SRAM design consists of 4 blocks [8]: Precharger to precharge the circuit, Sense Amplifier to sense and amplify signals on bitlines to read out data, Write Driver to write data onto the memory cell, and the SRAM Cell itself. The blocks are connected via the **BL** and **BLB** bitlines. The **PRE** signal activates the Precharger and the bitlines are pulled to HIGH. **sense** and **sense\_b** lines are connected to **BL** and **BLB** respectively. **REN** (Read Enable) in the SA is used to read the data stored inside the SRAM cell out to **RDO** and **RDO\_B**. In the Write Driver, the DI (Data Input) is the data to be written onto the cell. **WE** (Write Enable) is to enable Write Driver. In the SRAM cell, **WL** is controlled by the row decoder to activate particular memory rows.

### Read and Write Stability

Errors such as memory cells unable to hold data, read the wrong data or is written the wrong data can detriment the trust on SRAM designs [1, 5]. In order to evaluate the stability of SRAM designs, researchers usually based on Static Noise Margin (SNM) analysis [5]. In reality, changes in voltage sources and operating temperature can also cause errors in read and write operation [7]. Furthermore, SNM values are also affected by threshold voltages of the nMOS and pMOS transistors present in the SRAM [1, 6, 7].

#### Static Noise Margin

Static Noise Margin (SNM) value is used to evaluate how stable the Read and Write operations are. Data in a SRAM cell is stored in 2 coupled inverters. To measure stability, a rising DC voltage is applied to each inverter until the bit in the SRAM cell is flipped. The output curves of the two inverters are sketched together in one graph called “butterfly diagram”. The SNM is the biggest square that can be fit between the two output curves. SNM value directly correlates to SRAM cell stability. Larger SNM means higher stability and vice versa.

#### Read SNM

Read SNM (RSNM) shows the stability of the cell during Read operation. Reading operation is affected by the Access transistors. The pull-down transistors D1 and D2 must be stronger, or in other words, must have bigger sizes compared to those of the Access transistors A1 and A2 in order to counter bit-flipping during Read.

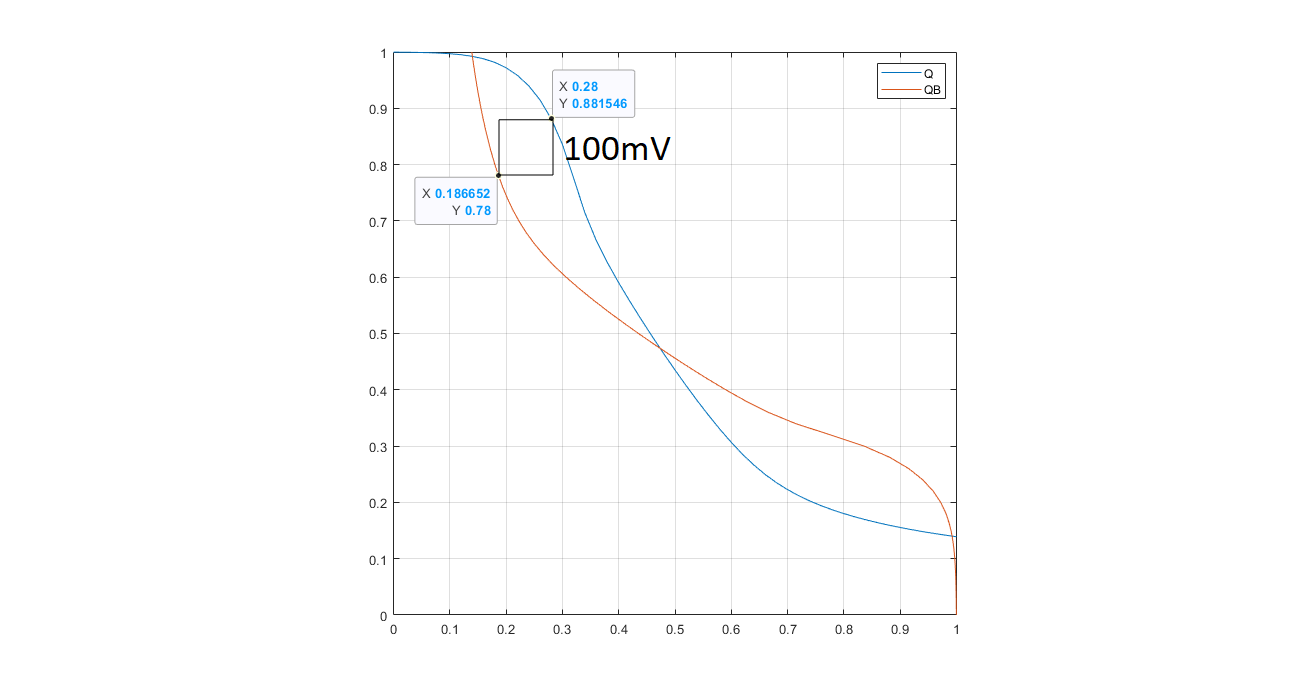
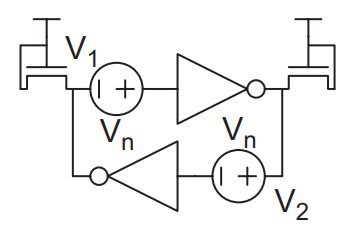


Figure 2. 7. 6T SRAM Read equivalent circuit [2] (left) and RSNM (right).

#### Write SNM

Write SNM (WSNM) shows the stability of the cell during Write operation. During Write operation, one of the two Bitlines will be pulled to Low through one of the pull-down transistors and the other Bitline is kept at High. If the Access transistor is weaker than the pMOS pull-up transistors, the Write operation becomes more unstable as voltage fluctuations at Q or Q\_B is larger than VDD/2. This however will make the RSNM larger due to weaker Access transistor. Thus it is important to balance the ratio between the 3 transistors.

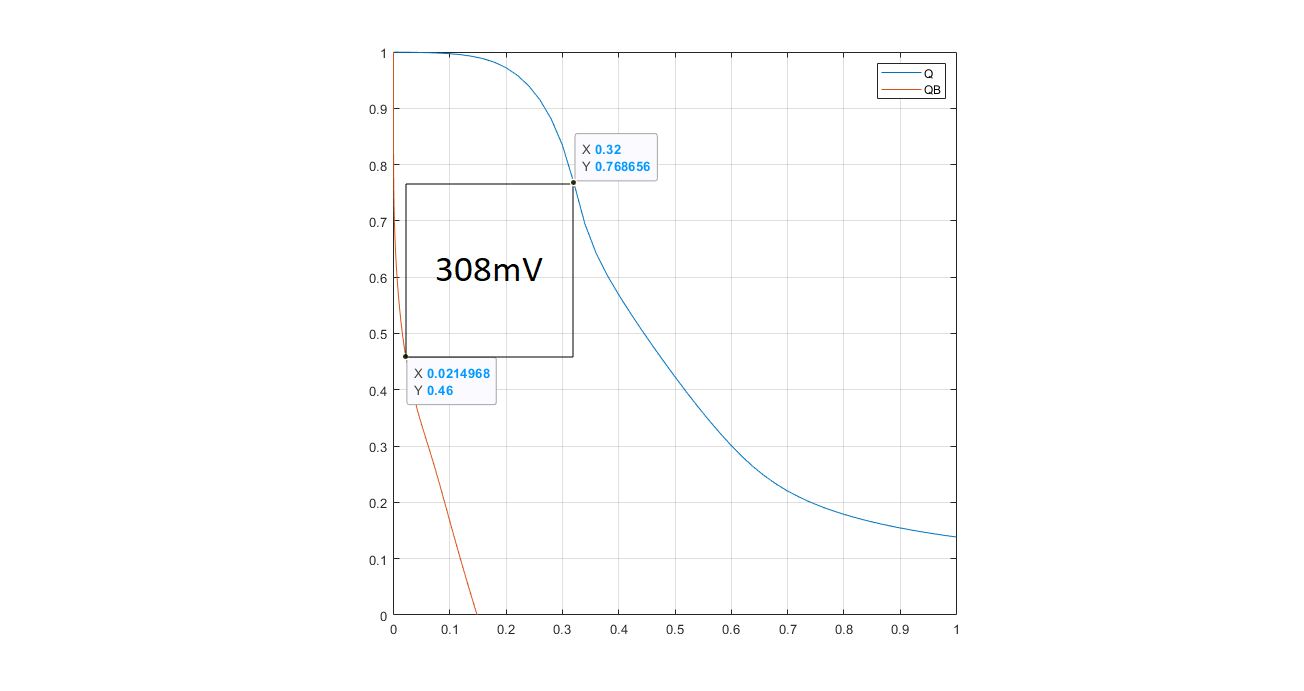
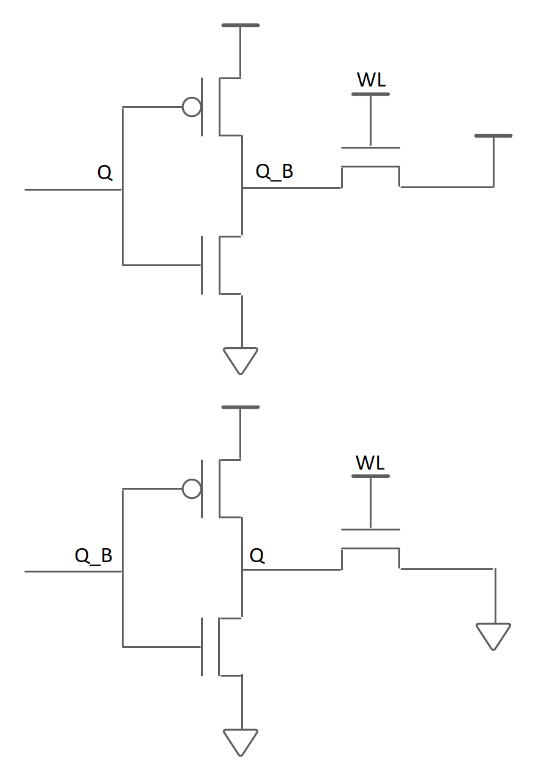


Figure 2. 8. 6T SRAM Write equivalent circuit (left) and WSNM (right).

## 8-Transistor (8T) SRAM

### Operation Principle

The compact 6T SRAM’s minimum operating voltage is limited by Read and Write margins, transistor size. As CMOS Transistors become smaller, we also want them to operate at lower voltages. However, lower voltages will come with tradeoffs, such as declining Read and Write margins, more noise. These tradeoffs are what limits the use of 6T SRAM.

From the problems faced when using 6T SRAM, the 8T SRAM design is proposed to counter the tradeoffs from reducing the operating voltage. The 8T SRAM, with its independent Write and Read ports, theoretically provides better SNM, which leads to better Read and Write stability of the cell, and allows it to operate at lower voltages, which can lead to better average power dissipation (particularly Dynamic power).

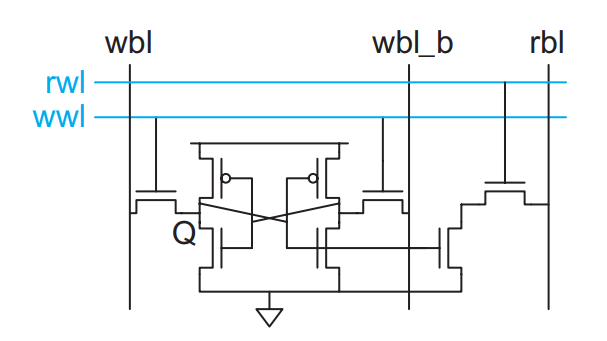


Figure 2. 9. Diagram of 8T SRAM Cell.

The 8T SRAM design is similar to that of the 6T SRAM, but with additional independent Read and Write ports (illustrasted in Figure 2.8), which results in the operation of the 8T SRAM is also mostly similar to 6T SRAM, with a few differences:

**Read Operation:**

* In a Read operation, the rbl bitline is precharged, then the rwl wordline is asserted. Write access transistors are isolated and the operation is only affected by the Read access transistors.

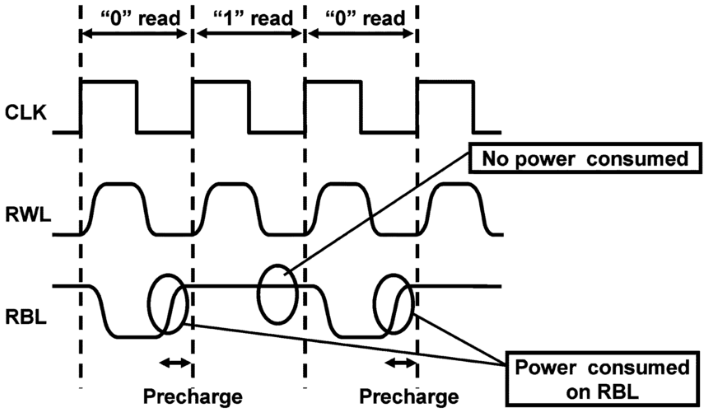


Figure 2. 10. 8T SRAM Read operation [4].

**Write operation:**

* In Write operation, the data and its complement are applied to the wbl and wbl\_b bitlines and the wwl wordline is raised to logic High.

### Read and Write Stability

The RSNM of the 8T SRAM is not affected by Write Access transistors, which results in a much higher RSNM value compared to that of the 6T SRAM. Meanwhile, The WSNM of the 8T SRAM stayed the same as the 6T due to having nearly no difference in Write operation equivalent circuit.

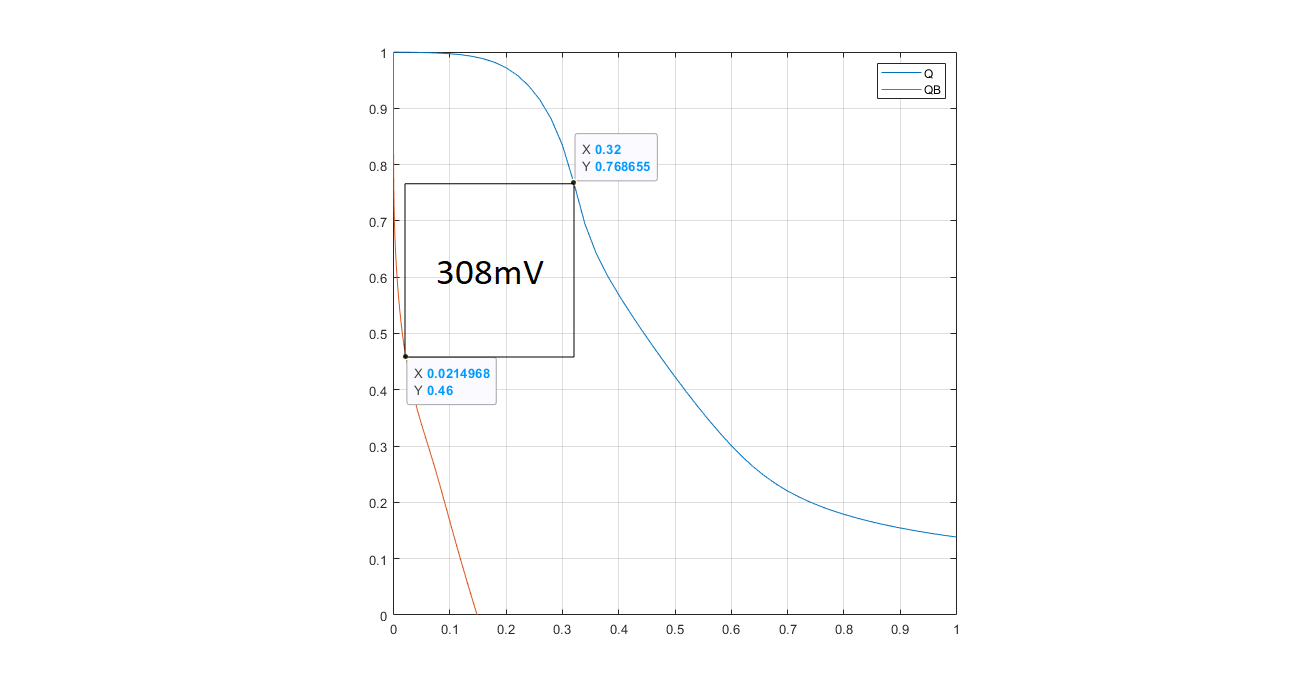
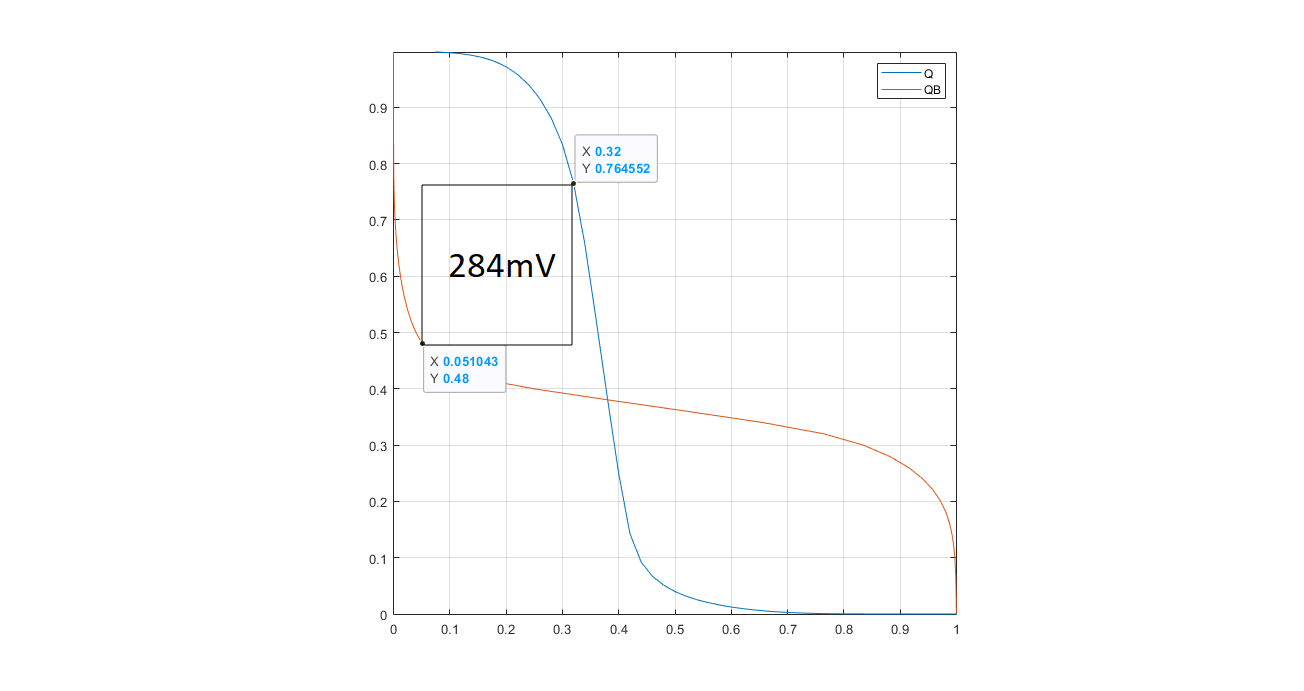


Figure 2. 11. 8T SRAM RSNM (left) and WSNM (right).

## Power Reduction Technique(s)

### Power

Power dissipation in CMOS circuits comprises of two components [2]:

* Dynamic power from
* Charging and discharging load capacitances when CMOS gates switch.
* “Short-circuit” current while both pMOS and nMOS are partially ON.
* Static power from
* Subthreshold leakage through transistors that are OFF.
* Gate leakage through gate dielectric.
* Junction leakage from source/drain diffusions
* Contention current in ratioed circuits.

The total power dissipation can be computed using the given equation:

[2]

While Power dissipation can be caused by numerous reasons, the most prominent causes are:

* Dynamic power from
* Charging and discharging load capacitances when CMOS gates switch.
* “Short-circuit” current while both pMOS and nMOS are partially ON.
* Static power from
* Subthreshold leakage through transistors that are OFF.

### Power Gating

Power Gating is the easiest way to reduce static current. This method essentially puts the circuits into “sleep mode”, cutting off the power supply to said blocks when they are not operating, cutting down static power [2]. The Power Gating method can be illustrated by the figure below.

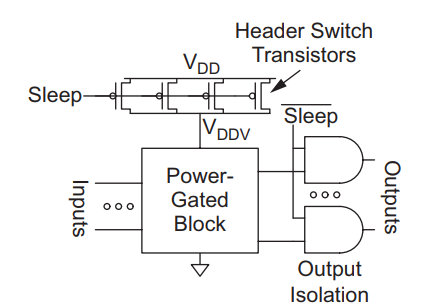


Figure 2. 12. Power Gating example.

The logic block gets its input power from a gated VDD rail, VDDV. When the block is turned ON, the header switch transistors are turned ON and connects VDDV to VDD. When the block is not operating, it will go to sleep by having the header switch transistors turned OFF, disconnecting VDDV from VDD and VDDV will be pulled to GND over time.

**Proposed Power-gated SRAM Designs:**

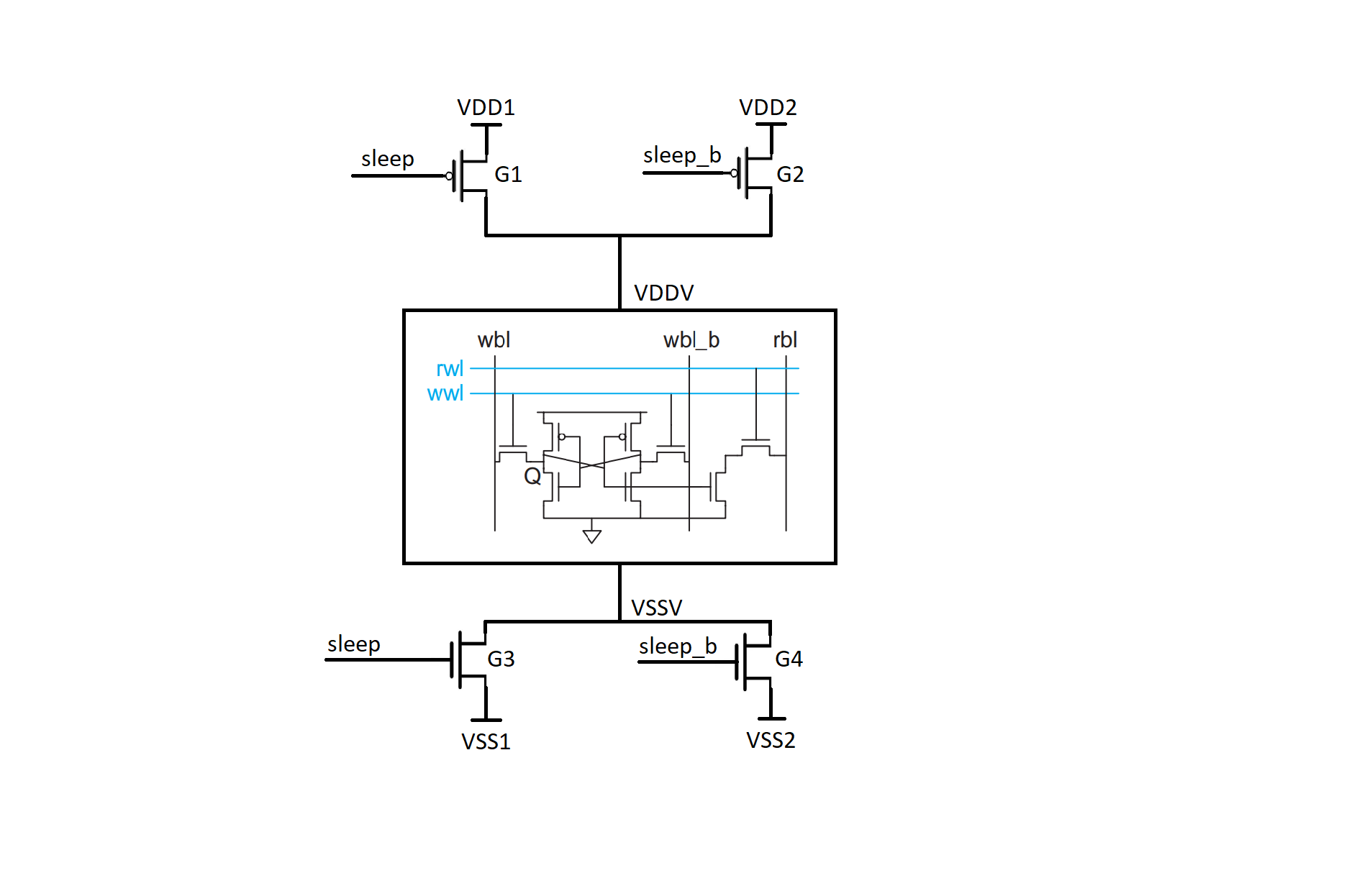
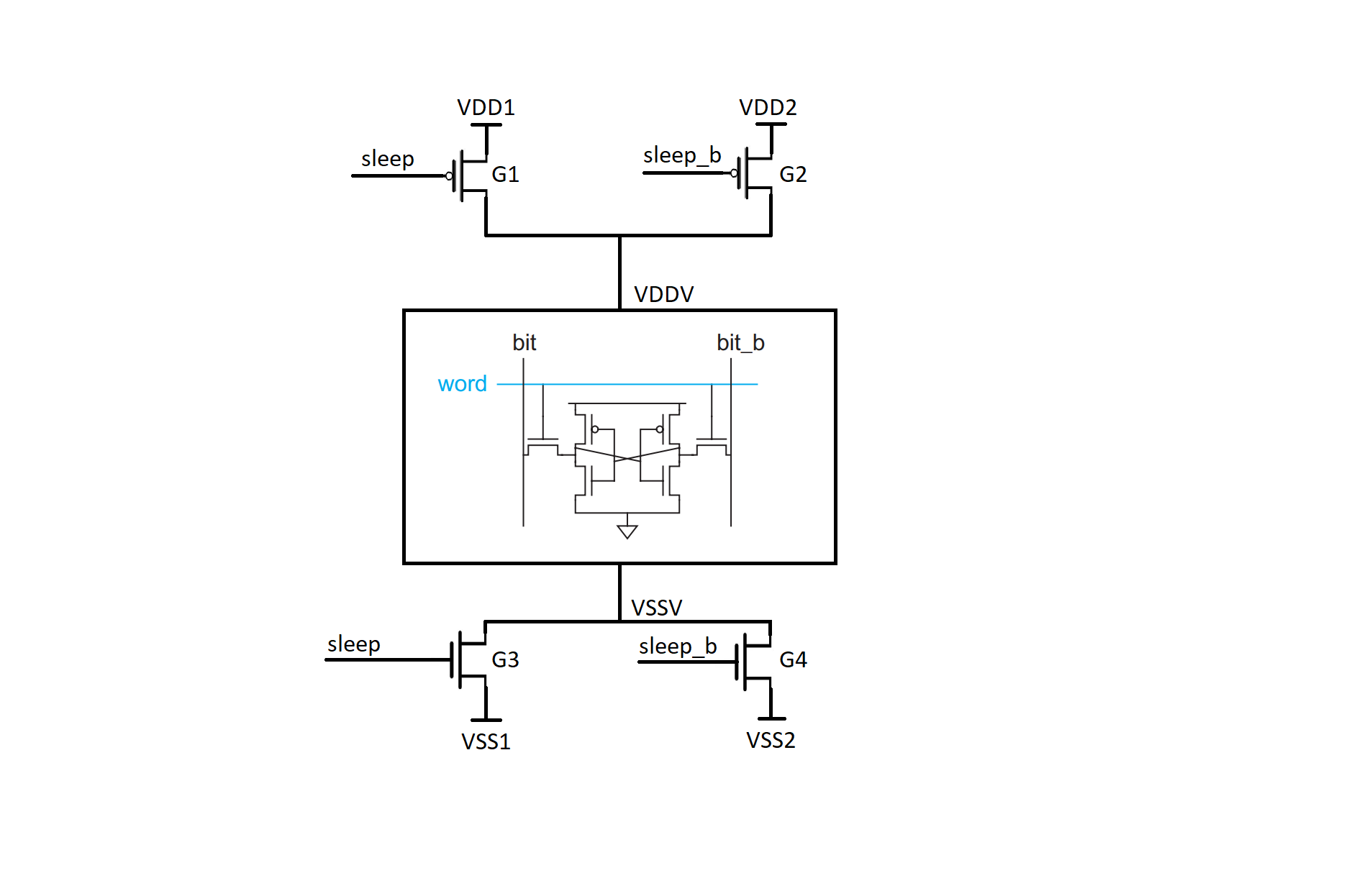
****

Figure 2. 13. Proposed Power Gated 6T SRAM Cell (left) and 8T SRAM Cell (right).

VDDV and VSSV are virtual power supply for the power gated designs. The power supplied to the gated cell will be from the voltage VDDV – VSSV applied to the cell.

* VDDV is provided by two Power gating transistor switches G1 and G2. VDD1 = 1V and VDD2 = 0.5V.
* VSSV is provided by two Power gating transistor switches G3 and G4. VSS1 = 0V and VSS2 = 0.3V.

When the cell is selected for write or read operation, the voltage applied to the cell will be VDD1 – VSS1 = 1V. When the cell is not selected, the voltage applied to the cell will be VDD2 – VSS2 = 0.2V. The reason for the low voltage instead of 0V at hold state is to limit power leakage.

# Simulation and Results

## Conventional 6T and 8T SRAM

### 6T SRAM

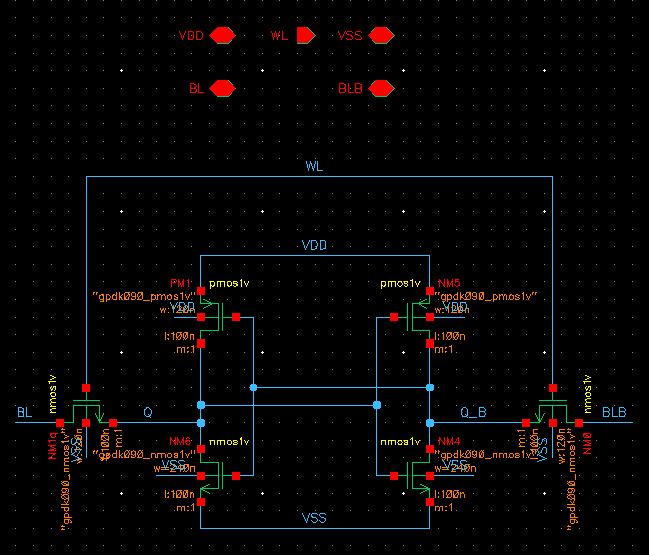


Figure 3. 1. Schematic of 6T SRAM Cell.

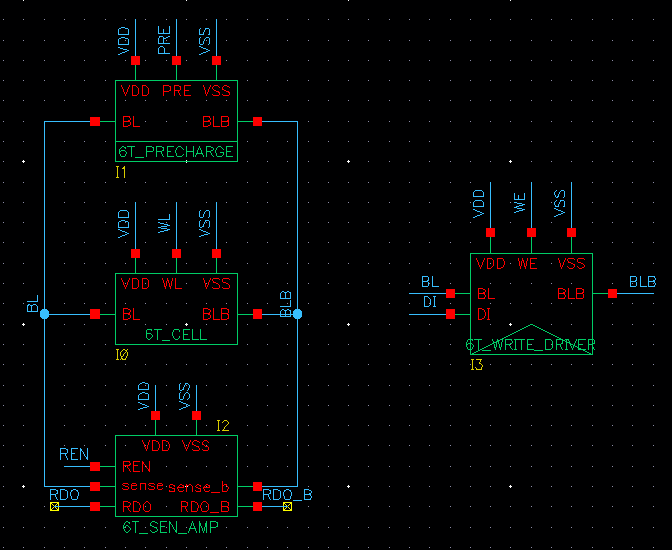


Figure 3. 2. 6T SRAM Circuit.

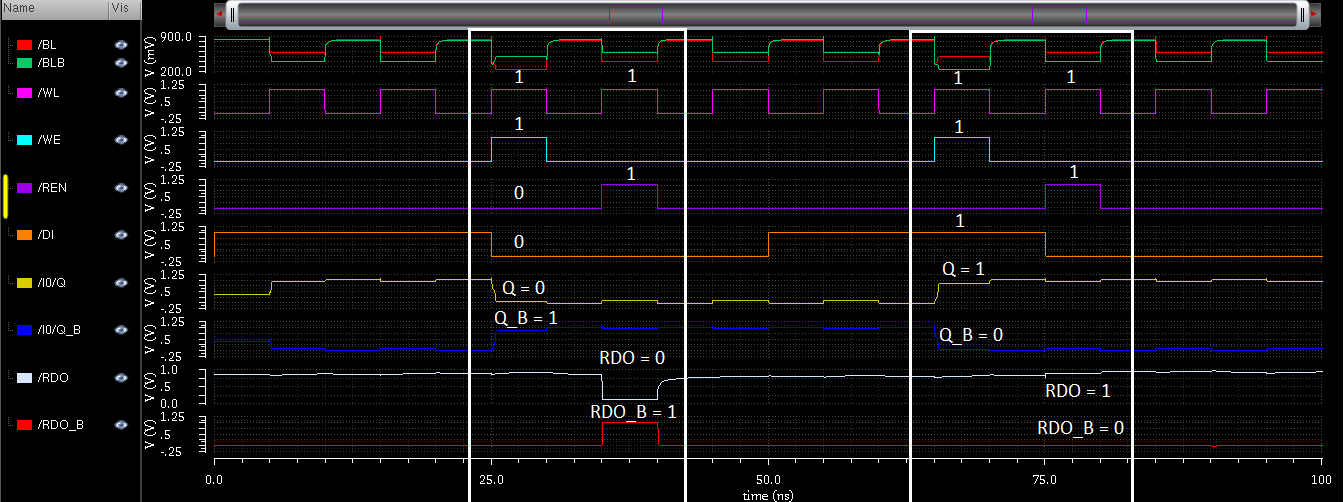


Figure 3. 3. Read and Write operation of 6T SRAM.

**First case: Input data = 0**

In the first box, write and read of input data = 0 is completed. When **WL** is activated and **WE** is enabled to write **DI** = 0 onto the cell, voltages at **Q** and **Q\_B** is flipped and **Q** = 0, **Q\_B** = 1, successfully writing data 0 onto the cell. After that, **WL** is activated again and **REN** is enabled to read data on the cell, reading **RDO** = **Q** = 0 and **RDO\_B** = **Q\_B** = 1.

**Second case: Input data = 1**

In the second box, write and read of input data = 1 is completed. When **WL** is activated and **WE** is enabled to write **DI** = 1 onto the cell, voltages at **Q** and **Q\_B** is flipped and **Q** = 1, **Q\_B** = 0, successfully writing data 1 onto the cell. After that, **WL** is activated again and **REN** is enabled to read data on the cell, reading **RDO** = **Q** = 1 and **RDO\_B** = **Q\_B** = 0.

### 8T SRAM

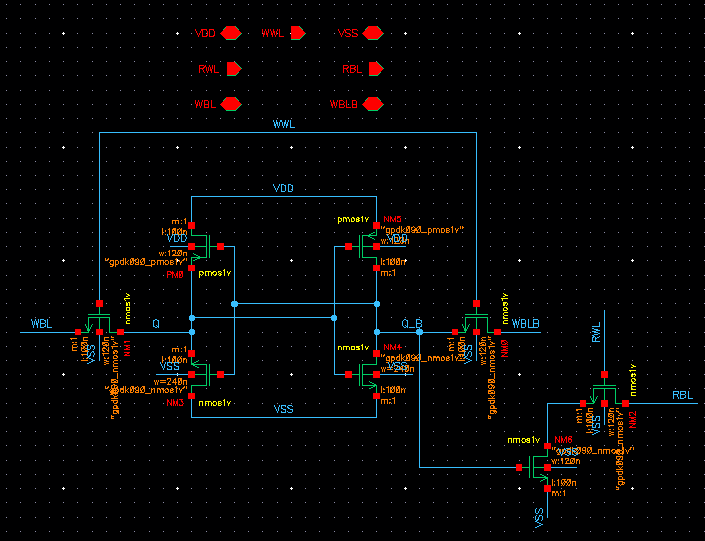


Figure 3. 4. Schematic of 8T SRAM Cell.

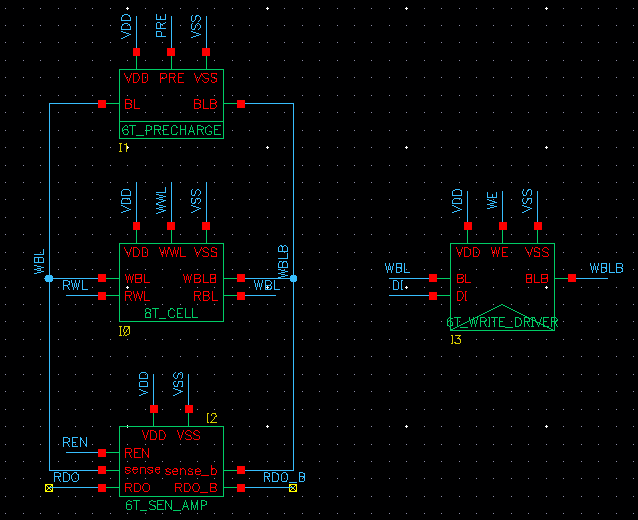


Figure 3. 5. 8T SRAM Circuit.

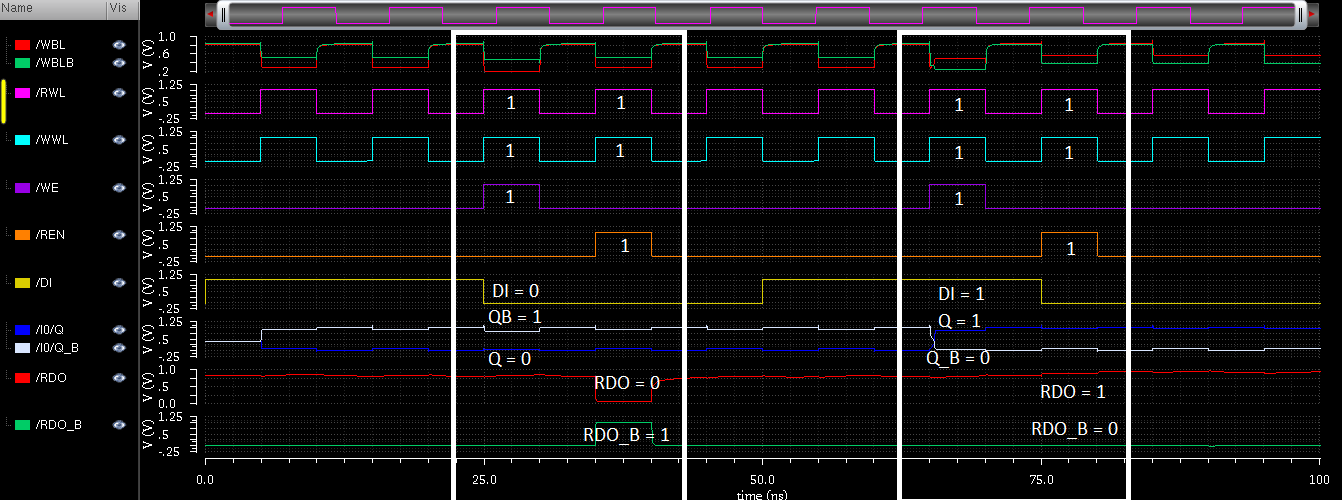


Figure 3. 6. Read and Write operation of 8T SRAM.

The operation of the 8T SRAM is similar to that of the 6T, with the difference is that read and write operations need their own ports activated.

**First case: Input data = 0**

In the first box, write and read of input data = 0 is completed. When **WWL** is activated and **WE** is enabled to write **DI** = 0 onto the cell, voltages at **Q** and **Q\_B** is flipped and **Q** = 0, **Q\_B** = 1, successfully writing data 0 onto the cell. After that, **RWL** is activated and **REN** is enabled to read data on the cell, reading **RDO** = **Q** = 0 and **RDO\_B** = **Q\_B** = 1.

**Second case: Input data = 1**

In the second box, write and read of input data = 0 is completed. When **WWL** is activated and **WE** is enabled to write **DI** = 1 onto the cell, voltages at **Q** and **Q\_B** is flipped and **Q** = 1, **Q\_B** = 0, successfully writing data 1 onto the cell. After that, **RWL** is activated again and **REN** is enabled to read data on the cell, reading **RDO** = **Q** = 1 and **RDO\_B** = **Q\_B** = 0.

## Low Power design of 6T and 8T SRAM

### Control Circuit

As stated in the “Power Gating” section, the SRAM cell needs to be isolated from the power source by a power gate. The power gate is represented by the Low Power Control Circuit (LP\_CTRL) with the design proposed in “Power Gating”.

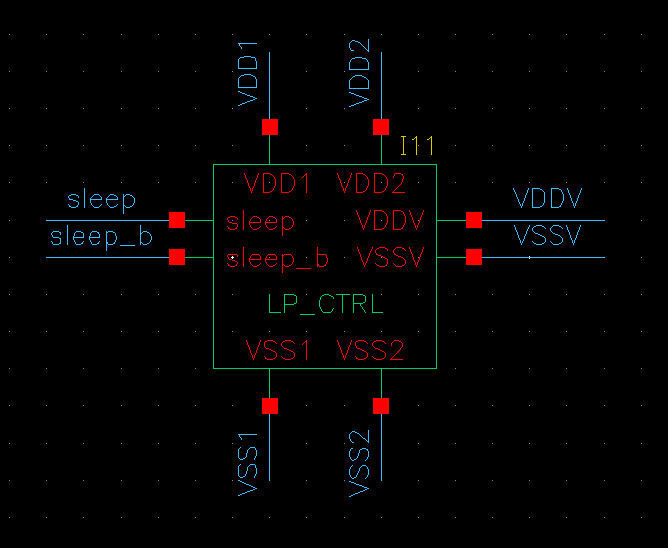
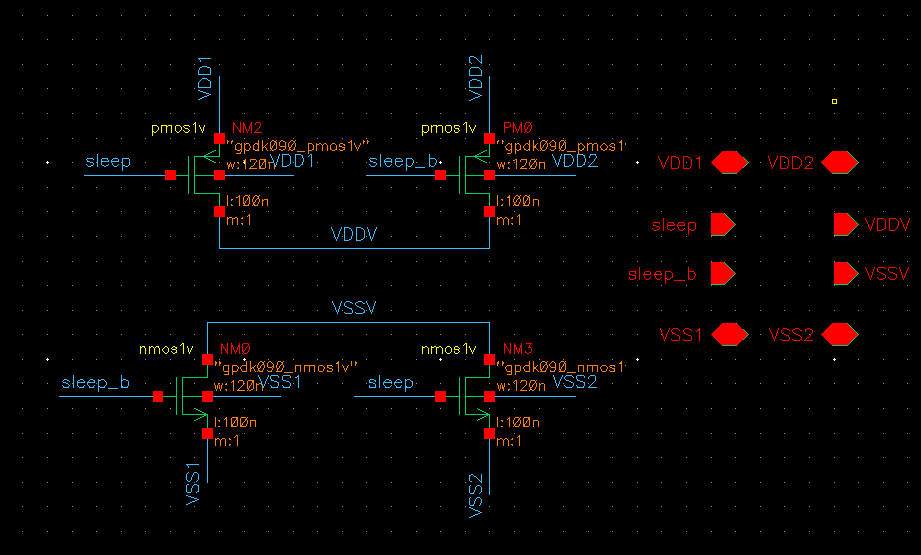


Figure 3. 7. LP\_CTRL Schematic (left) and Symbol (right).

The LP\_CTRL circuit has the following truth table:

|  |  |  |  |
| --- | --- | --- | --- |
| **INPUTS** | | **OUTPUTS** | |
| **sleep** | **sleep\_b** | **VDDV** | **VSSV** |
| 0 | 1 | VDD1 | VSS1 |
| 1 | 0 | VDD2 | VSS2 |

Table 3. 1. LP\_CTRL Truth table.

As presented in “Power Gating”, when the control circuit receives a sleep signal, it will isolate the SRAM Cell from the VDD = 1V and VSS = 0V power source and is instead connected to VDD2 = 0.5V and VSS2 = 0.3V to limit power dissipation. When there is no sleep signal, the SRAM is connected to VDD1 = 1V and VSS1 = 0V as usual.

### 6T SRAM

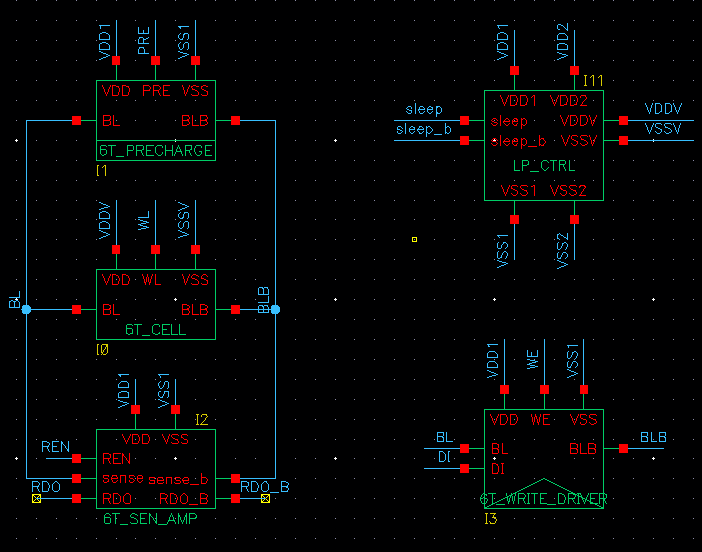


Figure 3. 8. Low Power 6T SRAM Circuit.

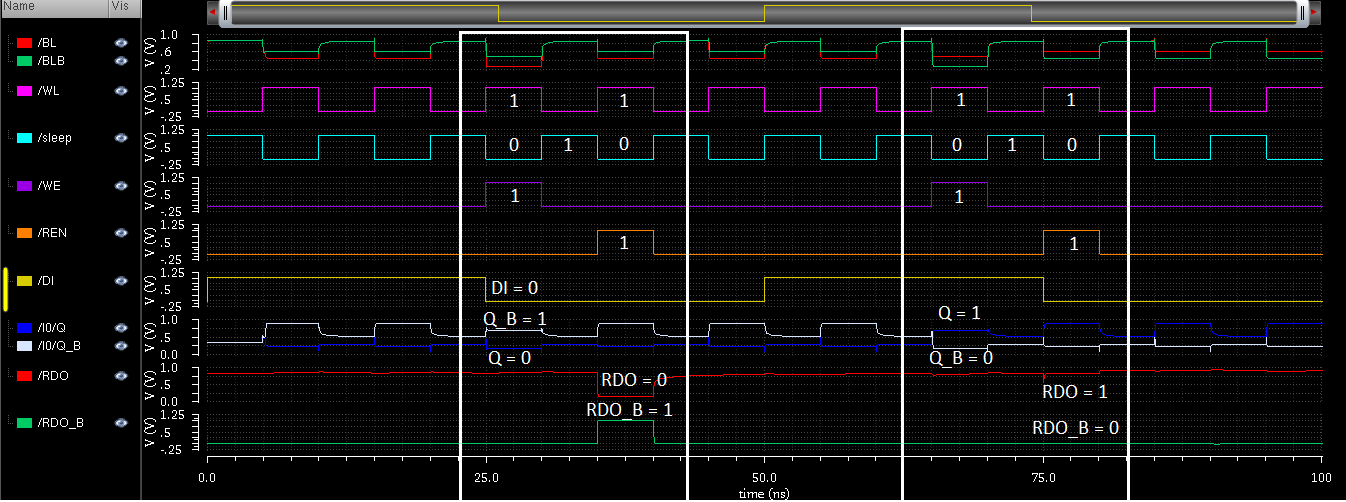


Figure 3. 9. Read and Write operation of Low Power 6T SRAM.

The operation of the Low Power 6T is similar to that of the conventional 6T, but with a small difference. When there is **sleep** signal, the SRAM cell is in “sleep” mode, isolated from VDD1 and VSS1, resulting in **Q** and **Q\_B** dropping in voltage significantly, when **sleep** is 0, voltages at **Q** and **Q\_B** is raised to their usual voltage and no bit flipping occurred, ensuring that no data corruption happened and the SRAM functions correctly.

### 8T SRAM

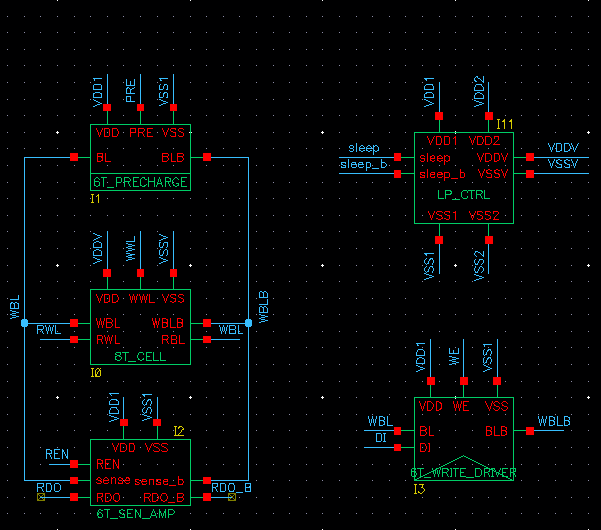


Figure 3. 10. Low Power 8T SRAM Circuit.

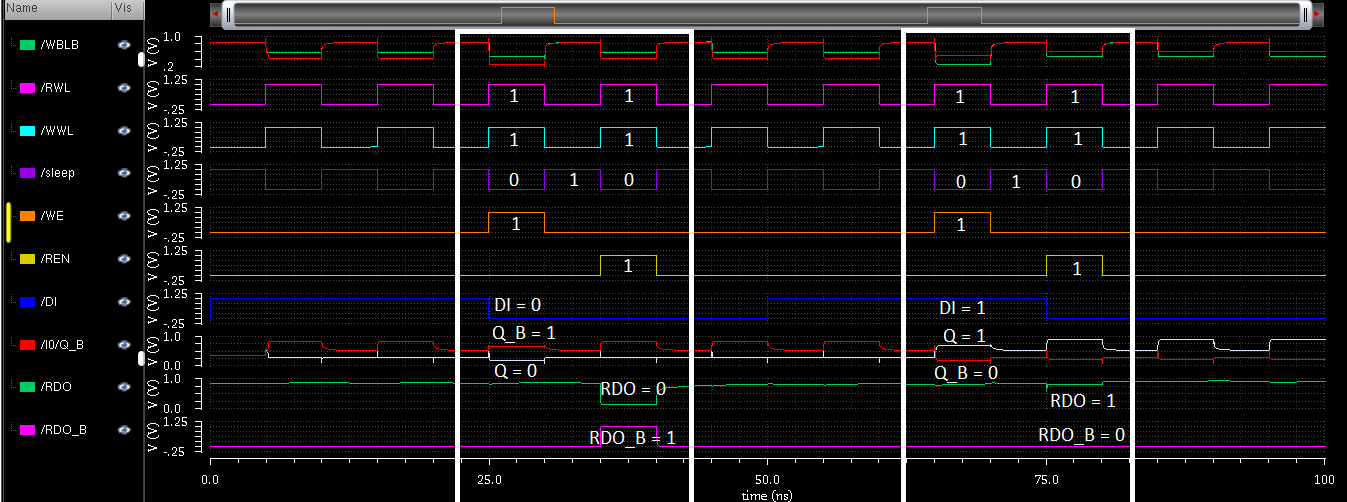


Figure 3. 11. Read and Write operation of Low Power 8T SRAM.

The operation of the Low Power 8T is similar to that of the conventional 8T, but with a small difference. When there is **sleep** signal, the SRAM cell is in “sleep” mode, isolated from VDD1 and VSS1, resulting in **Q** and **Q\_B** dropping in voltage significantly, when **sleep** is 0, voltages at **Q** and **Q\_B** is raised to their usual voltage and no bit flipping occurred, ensuring that no data corruption happened and the SRAM functions correctly.

# Evaluation

After simulating the 6T SRAM, 8T SRAM and their Low Power variants, evaluation of said designs in Power consumption and Delay is done in order to pick out the most suitable designs for different uses.

## Power consumption

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
|  | **Power consumption (uW)** | | | |
| **Temp (oC)** | **SRAM 6T** | **SRAM 8T** | **Low Power 6T** | **Low Power 8T** |
| -10 | 57 | 61.6 | 33.2 | 37.2 |
| 27 | 49.9 | 55.5 | 30 | 31.9 |
| 50 | 46.2 | 51.2 | 26 | 29.2 |
| 80 | 42.2 | 46.6 | 23.7 | 26.4 |

Table 4. 1. Total Power consumption of SRAM designs.

Figure 4. 1. Power consumption charts of SRAM designs.

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
|  | **Power consumption (W)** | | | | | |
| **SRAM 6T** | | | **SRAM 8T** | | |
| **Temp (oC)** | Static | Dynamic | Total | Static | Dynamic | Total |
| -10 | 2.32E-05 | 3.39E-05 | 5.70E-05 | 2.13E-05 | 4.03E-05 | 6.16E-05 |
| 27 | 2.13E-05 | 2.86E-05 | 4.99E-05 | 2.14E-05 | 3.40E-05 | 5.54E-05 |
| 50 | 2.03E-05 | 2.59E-05 | 4.62E-05 | 2.05E-05 | 3.08E-05 | 5.12E-05 |
| 80 | 1.92E-05 | 2.29E-05 | 4.22E-05 | 1.93E-05 | 2.72E-05 | 4.66E-05 |
|  | **Low Power 6T** | | | **Low Power 8T** | | |
| **Temp (oC)** | Static | Dynamic | Total | Static | Dynamic | Total |
| -10 | 9.21E-06 | 2.40E-05 | 3.32E-05 | 9.22E-06 | 2.79E-05 | 3.72E-05 |
| 27 | 8.38E-06 | 2.16E-05 | 3.00E-05 | 8.39E-06 | 2.35E-05 | 3.19E-05 |
| 50 | 7.97E-06 | 1.81E-05 | 2.6E-05 | 7.97E-06 | 2.12E-05 | 2.92E-05 |
| 80 | 7.52E-06 | 1.61E-05 | 2.37E-05 | 7.53E-06 | 1.89E-05 | 2.64E-05 |

Table 4. 2. Complete SRAM designs’ power consumption table.

From the tables and graphs above, we can see that the Low Power designs of both the 6T and 8T SRAM proved to be very effective, nearly halving their total power. This is because in the Low Power designs, Dynamic power is lowered by quite a large margin, but Static power is lowered by a whole order of magnitude (E-05 of Conventional design to E-06 of Low Power design).

By greatly reducing the power dissipation, the Low Power SRAM designs proved to be superior compared to the conventional designs in the Power saving competition, making it very viable for implementation in real life work.

## Delay

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
|  | **Write Delay time (ps)** | | | |
| **Temp (oC)** | **SRAM 6T** | **SRAM 8T** | **Low Power 6T** | **Low Power 8T** |
| T=-10 | 125.69 | 133.56 | 59.41 | 58.03 |
| T=27 | 174.93 | 189.22 | 70.6 | 68.35 |
| T=50 | 223.14 | 243.77 | 79.84 | 75.27 |
| T=80 | 300.36 | 389.32 | 80.88 | 86.28 |

Table 4. 3. Write delay time of SRAM designs.

Figure 4. 2. Write delay time graph of SRAM designs.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
|  | **Read Delay time (ps)** | | | |
| **Temp (oC)** | **SRAM 6T** | **SRAM 8T** | **Low Power 6T** | **Low Power 8T** |
| T=-10 | 15.74 | 17.28 | 16.71 | 16.85 |
| T=27 | 18.63 | 20.47 | 21.54 | 20.58 |
| T=50 | 20.53 | 22.81 | 29.17 | 22.56 |
| T=80 | 24.14 | 25.87 | 34.24 | 27.06 |

*Table 4. 4. Read delay time of SRAM designs.*

Figure 4. 3. Write delay time graph of SRAM designs.

From the tables and graphs above, we can see that:

**Write delay:** Conventional 6T and 8T has the highest write delays, with the 8T having the highest delay at T = 80. Meanwhile, the Low Power designs have significantly lower delay in Write, showing that the Low Power designs both lower not only power consumption but also delay, making it an advantage compared to conventional designs.

**Read delay:** While Low Power SRAM designs have much lower Write delay, they also have slightly higher values in Read delay, with the Low Power 6T design having the highest. This is speculated to be caused by the SRAM cells not connecting to a static voltage source, making the voltages on bitlines fluctuating slightly which leads to small delay in Read operation when sensed by the Sense Amplifier.

## Comparison with other works

|  |  |  |
| --- | --- | --- |
| **8T SRAM Design** | **Read SNM (mV)** | **Read Delay (ps)** |
| This project | 284 | 20.47 |
| [8] | 259 | 60.2 |
| [9] | 415 | 366 |
| [10] | 350 | 455 |

Table 4. 5. Comparison of RSNM and Read delay.

When compared to other researches, we found that the conventional 8T SRAM design of this project yielded both higher RSNM, which proves that it’s more stable when Reading, and lower Read delay time (3x lower than [8] and more than 15x lower than [9] and [10]). This can be a very big advantage for computers that are utilized in applications such as image and video processing and decoding.

# Conclusion and Development Direction

## Conclusion

This project has presented and illustrated the Read and Write operations and designs of the 6T and 8T SRAM and their Low Power counterparts with all of their Read and Write operations simulated using the Cadence Virtuoso Design Suite on the 90nm TSMC process node.

Performance of the 6T, 8T SRAM and their Low Power designs, which includes Power consumption and Delay, are evaluated under different temperatures.

## Evaluation

After evaluating the 6T, 8T SRAM and their Low Power designs using the Power Gating technique, this project concludes that the Low Power designs proved to be successful in:

* Conserving power, cutting power dissipation by more than 2x.
* Reducing Write and Read delay time.
* Lower Read SNM and Read delay time compared to various other researches and papers.

## Potential future development

* Research and implement more SRAM cell variants like 4T, 7T, 9T, 10T, etc…
* Develop entire memory array to be further implemented in other works such as CPU, DPU and other processes that utilize Cache memory.
* Research on SRAM cell layout and area to properly assess area usage by different types of SRAM.
* Utilize more power-saving techniques like Clock-gating, Dynamic Voltage Scaling, etc…
* Implement designs on smaller technology nodes like 45nm, 22nm, 14nm, etc…

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