Digital Design & Verilog – Beginner Assignment

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Part A: Digital Logic Warm-Up

1. Number System Conversion
255.375 (base 10)
Binary: 11111111.011
Octal: 377.3
Hexadecimal: FF.6

2. Binary to Decimal
110101.101 (base 2) = 53.625 (base 10)

3. Divisibility by 3
100111 (base 2) is not divisible by 3 since the alternating sum of bits is not divisible by 3.

4. Two’s Complement
-23 in 8-bit 2’s complement = 11101001

5. Boolean Simplification
F = (A + B)(A' + C)(B + C') simplifies to:
F = AC + A'B

6. K-Map Minimization
F(A,B,C) = Σm(1,3,5,7)
Minimized result: F = C