

Report on Design Task: A Low-power Single-ended Operational Amplifier using Sky130 PDK

1st Lochana Katugaha

Undergraduate, *Department of Electrical and Electronic Engineering*

Sri Lanka Institute of Information Technology

Malabe, Sri Lanka

lochanakatugaha.a30@gmail.com

Abstract—This report documents a single-ended op-amp circuit design using the SKY130 PDK, intended to function as a non-inverting unity-gain buffer for low-frequency analog signals (1–10 kHz) that will be submitted to the Analog IC Student Design Contest organized by IEEE CASS CEDA Joint SL Chapter and SkillSurf.

I. INTRODUCTION

The aim of this report is to document the submitted design so that anyone can understand the design decisions that were made to build a two-stage op-amp with miller compensation using the open source, Sky130A PDK. Fig. 1 shows the circuit that was designed to meet the required specifications.

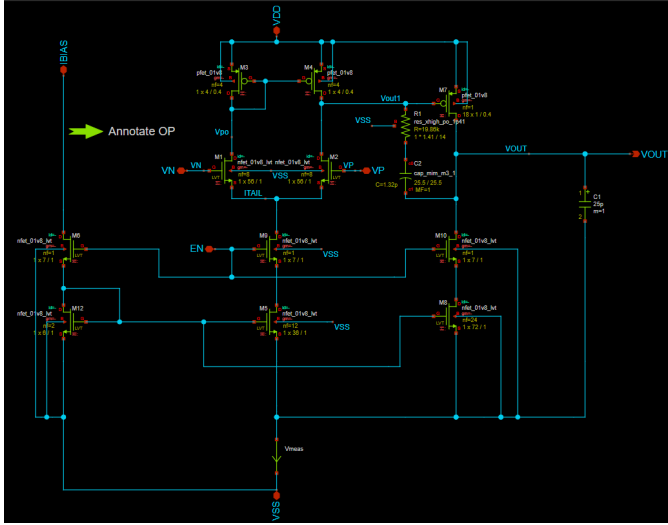


Fig. 1. The circuit that was designed.

II. DESIGN INPUTS AND TARGET SPECIFICATIONS

The amplifier must operate within strict power and performance constraints, targeting low-voltage and low-area applications. A non-inverting unity-gain buffer should present a high input impedance to avoid loading the preceding stage, while maintaining a low output impedance. According to (1), a higher open-loop gain A_0 , results in a lower output impedance when the op-amp is used as a unity-gain buffer. Therefore, a third source-follower stage was not included, since the

intended load already presents a high input impedance of $1\text{ M}\Omega$.

$$R_{\text{out,buffer}} \approx \frac{R_{\text{out}}}{A_0 + 1} \quad (1)$$

TABLE I
DESIRED PROJECT PERFORMANCE SPECIFICATIONS

Parameter	Project Specification
Technology	130 nm CMOS
Supply voltage V_{DD}	1.7 V – 1.9 V
Nominal input common-mode voltage	$(V_{DD}/2 - 0.2\text{ V}) - (V_{DD}/2 + 0.2\text{ V})$
Output load C_L	25 pF (capacitive)
Temperature range	20°C to 50°C
Input signal amplitude	< 0.4 V _{pp}
Input signal frequency	1 – 10 kHz
Open-loop low-frequency (DC) gain A_{DC}	$\geq 60\text{ dB}$
Gain bandwidth product (GBW)	$\geq 1\text{ MHz}$
Phase Margin (PM)	$\geq 60^\circ$
Quiescent current	< 100 μA
Input offset	< 3 mV
Slew rate (both open-loop and closed-loop) SR	$> 1\text{ V}/\mu\text{s}$
Disable current	< 2 nA
Final layout area	within $140\text{ }\mu\text{m} \times 80\text{ }\mu\text{m}$

III. POST-LAYOUT SIMULATION RESULTS

In this section, screenshots of the post layout results after parasitic extraction through magic have been included followed by a summarized table at the end of the section. The table includes detailed values. All results have been obtained using the file:

.lib /foss/pdks/sky130A/libs.tech/ngspice/sky130.lib.spice tt.

Figures Fig. 2 and Fig. 3 show the Open-loop low-frequency (DC) gain post-layout simulation results for the TT corner at temperatures 20°C and 50°C respectively.

Fig. 4 shows the normal operating point simulation result and Fig. 5 shows the operating point simulation result with enable set to logic LOW.

Fig. 6 shows an operating point test for the input offset.

Fig. 7, Fig. 8 and Fig. 9 show transient simulation results at 1 kHz, 10 kHz 100 kHz respectively for a 0.001 V sinusoidal input signal.

Fig. 10 shows transient behavior of the design in an open-loop slew rate test when a -0.4V pulse signal is applied. Fig. 11 shows a graph that shows the corresponding instantaneous slew rate. Fig. 12 shows transient behavior of the design in a closed-loop slew rate test when a -0.4V pulse signal is

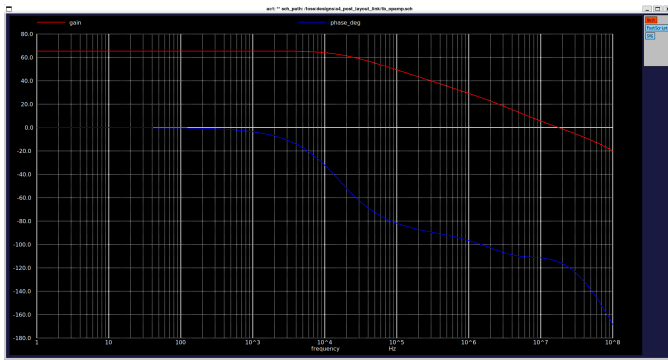


Fig. 2. Gain-phase plot at 20°C. Corner: tt

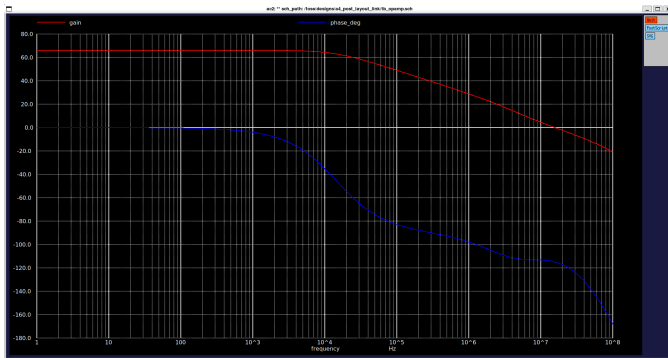


Fig. 3. Gain-phase plot at 50°C. Corner: tt

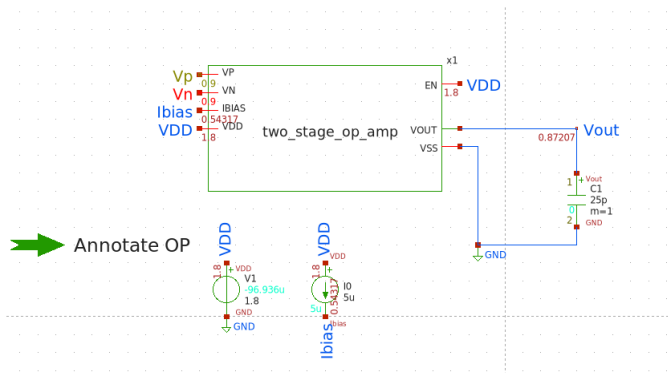


Fig. 4. Post-layout operating point simulation result. Corner: tt

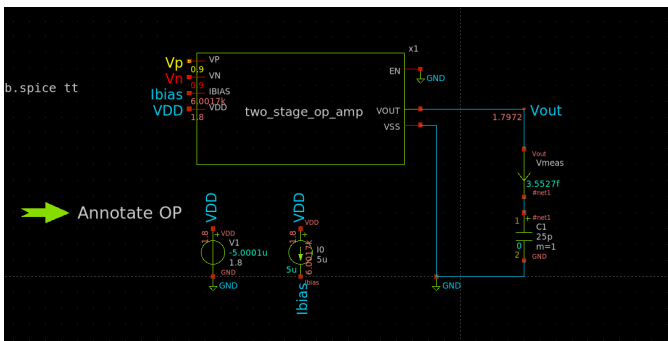


Fig. 5. Post-layout operating point simulation result with enable set to LOW. Corner: tt

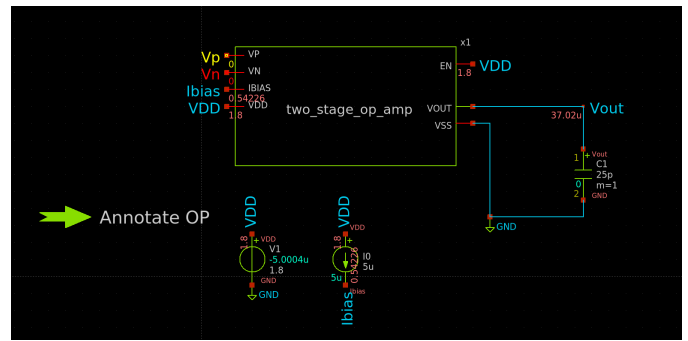


Fig. 6. Post-layout operating point simulation result to test input offset. Corner: tt

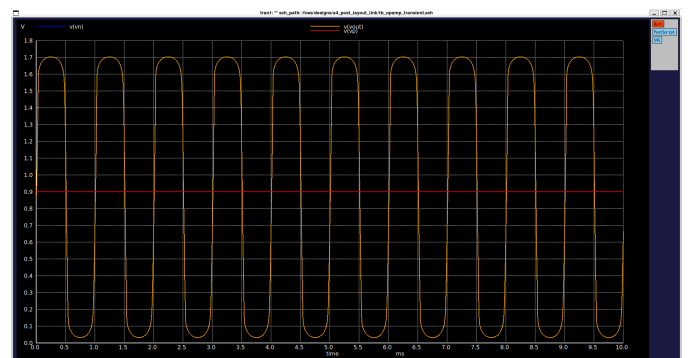


Fig. 7. Post-layout transient simulation result at 1 kHz. Corner: tt

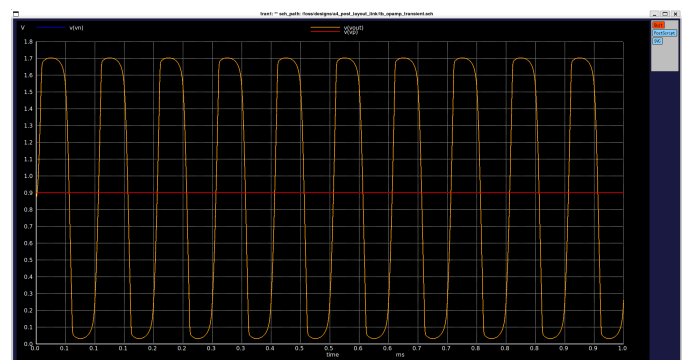


Fig. 8. Post-layout transient simulation result at 10 kHz. Corner: tt

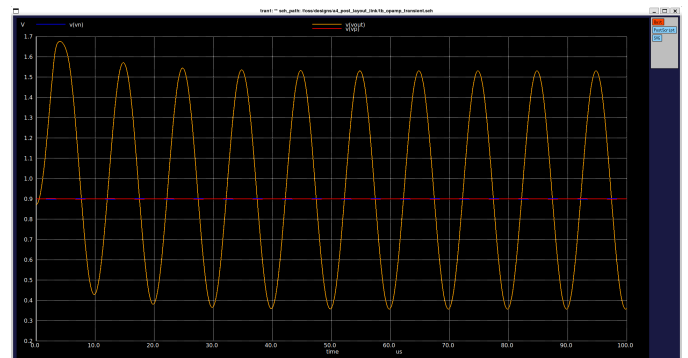


Fig. 9. Post-layout transient simulation result at 100 kHz. Corner: tt

applied. Fig. 13 shows a graph that shows the corresponding instantaneous slew rate.

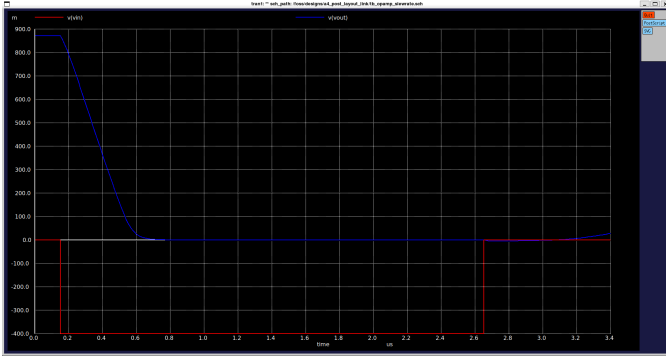


Fig. 10. Post-layout simulation result for open-loop slew rate transient behavior. Corner: tt

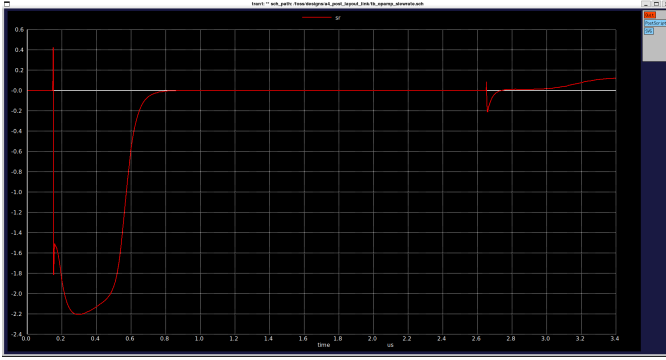


Fig. 11. Post-layout simulation result showing instantaneous slew rate (derivative) for plot in Fig. 10. Corner: tt

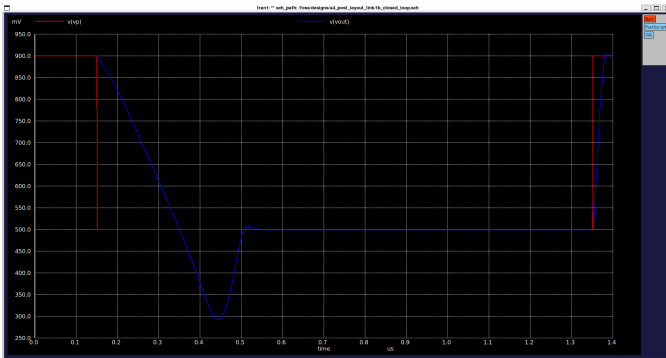


Fig. 12. Post-layout simulation result for closed-loop slew rate transient behavior. Corner: tt

The testbenches used to obtain these results are modified versions of the testbenches found at [1].

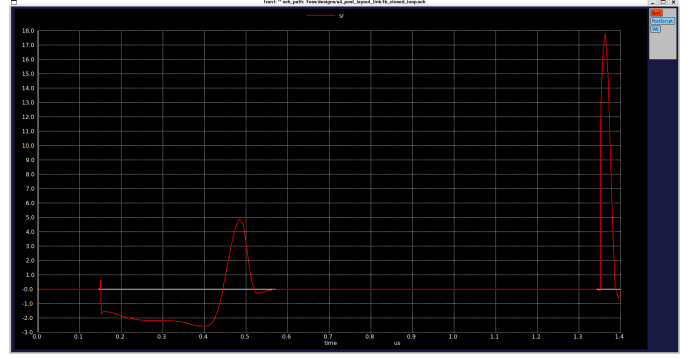


Fig. 13. Post-layout simulation result showing instantaneous slew rate (derivative) for plot in Fig. 12. Corner: tt

TABLE II
SUMMARY OF SPECIFICATIONS ACHIEVED ACROSS PVT VARIATIONS

Required Specification	Post-layout results		
	Process corner	Temp	Value
Input common-mode voltage range	tt	27°C	Min: 0.6 V Max: 1.1 V
Voltage Output Swing	tt	27°C	Min: 230 μ V Max: 1.746384 V
Open-loop low-frequency (DC) gain	tt	20°C	65.52092 dB
	ff	20°C	65.34496 dB
	ss	20°C	65.19360 dB
	sf	20°C	63.93024 dB
	tt	50°C	66.05768 dB
	ff	50°C	65.77095 dB
	ss	50°C	65.75350 dB
	sf	50°C	64.50855 dB
GBW	tt	20°C	17.71086 MHz
	ff	20°C	19.22627 MHz
	ss	20°C	15.96431 MHz
	sf	20°C	16.55620 MHz
	tt	50°C	15.74675 MHz
	ff	50°C	17.04043 MHz
	ss	50°C	14.24977 MHz
	sf	50°C	14.78315 MHz
Phase margin	tt	20°C	65.05970°
	ff	20°C	65.59540°
	ss	20°C	64.33450°
	sf	20°C	64.92370°
	tt	50°C	65.0853°
	ff	50°C	65.93650°
	ss	50°C	63.96400°
	sf	50°C	64.63400°
Quiescent current	tt	27°C	91.936 μ A
Input offset	tt	27°C	37.02 μ V
Slew rate (open-loop, negative pulse)	tt	27°C	-2.204151 V/ μ s
Slew rate (open-loop, positive pulse)	tt	27°C	15.85014 V/ μ s
Slew rate (closed-loop, negative pulse)	tt	27°C	-2.563842 V/ μ s
Slew rate (closed-loop, positive pulse)	tt	27°C	8.356167 V/ μ s
Disable current	tt	27°C	100 pA
Output node current	tt	27°C	3.5527 fA
Layout area	-	-	-

IV. SIZING TRANSISTORS

A. Sky130A PDK Specific Considerations

Different results were obtained depending on the different sky130.lib.spice file that was used. They are found in the lib.tech folder:

.lib/foss/pdks/sky130A/libs.tech/ngspice/sky130.lib.spice,
.lib/foss/pdks/sky130A/libs.tech/combined/sky130.lib.spice.

In order to match the results obtained by these different files it was decided that the design would use only "binned" $\frac{W}{L}$ ratios found in files such as:

/foss/pdks/sky130A/libs.ref/sky130_fd_pr/spice/sky130_fd_pr_nfet_01v8_lvt_tt_discrete.corner.spice,
/foss/pdks/sky130A/libs.ref/sky130_fd_pr/spice/sky130_fd_pr_pfet_01v8_tt_discrete.corner.spice

In two recordings at "Chipathon 2024" there was a discussion about unrealistic values related to the pfet_01v8 model. Fig. 14 shows a screenshot from the recording mentioned above in which unrealistic values were discussed. Since I lack the knowledge to understand most of this talk, I decided to restrict the design to use $\frac{W}{L}$ ratios that I felt were safe. It was decided that the maximum channel length of a pfet used in the design would be $0.5 \mu\text{m}$. Both recordings can be found at [3], under the title "Sizing Simple Circuits".

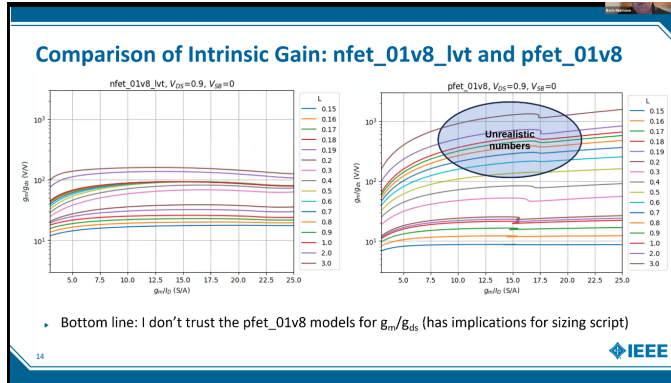


Fig. 14. Presentation on pfet_01v8 model issues

B. Initial Calculations - Work in progress

V. LAYOUT

A. Completed layout and layout plan

It was ensured that the layout was compact, had 0 DRC errors and was passing LVS. Area used by the layout is $2777.110 \mu\text{m}^2$ with a width of $48.500 \mu\text{m}$ and a length of $57.260 \mu\text{m}$. Fig. 15 shows the completed layout. Fig. 16 shows the layout plan.

B. Explanation of the layout of the NMOS differential pair

This was the most crucial part of the layout as the two MOSFETs M1 and M2 needed to be matched with very high accuracy. A common centroid layout made of 8 fingers each

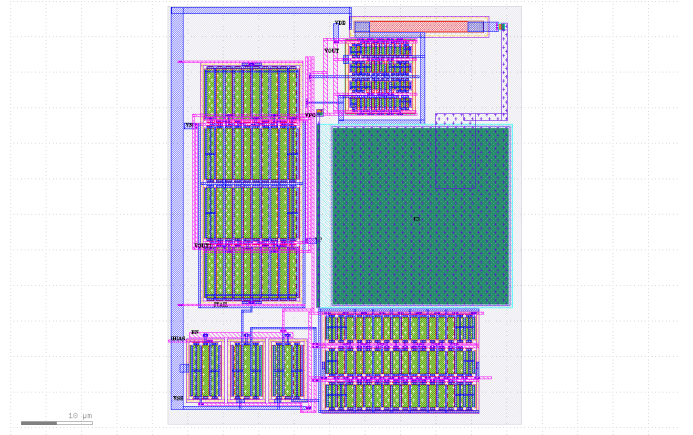


Fig. 15. Final layout of the two stage operational amplifier.

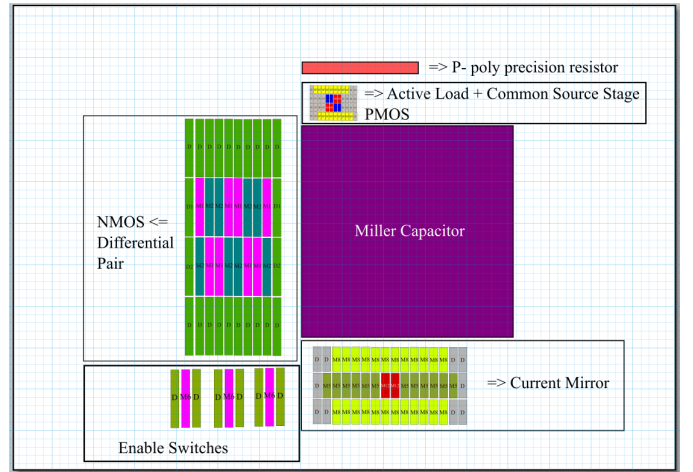


Fig. 16. Layout plan for the two stage operational amplifier.

from M1 and M2 were used with each finger having a $\frac{W}{L} = \frac{7}{1}$. These are the largest fingers in terms of size in the entire layout which may make it more susceptible to process gradients. Therefore, these fingers were placed as close as possible. Attempts were made to ensure that routing was symmetrical as well. The differential pair was surrounded by dummy transistors. There maybe unforeseen complications arising due to the D1 and D2 dummy transistors being connected to the drains of M1 and M2 respectively. This was only noted after completing much of the layout and when changes were made to it so that all the terminals were connected to the source node (ITAIL) of M1 and M2, the post-layout results were worse, so the decision was made to keep it as is. Fig. 17 shows the layout plan of the NMOS differential pair.

C. Explanation of the layout of the PMOS active loads and the common source stage input MOSFET

This was the second most crucial part of the layout as the two MOSFETs that form the active loads of the first stage, M3 and M4 needed to be matched. The common source stage MOSFET M7 needed to be matched as well. A common

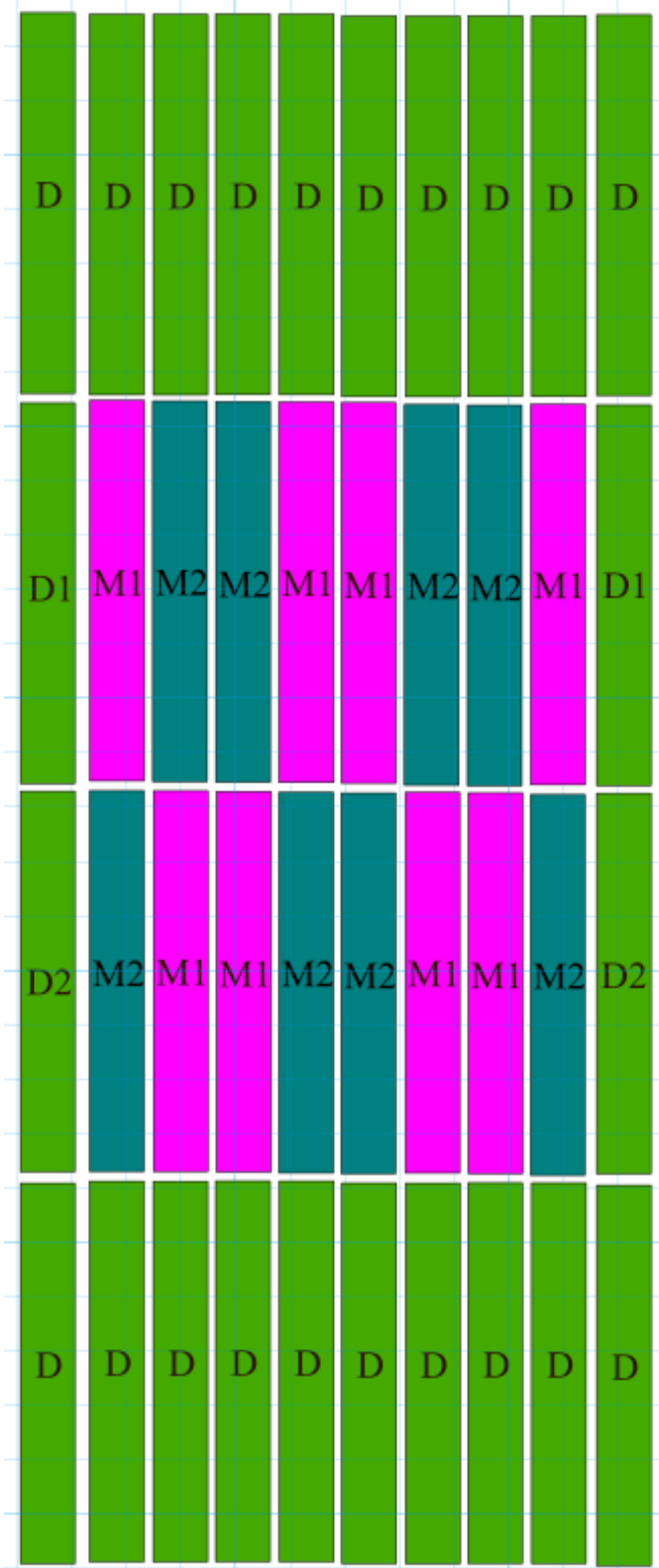


Fig. 17. Layout plan for the NMOS differential pair.

centroid layout made of 4 fingers each from M3 and M4 were used with each finger having a $\frac{W}{L} = \frac{1}{0.4}$. M3 and M4 are surrounded by dummy transistors from all sides while M7 was only surrounded by the left and right to save time during layout so that post-layout simulations could be performed as soon as possible. Fig. 18 shows the layout plan of these PFETs.

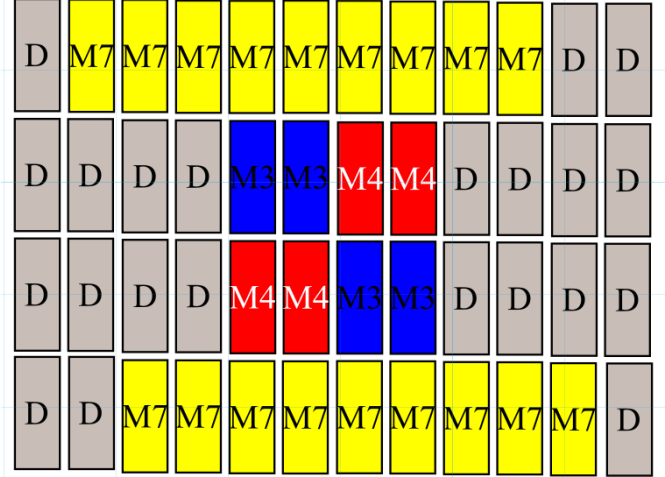


Fig. 18. Layout plan for all the PFETs in the layout.

D. Explanation of the layout of the NMOS current mirror and enable switches

This was also a crucial part of the layout as the three MOSFETs M12, M5 and M8 needed to be matched. The enable switches were not matched to save time and were laid out separately from the current mirror. An attempt at a common centroid layout made of 38 fingers with each finger having a $\frac{W}{L} = \frac{3}{1}$ was made. The goal here was to keep M5 and M8 as close as possible to M12 since M12 was considered as the reference device. M5 is surrounded by identical fingers (including dummy transistors) on all sides however M8 is only surrounded by the left and right sides. A decision must be made whether to include dummy transistors to the top and bottom of M8. Fig. 19 shows the layout plan for the current mirror and enable switches. The enable switches also had dummy transistors on the left and right however whether they are necessary is unknown.

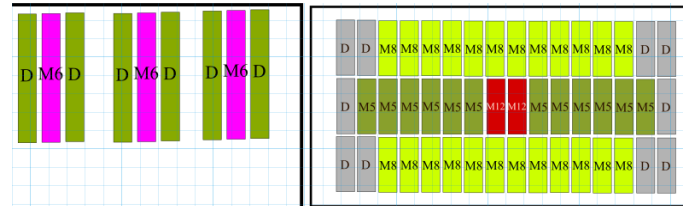


Fig. 19. Layout plan for current mirror and enable switches.

REFERENCES

- [1] https://github.com/SkillSurf/ttsky25_se_opamp/.
- [2] https://github.com/SkillSurf/ttsky25_se_opamp/tree/main/xschem.
- [3] <https://github.com/sscs-ose/sscs-chipathon-2024>.