Report on Design Task: A Low-power Single-ended Operational Amplifier using Sky130 PDK

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***Abstract*—This report documents a single-ended op-amp circuit design using the SKY130 PDK, intended to function as a non-inverting unity-gain buffer for low-frequency analog signals (1–10 kHz) that will be submitted to the Analog IC Student Design Contest organized by IEEE CASS CEDA Joint SL Chapter and SkillSurf.**

I. Introduction

The aim of this report is to document the submitted design so that anyone can understand the design decisions that were made to build a two-stage op-amp with miller compensation using the open source, Sky130A PDK. Fig. 1 shows the circuit that was designed to meet the required specifications.

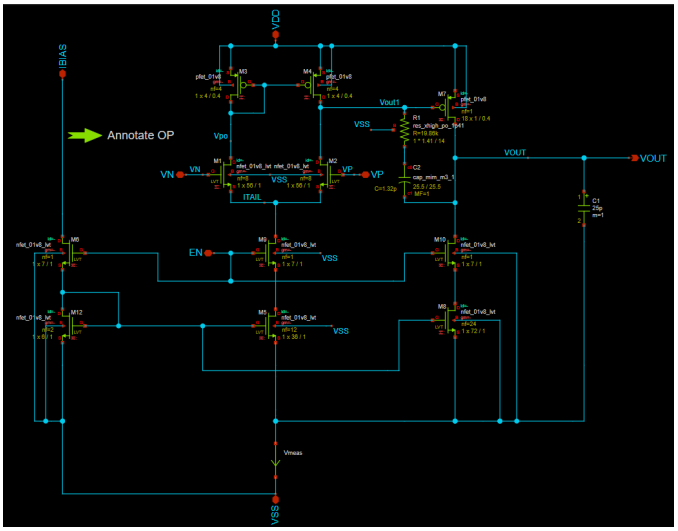

Fig. 1. The circuit that was designed.

II. Design Inputs and Target Specifications

The amplifier must operate within strict power and performance constraints, targeting low-voltage and low-area applications. A non-inverting unity-gain buffer should present a high input impedance to avoid loading the preceding stage, while maintaining a low output impedance. According to (1), a higher open-loop gain A_0, results in a lower output impedance when the op-amp is used as a unity-gain buffer. Therefore, a third source-follower stage was not included, since the intended load already presents a high input impedance of 1 MΩ.

$$R_{\text{out,buffer}} \approx \frac{R_{\text{out}}}{A_0 + 1} \tag{1}$$

TABLE I
Desired Project Performance Specifications

Parameter	Project Specification
Technology	130 nm CMOS
Supply voltage V_{DD}	1.7 V – 1.9 V
Nominal input common-mode voltage	$(V_{DD}/2 - 0.2\text{ V}) - (V_{DD}/2 + 0.2\text{ V})$
Output load C_L	25 pF (capacitive)
Temperature range	20°C to 50°C
Input signal amplitude	$< 0.4\ V_{pp}$
Input signal frequency	1 – 10 kHz
Open-loop low-frequency (DC) gain A_{DC}	≥ 60 dB
Gain bandwidth product (GBW)	≥ 1 MHz
Phase Margin (PM)	$> 60°$
Quiescent current	$< 100\ \mu$A
Input offset	< 3 mV
Slew rate (both open-loop and closed-loop) SR	$> 1\ V/\mu s$
Disable current	< 2 nA
Final layout area	within $140\ \mu m \times 80\ \mu m$

III. Post-Layout Simulation Results

In this section, screenshots of the post layout results after parasitic extraction through magic have been included followed by a summarized table at the end of the section. The table includes detailed values. All results have been obtained using the file:
.lib /foss/pdks/sky130A/libs.tech/ngspice/sky130.lib.spice tt.

Figures Fig. 2 and Fig. 3 show the Open-loop low-frequency (DC) gain post-layout simulation results for the TT corner at temperatures 20°C and 50°C respectively.

Fig. 4 shows the normal operating point simulation result and Fig. 5 shows the operating point simulation result with enable set to logic LOW.

Fig. 6 shows an operating point test for the input offset.

Fig. 7, Fig. 8 and Fig. 9 show transient simulation results at 1 kHz, 10 kHz 100 kHz respectively for a 0.001 V sinusoidal input signal.

Fig. 10 shows transient behavior of the design in a open-loop slew rate test when a -0.4V pulse signal is applied. Fig. 11 shows a graph that shows the corresponding instantaneous slew rate. Fig. 12 shows transient behavior of the design in a closed-loop slew rate test when a -0.4V pulse signal is

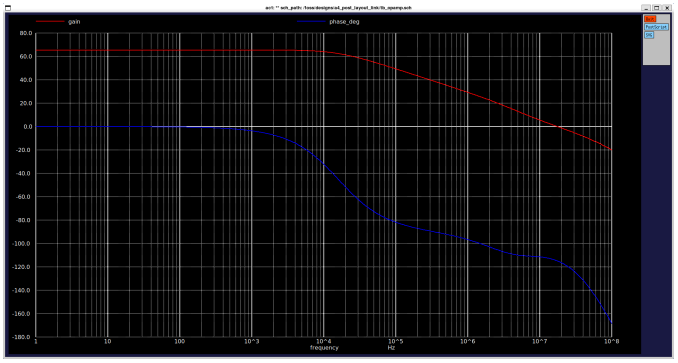

Fig. 2. Gain–phase plot at 20°C. Corner: tt

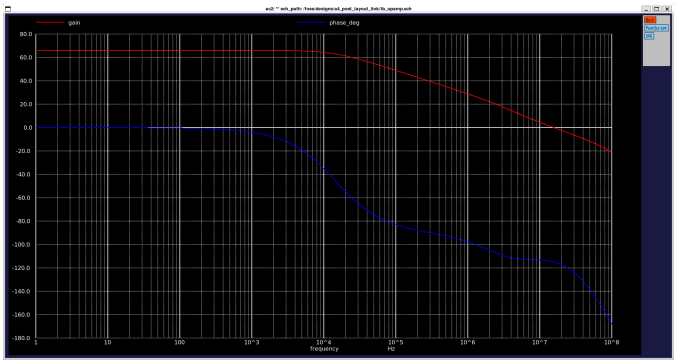

Fig. 3. Gain–phase plot at 50°C. Corner: tt

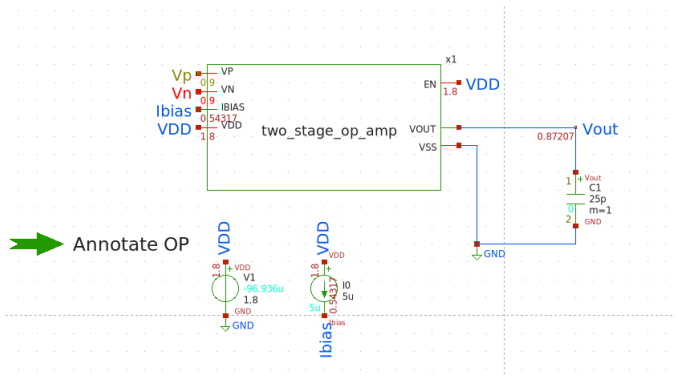

Fig. 4. Post-layout operating point simulation result. Corner: tt

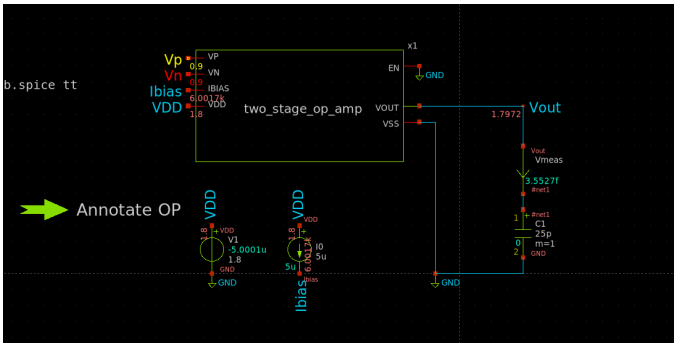

Fig. 5. Post-layout operating point simulation result with enable set to LOW. Corner: tt

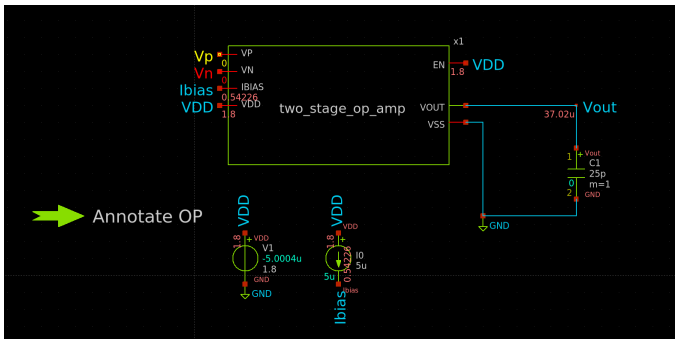

Fig. 6. Post-layout operating point simulation result to test input offset. Corner: tt

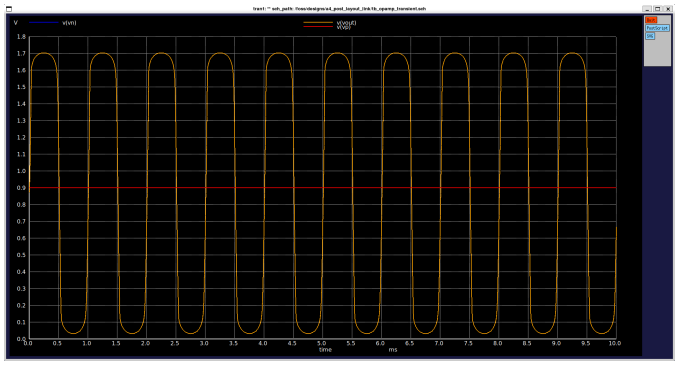

Fig. 7. Post-layout transient simulation result at 1 kHz. Corner: tt

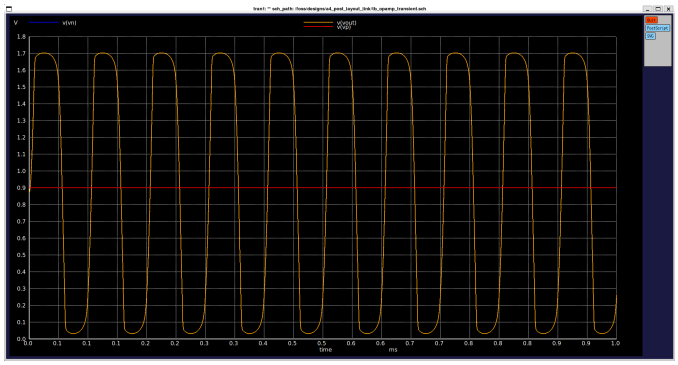

Fig. 8. Post-layout transient simulation result at 10 kHz. Corner: tt

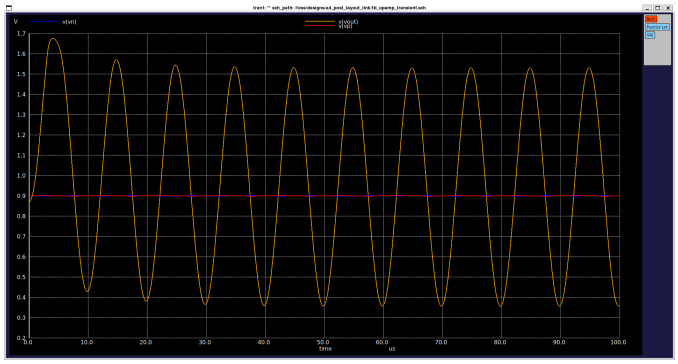

Fig. 9. Post-layout transient simulation result at 100 kHz. Corner: tt

applied. Fig. 13 shows a graph that shows the corresponding instantaneous slew rate.

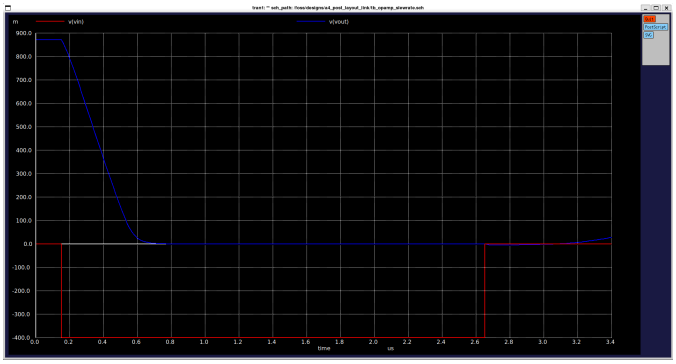

Fig. 10. Post-layout simulation result for open-loop slew rate transient behavior. Corner: tt

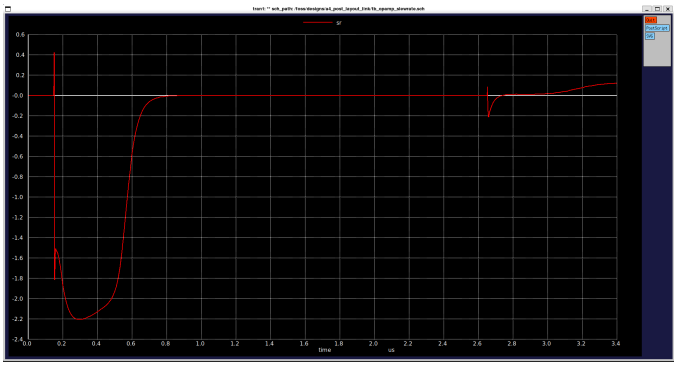

Fig. 11. Post-layout simulation result showing instantaneous slew rate (derivative) for plot in Fig. 10. Corner: tt

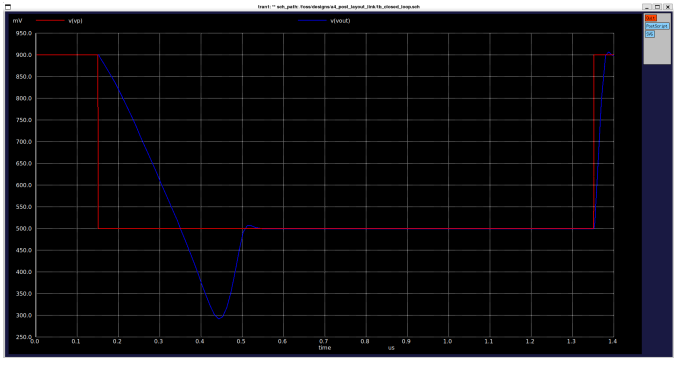

Fig. 12. Post-layout simulation result for closed-loop slew rate transient behavior. Corner: tt

The testbenches used to obtain these results are modified versions of the testbenches found at [1].

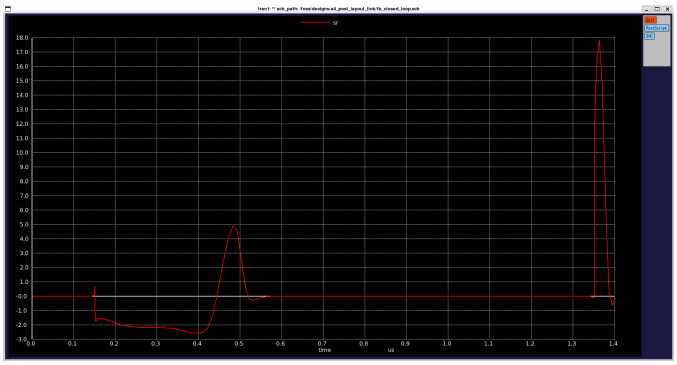

Fig. 13. Post-layout simulation result showing instantaneous slew rate (derivative) for plot in Fig. 12. Corner: tt

TABLE II
SUMMARY OF SPECIFICATIONS ACHIEVED ACROSS PVT VARIATIONS

Required Specification	**Post-layout results**		
	Process corner	***Temp***	***Value***
Input common-mode voltage range	tt	27°C	Min: 0.6 V Max: 1.1 V
Voltage Output Swing	tt	27°C	Min: 230 μV Max: 1.746384 V
Open-loop low-frequency (DC) gain	tt	20°C	65.52092 dB
	ff	20°C	65.34496 dB
	ss	20°C	65.19360 dB
	tt	50°C	66.05768 dB
	ff	50°C	65.77095 dB
	ss	50°C	65.75350 dB
GBW	tt	20°C	17.71086 MHz
	ff	20°C	19.22627 MHz
	ss	20°C	15.96431 MHz
	tt	50°C	15.74675 MHz
	ff	50°C	17.04043 MHz
	ss	50°C	14.24977 MHz
Phase margin	tt	20°C	65.05970°
	ff	20°C	65.59540°
	ss	20°C	64.33450°
	tt	50°C	65.0853°
	ff	50°C	65.93650°
	ss	50°C	63.96400°
Quiescent current	tt	27°C	91.936 μA
Input offset	tt	27°C	37.02 μV
Slew rate (open-loop, negative pulse)	tt	27°C	-2.204151 V/μs
Slew rate (open-loop, positive pulse)	tt	27°C	15.85014 V/μs
Slew rate (closed-loop, negative pulse)	tt	27°C	-2.563842 V/μs
Slew rate (closed-loop, positive pulse)	tt	27°C	8.356167 V/μs
Disable current	tt	27°C	100 pA
Output node current	tt	27°C	3.5527 fA
Layout area	-	-	-

IV. Sizing Transistors

A. Sky130A PDK Specific Considerations

Different results were obtained depending on the different sky130.lib.spice file that was used. They are found in the lib.tech folder:
.lib/foss/pdks/sky130A/libs.tech/ngspice/sky130.lib.spice,
.lib/foss/pdks/sky130A/libs.tech/combined/sky130.lib.spice.

In order to match the results obtained by these different files it was decided that the design would use only "binned" $\frac{W}{L}$ ratios found in files such as:
/foss/pdks/sky130A/libs.ref/sky130_fd_pr/spice/sky130_fd_pr__nfet_01v8_lvt__tt_discrete.corner.spice,
/foss/pdks/sky130A/libs.ref/sky130_fd_pr/spice/sky130_fd_pr__pfet_01v8__tt_discrete.corner.spice

In two recordings at "Chipathon 2024" there was a discussion about unrealistic values related to the pfet_01v8 model. Fig. 14 shows a screenshot from the recording mentioned above in which unrealistic values were discussed. Since I lack the knowledge to understand most of this talk, I decided to restrict the design to use $\frac{W}{L}$ ratios that I felt were safe. It was decided that the maximum channel length of a pfet used in the design would be 0.5 μ. Both recordings can be found at [3], under the title "Sizing Simple Circuits".

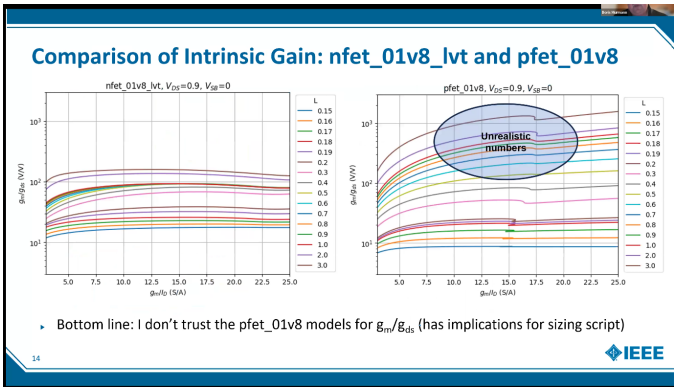

Fig. 14. Presentation on pfet_01v8 model issues

B. Initial Calculations - Work in progress

References

[1] https://github.com/SkillSurf/ttsky25_se_opamp/.
[2] https://github.com/SkillSurf/ttsky25_se_opamp/tree/main/xschem.
[3] https://github.com/sscs-ose/sscs-chipathon-2024.