Report on Design Task: A Low-power Single-ended Operational Amplifier using Sky130 PDK

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***Abstract*—This report documents a single-ended op-amp circuit design using the SKY130 PDK, intended to function as a non-inverting unity-gain buffer for low-frequency analog signals (1–10 kHz) that will be submitted to the Analog IC Student Design Contest organized by IEEE CASS CEDA Joint SL Chapter and SkillSurf.**

I. Introduction

The aim of this report is to document the submitted design so that anyone can understand the design decisions that were made to build a two-stage op-amp with miller compensation using the open source, Sky130A PDK. Fig. 1 shows the circuit that was designed to meet the required specifications.

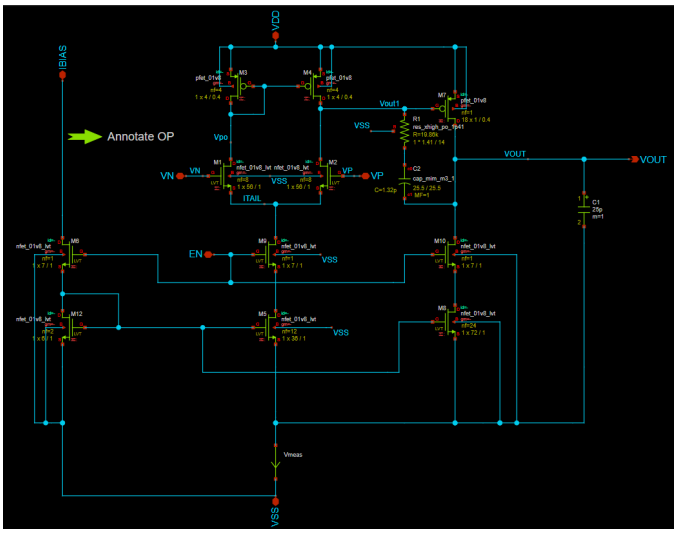

Fig. 1. The circuit that was designed.

II. Design Inputs and Target Specifications

The amplifier must operate within strict power and performance constraints, targeting low-voltage and low-area applications. A non-inverting unity-gain buffer should present a high input impedance to avoid loading the preceding stage, while maintaining a low output impedance. According to [1], a higher open-loop gain results in a lower output impedance when the op-amp is used as a unity-gain buffer.

TABLE I
Desired Project Performance Specifications

Parameter	Project Specification
Technology	130 nm CMOS
Supply voltage V_{DD}	1.7 V – 1.9 V
Nominal input common-mode voltage	$(V_{DD}/2 - 0.2\ \text{V})$ – $(V_{DD}/2 + 0.2\ \text{V})$
Output load C_L	25 pF (capacitive)
Temperature range	20°C to 50°C
Input signal amplitude	$< 0.4\ V_{pp}$
Input signal frequency	1 – 10 kHz
Open-loop low-frequency (DC) gain A_{DC}	≥ 60 dB
Gain bandwidth product (GBW)	≥ 1 MHz
Phase Margin (PM)	$> 60°$
Quiescent current	$< 100\ \mu$A
Input offset	< 3 mV
Slew rate (both open-loop and closed-loop) SR	$> 1\ V/\mu s$
Disable current	< 2 nA
Final layout area	within $140\ \mu m \times 80\ \mu m$

III. Post-Layout Simulation Results

In this section, screenshots of the post layout results after parasitic extraction through magic have been included followed by Table III with a summary. All results have been obtained keeping VDD constant at 1.8 V and nominal input common-mode voltage at 0.9 V (V_{CM}) while also using the lib file:
.lib /foss/pdks/sky130A/libs.tech/ngspice/sky130.lib.spice tt.

It was found that the circuit performs poorly (only in terms of open-loop DC gain) in the sf corner with increasing common mode voltages and Table II records the performance.

Figures Fig. 2 and Fig. 3 show the open-loop low-frequency (DC) gain post-layout simulation results for the tt corner at temperatures 20°C and 50°C respectively.

Fig. 4 shows the normal operating point simulation result and Fig. 5 shows the operating point simulation result with enable set to logic LOW.

Fig. 6 shows the voltage transfer curve for the op-amp.

Fig. 7 and Fig. 8 show open-loop transient simulation results at 1 kHz and 10 kHz respectively for a 0.1 mV sinusoidal input signal. Fig. 9 shows closed-loop transient simulation results at 1 Mhz for a sinusoidal signal of 0.2 Vpp magnitude with $V_{CM} = 0.9\ V$.

Fig. 10 shows transient behavior of the design in a open-loop slew rate test when a -0.4V pulse signal is applied. Fig. 11 shows a graph that shows the corresponding instantaneous slew rate.

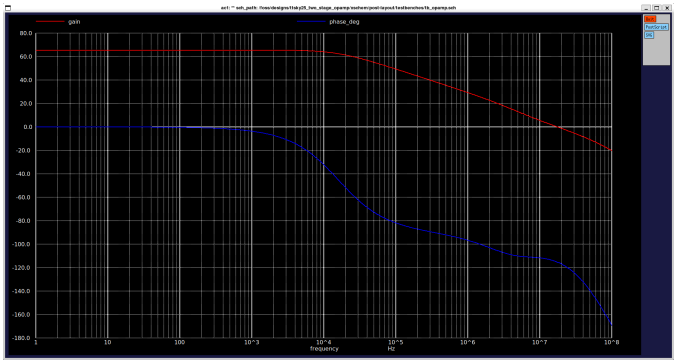

Fig. 2. Gain–phase plot at 20°C. Corner: tt

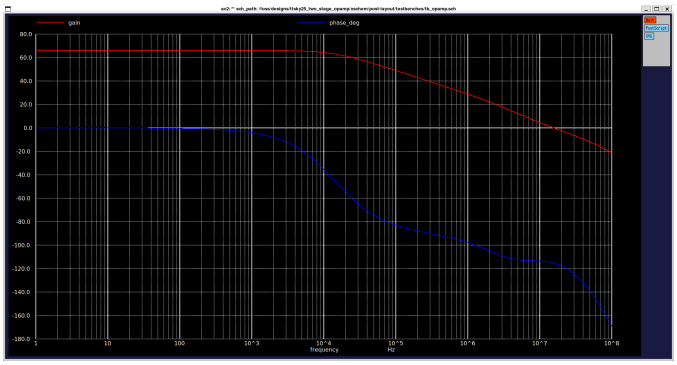

Fig. 3. Gain–phase plot at 50°C. Corner: tt

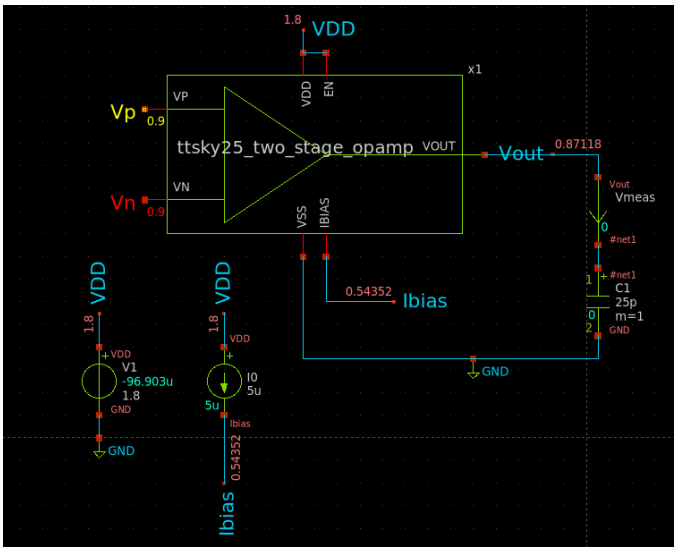

Fig. 4. Post-layout operating point simulation result. Corner: tt

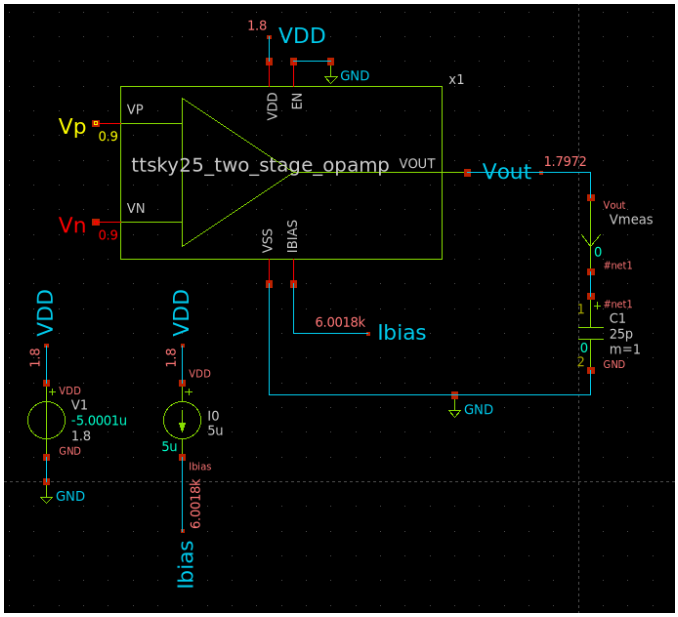

Fig. 5. Post-layout operating point simulation result with enable set to LOW. Corner: tt

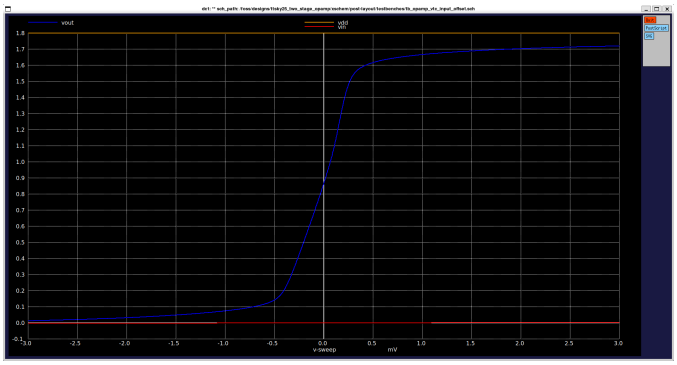

Fig. 6. Post-layout simulation result showing VTC curve. Input offset = 14.88233 μV. Corner: tt

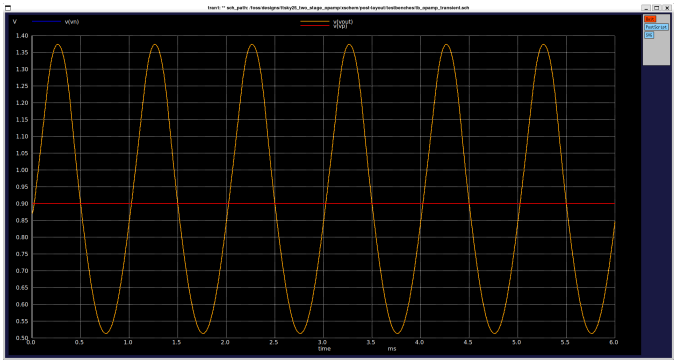

Fig. 7. Post-layout open-loop transient simulation result at 1 kHz. Corner: tt

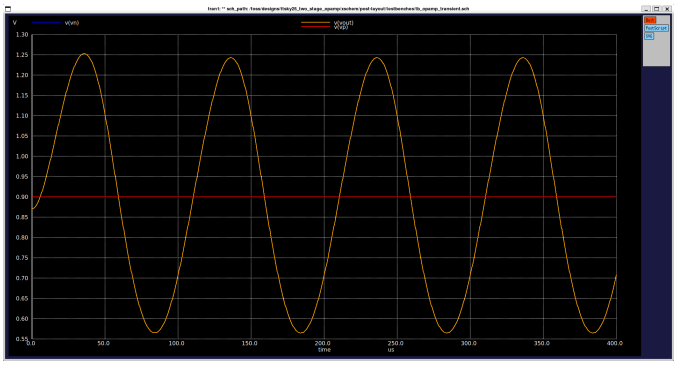

Fig. 8. Post-layout open-loop transient simulation result at 10 kHz. Corner: tt

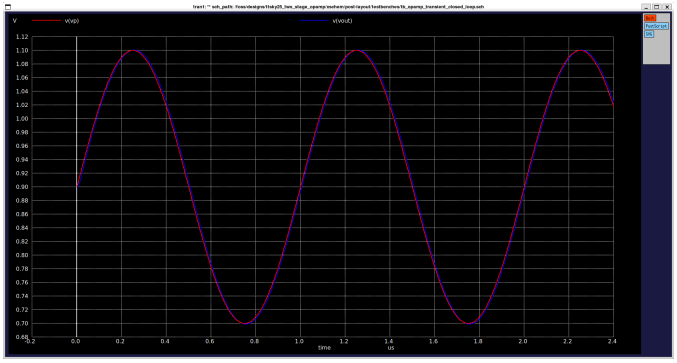

Fig. 9. Post-layout closed-loop transient simulation result at 1 MHz. Corner: tt

Fig. 12 shows transient behavior of the design in a closed-loop slew rate test when a -0.4V pulse signal is applied. Fig. 13 shows a graph that shows the corresponding instantaneous slew rate.

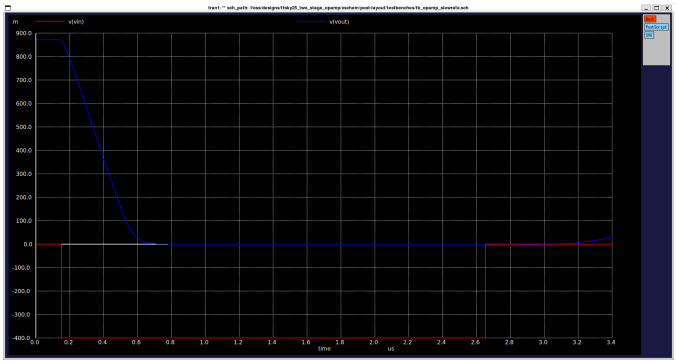

Fig. 10. Post-layout simulation result for open-loop slew rate transient behavior. Corner: tt

The testbenches used to obtain these results are modified versions of the testbenches found at [2].

Fig. 14 shows a histogram made using data obtained through 4500 tests run by CACE. The default documentation generated by CACE (including Monte Carlo results) can be found at [4]. The MC switch found in the combined sky130.lib.spice file was used for this, and the full data set can be found at [6].

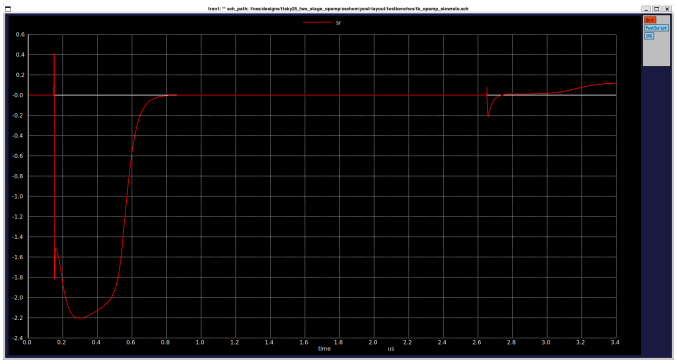

Fig. 11. Post-layout simulation result showing instantaneous slew rate (derivative) for plot in Fig. 10. Corner: tt

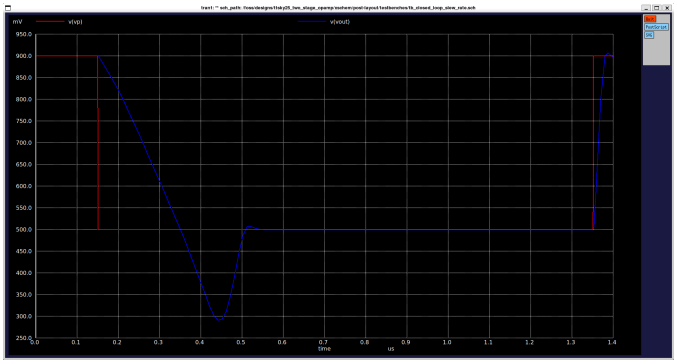

Fig. 12. Post-layout simulation result for closed-loop slew rate transient behavior. Corner: tt

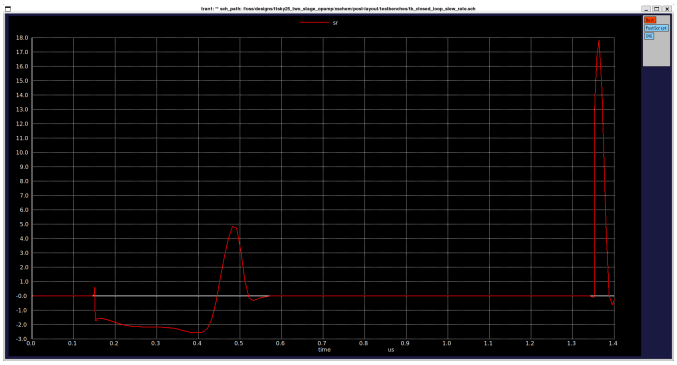

Fig. 13. Post-layout simulation result showing instantaneous slew rate (derivative) for plot in Fig. 12. Corner: tt

TABLE II
EFFECT OF V_{CM} ON OPEN-LOOP DC GAIN IN THE SF CORNER

VDD	V_{CM}	Temperature	Open-loop DC gain
1.8 V	1.1 V	20°C	43.050 dB
1.8 V	1.01 V	20°C	60.125 dB
1.7 V	1.01 V	20°C	37.141 dB
1.9 V	1.01 V	20°C	64.127 dB

TABLE III
SUMMARY OF SPECIFICATIONS ACHIEVED ACROSS PVT VARIATIONS
(VDD = 1.8 AND V_{CM} = 0.9)

Required	**Post-layout results**		
Specification	***Process corner***	***Temp***	***Value***
Input Common-Mode Voltage Range	tt	27°C	Min: 0.6 V Max: 1.1 V
Input Common-Mode Voltage Range (Worst case)	sf	20°C	Min: 0.6 V Max: 1.01 V
Open-loop low-frequency (DC) gain (Max value observed)	tt ff ss sf fs tt ff ss sf fs	20°C 20°C 20°C 20°C 20°C 50°C 50°C 50°C 50°C 50°C	65.522 dB 65.346 dB 65.195 dB 63.934 dB 66.004 dB 66.059 dB 65.772 dB 65.755 dB 64.512 dB 66.494 dB
Gain bandwidth product (Assuming GBW = UGF)	tt ff ss sf fs tt ff ss sf fs	20°C 20°C 20°C 20°C 20°C 50°C 50°C 50°C 50°C 50°C	17.67 MHz 19.18 MHz 15.93 MHz 16.52 MHz 18.20 MHz 15.72 MHz 17.00 MHz 14.22 MHz 14.76 MHz 16.14 MHz
Phase margin	tt ff ss sf fs tt ff ss sf fs	20°C 20°C 20°C 20°C 20°C 50°C 50°C 50°C 50°C 50°C	64.684° 65.191° 63.994° 64.573° 64.605° 64.754° 65.580° 63.663° 64.323° 64.896°
Quiescent current	tt	27°C	96.903 μA
Input offset	tt	27°C	14.88233 μV
Slew rate (open-loop, negative pulse)	tt	27°C	-2.20 V/μs
Slew rate (open-loop, positive pulse)	tt	27°C	15.88 V/μs
Slew rate (closed-loop, negative pulse)	tt	27°C	-2.56 V/μs
Slew rate (closed-loop, positive pulse)	tt	27°C	8.10 V/μs
Disable current	tt	27°C	100 pA
Output node current	tt	27°C	-
Layout area	-	-	$48.5 * 57.26$ μm^2

Results were obtained using, 150 MC switch process variations each for 3 temperature variations (20°C, 27°C, 50°C) * 3 VDD variations (1.7 V, 1.8 V, 1.9 V) * 3 V_{CM} variations.

IV. SIZING TRANSISTORS

A. Sky130A PDK Specific Considerations

Different results were obtained depending on the different sky130.lib.spice file that was used. They are found in the lib.tech folder:
.lib/foss/pdks/sky130A/libs.tech/ngspice/sky130.lib.spice,
.lib/foss/pdks/sky130A/libs.tech/combined/sky130.lib.spice.

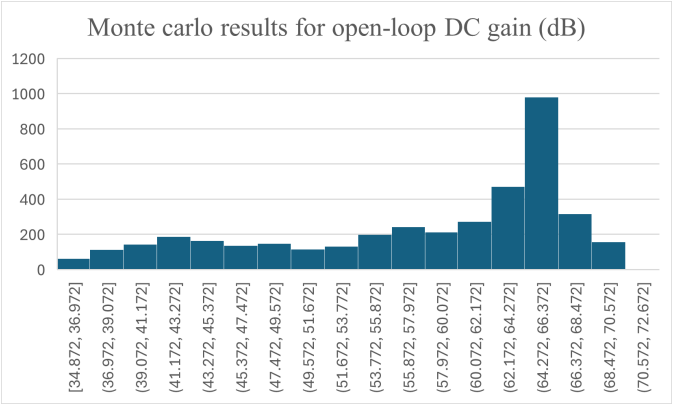

Fig. 14. Monte Carlo simulation attempt with 4050 runs

TABLE IV
AN ATTEMPT AT 3-SIGMA ANALYSIS OF DC GAIN USING 4500 MONTE CARLO RUNS

Mean open-loop DC gain	57.72378807 dB
Standard Deviation	9.412357149 dB
Median	61.70855 dB
1σ - Count and percentage	2850 (70.370%)
2σ - Count and percentage	3883 (95.877%)
3σ - Count and percentage	4050 (100%)

In order to match the results obtained by these different files it was decided that the design would use only "binned" $\frac{W}{L}$ ratios found in files such as:
"/foss/pdks/sky130A/libs.ref/sky130_fd_pr/spice/sky130_fd_pr__nfet_01v8_lvt__tt_discrete.corner.spice" and
"/foss/pdks/sky130A/libs.ref/sky130_fd_pr/spice/sky130_fd_pr__pfet_01v8__tt_discrete.corner.spice".

Due to various community discussions such as [3] and [5] about the the pfet_01v8 model, it was decided that the maximum channel length of PFETs used in the design would be 0.4 μm.

V. LAYOUT

A. Completed layout and layout plan

It was ensured that the layout was compact, had 0 DRC errors and was passing LVS. Area used by the layout is 2777.110 μm^2 with a width of 48.500 μm and a length of 57.260 μm. Fig. 15 shows the completed layout. Fig. 16 shows the layout plan.

B. Explanation of the layout of the NMOS differential pair

This was the most crucial part of the layout as the two MOSFETs M1 and M2 needed to be matched with very high accuracy. A common centroid layout made of 8 fingers each from M1 and M2 was used with each finger having a $\frac{W}{L} = \frac{7}{1}$. These are the largest fingers in terms of size in the entire layout, which may make it more susceptible to process gradients. Therefore, these fingers were placed as close as possible. Attempts were made to ensure that

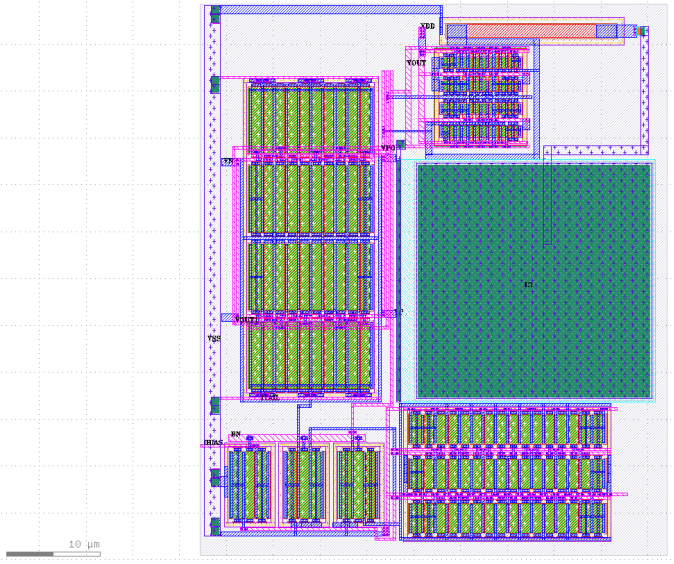

Fig. 15. Final layout of the two stage operational amplifier.

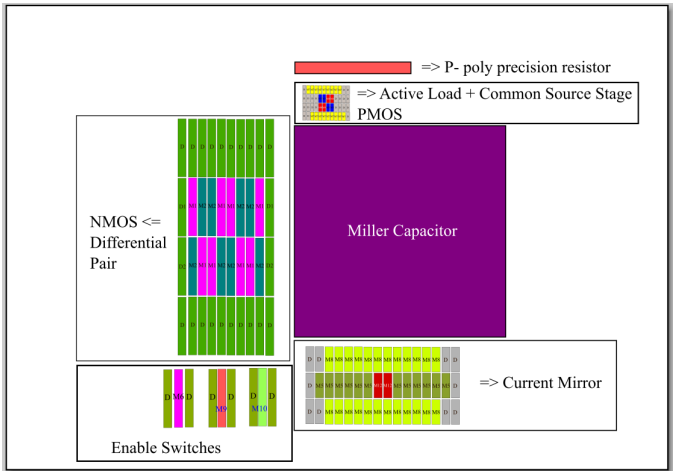

Fig. 16. Layout plan for the two stage operational amplifier.

routing was symmetrical as well. The differential pair was surrounded by dummy transistors. There may be unforeseen complications arising due to the D1 and D2 dummy transistors being connected to the drains of M1 and M2, respectively. This was only noted after completing much of the layout and when changes were made to it so that all the terminals were connected to the source node (ITAIL) of M1 and M2, the post-layout results were worse, so the decision was made to keep it as it is. Fig. 17 shows the layout plan of the NMOS differential pair.

C. Explanation of the layout of the PMOS active loads and the common source stage input MOSFET

This was the second most crucial part of the layout as the two MOSFETs that form the active loads of the first stage, M3 and M4 needed to be matched. The common source stage MOSFET M7 also needed to be matched. A common centroid

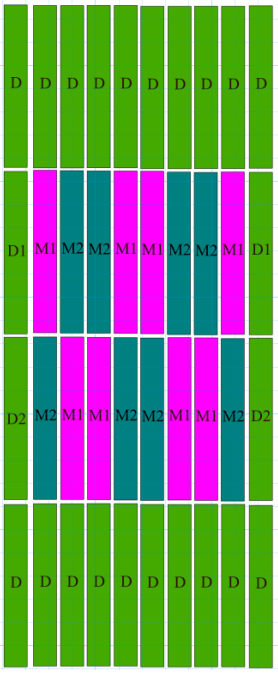

Fig. 17. Layout plan for the NMOS differential pair.

layout made of 4 fingers each from M3 and M4 was used with each finger having a $\frac{W}{L} = \frac{1}{0.4}$. M3 and M4 are surrounded by dummy transistors from all sides, while M7 was only surrounded by the left and right to save time during layout so that post-layout simulations could be performed as soon as possible. Fig. 18 shows the layout plan of these PFETs.

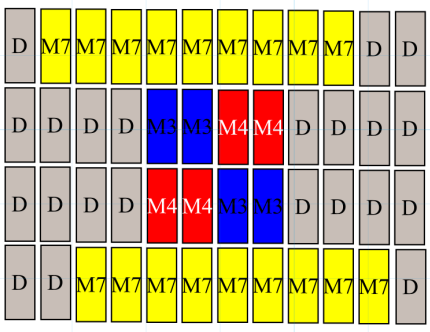

Fig. 18. Layout plan for all the PFETs in the layout.

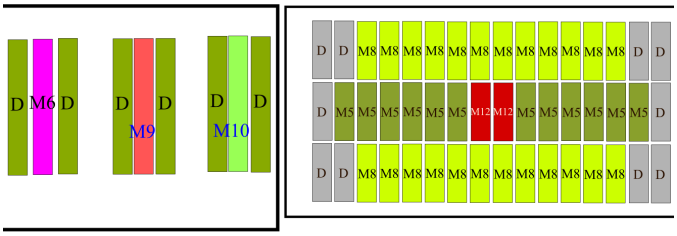

Fig. 19. Layout plan for current mirror and enable switches.

D. Explanation of the layout of the NMOS current mirror and enable switches

This was also a crucial part of the layout as the three MOSFETs M12, M5 and M8 needed to be matched. The enable switches were not matched to save time and were laid out seperately from the current mirror. An attempt at a common centroid layout made of 38 fingers with each finger having a $\frac{W}{L} = \frac{3}{1}$ was made. The goal here was to keep M5 and M8 as close as possible to M12 since M12 was considered as the reference device. M5 is surrounded by identical fingers (including dummy transistors) on all sides however M8 is only surrounded by the left and right sides. Fig. 19 shows the layout plan for the current mirror and enable switches. The enable switches also had dummy transistors on the left and right; however, whether they are necessary is unknown.

REFERENCES

[1] B. Razavi, Design of Analog CMOS Integrated Circuits, 2nd ed. New York, NY, USA: McGraw-Hill, 2016, p. 288.

[2] https://github.com/SkillSurf/ttsky25_se_opamp/tree/main/xschem

[3] https://github.com/bmurmann/Book-on-gm-ID-design/blob/main/starter_files_open_source_tools/sky130/README.md

[4] https://github.com/lochidev/ttsky25_two_stage_opamp/blob/main/docs/ttsky25_two_stage_opamp_rcx.md

[5] https://web.open-source-silicon.dev/t/16600198/are-there-near-plans-to-fix-the-skywater-analog-models-the-m

[6] https://github.com/lochidev/ttsky25_two_stage_opamp/blob/main/docs/results/Monte-Carlo/mc_4050.xlsx