Design of a single-ended two-stage op-amp with miller compensation using the Sky130A PDK

An explanation of my design submission to the Analog IC Student Design Contest organized by IEEE CASS CEDA Joint SL Chapter and SkillSurf.

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Design Evaluation, October 26th, 2025

Thank you so much for this awesome opportunity!

I would like to thank everyone involved in organizing the contest and the course. This is one of the best course I have ever taken. The knowledge that I gained was invaluable. I was really interested in microchips before the course started but could not see a clear entry point to start learning about the field. I learned a lot about the microscopic world and I'm really grateful for the opportunity to participate. Thank you so much for this awesome opportunity!

Desired Project Performance Specifications

Table: Desired Project Performance Specifications

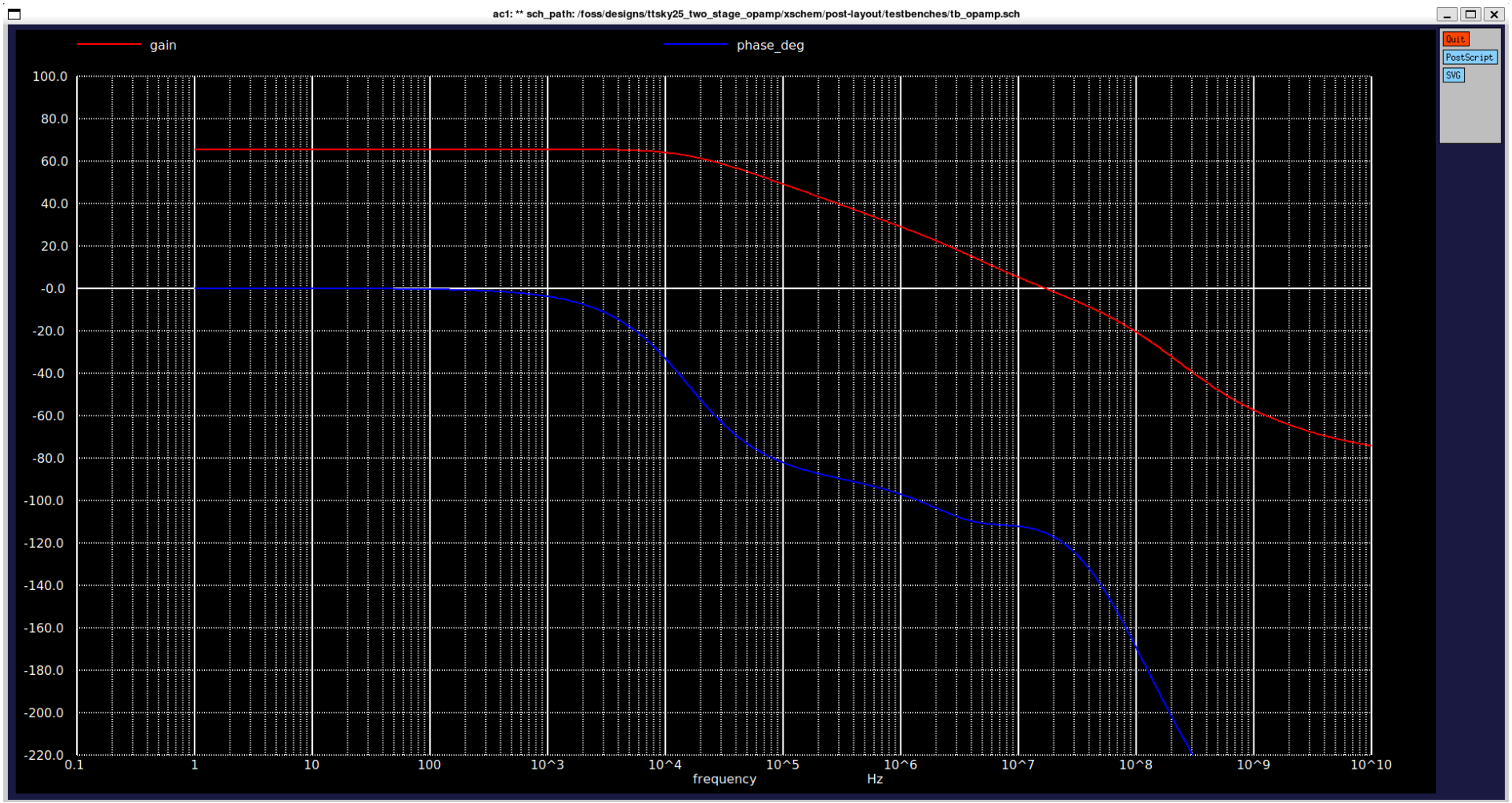
Parameter	**Project Specification**
Technology	130 nm CMOS
Supply voltage V_{DD}	1.7 V – 1.9 V
Nominal input common-mode voltage	$(V_{DD}/2 - 0.2\ \mathrm{V})$ – $(V_{DD}/2 + 0.2\ \mathrm{V})$
Output load C_L	25 pF (capacitive)
Temperature range	20°C to 50°C
Input signal amplitude	$< 0.4\ \mathrm{V_{pp}}$
Input signal frequency	1 – 10 kHz
Open-loop low-frequency (DC) gain A_{DC}	≥ 60 dB
Gain bandwidth product (GBW)	≥ 1 MHz
Phase Margin (PM)	$> 60°$
Quiescent current	$< 100\ \mu$A
Input offset	< 3 mV
Slew rate (both open-loop and closed-loop) SR	$> 1\ \mathrm{V}/\mu\mathrm{s}$
Disable current	< 2 nA
Final layout area	within $140\ \mu\mathrm{m} \times 80\ \mu\mathrm{m}$

Design that was chosen

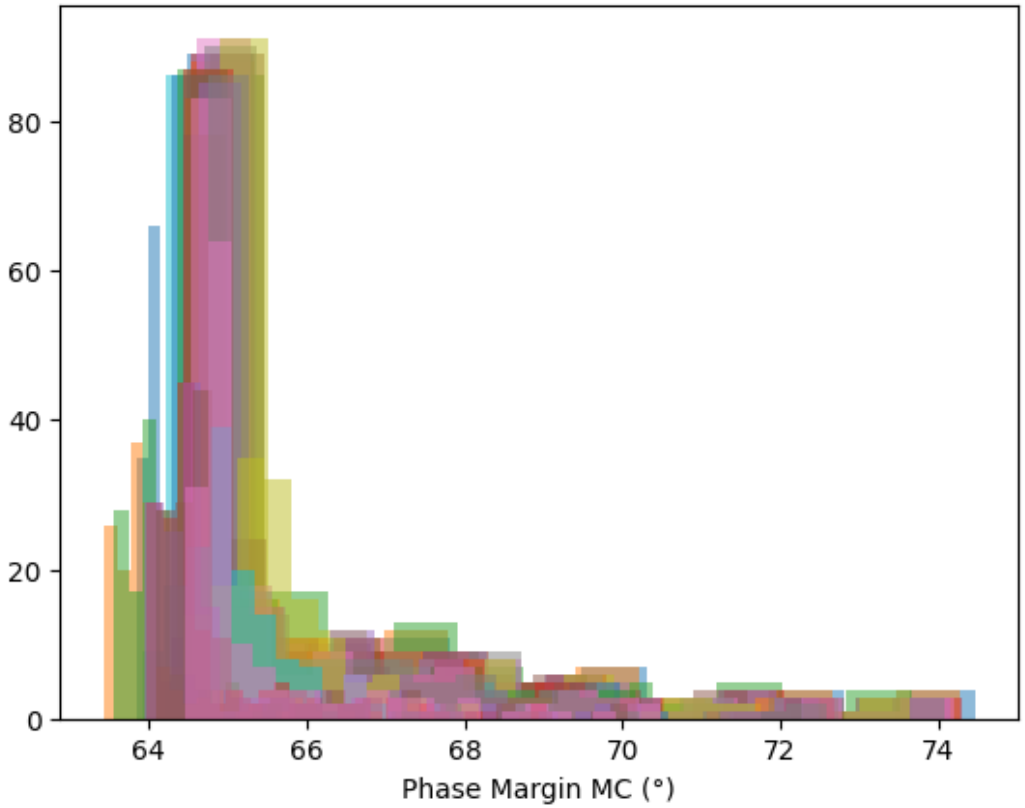
The two stage miller compensated operational amplifier design was chosen because of the following reasons.

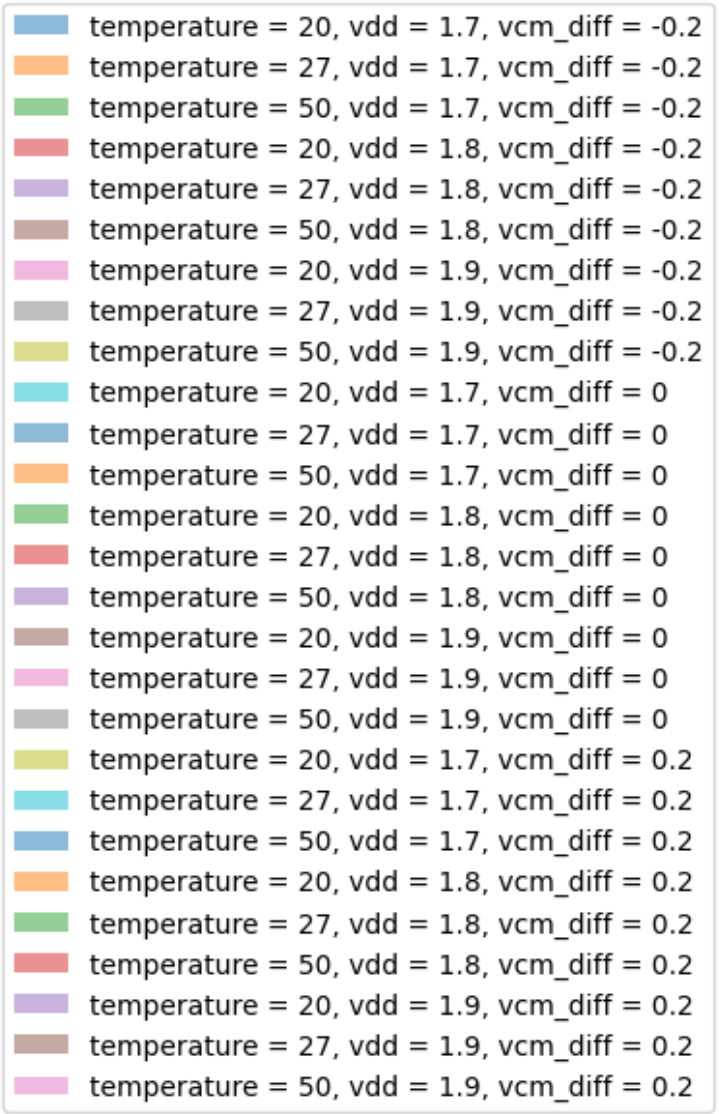
- Most of the online resources I could find were discussing this design.
- High open-loop gain can be obtained.
- Power constraints can be met because the design has only two stages.
- The common source second stage can provide high output swing.

DC gain-phase plot

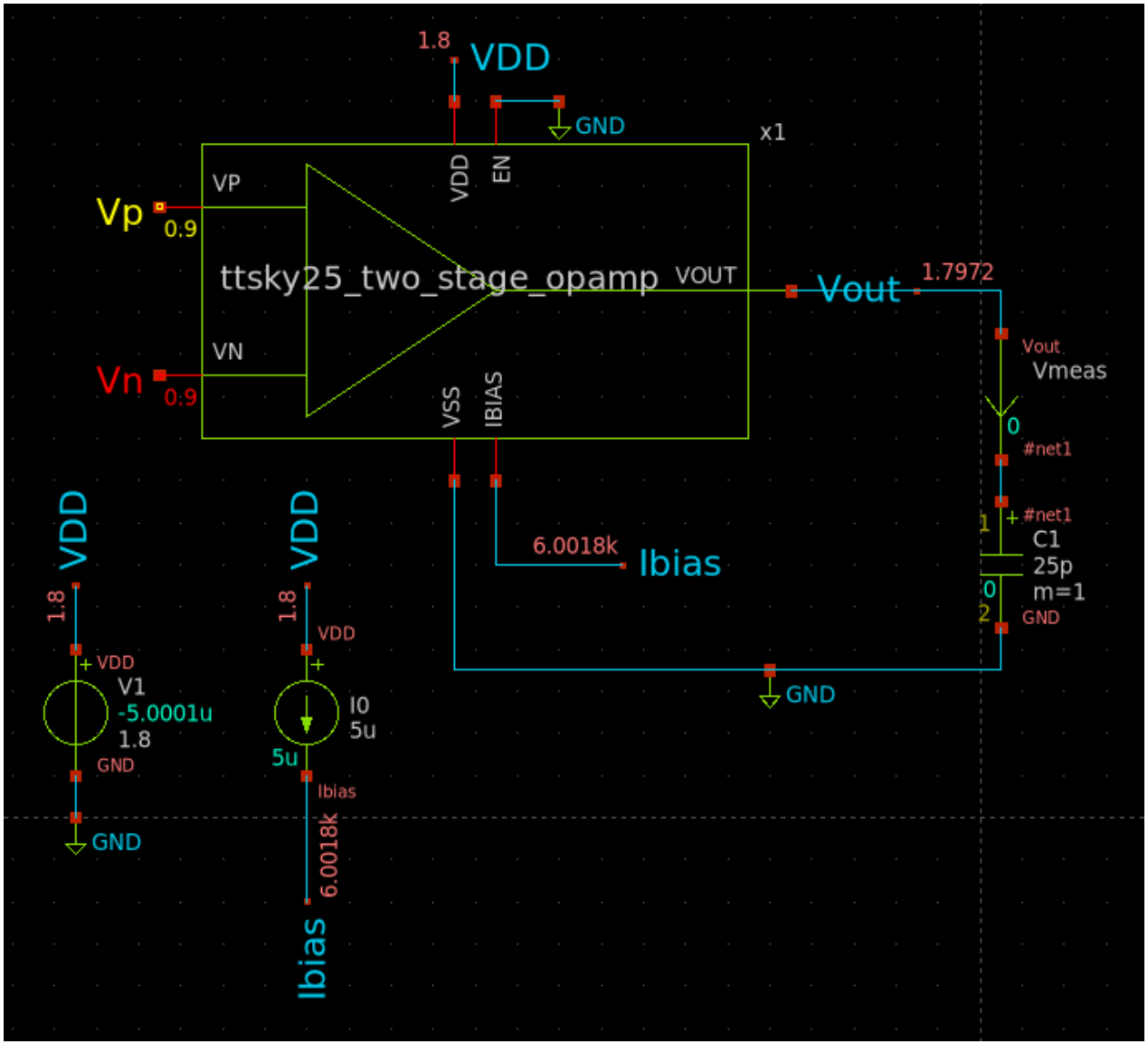


Phase margin Monte Carlo simulation result



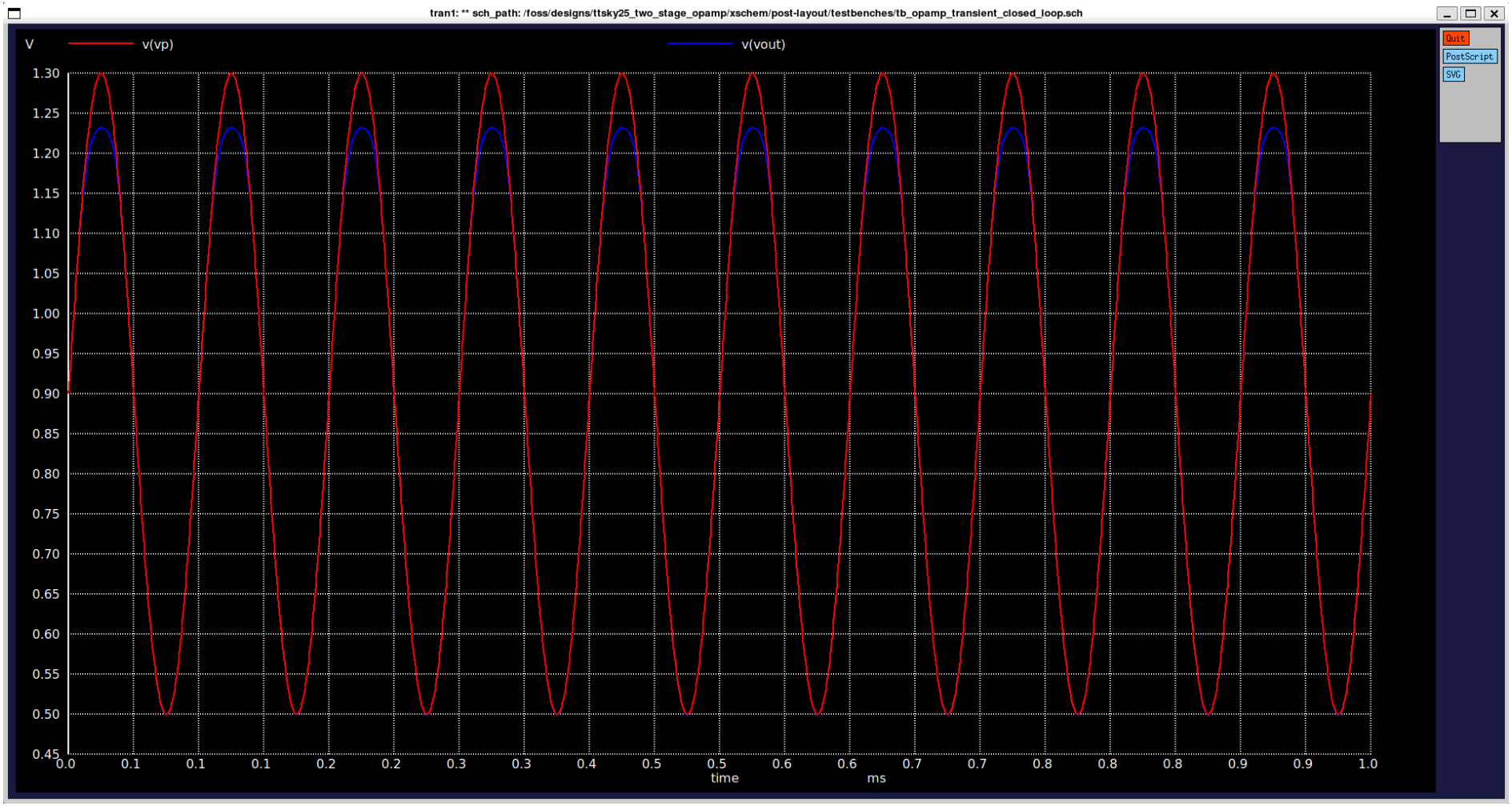


Open loop disable mode current

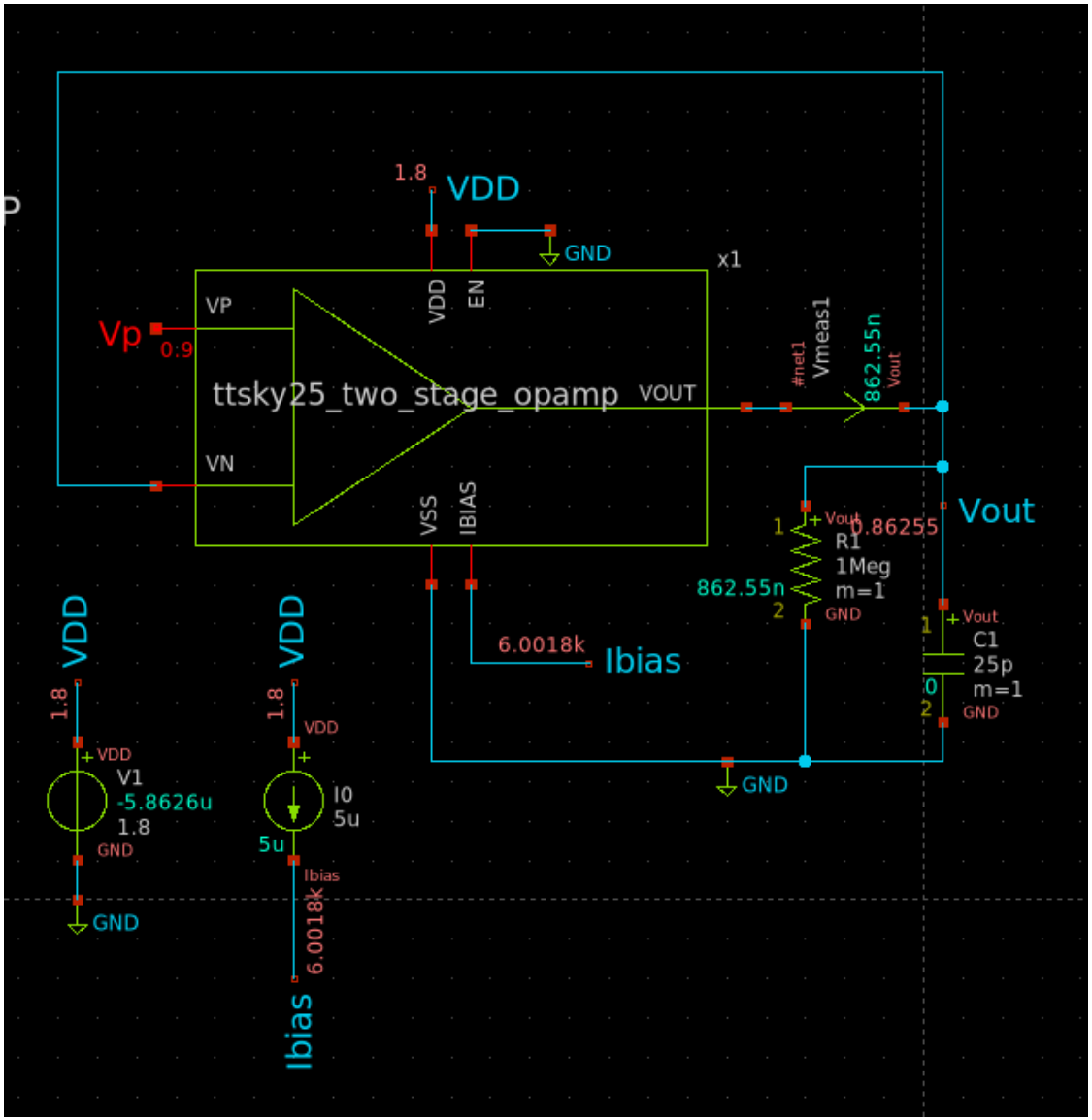


Closed loop transient simulation in sf corner

V_{pp} = 0.4 V at 10 kHz



Closed loop disable mode current issue



Performance Specifications Achieved By My Design

Table: Desired Project Performance Specifications

Parameter	**Project Specification**
Supply voltage V_{DD}* ✓	1.7 V – 1.9 V
Nominal input common-mode voltage* ✓	$(V_{DD}/2 - 0.2\ \mathrm{V})$ – $(V_{DD}/2 + 0.2\ \mathrm{V})$
Output load C_L ✓	25 pF (capacitive)
Temperature range ✓	20°C to 50°C
Input signal amplitude* ✓	$< 0.4\ \mathrm{V_{pp}}$
Input signal frequency ✓	1 – 10 kHz
Open-loop low-frequency (DC) gain A_{DC}* ✓	≥ 60 dB
Gain bandwidth product (GBW) ✓	≥ 1 MHz
Phase Margin (PM) ✓	$> 60°$
Quiescent current ✓	$< 100\ \mu$A
Input offset ✓	< 3 mV
Slew rate (both open-loop and closed-loop) SR ✓	$> 1\ \mathrm{V}/\mu\mathrm{s}$
Disable current ✓	< 2 nA
Final layout area ✓	within $140\ \mu\mathrm{m} \times 80\ \mu\mathrm{m}$

*Ignoring extremes at sf process corner

Initial Calculations

Initially, the technology parameters found in `https://github.com/SkillSurf/ttsky25_se_opamp/blob/main/README.md` was used to calculate the W/L ratios of the MOSFETs. However, half-way through the design I switched to LVT NMOS and instead of trying to find these technology parameters I relied heavily on SPICE to find parameters such as V_{th}. The figure below is a screenshot from the above link.

Parameter	nMOS	pMOS
V_{th} (V)	0.49439	-1.0652
$\mu_0(\frac{cm^2}{V \cdot s})$	301.97	24.424
t_{ox} (nm)	4.148	4.23

Initial Calculations

Slew rate

The procedure for mathematical calculations found in `https://github.com/SkillSurf/ttsky25_se_opamp/blob/main/README.md` was followed to ensure the design met the slew rate requirements. I kept in mind the following equations found in the above link throughout the design.

Initial C_{miller} value

$C_{miller} \geq 0.22\ C_{load}$ for phase margin to be greater than 60.

Determining ITAIL

$$SR = \frac{I_{TAIL}}{C_{miller}} > 1V/\mu s$$

$$I_{TAIL} > SR * C_{miller}$$

Initial Calculations

Input common-mode voltage range

The procedure for mathematical calculations found in `https://www.youtube.com/watch?v=QbxOYI6UjoE` were kept in mind to ensure both M1 and M2 were in saturation for the required input common mode range voltages.

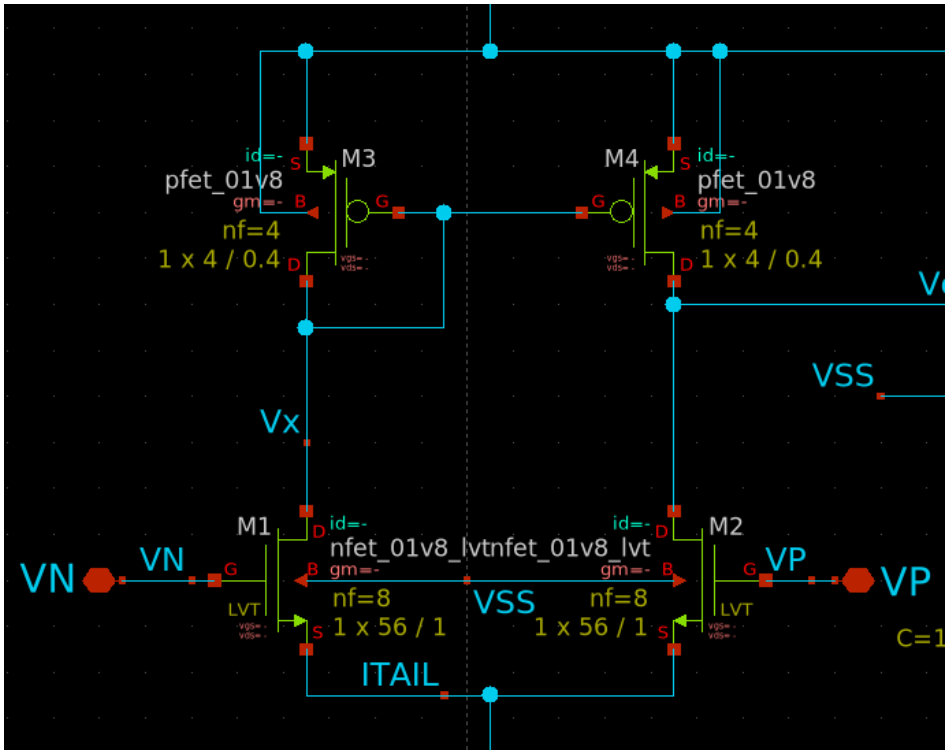


Figure: 1st stage NMOS differential pair with active load.

Initial Calculations

Input common-mode voltage range

V_{th} of M1 was found to be 0.55 V for this circuit using ngspice.

M1 being in saturation determines ICMR+ (Similarly M2)

$$V_x \geq V_{n,max} - V_{th}$$
$$V_x \geq 1.15\ V - 0.55\ V = 0.6\ V$$

$V_{D,sat}$ of M5 is a very low value in this design and it determines ICMR-.

Open-loop gain was used to determine the useful ICMR when used as a unity gain buffer. I only included input common-mode voltages that also produced a DC open-loop gain $\geq 60\ dB$. As a result, the design has trouble in the sf corner when it comes to ICMR due to it being unable to achieve the required gain.

Initial Calculations

Useful formulas that I kept in mind

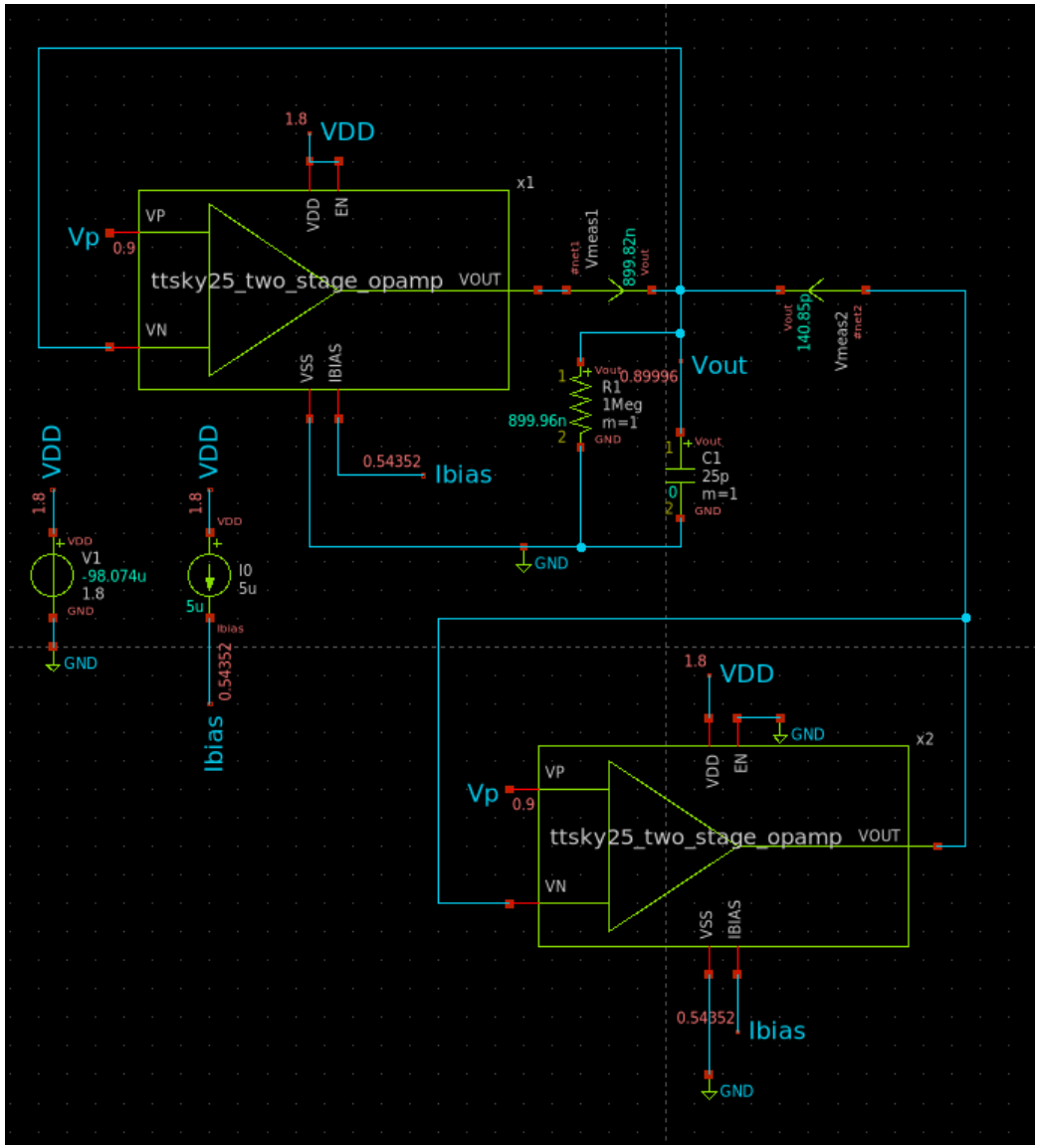
The following relationships and recommendations were obtained from `https://www.youtube.com/watch?v=PT31xAEd_v4`.

- The second stage consumes much more current than the first stage.

$$A_{OL} \approx g_{m2} R_{\text{out1}} \cdot g_{m7} R_{\text{out2}}$$

$$\omega_{p1} = \frac{1}{R_{\text{out1}} \cdot G_{m2} \cdot R_{\text{out2}} \cdot C_{\text{Miller}}}, \quad \omega_{p2} = \frac{G_{m2}}{C_L}$$

An attempt to measure output node current of the op amp



Thank you so much!