SYNOPSYS®

DATASHEET

Verdi Protocol Analyzer

Simulator independent protocol aware debug

Overview

With today's complex protocols, debug has become one of the most difficult and time-consuming aspects of functional verification. Verdi® Protocol Analyzer (See Figure 1), available with the VC Verification IP (VIP) family, is a simulator independent protocol-aware debug environment that enables users to quickly debug protocols and memory with any verification environment and easily share simulation results across teams. The Protocol Analyzer displays all levels of the protocol hierarchy enabling users to easily view relationships between transfers, transactions, data packets and handshaking.

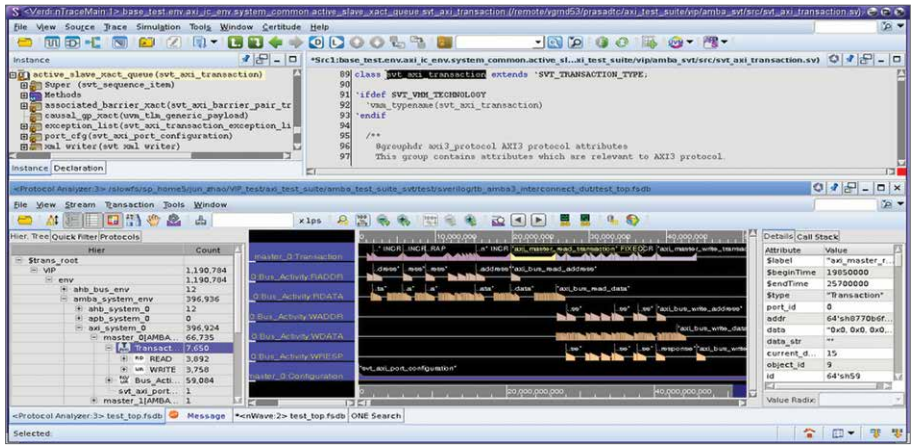

Figure 1: Verdi Transaction and Protocol Analyzer

The Protocol Analyzer is integrated with Synopsys' Verdi to synchronize the protocol and signal views, enabling engineers to easily correlate low level detailed signal activity with the higher-level protocol view.

Primary Features for Verdi Protocol Analyzer

Protocol and Memory support including: AMBA®, DDR, Ethernet, HDMI, LPDDR, PCIe and USB

- Side-by-side viewing and scrolling of multiple protocols or interfaces
- Shows all levels of protocol hierarchy
- Sophisticated filtering enables users to focus on objects and behavior of interest
- Simulator independent
- Integrated VIP class reference and user documents
- Integrated with Synopsys VIPs
- Included in Synopsys VIP Library

Complex Protocols Drive Growing Debug Challenge

The growth in complexity and increasing number of protocols used on SoCs is creating a rapidly increasing verification challenge and debug bottleneck for verification engineers. Verification engineers must quickly become protocol experts and try to correlate information across different sources of information to find the root cause of problems. Traditional debug methodologies use a combination of loosely connected waveforms, log-files, messages and documentation, which are insufficient for productive debug. The Protocol Analyzer, on the other hand, brings all the debug information into one place and provides protocol awareness to simplify root-cause analysis.

Verdi Protocol Analyzer

In the hardware world, bus analyzers and packet analyzers are widely used to debug hardware issues. These analyzers display information at a higher level of abstraction than more traditional logic analyzers that work at the signal level. Verdi Protocol Analyzer provides similar capabilities for verification engineers who are working with RTL and are faced with many of the same debug challenges. Protocol Analyzer utilizes data created by Synopsys VIP during verification of standard design interfaces like USB, PCI Express or AMBA. As VIP interacts with the design, it creates a high-level record of all the bus activity, as well as the values of its internal state machines and stores it in a common FSDB database along with the other design information. This integrated FSDB database provides better performance throughput, less memory footprint and occupies less disk space. Protocol Analyzer uses this data in conjunction with its own knowledge of the protocol to create a higher level, interactive display of the activity across the interface. It uses the simulation log generated by UVM to correlate errors, warnings and other messages with the protocol activity.

Multiple Panes

The Transaction and Protocol Analyzer pane provides a software-oriented waveform-like view (compared to the hardware hierarchical view in the nTrace window) for protocol/transaction level debug. The Protocol Browser window can be used to debug and analyze transactions and their activity by time and transaction type. (See Figure 2). The panes can be easily managed to optimize screen area.

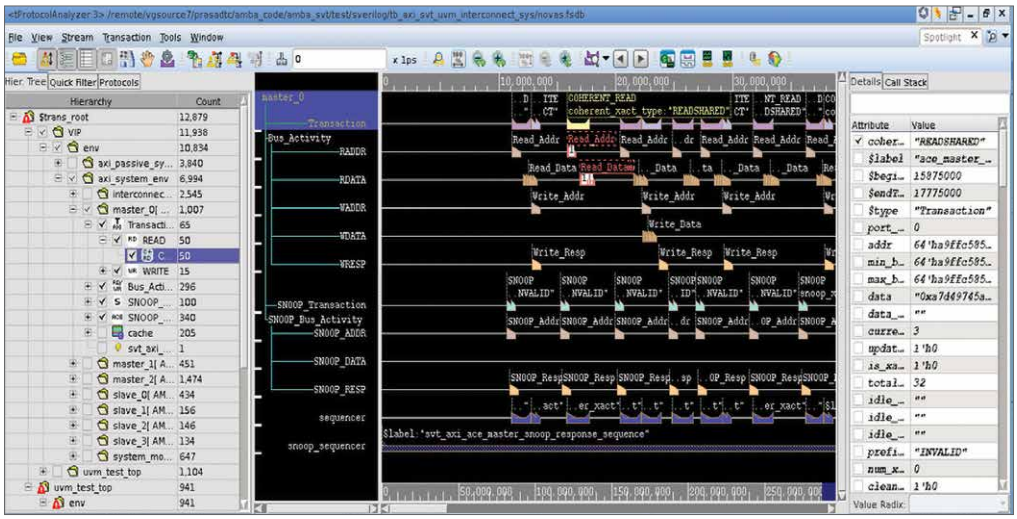

Figure 2: Protocol Browser Default layout

The default layout of the Transaction and Protocol Analyzer window is as follows:

- The left region contains the Hierarchy Tree pane
- The middle region contains Stream pane and Transaction pane
- The right region contains the Value pane

Hierarchy Tree Pane

After importing an FSDB file, the protocol hierarchy tree recorded in the FSDB file is shown in the Hierarchy Tree pane.

Stream and Transaction Pane

The FSDB file generated by the VIP contains streams grouped with channels, columns, and instances. The Stream pane in Transaction and Protocol Analyzer displays connections between channels, columns, and instances name. This makes it easier to identify channels, columns, and instances that belong to each other.

Value Pane

The Value pane contains two tabs: Details tab and Call Stack tab. The Value pane displays the attribute details or the call stack, which can be switched by selecting the tab for the selected transaction.

Search and Filter

A rich set of search and filtering in Protocol Analyzer allows verification engineers to exclude non-interesting objects from view and focus on the objects relevant to the issues being debugged.

Synchronization with nWave

When your FSDB file contains both transaction and signal levels, you can automatically connect Transaction and Protocol Analyzer and the primary nWave to debug your design with both waveforms together. The viewing range and cursor operations will be automatically synchronized.

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