Programmable Synaptic Chip for Electronic Neural Networks

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Abstract:

A binary synaptic matrix chip has been developed for electronic neural networks. The matrix chip contains a programmable 32X32 array

of "long channel" NMOSFET binary connection elements imple(cid:173) mented in a 3-um bulk CMOS process. Since the neurons are kept

off(cid:173) chip, the synaptic chip serves as a "cascadable" building block for a multi-chip synaptic network as large as 512X512

in size. As an alternative the programmable NMOSFET (long channel) connection elements, tailored thin film resistors are deposited, in series

with FET switches, on some CMOS test chips, to obtain the weak synaptic connections. Although deposition and patterning of the

resistors require additional they promise substantial savings in silcon area. The performance of a synaptic chip in a 32-neuron

breadboard system in an associative memory test application is discussed. processing steps, to