Mini-Project Report:

ASM-FSM Implementing Algorithms in Hardware

exercise 1:

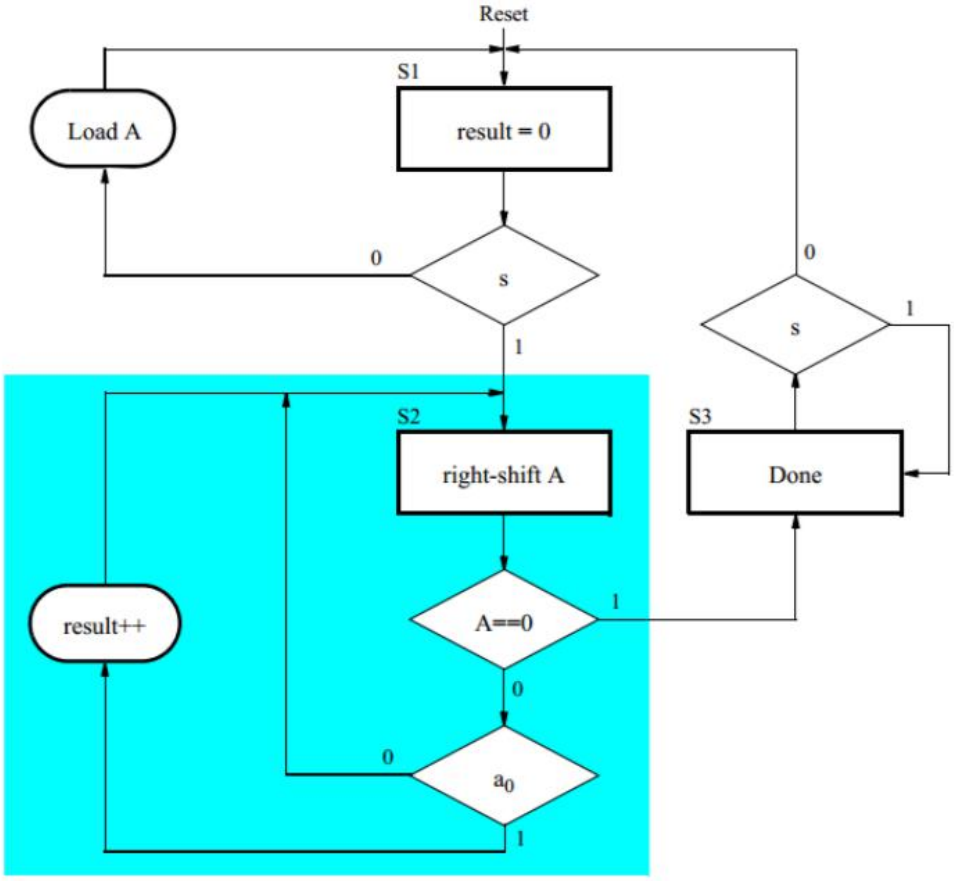
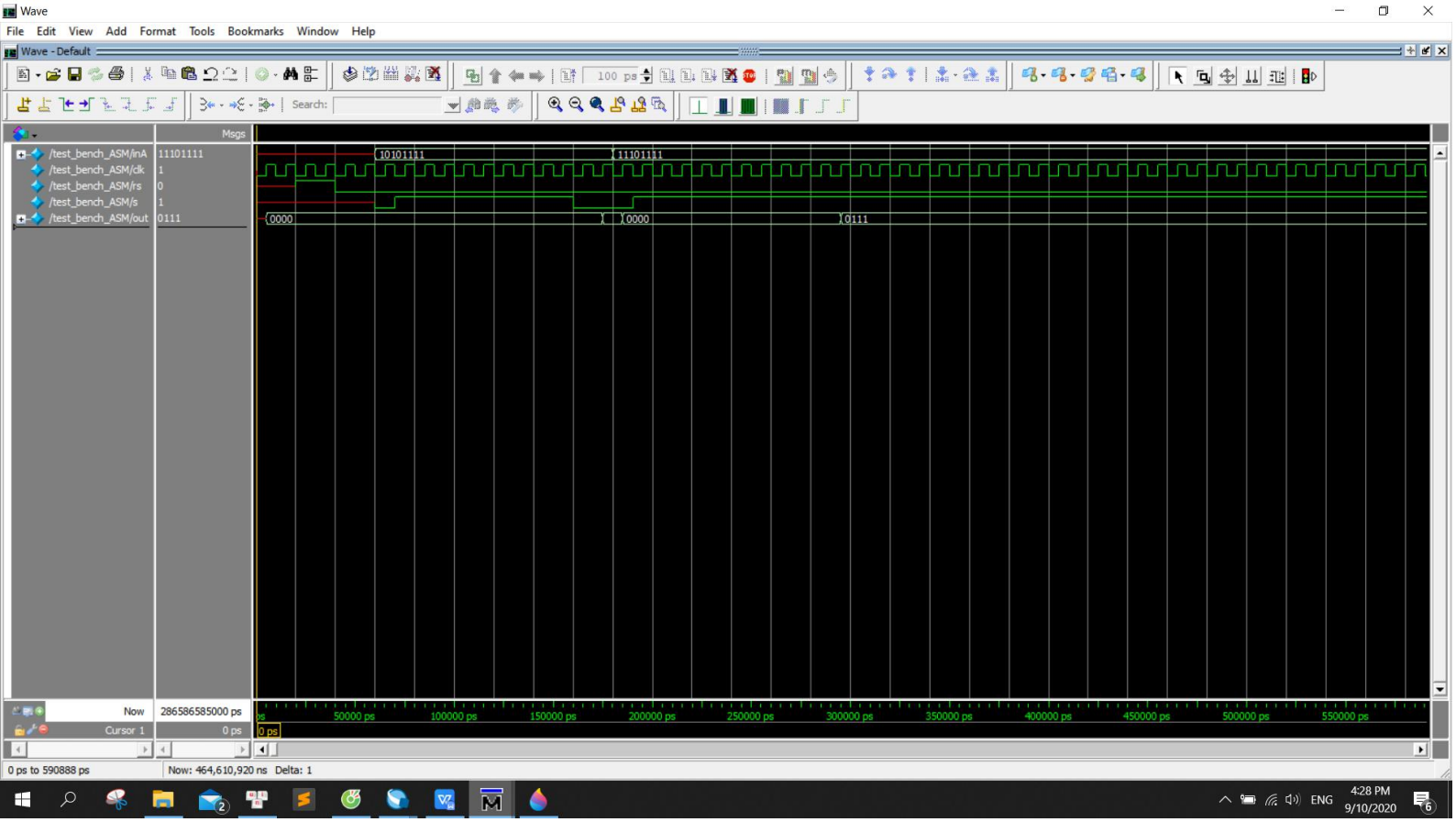
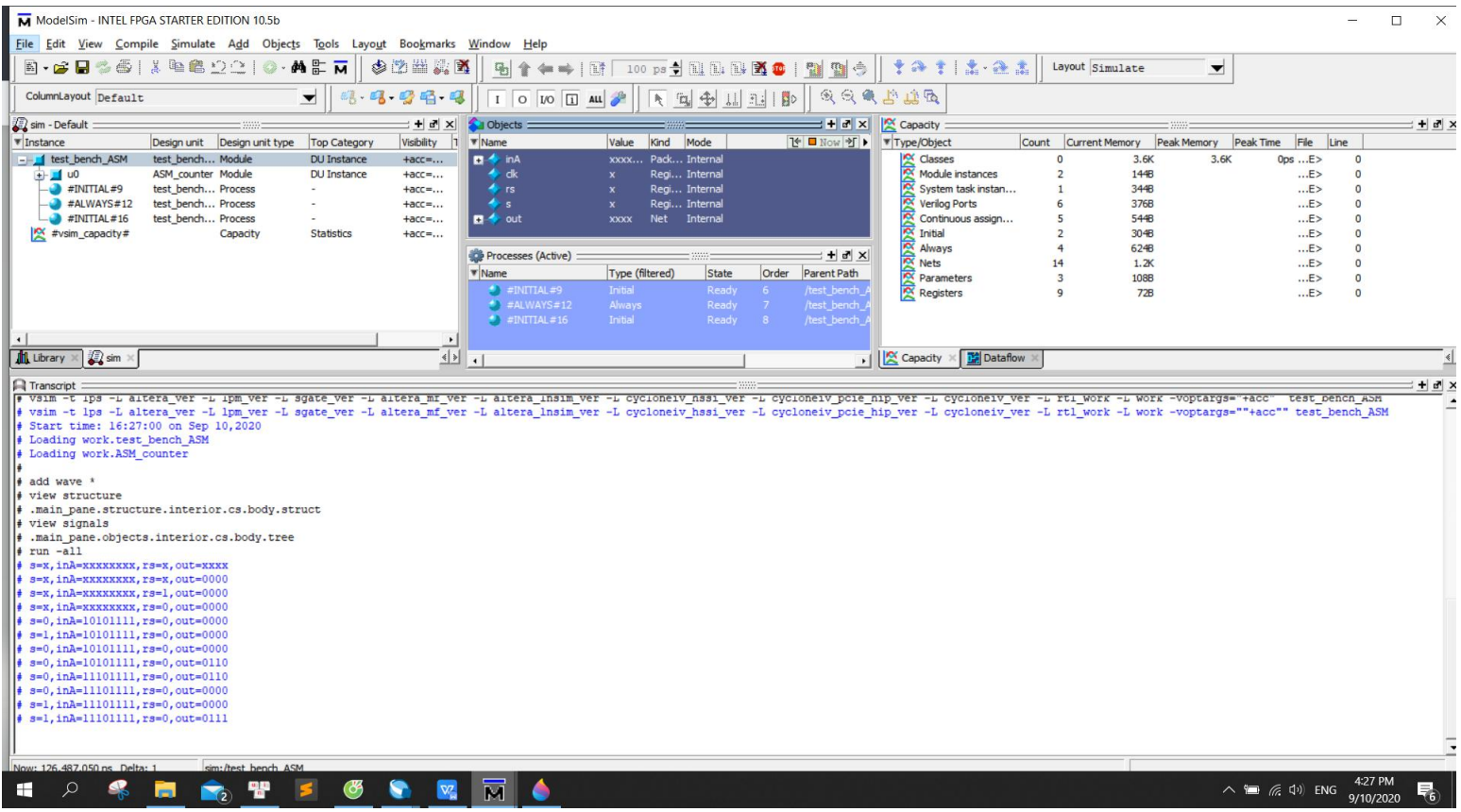


Figure 1: ASM chart for a bit counting circuit.

Here is testbench for exercise 1:


Wave
File Edit View Add Format Tools Bookmarks Window Help
Wave - Default
/test_bench_ASM/inA
/test_bench_ASM/clk
/test_bench_ASM/rs
/test_bench_ASM/s
/test_bench_ASM/out
11101111
1
0
1
0111
10101111
11101111
0000
0000
0111
Now
286586585000 ps
Cursor 1
0 ps
50000 ps
100000 ps
150000 ps
200000 ps
250000 ps
300000 ps
350000 ps
400000 ps
450000 ps
500000 ps
550000 ps
0 ps to 590888 ps
Now: 464,610,920 ns Delta: 1
ENG
4:28 PM
9/10/2020


ModelSim - INTEL FPGA STARTER EDITION 10.5b
File Edit View Compile Simulate Add Objects Tools Layout Bookmarks Window Help
Layout Simulate
ColumnLayout Default
sim - Default
Instance Design unit Design unit type Top Category Visibility
test_bench_ASM test_bench... Module DU Instance +acc=...
u0 ASM_counter Module DU Instance +acc=...
#INITIAL#9 test_bench... Process - +acc=...
#ALWAYS#12 test_bench... Process - +acc=...
#INITIAL#16 test_bench... Process - +acc=...
#vsim_capacity# Capacity Statistics +acc=...
Objects
Name Value Kind Mode
inA xxxx... Pack... Internal
clk x Regi... Internal
rs x Regi... Internal
s x Regi... Internal
out xxxx Net Internal
Processes (Active)
Name Type (filtered) State Order Parent Path
#INITIAL#9 Initial Ready 6 /test_bench_A
#ALWAYS#12 Always Ready 7 /test_bench_A
#INITIAL#16 Initial Ready 8 /test_bench_A
Capacity
Type/Object Count Current Memory Peak Memory Peak Time File Line
Classes 0 3.6K 3.6K 0ps ...E> 0
Module instances 2 144B ...E> 0
System task instan... 1 344B ...E> 0
Verilog Ports 6 376B ...E> 0
Continuous assign... 5 544B ...E> 0
Initial 2 304B ...E> 0
Always 4 624B ...E> 0
Nets 14 1.2K ...E> 0
Parameters 3 108B ...E> 0
Registers 9 72B ...E> 0
Library sim
Capacity Dataflow
Transcript
vsim -t 1ps -L altera_ver -L lpm_ver -L sgate_ver -L altera_mf_ver -L altera_lnsim_ver -L cycloneiv_hssi_ver -L cycloneiv_pcie_hip_ver -L cycloneiv_ver -L rtl_work -L work -voptargs="+acc" test_bench_ASM
vsim -t 1ps -L altera_ver -L lpm_ver -L sgate_ver -L altera_mf_ver -L altera_lnsim_ver -L cycloneiv_hssi_ver -L cycloneiv_pcie_hip_ver -L cycloneiv_ver -L rtl_work -L work -voptargs=""+acc"" test_bench_ASM
Start time: 16:27:00 on Sep 10,2020
Loading work.test_bench_ASM
Loading work.ASM_counter
#
add wave *
view structure
.main_pane.structure.interior.cs.body.struct
view signals
.main_pane.objects.interior.cs.body.tree
run -all
s=x,inA=xxxxxxxx,rs=x,out=xxxx
s=x,inA=xxxxxxxx,rs=x,out=0000
s=x,inA=xxxxxxxx,rs=1,out=0000
s=x,inA=xxxxxxxx,rs=0,out=0000
s=0,inA=10101111,rs=0,out=0000
s=1,inA=10101111,rs=0,out=0000
s=0,inA=10101111,rs=0,out=0000
s=0,inA=10101111,rs=0,out=0110
s=0,inA=11101111,rs=0,out=0110
s=0,inA=11101111,rs=0,out=0000
s=1,inA=11101111,rs=0,out=0000
s=1,inA=11101111,rs=0,out=0111
Now: 126,487,050 ns Delta: 1
sim:/test_bench_ASM
ENG
4:27 PM
9/10/2020