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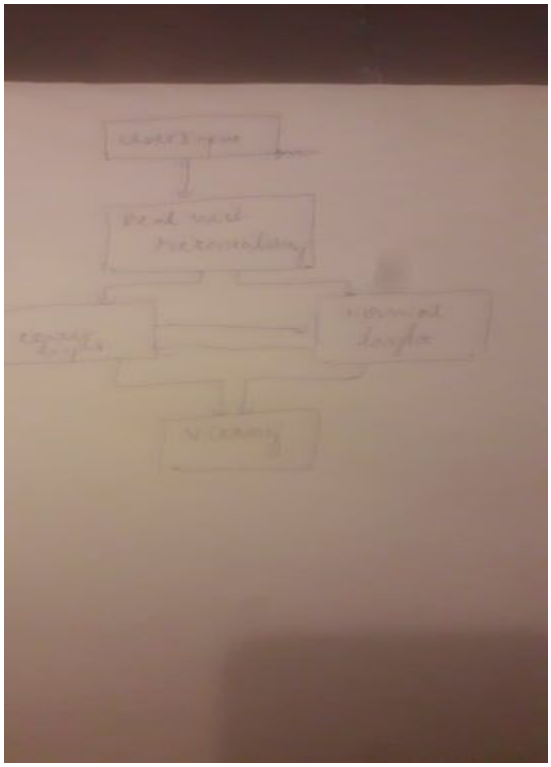
EE 271 Lab Report 4

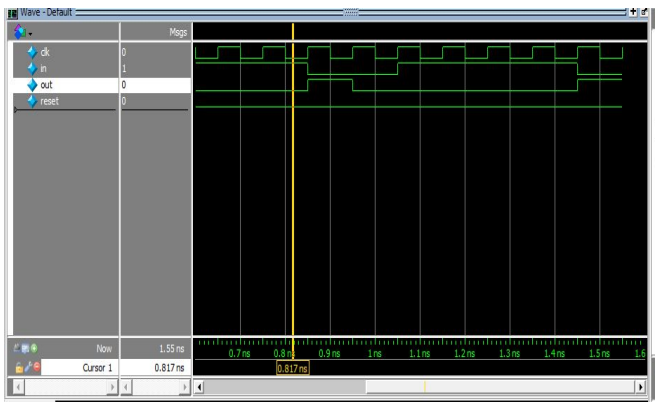
Procedure:
Initially, I drafted the top-level block diagram for the entire tug-of-war design, naming modules and logically connect them. Then, I drew the state diagrams for each modules, namely userInput, normalLight, centerLight, dealWithMetastability, and Victory before implementing them in Verilog. After the implementations, I then wrote the testbenches for each modules and simulate on modelSim for the convenience of debugging before combining them at the DE1_SoC module. When everything is connected, the only thing left is to download the design to FPGA and test the results.

Block diagram for the design:

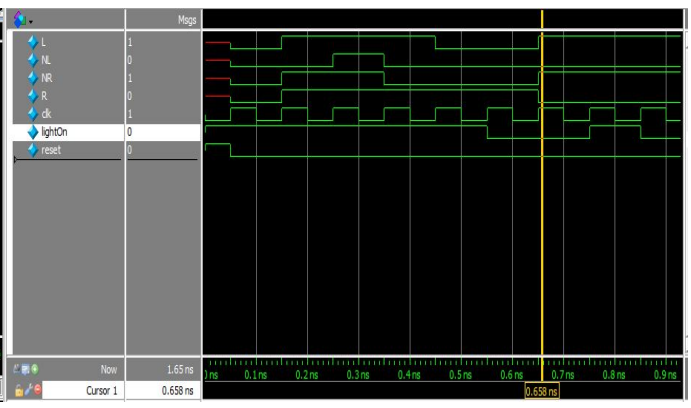


Results:

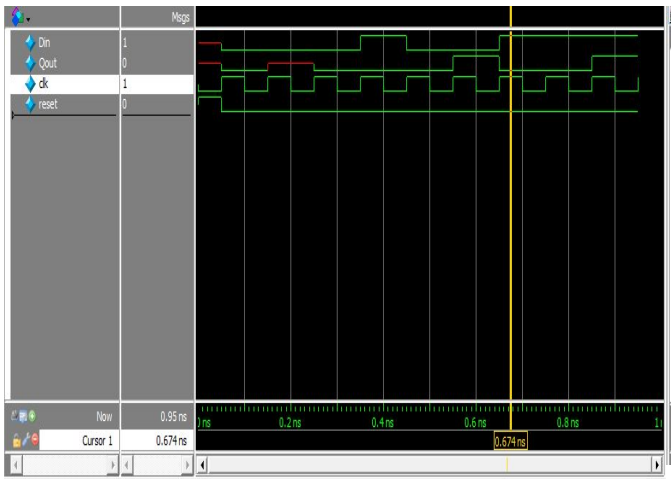
UserInput



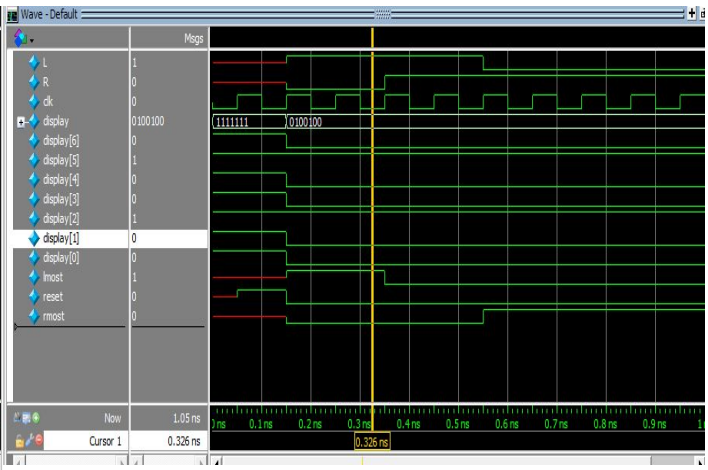
CenterLight



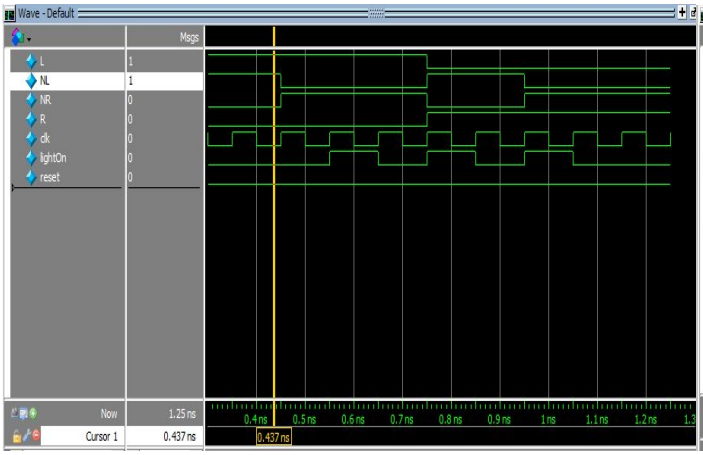
Metastability



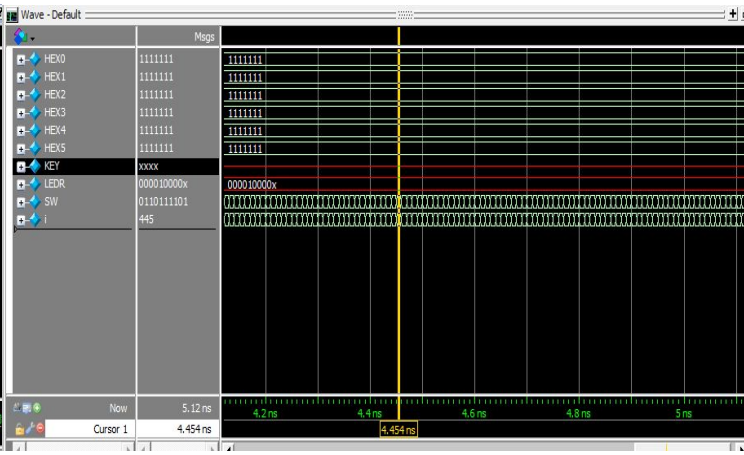
Victory



NormalLight



DE1_Soc



All the testbenches are based on upon the logic implemented in each module. Since the implementation used switch case to assign combinational logic to each state diagrams, the testbench will verify the matched behaviors of the FSMs before putting all of them together.

Utility Resource Screenshot

Analysis & Synthesis Resource Utilization by Entity

<<Filter>>

	Compilation Hierarchy Node	Combinational ALUTs	Dedicated Logic Registers	Block Memory Bits	DSP Blocks	Pins	Vir
1	◢ |DE1_SoC	24 (0)	17 (0)	0	0	67	0
1	|centerLight:center|	1 (1)	1 (1)	0	0	0	0
2	|dealWithMetastability:meta1|	2 (2)	2 (2)	0	0	0	0
3	|dealWithMetastability:meta2|	2 (2)	2 (2)	0	0	0	0
4	|normalLight:normal1|	1 (1)	1 (1)	0	0	0	0
5	|normalLight:normal2|	1 (1)	1 (1)	0	0	0	0
6	|normalLight:normal3|	1 (1)	1 (1)	0	0	0	0
7	|normalLight:normal4|	1 (1)	1 (1)	0	0	0	0
8	|normalLight:normal5|	1 (1)	1 (1)	0	0	0	0
9	|normalLight:normal6|	1 (1)	1 (1)	0	0	0	0
10	|normalLight:normal7|	1 (1)	1 (1)	0	0	0	0
11	|normalLight:normal8|	1 (1)	1 (1)	0	0	0	0

Since the design does not include the clock design, the size of the design is undetermined.

As we combine all the pieces together, the results are just as expected. Initially, the LEDR5 is always on while the rest are initially off. The output will be at only a clock cycle after the user inputs. Also, if one of the player reaches the end of the game field, HEX0 will display the winner accordingly.

Problems Faced and Feedback

The most troublesome task when it comes to this lab is to figure out the correct behavior and state diagrams of the design. Each individual has different design, but some are more efficient than others. I find myself spending a lot of time figuring out the efficient approach to the problem and sometimes it is a bit time-consuming. Yet, whenever I stumble into trouble, I double-check the state diagrams and used the testbench to debug the problem.

One advice I would give is to time yourself accordingly when doing this lab. Some people will the tasks simple and will spend very little time to accomplish everything; however, some still find it difficult. Thus, it is advised to be methodological in this lab. Start it early is the best option.