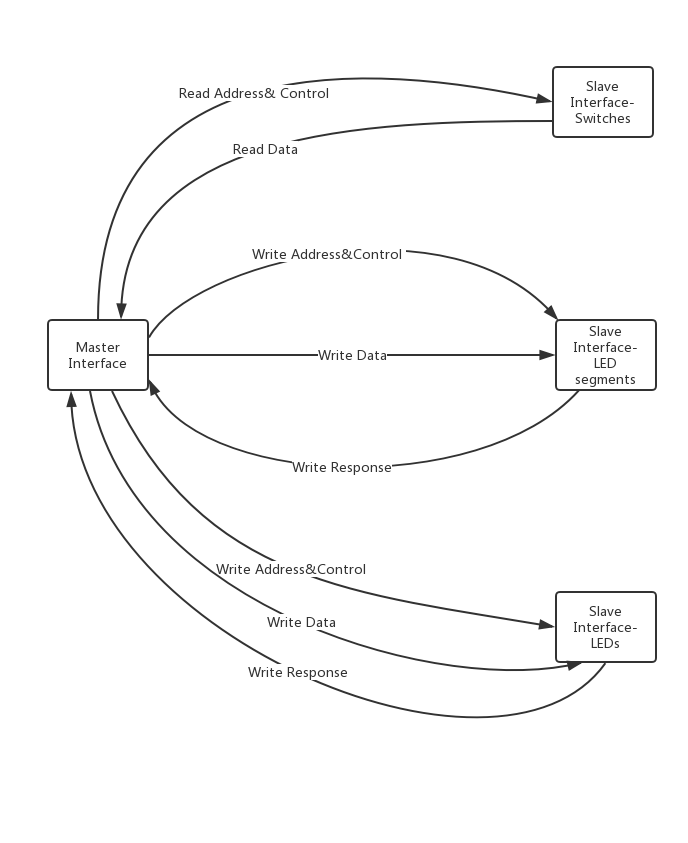
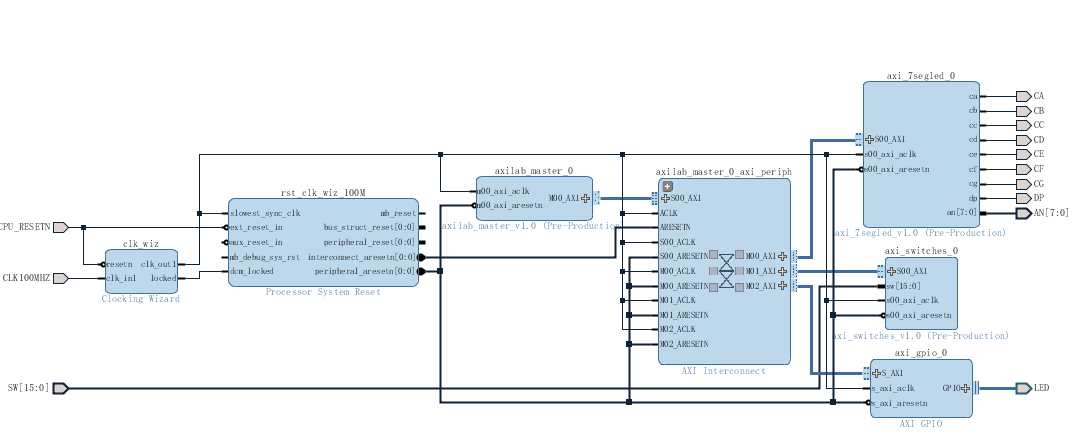
1. High-level Architecture Diagram

It is the first time that we use block design to integrate packaged IPs. The basic block diagram and design diagram are shown as following.

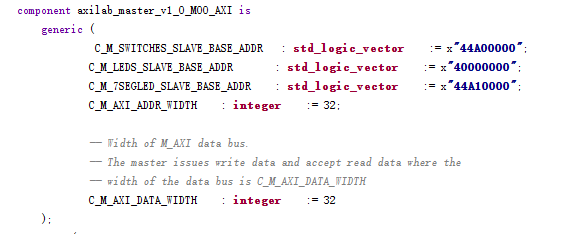
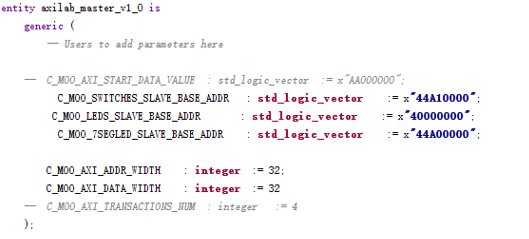


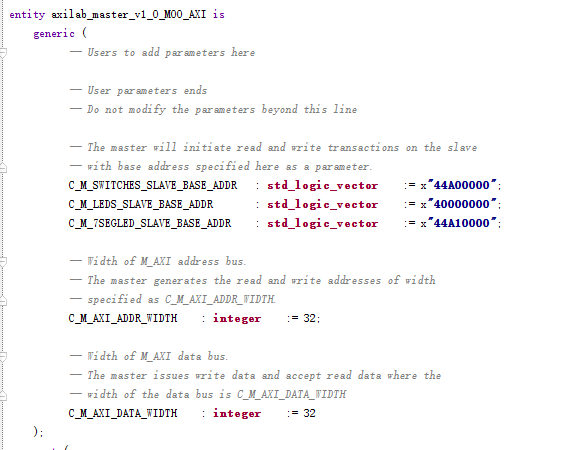
**

1. Description of Blocks

2.1 AXI Bus Master block

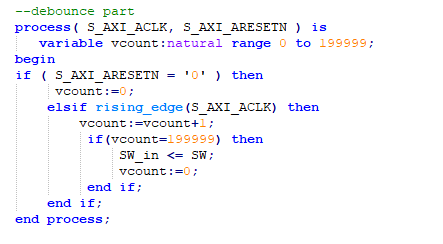
At first, I revised the master top module template **axilab\_master\_v1\_0**, adding three generic parameters of slavers’ base addresses and commenting out three unused ports. Then I changed the generic parameters in the given **axilab\_master\_v1\_0\_M00\_AXI**, to make them equal to those in top module **axilab\_master\_v1\_0**. All of these revisions are shown in following pictures.



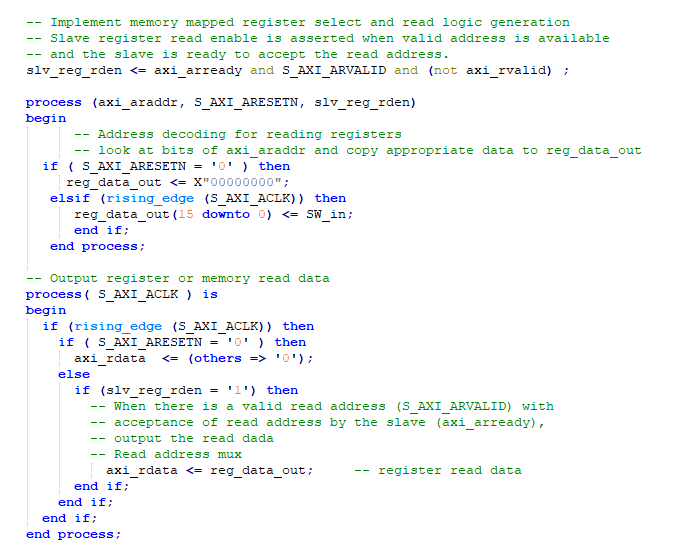


* 1. AXI Bus Switches Slave Block

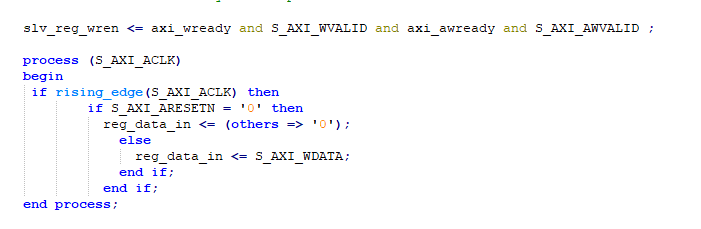
In this block, we should put data input by switches into AXI bus. This read process requires assigning input data to axi\_rdata, when slv\_reg\_rden is 1. I added two parts of new codes in given skeleton slave module. The first one is **debounce** part:



The second one is **read data** part.



* 1. AXI Bus 7segled Slave Block

In this block, we should assign S\_AXI\_WDATA from AXI bus to reg\_data\_in and then write data to output LED segments. I added two parts of new codes in given skeleton slave module. The first one is 

The second one is **data-to-LED** **segments transfer**

