Chapter 3 A Central Processing Unit runs programs · Every CPV has internal feadures to process commands of Every (PV runs code based on a specific machine language · CPUs use pyelines (cores) to optimize the placesing of commands o the capability of a CPU is measured by clock speed & cores · Modern CPUs support advanced features such as multi cores · ARM chips operate using reduced instudion set computing (RISC) methodology · Accelerated Placesing Units (APUS) are (pus with graphics colds built in 32-bit-(x86) 64-bit (x64) ISA (Instruction Sat Architecture) ISA X86-64 Supports 326+2646+ applications IA-32 is Intel Architecture & it supports X86 AKA 32 bit · XICH offers greater dot hardling, improved graphics, b better security e CPUs designed for laptops come with features to help with fourt consumption and laiding usage · Higher end (PVs offer more cores and a faster clock speed · Intensite tasks such as 30 gaming and video editing benefit from more CPU cons o some CPU's are unlocked been be overlaked intel RAMD are the man brains for CPVs the higher the CPV tier time better performance the generation gives a good indecutor of cpu age the model refers to the performme of the CPU the suffix denotes whether the CPU is unlatered or has integrated graphics Tayche per second = HZ

· Areat sinks use model find a pipes do passively transfer heat · thornal paste & pads we both used to filgaps are provide better Moderal countriesy brooksmik o their we numbers 51255 of fairs D-fail advers e liquid cooling has higher thorn-1 transfer capabilities than circooling Always USC ESD pleantier when handling CPVs · PBA is AMD and LGA is Intel they are Saket types · Zer - insertion force ZIF mechanism is used to secure CRVIN Motherbourd When tradseshading a non-functional CPU if 18st checkall conventions & make some the fan heat sink, and copy itsoff are seated propely before proceeding . Most CPU's measured in giga helts Lore is just another lare to the RAM at the sume time clarispeed is how quick for sec invisional in giga herts X86-32 bit, X64-64 bit | X86-64 support both

Intel Corein 12 900 K

Brind Tier benerius mile sitex haber tier = better previonee

AMD Ryzen 9 5 900 X X: comes overclocked bilintegrated go X X : comes averaliqued G: l'ategrades gragia is ESD = Electro Static discharge Intel uses land Grid (Flat connection) AMD uses Pin Grid (Pin connection) ZIF) Zero insertion Force: used to sauce (PU + socret When an instruction is sent to the CPU in a binny partern, how does the PU know what the instruction futtern Means? Code Book 2 Example of ISA - X64, X86, X86-64, IA32

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Chapter 3 continued notes What is the generation: Intel (ore 19 12900K 4) Before installing the COU What's best way to protect it? ESD mat