

Sec 3
Week 1Associate ~~professor~~ professor CSIS

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Computer Organization and Software Systems

5 Unit Course: 150 hrs

★ Evaluation Scheme ★

- ① Mid Sem - 90 min - 30% OB
- ② Comprehensive - 180 min - 40% OB
- Examination
- ③ Quiz ----- - 5% OB
- ④ Assignment ----- - 25% OB

★ Two Assignments ★ [Lab based]

- ① one pre-midsem exam: 12%
- ② one post-sem: 13%

→ Preparing Virtual lab (install) - Platifi

★ Important ★

T₁ & T₂ are the textbooks

Introduction to computer Systems

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* Definition of Computer

- is a complex system
- is a programmable device
- Must be able to process data
- must be able to move data
- must be able to control above three functions

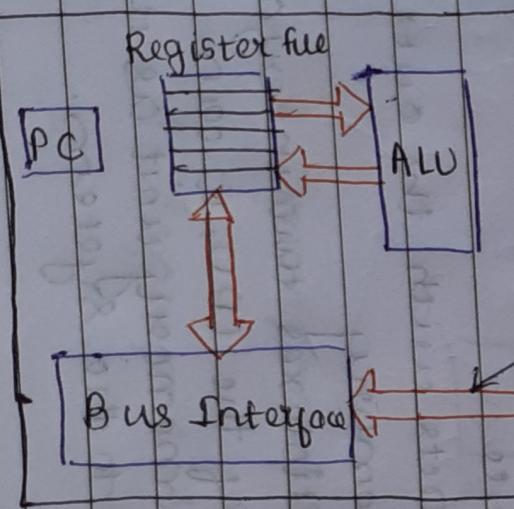
* Hardware

- central processing unit (CPU)
- Memory
- I/O devices

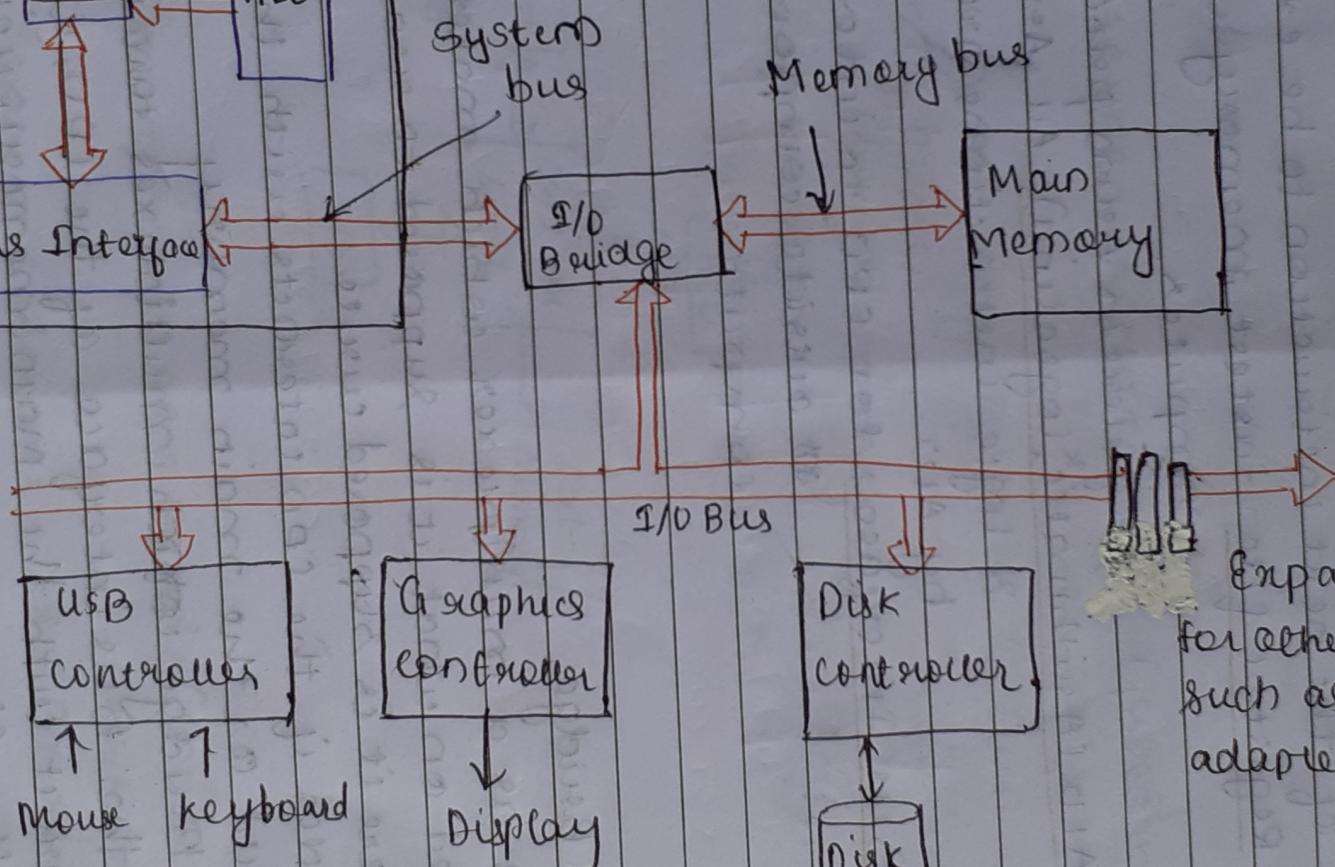
Software

- System Software
 - system management software
 - tools & utilities
- Application Software
 - General purpose
 - Specific purpose
 - ↳ calculator
 - ↳ mail

CPU



Hardware Organization of a computer Von Neumann Architecture



I] CPU

- ① Program counter: will have the address of the next instruction to be executed.
- ② Register file: fastest memory unit of a computer.
Registers in Arm processor >> X86.
- ③ ALU (Arithmetic & logic unit): All Arithmetic & logic instructions are executed by ALU.
- ④ Bus Interface: for CPU to interact with outside components of computer

II] I/O Bridge

- Acts as a multiplexer which makes variations based on what it is supposed to read or where it is supposed write.
- Decides if the CPU interacts with the outside world or the main memory.
- I/O Bridge ~~which~~ multiplexes two interfaces i.e. the Bus interface of the CPU, it can interact with the main memory unit as well as the I/O Bus attached to the system.

① von Neumann Architecture

Three Key Concepts:

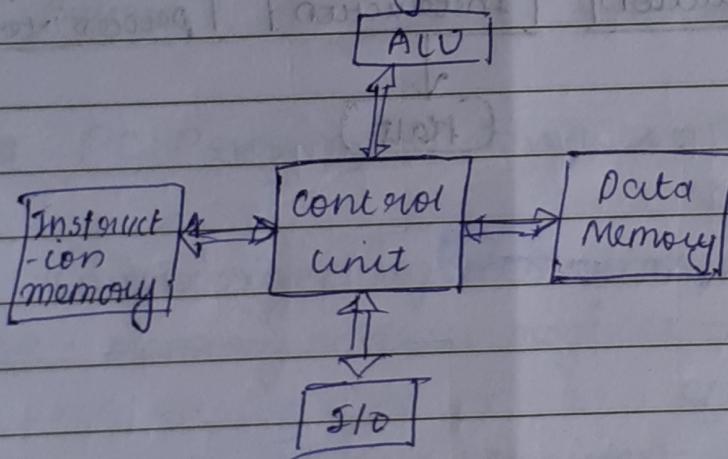
most widely used even presently

② HARVARD ARCHITECTURE (used mostly for cache memory)

uses two memory systems & two separate busses.

→ Instruction memory

→ Data memory



* Smartphones: ARM Based (CPU GPU architecture)

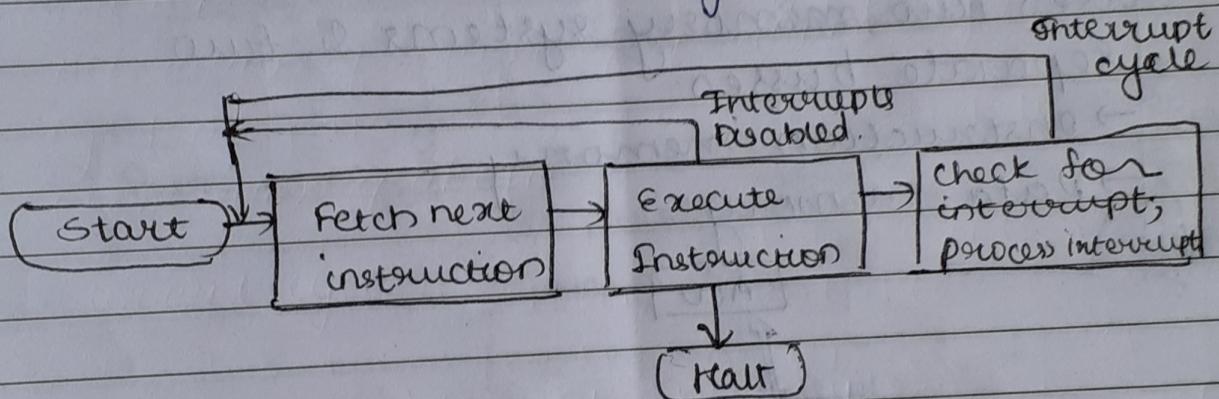
* laptops & servers : X86 Based

Instruction cycle Diagram.

Instruction Execution: Two steps

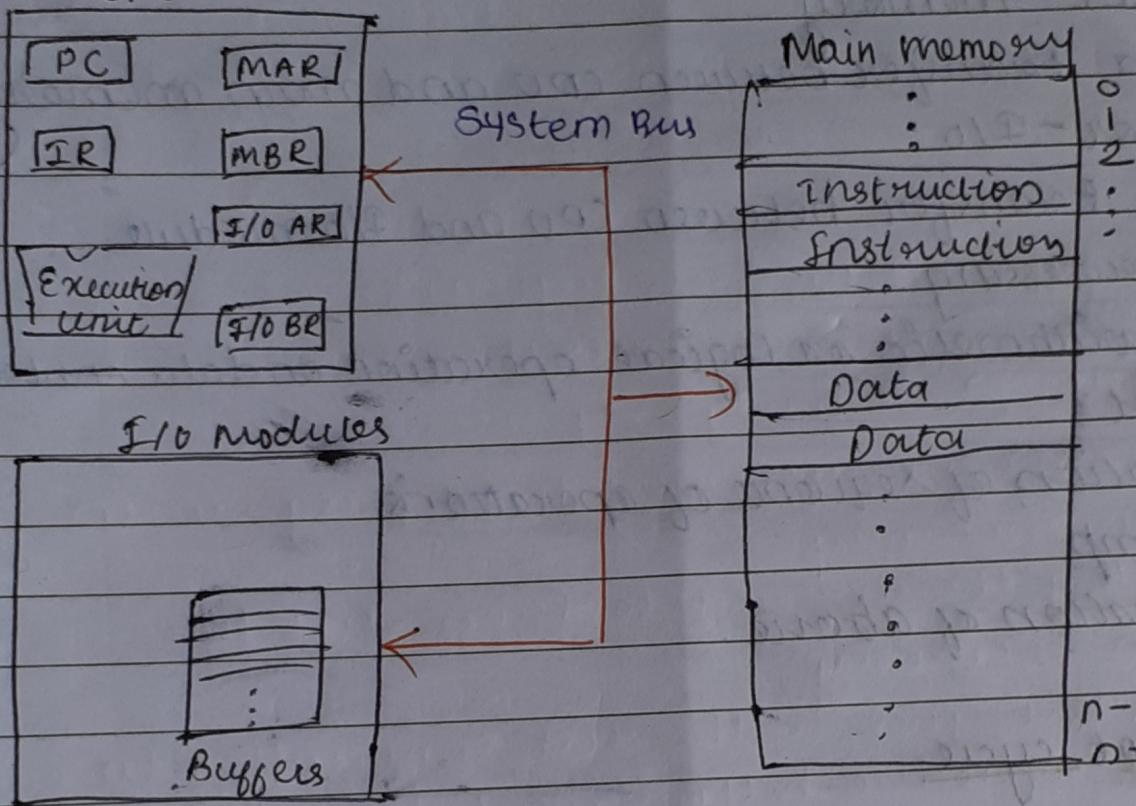
- Fetch
- Execute

Interrupt: Interrupt is checked at the end of instruction cycle



CPU

① Fetch cycle



- PC: Program counter - stores the address of the next instruction
- IR: Instruction register - stores the instruction
- MAR: Memory address register - stores the address of the instruction / data
- MBR: Memory buffer register - stores the data
- I/O AR - Input/output address register

② Execute cycle

- Processor - memory
 - Data transfer between CPU and main memory
- Processor - I/O
 - Data transfer between CPU and I/O module
- Data processing
 - Some arithmetic or logical operation on data
- Control
 - Alteration of sequence of operations
 - e.g. jump
- Combination of above.

③ Interrupt cycle

Types of Interrupts

① Program

e.g. overflow, divide by zero

② Timer

e.g. generated by internal processor timer

• used in pre-emptive multi tasking

③ I/O

④ Hardware failure

Operating System

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Types of Interrupts

Decimal Number System

1000	100	10	1	Base : 10.
1	2	3	4	

$10^3 \quad 10^2 \quad 10^1 \quad 10^0$

$$1234 = 1 \times 10^3 + 2 \times 10^2 + 3 \times 10^1 + 4 \times 10^0$$

Binary Number System

32	16	8	4	2	1
4	0	1	1	0	1

$2^5 \quad 2^4 \quad 2^3 \quad 2^2 \quad 2^1 \quad 2^0$

$$45 = 1 \times 2^5 + 0 \times 2^4 + 1 \times 2^3 + 1 \times 2^2$$

$$+ 0 \times 2^1 + 1 \times 2^0$$

Decimal to Binary

Reverse genes
↓ Binary No.

N	Quotient (N/2)	Remainder
45_{10}	22	1
22_{10}	11	0
11_{10}	5	1
5_{10}	2	1
2_{10}	1	0
1_{10}	0	1

$$45 = 101101$$

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Reading. ./hello command from keyboard.

Virtual lab - CPU OS Simulator is used for
01: Assignments #

- ① user types ./hello from keyboard
- ② The command lines reads it
- ③ input → I/O bridge → processor
- ④ processor initiates action to get program in main memory.
- ⑤ Loading the executable from disk to main memory.
- ⑥ Request goes to the disk controller to retrieve the hello executable
- ⑦ This transfer is known as "direct memory transfer" as processor is not involved in loading data from the disk to the main memory.
- ⑧ hello executable is sent back through the I/O bridge to the main memory.
- ⑨ the executable is run from the main memory and the data is displayed on the screen.

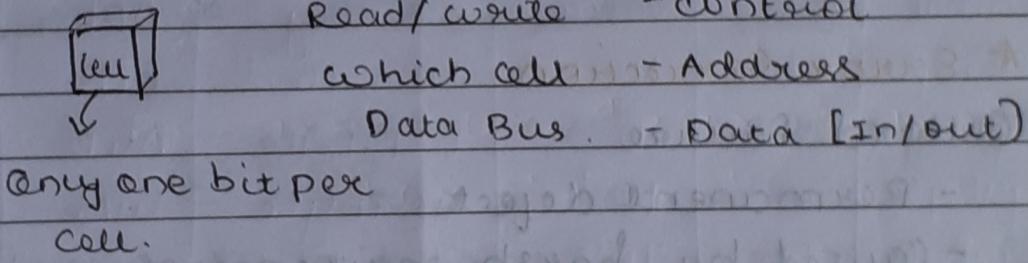
Week 2. Memory Organization

* Internal Memory Organization

- Main memory / primary memory
- Small data storage
- RAM, ROM

RAM: To bridge gap between processor speed (fast) & hard disk speed (slow)

* Semiconductor Memory



* Random - Access memory

- Key features

SRAM

DRAM

cell

chip

Volatile memories

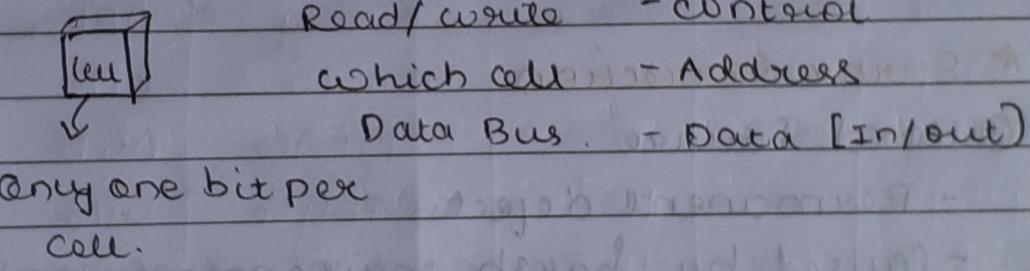
Week 2 Memory Organization

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◦ Key features

SRAM

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cell

chip

Volatile memories

Memory Read Operation

- ① In the CPU there is a Memory Address Register (MAR), with the data to be

Memory write operation [store]

- ② MDR/MBR received from memory or MAR contains a large number (+ve)

★ SDR and DDR

- Single Data Rate

★ Error Correction

- ③ Hard failure

- Permanent defect

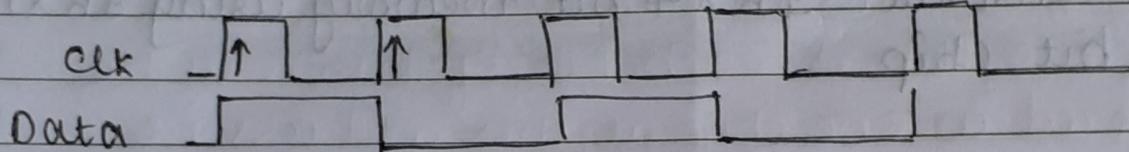
- Caused by harsh environmental abuse or manufacturing defects

SDR VS DDR

SDR → single data Rate

DDR → Double data Rate

① SDR

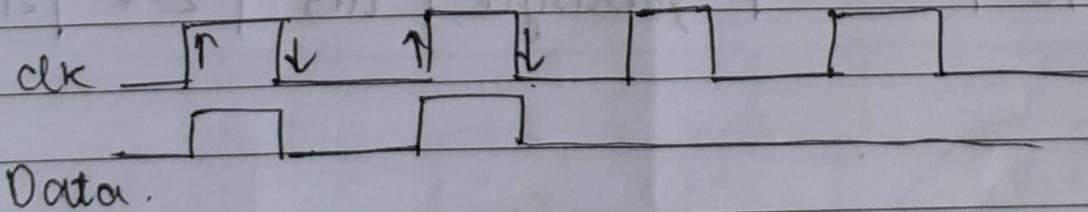


SDR: one clock cycle to read or write the data.

→ only data is transferred on rising edge.

② DDR

- Rising & Data transfer takes place on rising as well as falling edge.
- Hence double data Rate.



1Kx1



It can store 1 kilo bits $\rightarrow 2^{10} \rightarrow 1024$ bits

* Typical memory connection

(Q1) construct 4K x 4 bit memory using 1K x 1 bit chip

1K x 1 \rightarrow it can store 1 kilo bits

$\rightarrow 2^{10}$ bits

$\rightarrow 1024$ bits

<u>Decimal</u>	<u>Abbrev.</u>	<u>value</u>	<u>Binary</u>	<u>Abbrev.</u>	<u>value</u>	<u>large</u>
kilobyte	KB	10^3	kibibyte	KiB	2^{10}	2%
megabyte	MB	10^6	mebibyte	MiB	2^{20}	5%
gigabyte	GB	10^9	gibibyte	GiB	2^{30}	7%
terabyte	TB	10^{12}	tebibyte	TiB	2^{40}	10%
petabyte	PB	10^{15}	pebibyte	PiB	2^{50}	13%
exabyte	EB	10^{18}	exbibyte	EiB	2^{60}	15%
zettabyte	ZB	10^{21}	zebibyte	ZiB	2^{70}	18%
yottabyte	YB	10^{24}	yobibyte	YiB	2^{80}	21%

$$K = \text{Address bits} = 10 \log_2$$

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Q1 construct $1K \times 4$ bit memory using $1K \times 1$ bit chip

* $1K \times 1 \rightarrow 1 \text{ kilo bits} = 1024 \text{ bits}$
 $= 2^{10} \text{ bits}$

we are capable of
addressing each of this bit

* to address 2^{10} bits we need
10 bits address bus.

Ans ① For $1K \times 1$ bit chip, we have

$1K = 1024 = 2^{10} \text{ bits}$

and each bit is addressable hence
each bit will have unique address.

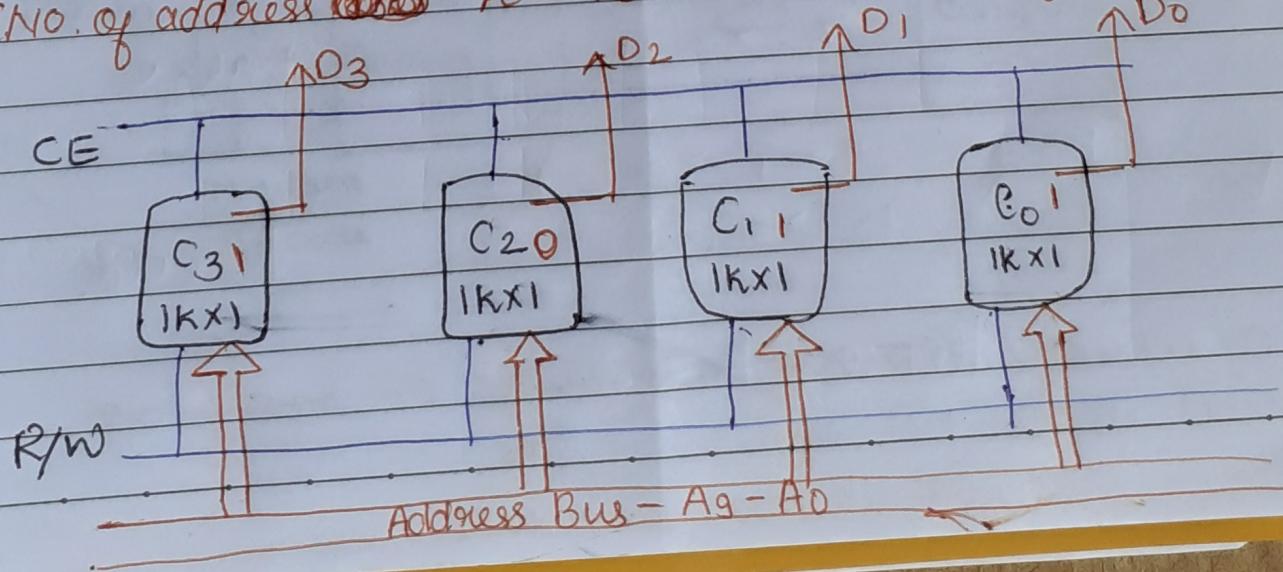
② To have unique address for 1024 bits
i.e. 2^{10} bits we need address bus
of 10 bit size

address:

$$\begin{aligned} (\text{No. of bits}) &= 2^{10} \text{ bits} \\ (\text{No. of address bits}) &= K = 10 \end{aligned}$$

01010101100

Data: 1011
D₃ D₂ D₁ D₀



Explanations:

① of the data is 1011

Address is 100101011100

This address is present at C₃, C₂, C₁ & C₀.
Hence ~~& there~~ each bit of data will be stored in one chip at this address i.e.

$$D = 1011$$

D₃ D₂ D₁ D₀

100101011100

D₀: 0
D₁: 1
D₂: 0
D₃: 1

D₀: 1
D₁: 0
D₂: 1
D₃: 0

D₀: 1
D₁: 0
D₂: 1
D₃: 0

D₀: 1
D₁: 0
D₂: 1
D₃: 0

C₀: 1
C₁: 0
C₂: 1
C₃: 0

Q2. Construct 2×4 bit memory using
 $1K \times 4$ bit chip

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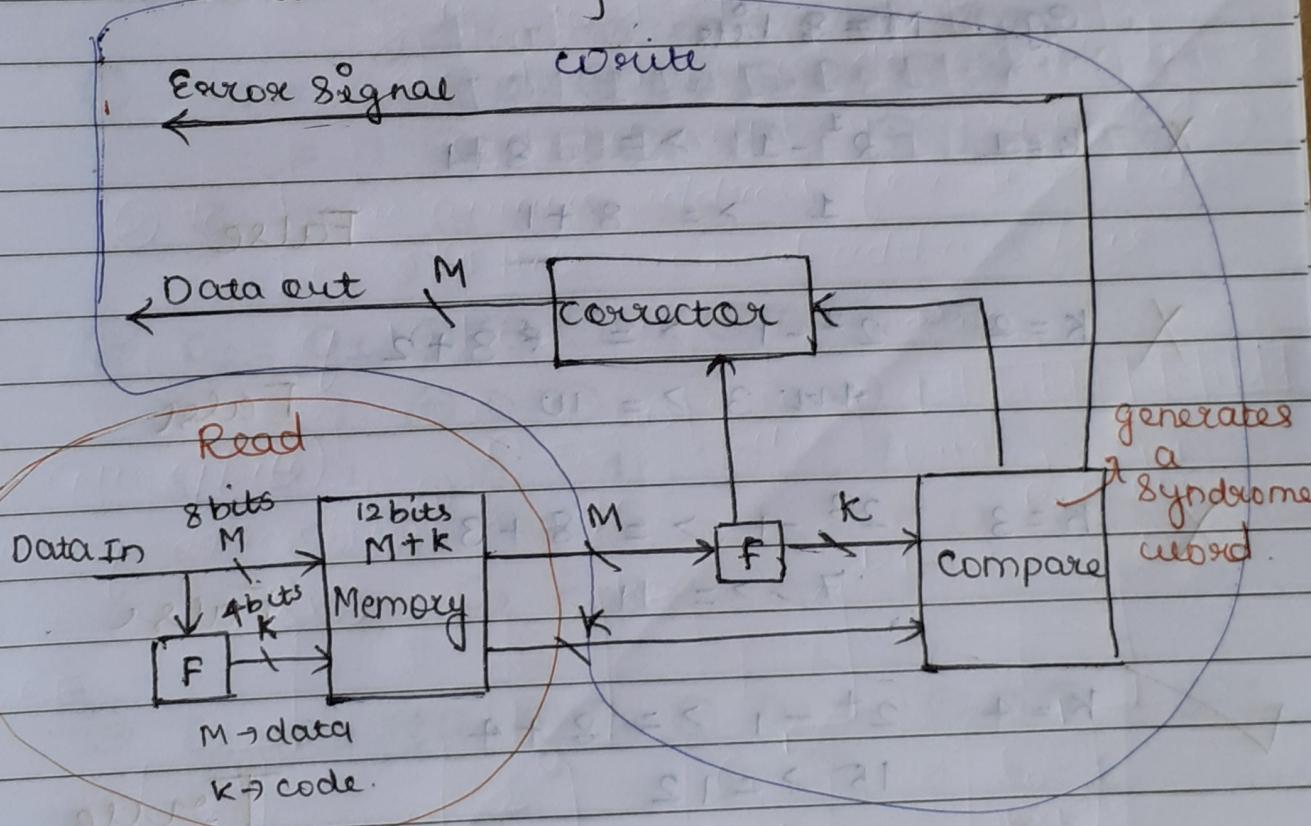
Ans $2K = 2^1 \times 2^{10} = 2^{11}$

Error Correction

- ① Hard Failure
- ② Soft Failure

→ corrected using Hamming Error detecting codes

* Error & Correcting Code function (Hamming
 Error detecting codes)



only one → correction is possible only in
 case of single bit error using
 Hamming error detecting code.

Hamming code

- * what should be the length of the code k ?
- * Result of comparison is known as the syndrome word.
- * length of the syndrome word is k bits, length of Data is " m " bits.
- * length of k should satisfy

$$2^k - 1 \geq m + k$$

e.g. $m = 8$ bits

X $k=1$ $2^1 - 1 \geq 8 + 1$
 $1 \geq 8 + 1$ False

X $k=2$ $2^2 - 1 \geq 8 + 2$
 $4 \geq 10$ False

X $k=3$ $2^3 - 1 \geq 8 + 3$
 $7 \geq 11$ False

✓ $k=4$ $2^4 - 1 \geq 8 + 4$
 $15 \geq 12$ True

Hence $k = 2$

Problem 1:

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Consider the data + check bit is as follows.

110101011101

Find out if there is an error. If so which bit is having.

Bit Position	12	11	10	9	8	7	6	5	4	3	2	1
Position Number	1100	1011	1010	1001	1000	0111	0110	0101	0100	0011	0010	0001
Data bits	D ₈	D ₇	D ₆	D ₅		D ₄	D ₃	D ₂		D ₁		
Check bits				C ₄					C ₃		C ₂	C ₁

1 1 0 1 0 1 1 0 1 1 0 1

error

considering even parity

$$\textcircled{1} \quad C_1 = D_1 \oplus D_2 \oplus D_4 \oplus D_5 \oplus D_7$$

$$1 = 1 \oplus 1 \oplus 0 \oplus 1 \oplus 1 \oplus 1 = 6$$

C₁ is correct

$$\textcircled{2} \quad C_2 = D_1 \oplus D_3 \oplus D_4 \oplus D_6 \oplus D_7$$

$$1 = 1 \oplus 0 \oplus 1 \oplus 0 \oplus 1$$

$$1 = 1 \quad 0 \quad 1 \quad 0 \quad 1$$

X C₂ has to be 1 but it is zero
Hence C₂ has error.

$$\textcircled{3} \quad C_3 = D_2 \oplus D_3 \oplus D_4 \oplus D_8 = 1 \oplus 0 \oplus 1 \oplus 1$$

$$1 = 1 \quad 0 \quad 1 \quad 1$$

C₃ = 1 hence correct.

$$\textcircled{4} \quad C_4 = D_5 \oplus D_6 \oplus D_7 \oplus D_8 = 1 \oplus 0 \oplus 1 \oplus 1$$

C₄ has to be 1 but it is 0, hence it has error.

2 bits in the syndrome has error.

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$$K = 0101 + \underline{000}$$

actually it should be 11110101

Hence

$$\begin{array}{r} 111 \\ + 0101 \\ \hline \end{array}$$

1010 → Syndrome

Two bits are set in syndrome bit

1010 value is 10

Hence the error is at bit position 10

The bit at bit position 10 needs to be changed from 0 to 1

Old Data: 110101011101

Data: 111101011101

Types of External Memory.

- Magnetic Disk

- ① RAID

- ② Removable

- Optical

- ① CD - ROM

- ② CD - Recordable (CD - R)

- ③ CD - R/W

- ④ DVD

- Magnetic Tape.

#1 RAID (Redundant Array of Independent Disks)

#2 RAID Categories

- Striping (Level 0)
- Mirroring (Level 1)
- Parallel access (Level 2, 3)
- Independent access (Level 4, 5, 6)