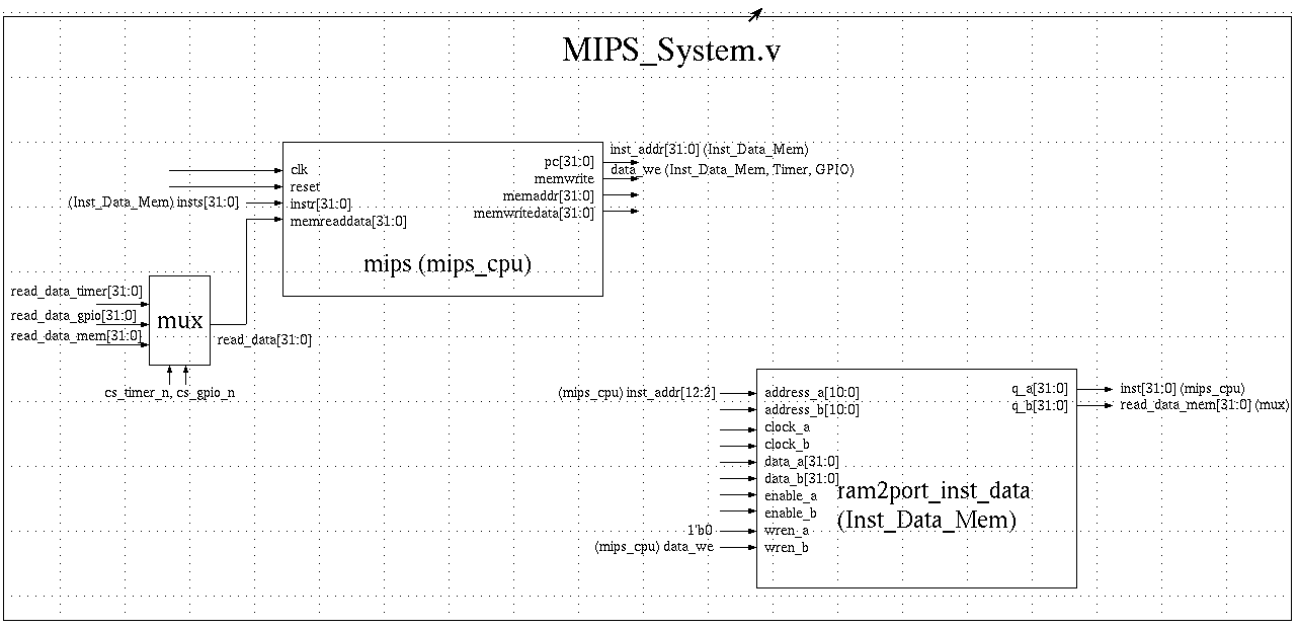
COSE222 Computer Architecture
Final Project: 2nd Milestone

No late turn-in accepted

Draw the DETAILED schematic diagram of the single-cycle RISC-V processor posted on the class web. The top module is `RV32I_System.v` and you should draw the schematic of all the hierarchy (from the top to the bottom modules). The source code is written in Verilog HDL. You may use any tool you want to use, but you should draw it manually (The RTL viewer capture of Quartus-II is NOT acceptable). Note that in the schematic diagram, you should specify all the input and output ports with the width information listed in the Verilog modules.

The schematic you draw will help you design the pipelined RISC-V (You mostly likely should have the schematic in handy throughout the final project, especially when you debug your design with ModelSim). So, while drawing the schematic, try to think why you should have the input and output ports listed in the modules, and make such connections. It would be best if you are able to draw a schematic in one page for `RV32I_System.v` and another schematic in one page for CPU (`rv32i_cpu.v`), so you can see the whole flow with bird's-eye view. Again, this will be used as your reference throughout the final project. So, try your best to make it neat!

An example schematic is below:



What and How to submit:

- Upload your drawing (pdf) to the instructed place (from TA)