Application Report
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# Electrical Transient Immunity for Power-Over-Ethernet

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**ABSTRACT**

Electrical overstresses can cause failure, permanent degradation, or temporary erratic behavior of electronic devices or systems. The trend to reduce circuit geometries for communication systems and applications results in an increasing sensitivity to such electrical transients. The suppression of these transients can be a challenge to designers because the origin and severity of the overvoltage may be unknown.

To assist designers in coping with these issues, this application report defines simple design rules that can adequately protect the sensitive electronic parts of the system with cost-effective solutions.

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# 1 Introduction

Electrical overstresses can cause failure, permanent degradation, or temporary erratic behavior of electronic devices or systems. The trend to reduce circuit geometries for communication systems and applications results in an increasing sensitivity to such electrical transients. The suppression of these transients can be a challenge to designers because the origin and severity of the overvoltage may be unknown.

When designing an electronic circuit or when defining a complete system, it is important to identify the sources of those stresses and have a correct understanding of their mechanism, for a defined environment in which the system will operate. In so doing, it is possible to define simple design rules that can adequately protect the sensitive electronic parts of the system with cost-effective solutions

This application report discusses the Ethernet network application, specifically Power-over-Ethernet (PoE) equipment which provides power to Ethernet remote equipment or powered device (PD) through the data cable (see Figure 1).

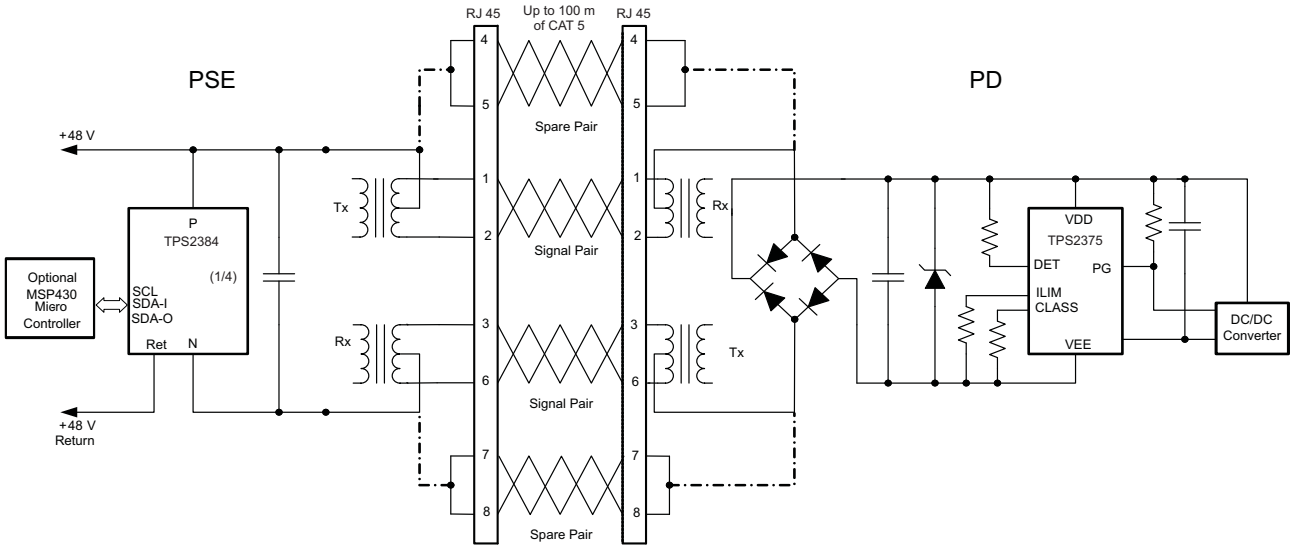



**Figure 1. Typical PoE Application Diagram**

In a PoE application, the environment can range from offices to industrial networks. Installations of Ethernet cables and/or equipment are located mostly indoors, but in some applications part of the installation can be outdoors.

Many standards have been developed to simulate or represent the transient overvoltage environment in various applications, including telecom and industrial. For example, per IEC transient immunity standards, the transients can be classified into three categories:

- IEC 61000-4-2: Electrostatic Discharge (ESD)
- IEC 61000-4-4: Electrical Fast Transient/Burst (EFT)
- IEC 61000-4-5: Surges

These IEC standards also define immunity test methods applicable to each transient category. They provide to manufacturers of transient suppression components some standardized waveforms and overvoltage levels to which their components can be characterized and specified.

## 2 ESD

ESD (electrostatic discharge) results from conditions which allow the build up of electrical charge from contact and separation of two nonconductive materials, followed by the release of the corresponding energy when the charged body is brought into proximity to another object of lower potential. For example, a person walking across a carpet can charge to over 15 kV.

ESD is first of all a common-mode electrical event; normally, ESD is a discharge from one unit to the chassis ground. One important design guideline is to clearly identify the path that is taken by the current and to ensure that this is not harmful to sensitive circuitry. It is even better to provide an alternate path for the discharge current to bypass this sensitive circuitry.

The IEC 61000-4-2 standard simulates an ESD event of a human holding a metal implement, referred to as the Human/Metal Model. Discharge into equipment can be through direct contact (contact discharge) or through proximity (air discharge).

The test levels of this model are listed in Table 1. A diagram showing the ESD waveform is presented in Figure 2.The waveform parameters of the ESD generator in contact mode are summarized in Table 2. The rise time can be expected to be less than 1 ns, which is extremely fast. The total duration of the current pulse is around 150 ns.

**Table 1. IEC61000-4-2 Test Levels**

| CONTACT DISCHARGE | | AIR DISCHARGE | |
|---|---|---|---|
| LEVEL | TEST VOLTAGE (kV) | LEVEL | TEST VOLTAGE (kV) |
| 1 | 2 | 1 | 2 |
| 2 | 4 | 2 | 4 |
| 3 | 6 | 3 | 8 |
| 4 | 8 | 4 | 15 |

**Table 2. IEC61000-4-2 Waveform Parameters**

| LEVEL | INDICATED VOLTAGE (kV) | FIRST PEAK CURRENT OF DISCHARGE (A) | RISE TIME tr WITH DISCHARGE SWITCH (ns) | CURRENT AT 30 ns (A) | CURRENT AT 60 ns (A) |
|---|---|---|---|---|---|
| 1 | 2 | 7.5 | 0.7 to 1 | 4 | 2 |
| 2 | 4 | 15 | 0.7 to 1 | 8 | 4 |
| 3 | 6 | 22.5 | 0.7 to 1 | 12 | 6 |
| 4 | 8 | 30 | 0.7 to 1 | 16 | 8 |

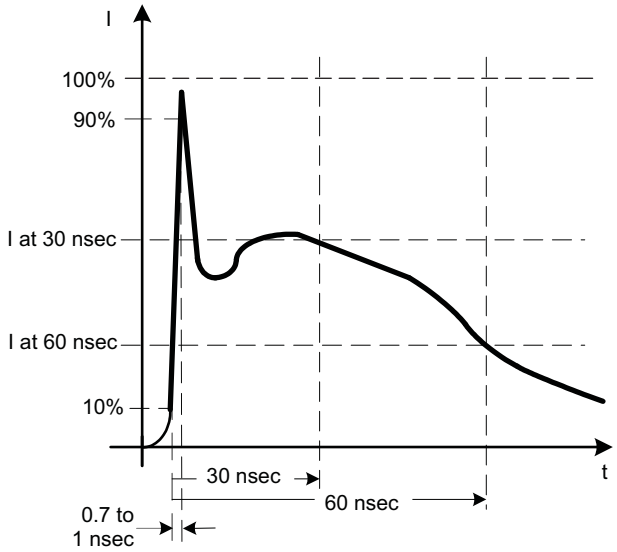



**Figure 2. Typical Waveform of Output Current of ESD Generator**

Another threat is identified as a cable discharge event (CDE). For example, this occurs when an Ethernet cable becomes charged and then is discharged into a circuit when the cable is connected to it. The cable could be charged primarily due to tribocharging (e.g., by dragging it on the carpet) or induction (e.g., from a charged person holding it).

A standard to define a cable discharge event with test method has yet to be established, but most manufacturers use internal CDE test setups to evaluate their designs; a few deem it sufficient to test to the IEC Level-4 specifications to protect against such discharges.

**Note:** The idea of the equipment being able to withstand CDE if it passes IEC 61000-4-2 Level-4 discharges is not always correct. This is because the charged capacitances in the two tests are different, which is 150 pF for IEC ESD versus much larger capacitance depending on the length of the cable involved for CDE and the cable elevation over the earth GND. There is also a transmission line effect with some distributed capacitance as opposed to a lumped capacitance. CDE discharges typically dump more energy than IEC Level-4 discharges into the equipment under test.

## 3 EFT

EFT (electrical fast transient) occurs as a result of arcing contacts in switches and relays, with motors and other inductive loads, which is common in industrial environments. This type of transient is normally of common-mode type and is introduced on telecommunication cables by capacitive coupling.

IEC 61000-4-4 defines this transient as a burst of fast and high-voltage spikes at a repetition rate of 5 kHz or 100 kHz. A diagram showing the EFT waveform, the EFT burst repetition rate, and burst period is presented in Figure 3 and Figure 4. Also, the voltage and current characteristics of the EFT burst generator are summarized in Table 3. Short-circuit current values are estimated by dividing the open-circuit voltage by the 50-Ω source impedance.

**Table 3. IEC61000-4-4 Severity Test Levels**

| Open-Circuit Output Test Voltage, Short-Circuit Current, and Repetition Rate of the Impulses | | | | | |
|---|---|---|---|---|---|
| **LEVEL** | **POWER-SUPPLY PORT** | | **I/O SIGNAL, DATA, AND CONTROL PORTS** | | |
| | **OPEN-CIRCUIT VOLTAGE PEAK (kV)** | **SHORT-CIRCUIT CURRENT PEAK (A)** | **OPEN-CIRCUIT VOLTAGE PEAK (kV)** | **SHORT-CIRCUIT CURRENT PEAK (A)** | **REPETITION RATE (kHz)** |
| 1 | 0.5 | 10 | 0.25 | 5 | 5 or 100 |
| 2 | 1 | 20 | 0.5 | 10 | 5 or 100 |
| 3 | 2 | 40 | 1 | 20 | 5 or 100 |
| 4 | 4 | 80 | 2 | 40 | 5 or 100 |

It is worth noting that even though it is a power signal that is transmitted on the PoE cable, this transmission is still on a communication data cable, which means that it is considered as such when installed and used. Consequently, it belongs to the I/O signal, data, and control ports category.

The following equation gives a good approximation of the EFT voltage waveform:

$$V_{EFT}(t) = A \times V_p \times \left(1 - \exp\left(\frac{-t}{\tau_1}\right)\right) \times \exp\left(\frac{-t}{\tau_2}\right) \quad (1)$$

with:

$A = 1.270 \qquad \tau_1 = 3.5\ ns \qquad \tau_2 = 55.6\ ns$

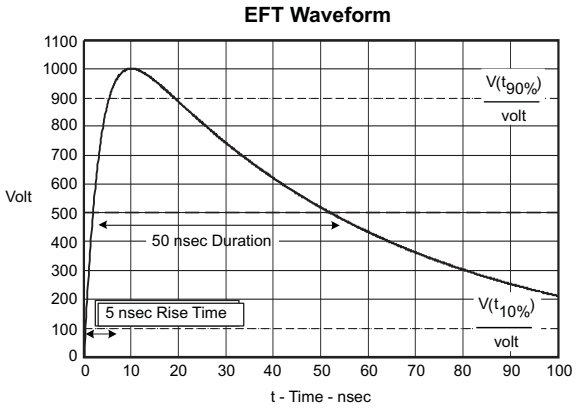



**Figure 3. Voltage of EFT Into 50-Ω Load**

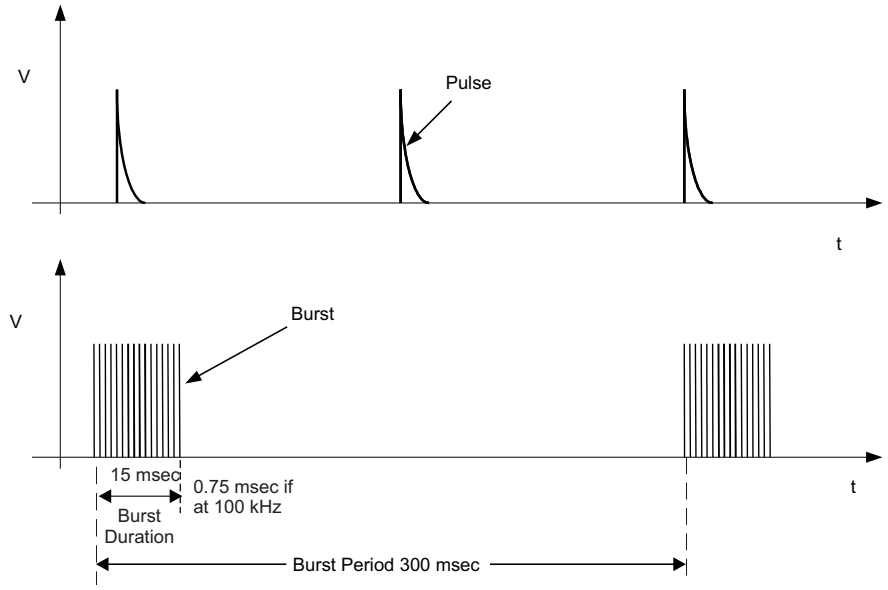



**Figure 4. General Graph of EFT (Fast Transient/Burst)**

Per IEC61000-4-4, a capacitive coupling clamp over the communication cable is the preferred method for coupling the test voltage in communication ports, and this includes an Ethernet cable. This means that the coupling is done without any galvanic connection to the port.

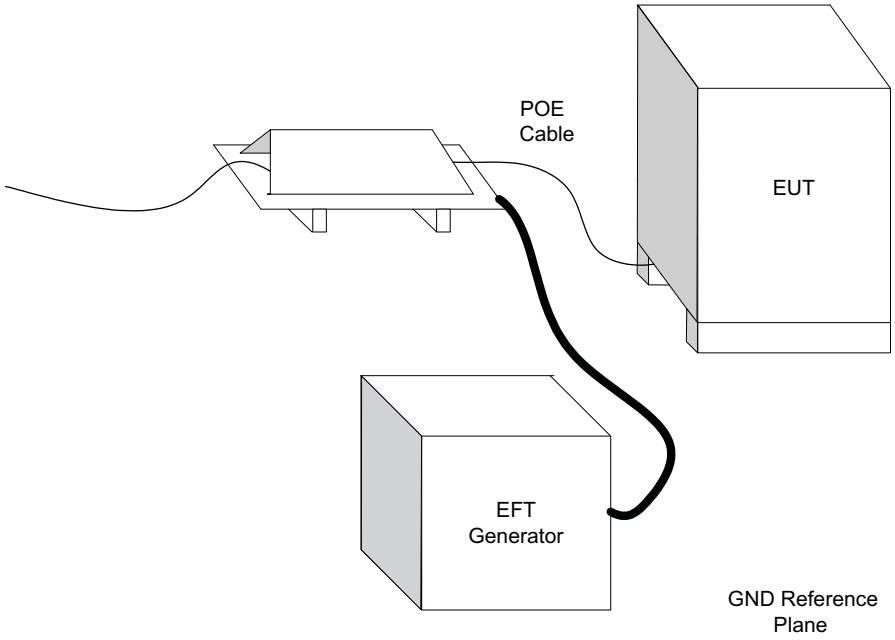



**Figure 5. EFT Test Setup**

Another acceptable means is directly through a 100-pF discrete capacitor.

It is worth noting that because of their repetitive nature, EFT events can also result in erratic behavior of a communication system.

## 4 Electrical Surge

These transients are the most severe of all, in terms of peak current and duration, although they are the least severe in terms of rate of rise. They are caused by lightning strikes (direct strike or induced voltages and currents due to an indirect strike) and switching on power systems (also includes load changes and short circuit). The degree of severity of the transient can change depending on if the cable installation is inside or outside the building.

This type of transient is either of common-mode type or differential-mode type. It is introduced on telecommunication cables by capacitive or magnetic coupling. Remember that in PoE applications, the DC power is transmitted by using both wires of each transmit and receive pair which means, for example, that the positive P-side of DC voltage could be on the TX pair while the return N-side would be on the RX pair. On a twisted-pairs cable, the two wires of each pair are twisted together, but there is no twisting between pairs at all (in fact, each pair is well separated from its neighbors). Consequently, a differential-mode transient between P and N is likely with that type of cable, and this tandem of pairs can be considered as an unbalanced line as far as the test voltages are concerned.

IEC 61000-4-5 defines this transient as two surge waveforms: the 1.2 × 50-µs open-circuit voltage waveform and the 8 × 20-µs short-circuit current waveform. See Figure 6, Figure 7, and Table 4.

The following equation gives a good approximation of the surge short-circuit current waveform:

$$I_{surge}(t) = Ai \times I_p \times t^3 \times \exp\left(\frac{-t}{\tau}\right)$$

with:

$$\tau = 3.911 \times \mu s \qquad Ai = \frac{0.01243}{\mu s^3} \tag{2}$$

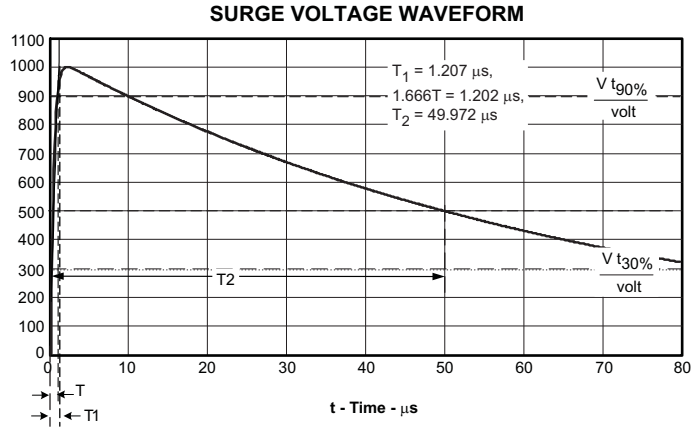



**Figure 6. Typical Waveform of Open-Circuit Voltage of Surge Generator When Set to 1-kV Peak**

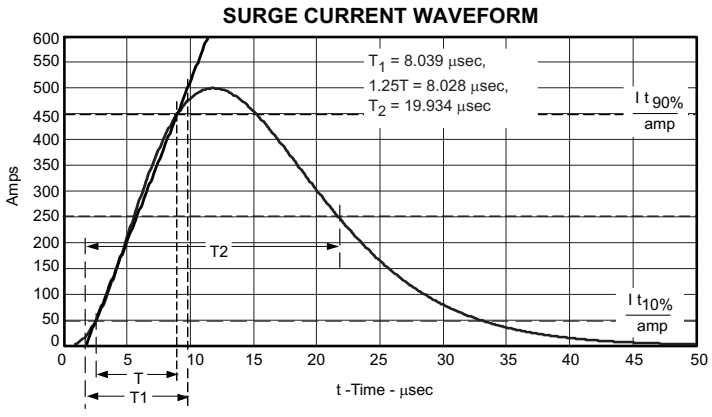



**Figure 7. Typical Waveform of Short-Circuit Current of Surge Generator When Set to 1-kV Peak with 2-Ω Source Impedance**

**Table 4. IEC 61000-4-5 Severity Levels**

| | | TEST LEVELS | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| INSTALL CLASS | | POWER-SUPPLY | | UNBALANCED OPERATED CIRCUITS/LINES, LONG DISTANCE BUS | | BALANCED OPERATED CIRCUITS/LINES | | SHORT DISTANCE DATA BUS (Less Than 30 m) | |
| | | COUPLING MODE | | COUPLING MODE | | COUPLING MODE | | | |
| | | Line to Line Zs = 2 Ω | L8ine to GND Zs = 12 Ω | Line to Line Zs = 42 Ω | Line to GND Zs = 42 Ω | Line to Line Zs = 42 Ω | Line to GND Zs = 42 Ω | Line to Line Zs = 42 Ω | Line to GND Zs = 42 Ω |
| 1 | Voltage | N/A | 0.5 kV | N/A | 0.5 kV | N/A | 0.5 kV | N/A | N/A |
| | Current | | 42 A | | 12 A | | 12 A | | |
| 2 | Voltage | 0.5 kV | 1.0 kV | 0.5 kV | 1.0 kV | N/A | 1.0 kV | N/A | 0.5 kV |
| | Current | 250 A | 83 A | 12 A | 24 A | | 24 A | | 12 A |
| 3 | Voltage | 1.0 kV | 2.0 kV | 1.0 kV | 2.0 kV | N/A | 2.0 kV | N/A | N/A |
| | Current | 500 A | 167 A | 24 A | 48 A | | 48 A | | |
| 4 | Voltage | 2.0 kV | 4.0 kV | 2.0 kV | 4.0 kV | N/A | 2.0 kV | N/A | N/A |
| | Current | 1 kA | 333 A | 48 A | 95 A | | 48 A | | |
| 5 | Voltage | Depends on class of local power supply system | | 2.0 kV | 4.0 kV | N/A | 4.0 kV | N/A | N/A |
| | Current | | | 48 A | 95 A | | 95 A | | |

IEC 61000-4-5 classes 3 to 5 are applicable to outdoor applications and higher threat-level conditions. In the majority of PoE applications, only indoor cable installation (office environment) is considered. Also, the IEEE 802.3 requires the networks to withstand a 1500-V dielectric test to earth. As a result, only Class 2 (semi-protected environments) is applicable.

Also, for an Ethernet cable used for PoE, the categories applicable are the unbalanced and balanced circuits/lines. Note that for a balanced line, there is no explicit line-to-line test, but this is implicitly done with a line-to-GND test setup using coupling through arrestors instead of capacitors; this setup is such that it does not influence the specified functional condition of the circuit to be tested.

Other possible standards are the ITU-T recommendations K.20, K.21, K.44, and K.45, and in some cases the GR-1089-CORE (intra-building lightning surge specification).

Another typical telecommunication standard is the 10/700-µs voltage waveform. This standard is not applicable for Ethernet networks because it only applies in situations of long-distance telecommunication signal lines, with both indoor and outdoor installation.

## 5 Transients Protection Circuit Guidelines

Many guidelines apply to voltage transients protection for electronic systems. The following is a list of some practical rules along with circuits design strategies.

- The source of transient voltage can be of differential- or common-mode type or both.
- The main categories of protection techniques against transient voltages are shielding and grounding, filtering, isolation, and nonlinear devices.
- A well-designed circuit protection interface is normally the result of a good combination of blocking and diverting techniques.
- The selected voltage suppressor must have the speed/robustness (short-circuit current and waveform) required for the application. Shunt (line-to-earth GND) capacitors that may take direct transient hits should be rated for high voltage (≥ 2 kV). These capacitors must also have the following characteristics: low ESR at high frequency and low parasitic inductance.
- The protection circuit should not interfere with the normal behavior of the circuitry to be protected.
- The protection circuit should be able to prevent any voltage transient from causing an erratic (repetitive or not) behavior of the complete system. EFT is an example. Use common-mode chokes when

necessary.

- The basic rules of circuit layout design are:
  - Define a low-impedance path that diverts any transient current/voltage away from sensitive components. Do not let ESD find its way to earth GND by itself.
  - Have a good, solid, and low-impedance earth ground connection onboard.
  - Keep the transient current density and the current path impedances as low as possible by using multipoint grounds where the current is designed to flow, and single-point grounds where it is not.
  - The loop within which the fast-rising currents have to circulate must be a small area. For fast transients, use local ceramic capacitors whenever necessary, particularly when clamping diodes to a power-supply rail are used. See Figure 20.
  - Create physical separation between high-voltage/current transients area, in close proximity to I/O connectors, and the sensitive circuitry. The high-current suppressors must be located in that I/O area, as well as the switches, LEDs, and displays
  - Put all the connectors on one edge of the circuit, if possible. Place sensitive circuitry at the center of the printed-circuit board, if possible.
  - Route each protected signal from the suppressor to the sensitive circuitry in parallel with its individual return signal in order to prevent any inadvertent transformer effect.
  - Use surface-mount package for suppressors. Use 4-terminal connection type in order to mitigate parasitic inductance effect. See Figure 8 and Figure 20.
  - Mitigate parasitic capacitances bypassing blocking series elements. However, having parasitic inductance in series with blocking elements is not a problem.

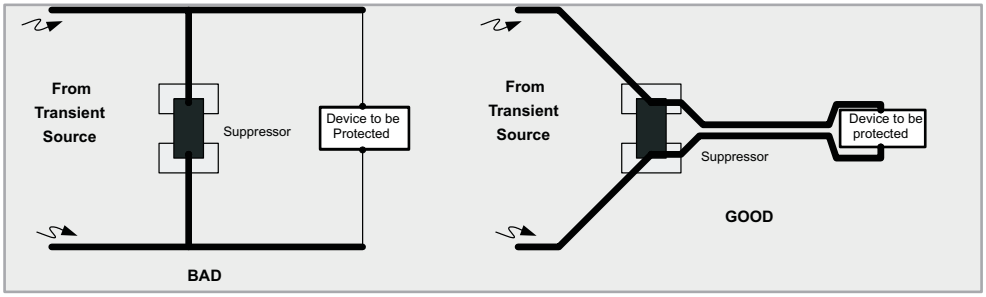



**Figure 8. Interconnection of Transient Voltage Suppressor on Printed-Circuit Board**

## 6 Circuit Protection Solutions for PoE

Only secondary protection, usually deployed within the equipment to be protected, is discussed in this document. However, it is worth noting that where telecommunication cable is run outside, primary telecommunication protectors (PTC thermistors, SIDACtors, etc.) must be deployed at points where exposed twisted pairs enter a building or residence.

In a PoE application, the PSE (power source equipment) is powered from a 48-V power supply, which normally has some common-mode capacitances connected to earth ground; those capacitances can be either discrete capacitors and/or capacitance between layers in the printed-circuit board.

Therefore, because the PSE is not really floating, any common-mode voltage transient applied on the data connector can result in a voltage breakdown of PSE components, and particularly the PSE port power switch.

Figure 9 presents an example of the effect of such a transient, along with the high-current path which results in the destruction of the PSE power switch when no appropriate protection is implemented. C_CM represents the capacitance between the 48-V lines and chassis GND. Such capacitance can be either on the + or – line of the 48 V, but in order to simplify the illustration, C_CM is shown only on the – line. The configuration shown is applicable when the AC disconnect circuitry is used, which requires the use of D1. This is the worst case for transient protection.

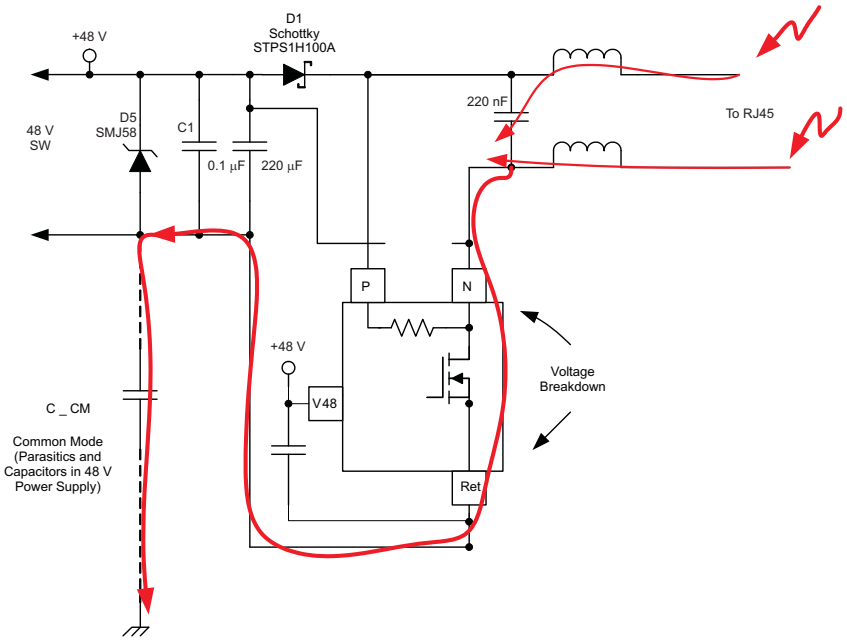



**Figure 9. Effect of ESD/EFT on PSE Power Switch When There is no Protection Circuitry**

In general, the categories of protection techniques against transient voltages are:

- Shielding and grounding
- Filters: capacitors, inductors, ferrite beads, chokes, etc.
- Nonlinear devices, including clamping diodes, TVSs, varistors, etc.
- Isolation

In an actual application, where RJ-45 cables are used, cable shielding is usually not an available solution.

The following solution is proposed in order to adequately protect the PSE integrated circuit. See Figure 10. This configuration is applicable when the AC disconnect circuitry is used. If this is not the case, then D1 and D3 are not used.

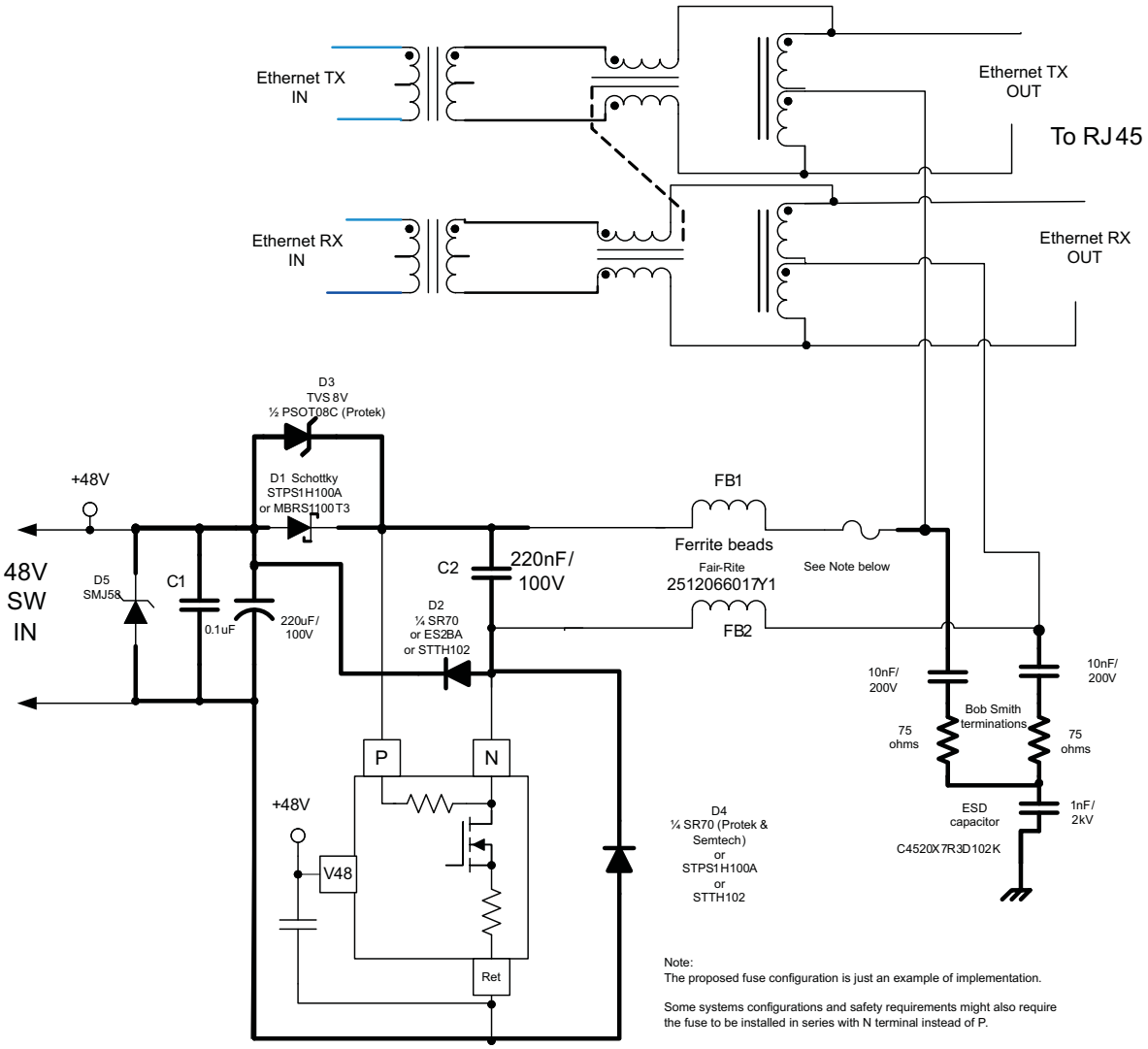



**Figure 10. Basic Circuit With Transient Protection**

The major elements of this protection circuit are:

- Clamping diodes D2 and D4: key parameters are the forward recovery time and capability to handle transient currents for a specific duration, as mentioned in the previous ESD, EFT, and surges sections. The resultant forward voltage transient must be acceptable. Within the selected diodes, the SR70 has the additional advantage of a small package.
- TVS D3: key parameters are response time and current-handling capability along with low impedance. D3 is required only if D1 is used (for AC disconnect function).
- Note: If the application requires the consideration of more severe surges like the ones defined in the GR-1089-CORE (intra-building lightning surge specification) standard, it is recommended to use the STPS1H100A or STTH102 for D2 and D4 and a 1500-W TVS (SMCG8.0, for example) for D3, which are more robust.
- Schottky diode D1: using a Schottky provides a fast protection against negative voltage transients, in addition to improving efficiency of the PSE.
- Bob Smith terminations or line-to-GND capacitors: the initial ESD/EFT transient hits circulate through those terminations to earth ground.
- Ferrite beads: these provide blocking impedance.
  - The main function of the ferrite beads is to provide isolation at high frequency between the Bob Smith terminations and the internal capacitor placed between P and N. Without these beads, the

terminations might not work correctly.
  - The ferrite beads also play an important role against ESD.
- Fuse:
  - Note that the fuse must be selected so it will withstand, without opening, the energy associated to the normal transients. The worst case happens during a surge event applied in differential from N to P. In this case, the $I^2t$ can reach $10 \times 10^{-3}$ $A^2$ sec within 35 µs. A good design rule is to select a fuse with ensured capacity of at least 2 times that $I^2t$.
  - Also, some systems configurations and/or safety requirements might also require the fuse to be installed in series with the N-terminal instead of the P-terminal.
- Decoupling capacitor (100 nF) on 48-V bus and on PN: these must be low-impedance ceramic types. It is important to locate C1 close to the clamping diodes and preferably use one such capacitor per group of two (or perhaps four) ports. Also important is the location of C2 in close proximity to the same circuitry.
- TVS on input 48-V bus: this TVS is normally located close to the 48-V input connector, as well as the 220- µF.
- All the components selected feature a surface-mount package for low parasitic inductance.

As can be seen, the protection components keep any transient current from flowing through the N-to-RTN or the P-to-RTN of the IC, in either positive or negative polarity.

However, those transient currents may follow different paths depending on the source of the transient. This is illustrated from Figure 11 to Figure 14.

The case of ESD or EFT, which are fast and common-mode events, is illustrated in Figure 11 and Figure 12. The case of surges, which are much slower, is illustrated in Figure 13 and Figure 14; both common and differential (between P and N pairs) mode surges are handled by the circuitry although only the first (common-mode) type is illustrated.

One interesting point is that the DC voltage levels on C1 and C2 just prior to the transient event directly effect the paths that those transient currents follow.

For example, with a negative EFT event on N while the PSE power switch is OFF, consider the following scenarios:

- In all scenarios, at the beginning of every EFT pulse, the current circulates for a short time in the Bob Smith termination.
- If the 56-V power supply is ON just prior to the event: the transient current only circulates through the path of D1, C1, and C2, and does not circulate at all through the clamping diode D4.
- If the 56-V power supply is OFF but still connected and if C2 is not charged: during the first EFT pulses of that event, the current circulates through D1, C1, and C2. The capacitor C2 accumulates some charge, and its voltage increases from one EFT pulse to the next one.
- If the 56-V power supply is OFF but still connected and if C2 is charged to a certain level: the current follows two paths depending on the voltage accumulated in C2, and from one EFT pulse to the next one, the C2 path takes a higher proportion of that current.
- This is illustrated at the left in Figure 12. Simulation results are also shown in Figure 15 to Figure 17.

Simulation results in Figure 18 also show a similar behavior but with a surge, which is much slower than EFT.

On ESD or EFT simulations, it is clear that the BS termination, along with the ferrite beads, play an important role in ESD/EFT suppression. BS terminations are first of all used for EMC reasons. The pair-to-pair relationship of a Cat-5 cable form transmission lines in themselves, which need BS terminations in order to avoid multiple reflections and standing wave problems. Secondly, those terminations clearly define the first path that an ESD or EFT strike will follow. Note that substituting BS terminations with capacitors to chassis ground without any series matching (or damping) resistor results in a low pair-to-pair matching impedance which might result in even stronger EMC problems.

It is interesting to note that for the mentioned threat levels and based on simulation results, the maximum possible voltage on a line-to-earth GND capacitor is approximately 1 kV; so, a 2-kV-rated capacitor is a safe choice. Simulations indicate that with 8-kV ESD applied and with a150pF/330-Ω human/metal model, the resultant voltage on the 1 nF of the Bob Smith termination is less than 100 V. The worst-case high voltage on this capacitor occurs during the surge test which is at 1 kV for Class-2. Similarly, a 200-V rating for the 10 nF is a safe choice.

Tests have been performed with the clamp diodes plus Bob Smith termination and ferrite beads. The results have been satisfactory and demonstrate that the TPS2384 and its circuitry can tolerate some forward voltage drop on D2 and D4 while supporting high transient currents. Examples of suggested board layouts are shown in Figure 19 and Figure 21.

Note that the optional common mode choke can be used in situations where EFT events cause erratic behavior of the system. In order for this choke to be effective, all signals have to pass through it, which means the Ps, Ns, the 48 V and the GND connection.

Clearly, the following components and the connectors (power input and RJ-45) must be close together in order to keep the area of the transient current loop (and its impedance) as small as possible: D2, D4, D3, D1, C1, and C2.

For example, the effectiveness of the clamping diode D2 is greatly reduced if C1 is not located nearby in ESD or EFT application.

In applications with multiple ports, it is recommended to have one such C1 per group of ports (preferably two or four) and to place it physically close to its group of components.

It is also important to provide sufficient copper area for the suppressor device in order to facilitate heatsinking.

Note that Ethernet interface circuitry usually also requires data line protectors for the data line driver circuitry. However, this discussion has mainly focused on protection techniques applicable to Power-Over-Ethernet circuitry.

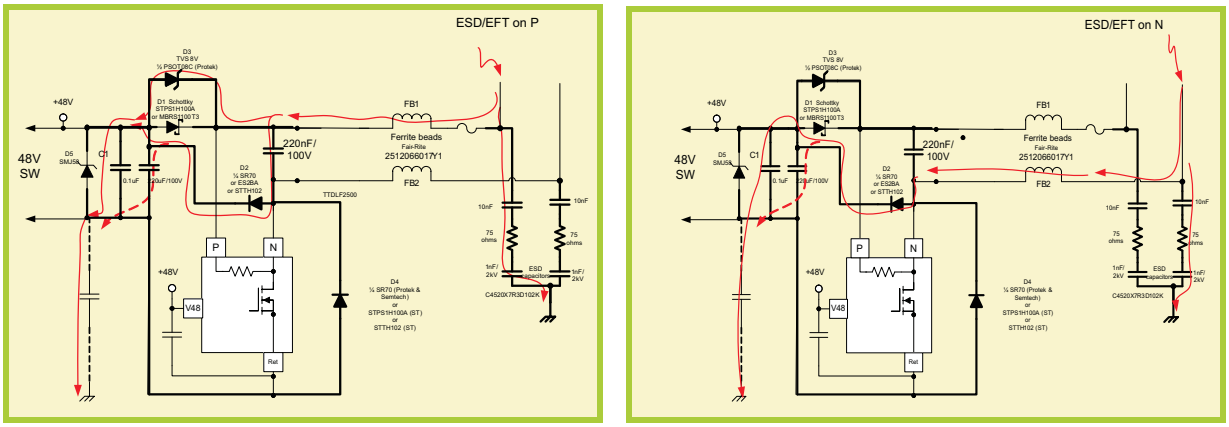



**Figure 11. Current Path in Positive Polarity ESD/EFT Event Common Mode: Line-to-GND**

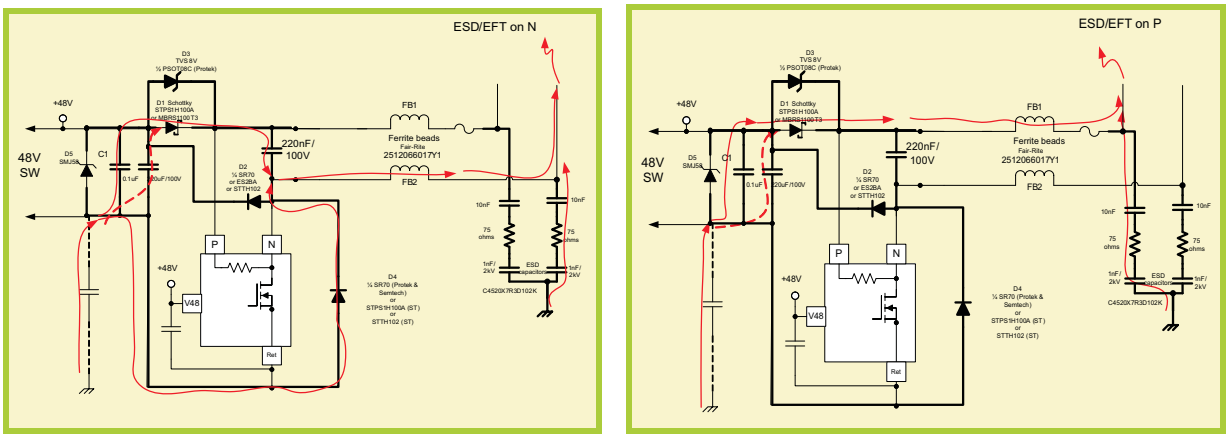



**Figure 12. Current Path in Negative Polarity ESD/EFT Event Common Mode: Line-to-GND**

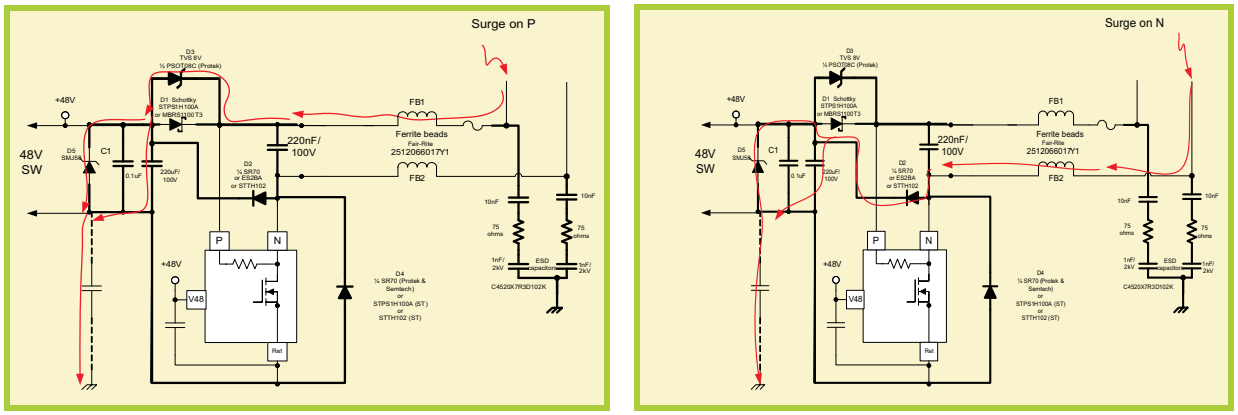



**Figure 13. Current Path in Positive Polarity Surge Event Common Mode: Line-to-GND**

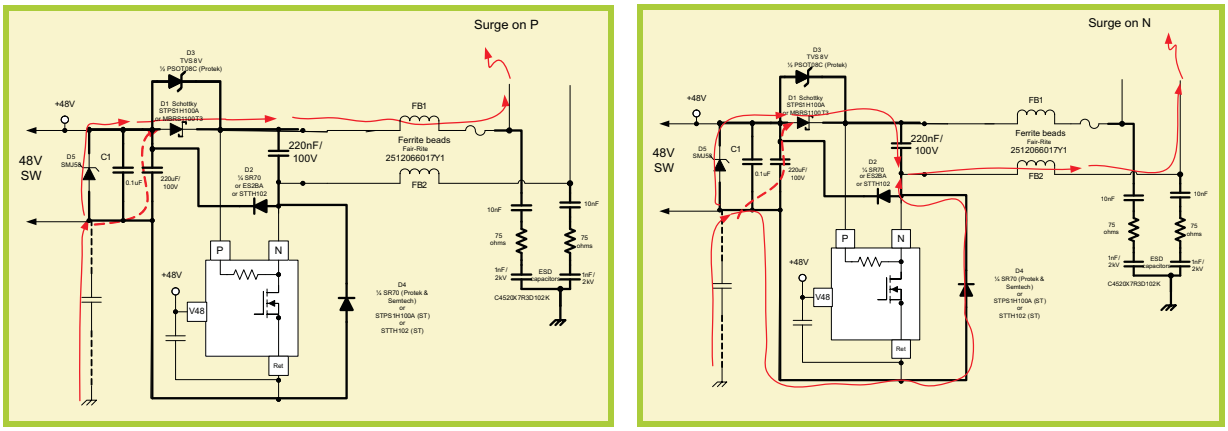
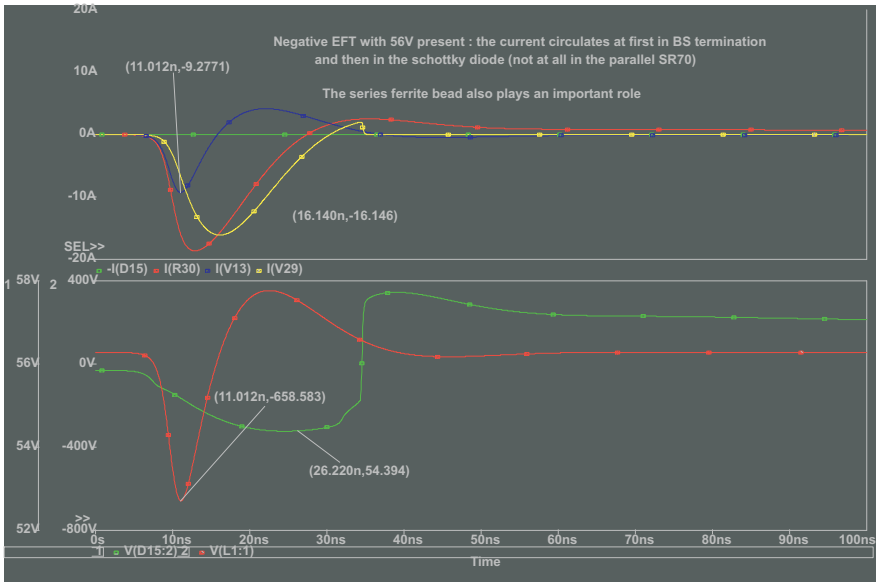
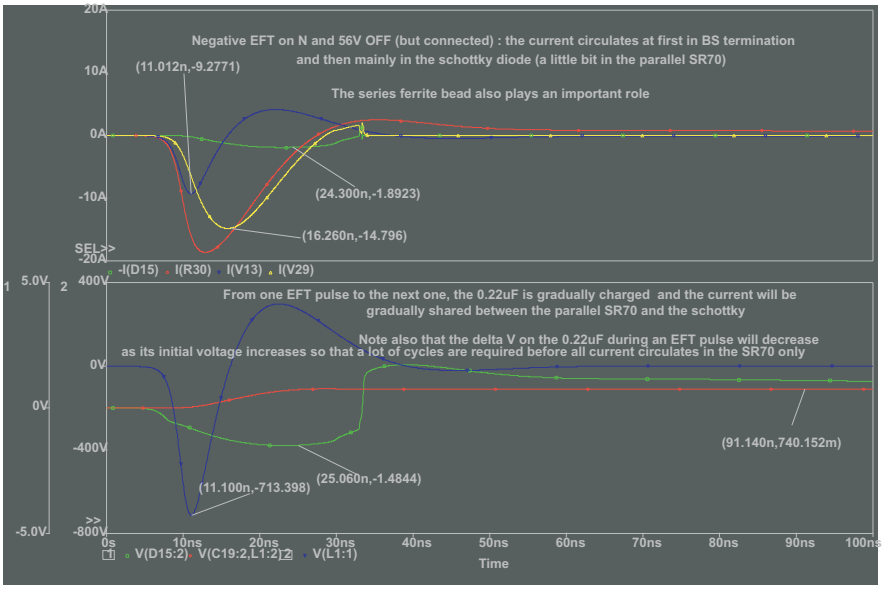



**Figure 14. Current Path in Negative Polarity Surge Event Common Mode: Line-to-GND**



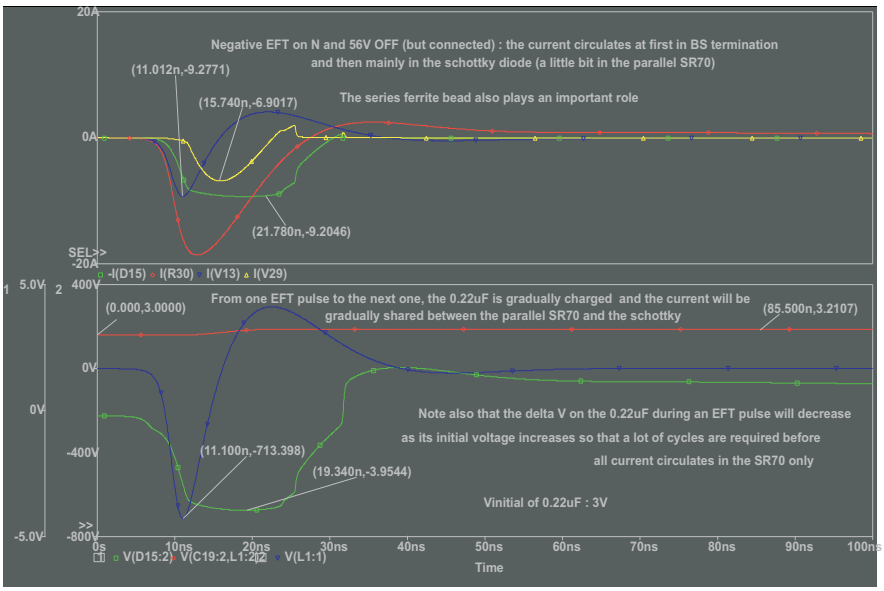

NOTE: **Upper graph:** BS termination current (blue), upper SR70 diode current (green), Schottky diode current (yellow)
**Lower graph:** N (drain) terminal voltage of PSE power switch (green), BS termination voltage (red)

**Figure 15. Negative EFT Simulation on N Terminal With 56V Power Supply ON**



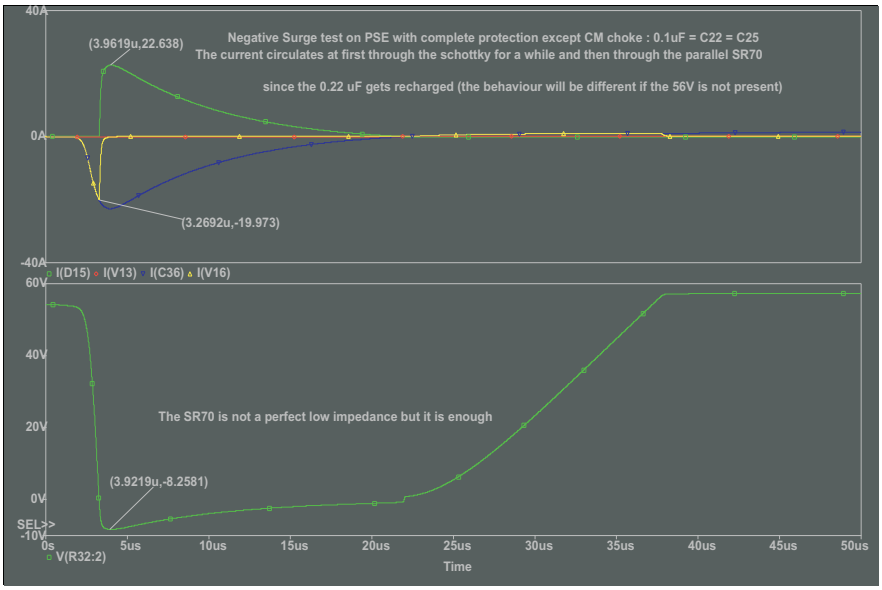

NOTE: **Upper graph:** BS termination current (blue), upper SR70 diode current (green), Schottky diode current (yellow)
**Lower graph:** voltage on N (drain) terminal of PSE power switch (green), voltage on capacitor C2 (across P and N) (red), BS termination voltage (blue).

**Figure 16. Negative EFT Simulation on N Terminal With 56V Power Supply OFF**




NOTE: **Upper graph:** BS termination current (blue), upper SR70 diode current (green), Schottky diode current (yellow)
**Lower graph:** voltage on N (drain) terminal of PSE power switch (green), voltage on capacitor C2 (across P and N) (red), BS termination voltage (blue)

**Figure 17. Negative EFT Simulation on N Terminal With 56V Power Supply OFF and With 3V Initially on C2**




**Upper graph:** lower SR70 diode current (green), Schottky diode current (yellow)
**Lower graph:** voltage on N (drain) terminal of PSE power switch (green)

**Figure 18. Negative Surge Simulation on N Terminal With 56 V Power Supply ON**

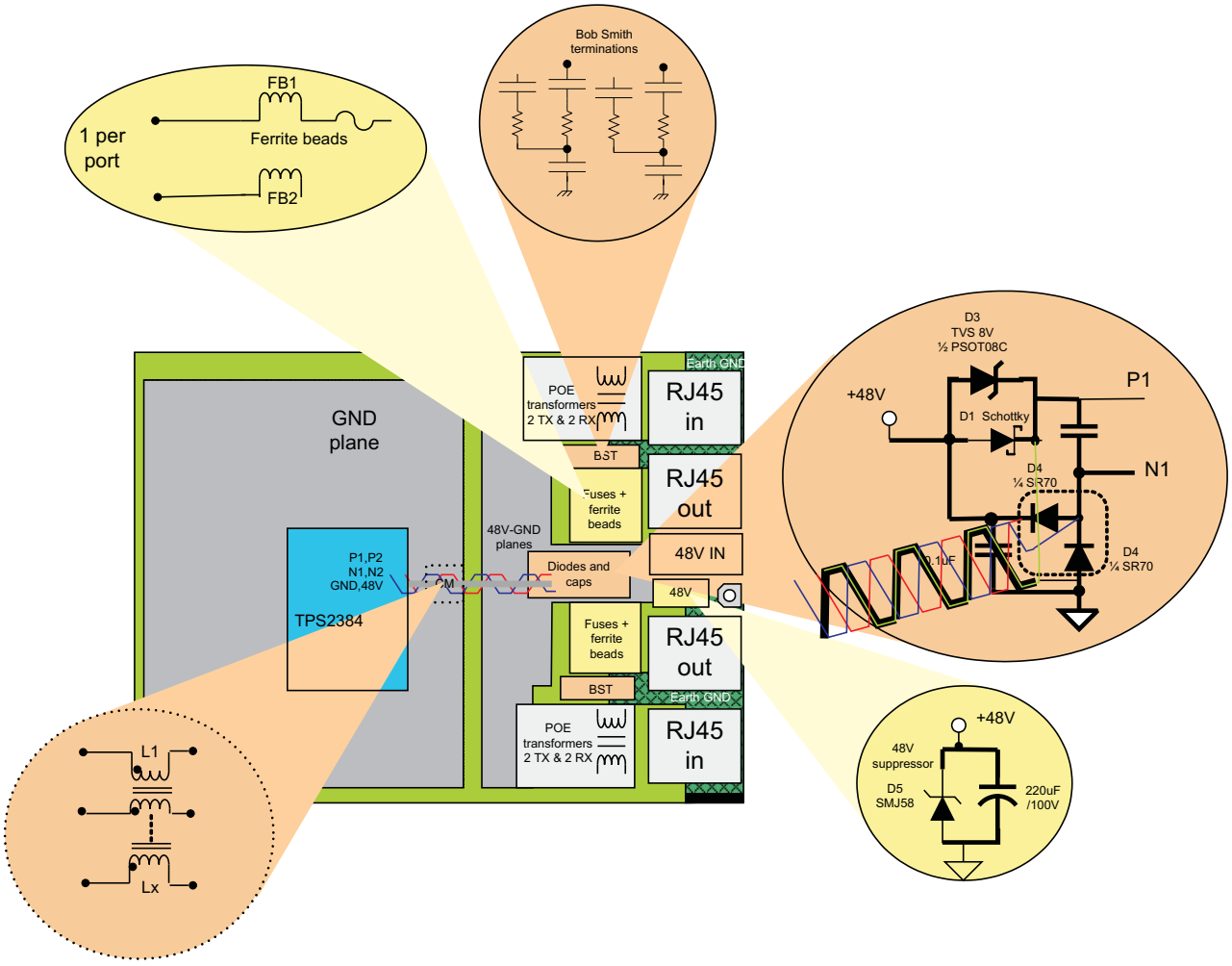



**Figure 19. Layout for a Dual Port PSE**

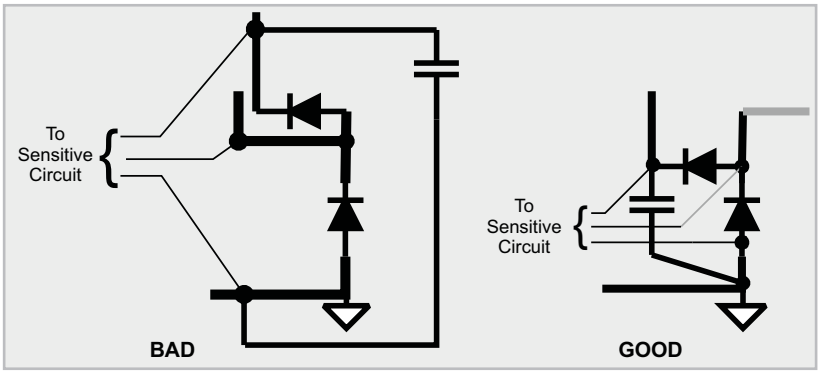



**Figure 20. Interconnection to Clamping Devices**

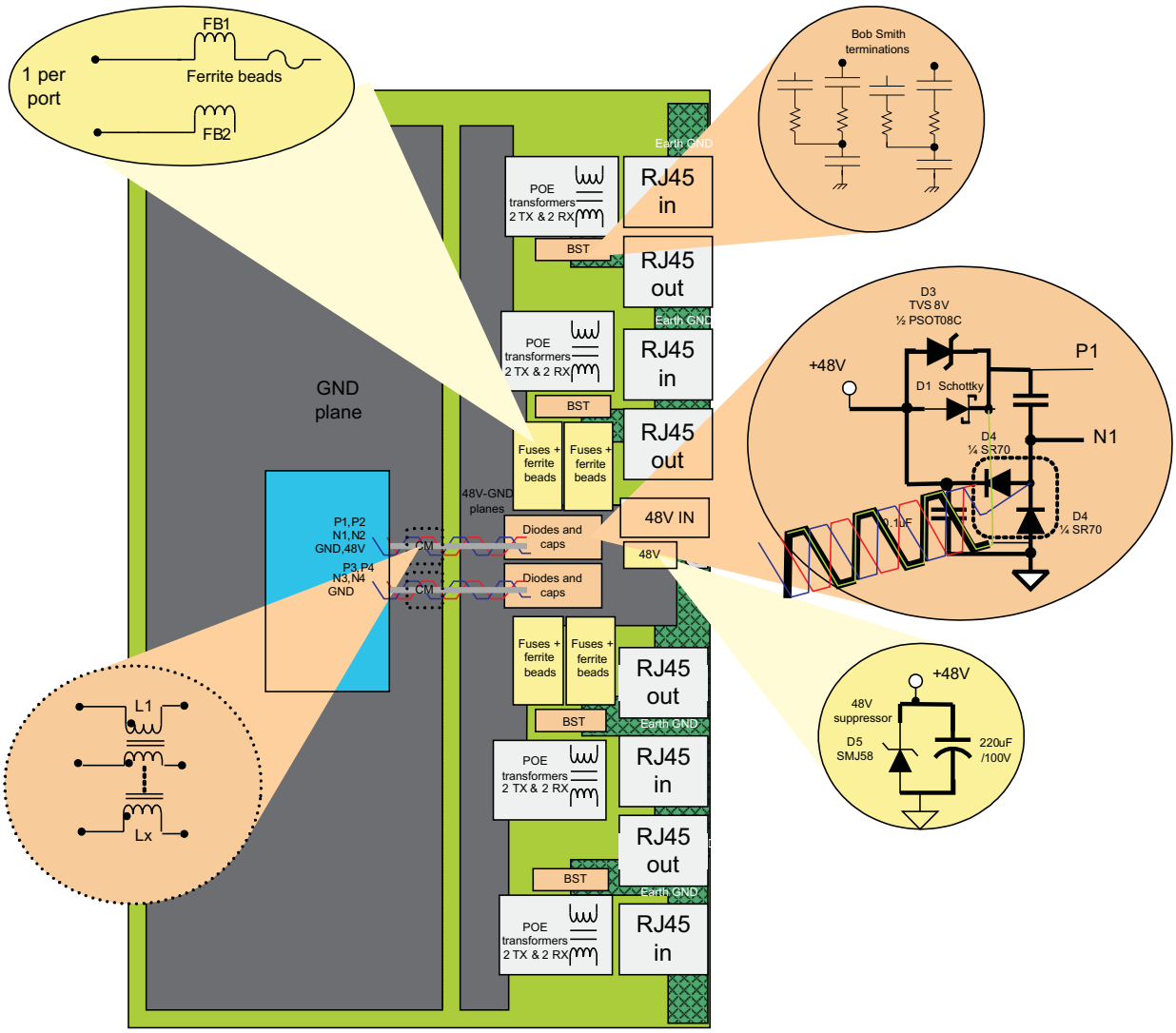



**Figure 21. Layout for a Quad Port PSE**

## 7 References

1. *Protection of Electronic Circuits from Overvoltages*, Ronald B. Standler, Dover Publications inc., 2002
2. IEC 61000-4-2, 2001-04
3. IEC 61000-4-4, 2004-7
4. IEC 61000-4-5, 2001-4
5. ITU-T recommendations K.20, K.21, K.44, and K.45
6. GR-1089-CORE, Issue 4.
7. *Design in Transient Protection for Power-Bus and Data Lines*, David W. Hutchins, Electronic Design, July 1990
8. *Electrical-Transient Immunity: a Growing Imperative for System Design*, O. Melville Clark and Donald E. Neill, Electronic Design, January 1992
9. *TVS Diode Application Note*, Semtech AN96-07, Revision 02/4/2002
10. *Method to Enhance the Performance of Category 5 Cable in the Electromagnetic Environment*, Bob Smith, January 25th, 1993

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