802.3at™

IEEE Standard for Information technology—Telecommunications and information exchange between systems—Local and metropolitan area networks—Specific requirements

Part 3: Carrier Sense Multiple Access with Collision Detection (CSMA/CD) Access Method and Physical Layer Specifications

Amendment 3: Data Terminal Equipment (DTE) Power via the Media Dependent Interface (MDI) Enhancements

IEEE Computer Society

Sponsored by the
LAN/MAN Standards Committee

IEEE
3 Park Avenue
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IEEE Std 802.3at™-2009
(Amendment to
IEEE Std 802.3™-2008)

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Approved 11 September 2009
IEEE-SA Standards Board

Abstract: This amendment includes changes to IEEE Std 802.3-2008 to augment the capabilities of IEEE Std 802.3 with higher power levels and improved power management information.

Keywords: Data Link Layer classification, MPS, PD, PI, POE+, power, Power over Ethernet plus, PSE, Type 1, Type 2

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Introduction

This introduction is not part of IEEE Std 802.3at-2009, IEEE Standard for Information technology—Telecommunications and information exchange between systems—Local and metropolitan area networks—Specific requirements, Part 3: CSMA/CD Access Method and Physical Layer Specifications, Amendment 3: Data Terminal Equipment (DTE) Power via the Media Dependent Interface (MDI) Enhancements.

IEEE Std 802.3™ was first published in 1985. Since the initial publication, many projects have added functionality or provided maintenance updates to the specifications and text included in the standard. Each IEEE 802.3 project/amendment is identified with a suffix (e.g., IEEE Std 802.3at-2009).

The Media Access Control (MAC) protocol specified in IEEE Std 802.3 is Carrier Sense Multiple Access with Collision Detection (CSMA/CD). This MAC protocol was included in the experimental Ethernet developed at Xerox Palo Alto Research Center. While the experimental Ethernet had a 2.94 Mb/s data rate, IEEE Std 802.3-1985 specified operation at 10 Mb/s. Since 1985 new media options, new speeds of operation, and new capabilities have been added to IEEE Std 802.3.

Some of the major additions to IEEE Std 802.3 are identified in the marketplace with their project number. This is most common for projects adding higher speeds of operation or new protocols. For example, IEEE Std 802.3u™ added 100 Mb/s operation (also called Fast Ethernet), IEEE Std 802.3x™ specified full duplex operation and a flow control protocol, IEEE Std 802.3z™ added 1000 Mb/s operation (also called Gigabit Ethernet), IEEE Std 802.3ae™ added 10 Gb/s operation (also called 10 Gigabit Ethernet) and IEEE Std 802.3ah™ specified access network Ethernet (also called Ethernet in the First Mile). These major additions are all now included in, and are superseded by, IEEE Std 802.3-2008 and are not maintained as separate documents.

At the date of IEEE Std 802.3at-2009 publication, IEEE Std 802.3 is comprised of the following documents:

IEEE Std 802.3-2008

Section One—Includes Clause 1 through Clause 20 and Annex A through Annex H and Annex 4A. Section One includes the specifications for 10 Mb/s operation and the MAC, frame formats and service interfaces used for all speeds of operation.

Section Two—Includes Clause 21 through Clause 33 and Annex 22A through Annex 33E. Section Two includes management attributes for multiple protocols and speed of operation as well as specifications for providing power over twisted pair cabling for multiple operational speeds. It also includes general information on 100 Mb/s operation as well as most of the 100 Mb/s Physical Layer specifications.

Section Three—Includes Clause 34 through Clause 43 and Annex 36A through Annex 43C. Section Three includes general information on 1000 Mb/s operation as well as most of the 1000 Mb/s Physical Layer specifications.

Section Four—Includes Clause 44 through Clause 55 and Annex 44A through Annex 55B. Section Four includes general information on 10 Gb/s operation as well as most of the 10 Gb/s Physical Layer specifications.

Section Five—Includes Clause 56 through Clause 74 and Annex 57A through Annex 74A. Clause 56 through Clause 67 and associated annexes specify subscriber access and other Physical Layers and sublayers for operation from 512 kb/s to 1000 Mb/s, and defines services and protocol elements that enable the exchange of IEEE Std 802.3 format frames between stations in a subscriber access network.

Clause 68 specifies a 10 Gb/s Physical Layer specification. Clause 69 through Clause 74 and associated annexes specify Ethernet operation over electrical backplanes at speeds of 1000 Mb/s and 10 Gb/s.

IEEE Std 802.3av™-2009

This amendment includes changes to IEEE Std 802.3-2008 and adds Clause 75 through Clause 77 and Annex 75A through Annex 76A. This amendment adds new Physical Layers for 10 Gb/s operation on point-to-multipoint passive optical networks.

IEEE Std 802.3bc™-2009

This amendment includes changes to IEEE Std 802.3-2008 and adds Clause 79. This amendment moves the Ethernet Organizationally Specific Type, Length, Value (TLV) information elements that were specified in IEEE Std 802.1AB to IEEE Std 802.3.

IEEE Std 802.3at-2009

This amendment includes changes to IEEE Std 802.3-2008. This amendment augments the capabilities of IEEE Std 802.3-2008 with higher power levels and improved power management information.

IEEE Std 802.3 will continue to evolve. New Ethernet capabilities are anticipated to be added within the next few years as amendments to this standard.

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Special symbols and operators

Printed character	Meaning	Font
*	Boolean AND	Symbol
+	Boolean OR, arithmetic addition	Symbol
^	Boolean XOR	Times New Roman
!	Boolean NOT	Symbol
×	Multiplication	Symbol
<	Less than	Symbol
≤	Less than or equal to	Symbol
>	Greater than	Symbol
≥	Greater than or equal to	Symbol
=	Equal to	Symbol
≠	Not equal to	Symbol
⇐	Assignment operator	Symbol
∈	Indicates membership	Symbol
∉	Indicates nonmembership	Symbol
±	Plus or minus (a tolerance)	Symbol
°	Degrees	Symbol
∑	Summation	Symbol
√	Square root	Symbol
—	Big dash (em dash)	Times New Roman
–	Little dash (en dash), subtraction	Times New Roman
|	Vertical bar	Times New Roman
†	Dagger	Times New Roman
‡	Double dagger	Times New Roman
α	Lower case alpha	Symbol
β	Lower case beta	Symbol
γ	Lower case gamma	Symbol
δ	Lower case delta	Symbol
ε	Lower case epsilon	Symbol
λ	Lambda	Symbol
μ	Micro	Times New Roman
Ω	Omega	Symbol

Contents

IEEE Standard for Information technology—Telecommunications and information exchange between systems—Local and metropolitan area networks—Specific requirements

Part 3: Carrier Sense Multiple Access with Collision Detection (CSMA/CD) Access Method and Physical Layer Specifications

Amendment 3: Data Terminal Equipment (DTE) Power via the Media Dependent Interface (MDI) Enhancements

[This amendment is based on IEEE Std 802.3-2008.]

NOTE—The editing instructions contained in this amendment define how to merge the material contained therein into the existing base standard and its amendments to form the comprehensive standard. When the source of the base text is other than IEEE Std 802.3-2008, the source is indicated in the change instruction.

The editing instructions are shown in ***bold italic***. Four editing instructions are used: change, delete, insert, andreplace. ***Change*** is used to make corrections in existing text or tables. The editing instruction specifies the location of the change and describes what is being changed by using ~~strikethrough~~ (to remove old material) and underscore (to add new material). ***Delete*** removes existing material. ***Insert*** adds new material without disturbing the existingmaterial. Insertions may require renumbering. If so, renumbering instructions are given in the editing instruction. ***Replace*** is used to make changes in figures or equations by removing the existing figure or equation and replacing it with a new one. Editing instructions, change markings, and this NOTE will not be carried over into future editions because the changes will be incorporated into the base standard.[1]

[1]Notes in text, tables, and figures are given for information only and do not contain requirements needed to implement the standard.

1. Introduction

1.3 Normative references

Insert the following new references in alphanumerical order:

ANSI/TIA-568-C.0—Generic Telecommunications Cabling.

ANSI/TIA-568-C.2—Copper Cabling Components.

1.4 Definitions

Insert the following definitions alphabetically and renumber as required:

1.4.x 1-Event class signature: The response of the PD to 1-Event classification (see IEEE 802.3, Clause 33).

1.4.x 1-Event classification: The application of a single class event during PI probing (see IEEE 802.3, Clause 33, 33.2.6).

1.4.x 2-Event class signature: The response of the PD to 2-Event classification (see IEEE 802.3, Clause 33).

1.4.x 2-Event classification: The application of two class events during PI probing (see IEEE 802.3, Clause 33, 33.2.6).

1.4.x I_{Port}: The total power-pair current going into the PI (see IEEE 802.3, Clause 33).

1.4.x Midspan PSE, 1000BASE-T: A Midspan PSE that results in a link that can support 10BASE-T, 100BASE-TX, and 1000BASE-T operation (see IEEE 802.3, Clause 33).

1.4.x Midspan PSE, 10BASE-T/100BASE-TX: A Midspan PSE that results in a link that can only support 10BASE-T and 100BASE-TX operation (see IEEE 802.3, Clause 33).

1.4.x TP-PMD: Twisted Pair, Physical Medium Dependent (ANSI X3.263-1995).

1.4.x Type 1 PD: A PD that does not provide a Class 4 signature during Physical Layer classification (see IEEE 802.3, Clause 33).

1.4.x Type 1 PSE: A PSE that supports only a Type 1 PD (see IEEE 802.3, Clause 33).

1.4.x Type 2 PD: A PD that provides a Class 4 signature during Physical Layer classification, understands 2-Event classification, and is capable of Data Link Layer classification (see IEEE 802.3, Clause 33).

1.4.x Type 2 PSE: A PSE that supports both a Type 1 and a Type 2 PD (see IEEE 802.3, Clause 33).

1.4.x V_{PD}: The voltage at the PD PI measured between any conductor of one power pair and any conductor of the other power pair (see IEEE 802.3, Clause 33).

1.4.x V_{PSE}: The voltage at the PSE PI measured between any conductor of one power pair and any conductor of the other power pair (see IEEE 802.3, Clause 33).

25. Physical Medium Dependent (PMD) sublayer and baseband medium, type 100BASE-TX

25.4 Specific requirements and exceptions

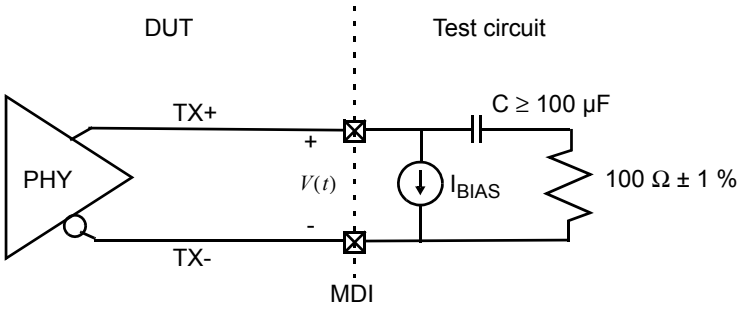
Insert new subclause 25.4.4a after 25.4.4 as follows:

25.4.4a Change to 9.1.7, "Worst case droop of transformer"

A receiver in a Type 2 Endpoint PSE or Type 2 PD (see Clause 33) shall meet the requirements of 25.4.5a. A transmitter in a Type 2 Endpoint PSE or Type 2 PD delivering or accepting more than 13.0 W average power shall meet either the Open Circuit Inductance (OCL) requirement in 9.1.7 of TP-PMD, or meet the requirements of 25.4.4a.1.

25.4.4a.1 Equivalent system time constant

While transmitting the Data Dependent Jitter (DDJ) packet of TP-PMD A.2, using the test circuit shown in Figure 25–1, the equivalent system time constant, τ, shall be greater than 2.4 μs when calculated using measurement points A and C as shown in Figure 25–2.



DUT = Device under test

NOTE— I_{BIAS} is the current I_{unb} / 2 defined in Clause 33.

Figure 25–1—Type 2 system time constant test circuit

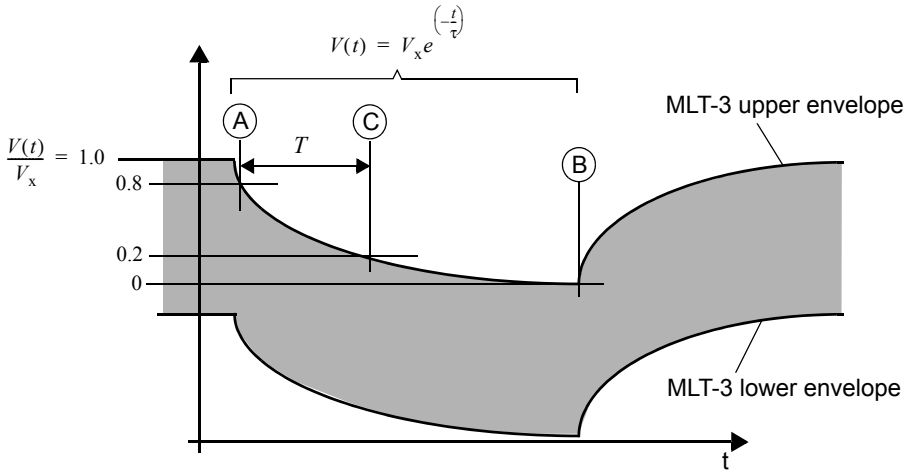


Figure 25–2—Type 2 system time constant measurement

Point B is the point of maximum baseline wander droop, and is the zero point for the vertical axis. Point A, with MDI voltage V_A, is earlier in time from B, with a magnitude that is 80 % of the MLT-3 upper envelope value. Point C, with MDI voltage V_C, is between A and B, with a magnitude that is 20 % of the MLT-3 upper envelope value. The time between A and C is *T*.

These measurements are to be made for the transmitter pair, observing the differential signal output at the MDI with intervening cable, meeting or exceeding the requirements of 25.4.7, less than 1 m long.

The time constant of the transmitter MDI connected to the test circuit of Figure 25–1 is given by Equation (25–1).

$$\left\{ \tau = \frac{T}{\ln\left(\frac{V_A}{V_C}\right)} = \frac{2L}{R} \right\}_s \tag{25–1}$$

where

τ	is the effective time constant of the transmitter
T	is the time in seconds from point A to point C as shown in Figure 25–2
V_A	is the MDI voltage at point A
V_C	is the MDI voltage at point C
L	is the open-circuit inductance of the Ethernet isolation transformer
R	is the 100 Ω termination impedance

Insert new subclause 25.4.5a after 25.4.5 as follows:

25.4.5a Addition to 10.1, "Receiver"

Differential voltage signals generated by a remote transmitter that meets the specifications of Clause 25; passed through a link specified in 25.4.6; and received at the MDI of a 100BASE-TX PMD in a Type 2 Endpoint PSE or a Type 2 PD shall be translated into one of the PMD_UNITDATA.indicate messages with a bit error ratio less than 10^{-9} after link reset completion.

25.5 Protocol implementation conformance statement (PICS) proforma for Clause 25, Physical Medium Dependent (PMD) sublayer and baseband medium, type 100BASE-TX[2]

25.5.3 Major capabilities/options

Add new subclause, 25.5.3.1, as follows:

25.5.3.1 DTE Power via MDI major capabilities/options

Item	Feature	Subclause	Status	Support	Value/Comment
*PSET2	Type 2 PSE implementation	33.1.4	O	Yes [ ] No [ ]	Optional
*PDT2	Type 2 PD implementation	33.3.2	O	Yes [ ] No [ ]	Optional

25.5.4 PICS proforma tables for the Physical Medium Dependent (PMD) sublayer and baseband medium, type 100BASE-TX

Add new subclause, 25.5.4.4, after 25.5.4.3 as follows:

25.5.4.4 DTE Power via MDI compliance

Item	Feature	Subclause	Status	Support	Value/Comment
DTEP1	Type 2 PD receiver worst-case droop transformer	25.4.4a	PDT2:M	Yes [ ] No [ ]	Meet requirements of 25.4.5a: differential voltage signals translated into one of the PMD_UNITDATA.indicate messages with a bit error ratio less than 10^{-9} after link reset completion
DTEP2	Type 2 Endpoint PSE receiver worst-case droop transformer	25.4.4a	PSET2:M	Yes [ ] No [ ]	Meet requirements of 25.4.5a: differential voltage signals translated into one of the PMD_UNITDATA.indicate messages with a bit error ratio less than 10^{-9} after link reset completion

[2]Copyright release for PICS proformas: Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

Item	Feature	Subclause	Status	Support	Value/Comment
DTEP3	Type 2 PD transmitter worst-case droop transformer while accepting more than 13 W average power	25.4.4a	PDT2:M	Yes [ ] No [ ]	Meet OCL requirements of 9.1.7 or requirements in 25.4.4a.1
DTEP4	Type 2 Endpoint PSE transmitter worst-case droop transformer while delivering more than 13 W average power	25.4.4a	PSET2:M	Yes [ ] No [ ]	Meet OCL requirements in 9.1.7 or requirements in 25.4.4a.1
DTEP5	Equivalent system time constant	25.4.4a.1	M	Yes [ ] N/A [ ]	Greater than 2.4 µs when calculated using measurement points A and C in Figure 25–2

30. Management

30.2 Managed objects

30.2.2 Overview of managed objects

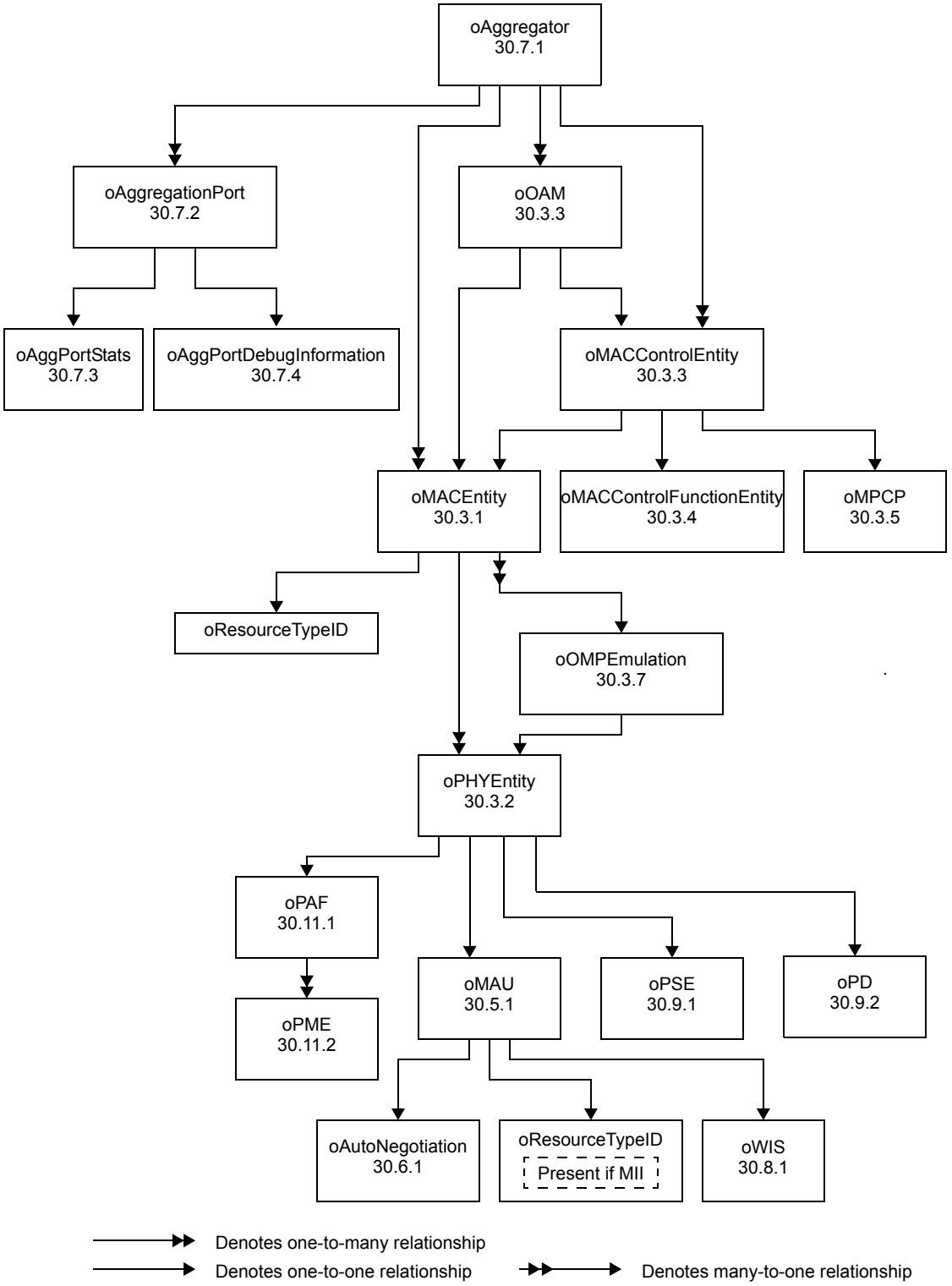
30.2.2.1 Text description of managed objects

Change the following paragraphs as shown:

oPAF	The oPAF managed object class provides the management controls necessary to allow an instance of a PME aggregation function (PAF) to be managed. The PAF managed object class also provides a view of a collection of PMEs.
oPD	The managed object of that portion of the containment trees shown in Figure 30–3, Figure 30–4, and Figure 30–5. This managed object class provides the attributes, actions, and notifications required for management by a PSE system.
oPME	The oPME managed object class provides the management controls necessary to allow an instance of a PME to be managed. The oPAF managed object contains the PME managed object in a DTE.
oPSE	The managed object of that portion of the containment trees shown in Figure 30–3, Figure 30–4, and Figure 30–5. This managed object class provides the ~~The~~ attributes, ~~and~~ actions, and notifications ~~defined in this subclause are contained within the oPSE managed object~~ required for management of a PD system.
oPSEGroup	The PSE Group managed object class is a view of a collection of PSEs.

30.2.3 Containment

Replace Figure 30–3 and Figure 30–4 with the following:



NOTE—The objects oAggregator, oAggregationPort, oAggPortStats, and oAggPortDebugInformation are deprecated by IEEE Std 802.1AX-2008.

Figure 30–3—DTE System entity relationship diagram

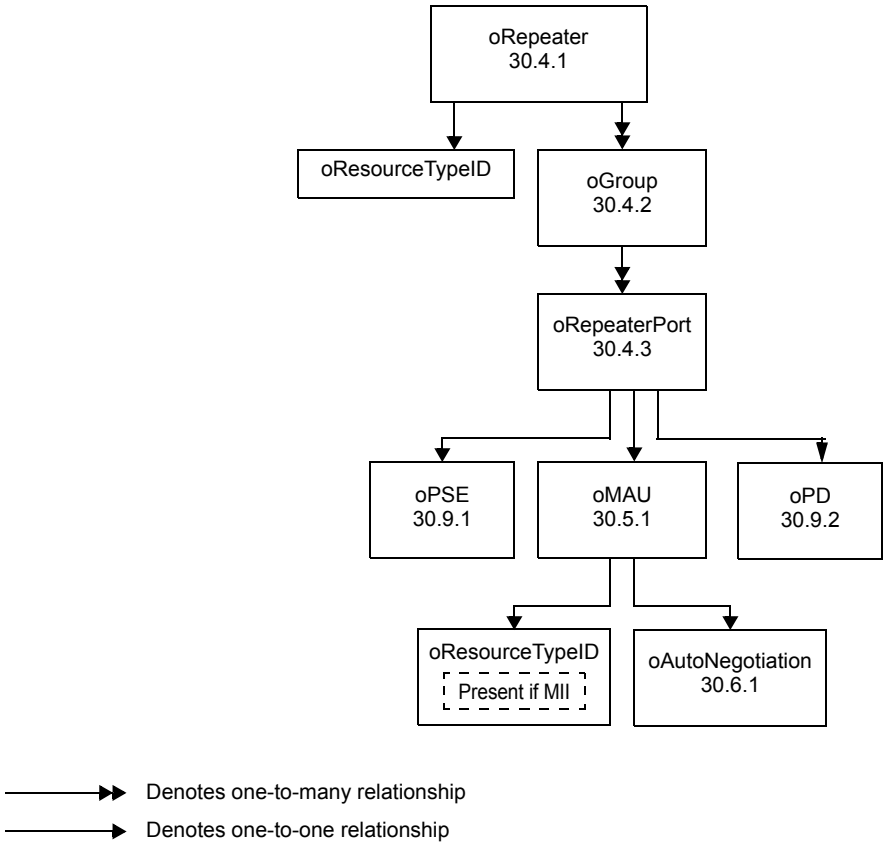


Figure 30–4—Repeater entity relationship diagram

30.2.5 Capabilities

Change the following paragraphs as shown (30.2.5 previously changed by IEEE Std 802.3bc-2009):

The 1000 Mb/s Burst Monitor Capability provides additional attributes that relate only to 1000 Mb/s operation, while the 100 Mb/s Monitor Capability has attributes that apply to a mixed 100 and 1000 Mb/s operation. These attributes are provided to complement the counter attributes of the optional packages and capabilities that apply to 10 Mb/s and mixed 10, 100, and 1000 Mb/s implementations. It is recommended that when the 100/1000 Mb/s Monitor Capability or 1000 Mb/s Burst Monitor Capability is implemented, the appropriate complementary counter packages and capabilities are also implemented.

For managed PSEs, the PSE Basic Package is mandatory and the PSE Recommended Package is optional. For managed PDs, the PD Basic Package is mandatory. For a managed PSE to be conformant to this standard, it shall fully implement the PSE Basic Package. For a managed PD to be conformant to this standard, it shall fully implement the PD Basic Package. For a managed PSE to be conformant to the optional Recommended Package it shall implement that entire package. PSE and PD management is optional with respect to all other CSMA/CD management.

For managed Midspans, the Midspan managed object class shall be implemented in its entirety. All attributes and notifications are mandatory. Midspan management is optional with respect to all other CSMA/CD management.

~~For LLDP management, the LLDP Basic Package is mandatory, the LLDP Local Package and LLDP Remote Package are conditional on the LLDP operating mode (see IEEE Std 802.1AB-20XX Clause 10). The LLDP Local Package is mandatory for LLDP transmit only mode and LLDP transmit and receive mode. The LLDP Remote Package is mandatory for LLDP receive only mode and LLDP transmit and receive mode.~~

For LLDP management, the LLDP Basic Package is mandatory. All other LLDP packages are conditional on the IEEE 802.3 Organizationally Specific TLVs supported and the LLDP operating mode (see IEEE Std 802.1AB, Clause 10).

LLDP MAC/PHY Configuration/Status Local Package is mandatory for managed entities that support IEEE 802.3 Organizationally Specific TLV named "MAC/PHY Configuration/Status" and are either in LLDP transmit only mode or in LLDP transmit and receive mode. LLDP MAC/PHY Config/Status Remote Package is mandatory for managed entities that support IEEE 802.3 Organizationally Specific TLV named "MAC/PHY Configuration/Status" and are either in LLDP receive only mode or in LLDP transmit and receive mode.

LLDP Power via MDI Local Package is mandatory for managed entities that support IEEE 802.3 Organizationally Specific TLV named "Power via MDI" and are either in LLDP transmit only mode or in LLDP transmit and receive mode. LLDP Power via MDI Remote Package is mandatory for managed entities that support IEEE 802.3 Organizationally Specific TLV named "Power via MDI" and are either in LLDP receive only mode or in LLDP transmit and receive mode.

LLDP Link Aggregation Local Package is mandatory for managed entities that support IEEE 802.3 Organizationally Specific TLV named "Link Aggregation" and are either in LLDP transmit only mode or in LLDP transmit and receive mode. LLDP Link Aggregation Remote Package is mandatory for managed entities that support IEEE 802.3 Organizationally Specific TLV named "Link Aggregation" and are either in LLDP receive only mode or in LLDP transmit and receive mode.

LLDP Max Frame Size Local Package is mandatory for managed entities that support IEEE 802.3 Organizationally Specific TLV named "Max Frame Size" and are either in LLDP transmit only mode or in LLDP transmit and receive mode. LLDP Max Frame Size Remote Package is mandatory for managed entities that IEEE 802.3 Organizationally Specific TLV named "Max Frame Size" and are either in LLDP receive only mode or in LLDP transmit and receive mode.

Replace Table 30–4 with the following:

Table 30–4—DTE Power via MDI capabilities

			PSE Basic Package (mandatory)	PSE Recommended Package (optional)	Midspan Basic Capability (mandatory)	PD Basic Package (mandatory)
oResourceTypeID managed object						
aResourceTypeIDName	ATTRIBUTE	GET			X	
aResourceInfo	ATTRIBUTE	GET			X	
oMidSpan managed object class (30.10.1)						
aMidSpanID	ATTRIBUTE	GET			X	
aMidSpanPSEGroupCapacity	ATTRIBUTE	GET			X	
aMidSpanPSEGroupMap	ATTRIBUTE	GET			X	
nMidSpanPSEGroupMapChange	NOTIFICATION				X	
oPSEGroup managed object class (30.10.2)						
aPSEGroupID	ATTRIBUTE	GET			X	
aPSECapacity	ATTRIBUTE	GET			X	
aPSEMap	ATTRIBUTE	GET			X	
nPSEMapChange	NOTIFICATION				X	
oPSE managed object class (30.9.1)						
aPSEID	ATTRIBUTE	GET	X			
aPSEAdminState	ATTRIBUTE	GET	X			
aPSEPowerPairsControlAbility	ATTRIBUTE	GET	X			
aPSEPowerPairs	ATTRIBUTE	GET-SET	X			
aPSEPowerDetectionStatus	ATTRIBUTE	GET	X			
aPSEPowerClassification	ATTRIBUTE	GET		X		
aPSEInvalidSignatureCounter	ATTRIBUTE	GET		X		
aPSEPowerDeniedCounter	ATTRIBUTE	GET		X		
aPSEOverLoadCounter	ATTRIBUTE	GET		X		
aPSEShortCounter	ATTRIBUTE	GET		X		
aPSEMPSAbsentCounter	ATTRIBUTE	GET		X		
acPSEAdminControl	ACTION		X			
oPD managed object class (30.9.2)						
aPDID	ATTRIBUTE	GET				X
Common Attributes Template						
aCMCounter	ATTRIBUTE	GET		X		

Replace Table 30–5 with the following (Table 30-5 inserted by IEEE Std 802.3bc-2009):

Table 30–5—LLDP capabilities

			LLDP Basic Package (mandatory)	LLDP MAC/PHY Configuration/Status Local Package (conditional)	LLDP MAC/PHY Configuration/Status Remote Package (conditional)	LLDP Power via MDI Local Package (conditional)	LLDP Power via MDI Remote Package (conditional)	LLDP Link Aggregation Local Package (conditional)	LLDP Link Aggregation Remote Package (conditional)	LLDP Maximum Frame Size Local Package (conditional)	LLDP Maximum Frame Size Remote Package (conditional)
oLldpXdot3Config managed object class (30.12.1)											
aLldpXdot3PortConfigTLVsTxEnable	ATTRIBUTE	GET-SET	X								
oLldpXdot3LocSystemsGroup managed object class (30.12.2)											
aLldpXdot3LocPortAutoNegSupported	ATTRIBUTE	GET		X							
aLldpXdot3LocPortAutoNegEnabled	ATTRIBUTE	GET		X							
aLldpXdot3LocPortAutoNegAdvertisedCap	ATTRIBUTE	GET		X							
aLldpXdot3LocPortOperMauType	ATTRIBUTE	GET		X							
aLldpXdot3LocPowerPortClass	ATTRIBUTE	GET				X					
aLldpXdot3LocPowerMDISupported	ATTRIBUTE	GET				X					
aLldpXdot3LocPowerMDIEnabled	ATTRIBUTE	GET				X					
aLldpXdot3LocPowerPairControlable	ATTRIBUTE	GET				X					
aLldpXdot3LocPowerPairs	ATTRIBUTE	GET				X					
aLldpXdot3LocPowerClass	ATTRIBUTE	GET				X					
aLldpXdot3LocLinkAggStatus	ATTRIBUTE	GET						X			
aLldpXdot3LocLinkAggPortId	ATTRIBUTE	GET						X			
aLldpXdot3LocMaxFrameSize	ATTRIBUTE	GET								X	
aLldpXdot3LocPowerType	ATTRIBUTE	GET				X					
aLldpXdot3LocPowerSource	ATTRIBUTE	GET				X					
aLldpXdot3LocPowerPriority	ATTRIBUTE	GET-SET				X					
aLldpXdot3LocPDRequestedPowerValue	ATTRIBUTE	GET				X					
aLldpXdot3LocPSEAllocatedPowerValue	ATTRIBUTE	GET				X					
aLldpXdot3LocResponseTime	ATTRIBUTE	GET				X					
aLldpXdot3LocReady	ATTRIBUTE	GET				X					
aLldpXdot3LocReducedOperationPowerValue	ATTRIBUTE	GET				X					

Table 30–5—LLDP capabilities *(continued)*

			LLDP Basic Package (mandatory)	LLDP MAC/PHY Configuration/Status Local Package (conditional)	LLDP MAC/PHY Configuration/Status Remote Package (conditional)	LLDP Power via MDI Local Package (conditional)	LLDP Power via MDI Remote Package (conditional)	LLDP Link Aggregation Local Package (conditional)	LLDP Link Aggregation Remote Package (conditional)	LLDP Maximum Frame Size Local Package (conditional)	LLDP Maximum Frame Size Remote Package (conditional)
oLldpXdot3RemSystemsGroup managed object class (30.12.3)											
aLldpXdot3RemPortAutoNegSupported	ATTRIBUTE	GET			X						
aLldpXdot3RemPortAutoNegEnabled	ATTRIBUTE	GET			X						
aLldpXdot3RemPortAutoNegAdvertisedCap	ATTRIBUTE	GET			X						
aLldpXdot3RemPortOperMauType	ATTRIBUTE	GET			X						
aLldpXdot3RemPowerPortClass	ATTRIBUTE	GET					X				
aLldpXdot3RemPowerMDISupported	ATTRIBUTE	GET					X				
aLldpXdot3RemPowerMDIEnabled	ATTRIBUTE	GET					X				
aLldpXdot3RemPowerPairControlable	ATTRIBUTE	GET					X				
aLldpXdot3RemPowerPairs	ATTRIBUTE	GET					X				
aLldpXdot3RemPowerClass	ATTRIBUTE	GET					X				
aLldpXdot3RemLinkAggStatus	ATTRIBUTE	GET							X		
aLldpXdot3RemLinkAggPortId	ATTRIBUTE	GET							X		
aLldpXdot3RemMaxFrameSize	ATTRIBUTE	GET									X
aLldpXdot3RemPowerType	ATTRIBUTE	GET					X				
aLldpXdot3RemPowerSource	ATTRIBUTE	GET					X				
aLldpXdot3RemPowerPriority	ATTRIBUTE	GET					X				
aLldpXdot3RemPDRequestedPowerValue	ATTRIBUTE	GET					X				
aLldpXdot3RemPSEAllocatedPowerValue	ATTRIBUTE	GET					X				

Change the title of 30.9 as follows:

30.9 Management for DTE Power via MDI ~~Sourcing Equipment (PSE)~~

Insert new subclause 30.9.2 after 30.9.1 as follows:

30.9.2 PD managed object class

This subclause formally defines the behaviours for the oPD managed object class attributes.

30.9.2.1 PD attributes

30.9.2.1.1 aPDID

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
The value of aPDID is assigned so as to uniquely identify a PD Power via MDI classification local system among the subordinate managed objects of the containing object.;

30.12.2 LLDP Local System Group managed object class

30.12.2.1 LLDP Local System Group attributes

Insert new subclauses 30.12.2.1.14 through 30.12.2.1.21 after 30.12.2.1.13 (30.12.2 inserted by IEEE Std 802.3bc-2009):

30.12.2.1.14 aLldpXdot3LocPowerType

ATTRIBUTE

APPROPRIATE SYNTAX:
BIT STRING [SIZE (2)]

BEHAVIOUR DEFINED AS:
A GET attribute that returns a bit string indicating whether the local system is a PSE or a PD and whether it is Type 1 or Type 2. The first bit indicates Type 1 or Type 2. The second bit indicates PSE or PD. A PSE shall set this bit to indicate a PSE. A PD shall set this bit to indicate a PD.;

30.12.2.1.15 aLldpXdot3LocPowerSource

ATTRIBUTE

APPROPRIATE SYNTAX:
BIT STRING [SIZE (2)]

BEHAVIOUR DEFINED AS:
A GET attribute that returns a bit string indicating the power sources of the local system. A PSE indicates whether it is being powered by a primary power source; a backup power source; or unknown. A PD indicates whether it is being powered by a PSE and locally; by a PSE only; or unknown.;

30.12.2.1.16 aLldpXdot3LocPowerPriority

ATTRIBUTE

APPROPRIATE SYNTAX:
An ENUMERATED value list that has the following entries:

low	low priority PD
high	high priority PD
critical	critical priority PD
unknown	priority unknown

BEHAVIOUR DEFINED AS:

A GET attribute that returns the priority of a PD system. For a PSE, this is the priority that the PSE assigns to the PD. For a PD, this is the priority that the PD requests from the PSE.
A SET operation changes the priority of the PD system to the indicated value.;

30.12.2.1.17 aLldpXdot3LocPDRequestedPowerValue

ATTRIBUTE

APPROPRIATE SYNTAX:

INTEGER

BEHAVIOUR DEFINED AS:

A GET attribute that returns the PD requested power value. For a PD, it is the power value that the PD has currently requested from the remote system. PD requested power value is the maximum input average power the PD ever draws under this power allocation if accepted. For a PSE, it is the power value that the PSE mirrors back to the remote system. This is the PD requested power value that was used by the PSE to compute the power it has currently allocated to the remote system. The PD requested power value is encoded according to Equation (79–1), where *X* is the decimal value of aLldpXdot3LocPDRequestedPowerValue.;

30.12.2.1.18 aLldpXdot3LocPSEAllocatedPowerValue

ATTRIBUTE

APPROPRIATE SYNTAX:

INTEGER

BEHAVIOUR DEFINED AS:

A GET attribute that returns the PSE allocated power value. For a PSE, it is the power value that the PSE has currently allocated to the remote system. The PSE allocated power value is the maximum input average power that the PSE wants the PD to ever draw under this allocation if it is accepted. For a PD, it is the power value that the PD mirrors back to the remote system. This is the PSE allocated power value that was used by the PD to compute the power that it has currently requested from the remote system. The PSE allocated power value is encoded according to Equation (79–2), where *X* is the decimal value of aLldpXdot3LocPSEAllocatedPowerValue.;

30.12.2.1.19 aLldpXdot3LocResponseTime

ATTRIBUTE

APPROPRIATE SYNTAX:

INTEGER

BEHAVIOUR DEFINED AS:

A GET attribute that returns the response time in seconds of the local system. For a PD, it is the maximum time required to update the value of attribute aLldpXdot3LocPDRequestedPowerValue when the remote system requests the PD to change its max power draw. For a PSE, it is the maximum time required to update the value of attribute aLldpXdot3LocPDRequestedPowerValue when the remote system requests of the PSE a new power value.;

30.12.2.1.20 aLldpXdot3LocReady

ATTRIBUTE

APPROPRIATE SYNTAX:
A BOOLEAN value:
FALSE: Local system has not completed initialization of the Data Link Layer classification engine and is not ready to receive/transmit an LLDPDU containing a Power via MDI TLV.
TRUE: Local system has initialized the Data Link Layer classification engine and is ready to receive/transmit an LLDPDU containing a Power via MDI TLV.

BEHAVIOUR DEFINED AS:
A GET operation returns the initialization status of the Data Link Layer classification engine on the local system.;

30.12.2.1.21 aLldpXdot3LocReducedOperationPowerValue

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
A GET attribute that returns the reduced operation power value. For a PD, it is a power value that is lower than the currently requested power value. This reduced operation power value represents a power state in which the PD could continue to operate, but with less functionality than at the current PD requested power value. The PSE could optionally use this information in the event that the PSE subsequently requests a lower PD power value than the PD requested power value. For a PSE, it is a power value that the PSE could ask the PD to move to if the PSE wants the PD to move to a lower power state. The definition and encoding of PD requested power value is the same as described in aLldpXdot3LocPDRequestedPowerValue (30.12.2.1.17). The default value for this field is the hexadecimal value FFFF.;

30.12.3 LLDP Remote System Group managed object class

30.12.3.1 LLDP Remote System Group attributes

Insert new subclauses 30.12.3.1.14 through 30.12.3.1.18 after 30.12.3.1.13 (30.12.3 inserted by IEEE Std 802.3bc-2009):

30.12.3.1.14 aLldpXdot3RemPowerType

ATTRIBUTE

APPROPRIATE SYNTAX:
BIT STRING [SIZE (2)]

BEHAVIOUR DEFINED AS:
A GET attribute that returns a bit string indicating whether the remote system is a PSE or a PD and whether it is Type 1 or Type 2. The first bit indicates Type 1 or Type 2. The second bit indicates PSE or PD.;

30.12.3.1.15 aLldpXdot3RemPowerSource

ATTRIBUTE

APPROPRIATE SYNTAX:
BIT STRING [SIZE (2)]

BEHAVIOUR DEFINED AS:
A GET attribute that returns a bit string indicating the power sources of the remote system. When the remote system is a PSE, it indicates whether it is being powered by a primary power source; a backup power source; or unknown. When the remote system is a PD, it indicates whether it is being powered by a PSE and locally; locally only; by a PSE only; or unknown.;

30.12.3.1.16 aLldpXdot3RemPowerPriority

ATTRIBUTE

APPROPRIATE SYNTAX:
An ENUMERATED value list that has the following entries:

low	low priority PD
high	high priority PD
critical	critical priority PD
unknown	priority unknown

BEHAVIOUR DEFINED AS:
A GET operation returns the priority of the PD system received from the remote system. For a PSE, this is the priority that the remote system requests from the PSE. For a PD, this is the priority that the remote system has assigned to the PD.;

30.12.3.1.17 aLldpXdot3RemPDRequestedPowerValue

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
A GET attribute that returns the PD requested power value that was used by the remote system to compute the power value that is has currently allocated to the PD. For a PSE, it is the PD requested power value received from the remote system. The definition and encoding of PD requested power value is the same as described in aLldpXdot3LocPDRequestedPowerValue (30.12.2.1.17).;

30.12.3.1.18 aLldpXdot3RemPSEAllocatedPowerValue

ATTRIBUTE

APPROPRIATE SYNTAX:
INTEGER

BEHAVIOUR DEFINED AS:
A GET attribute that returns the PSE allocated power value received from the remote system. For a PSE, it is the PSE allocated power value that was used by the remote system to compute the power value that it has currently requested from the PSE. For a PD, it is the PSE allocated power value received from the remote system. The definition and encoding of PSE allocated power value is the same as described in aLldpXdot3LocPSEAllocatedPowerValue (30.12.2.1.18).;

Replace Clause 33 with the following:

33. Data Terminal Equipment (DTE) Power via Media Dependent Interface (MDI)

33.1 Overview

This clause defines the functional and electrical characteristics of two optional power (non-data) entities, a Powered Device (PD) and Power Sourcing Equipment (PSE), for use with the MAU defined in Clause 14 and the PHYs defined in Clause 25 and Clause 40. These entities allow devices to draw/supply power using the same generic cabling as is used for data transmission.

DTE powering is intended to provide a 10BASE-T, 100BASE-TX, or 1000BASE-T device with a single interface to both the data it requires and the power to process this data. This clause specifies the following:

a) A power source to add power to the 100 Ω balanced cabling system
b) The characteristics of a powered device's load on the power source and the structured cabling
c) A protocol allowing the detection of a device that requests power from a PSE
d) Methods to classify devices based on their power needs
e) A method for powered devices and power sourcing equipment to dynamically negotiate and allocate power
f) A method for scaling supplied power back to the detect level when power is no longer requested or required

The importance of item c) above should not be overlooked. Given the large number of legacy devices (both IEEE 802.3 and other types of devices) that could be connected to a 100 Ω balanced cabling system, and the possible consequences of applying power to such devices, the protocol to distinguish compatible devices and non-compatible devices is important to prevent damage to non-compatible devices.

The detection and powering algorithms are likely to be compromised by cabling that is not point-to-point, resulting in unpredictable performance and possibly damaged equipment.

This clause differentiates between the two ends of the powered portion of the link, defining the PSE and the PD as separate but related devices.

33.1.1 Objectives

The following are objectives of Power via MDI:

a) *Power*—A PD designed to the standard, and within its range of available power, can obtain both power and data for operation through the MDI and therefore needs no additional connections.
b) *Safety*—A PSE designed to the standard does not introduce non-SELV (Safety Extra Low Voltage) power into the wiring plant.
c) *Compatibility*—Clause 33 utilizes the MDIs of 10BASE-T, 100BASE-TX, and 1000BASE-T without modification. Type 1 operation adds no significant requirements to the cabling. Type 2 operation requires ISO/IEC 11801:1995 Class D or better cabling and a derating of the cabling maximum ambient operating temperature. The clause does not address the operation of 10GBASE-T. For 10GBASE-T operation, the channel model specified in Clause 55 needs to be met without regard to DTE Power via MDI presence or operation.

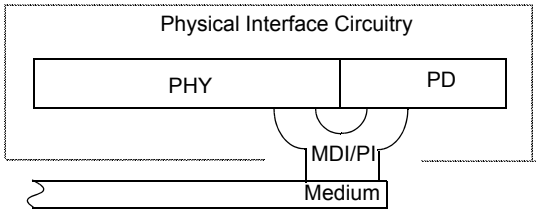
d) *Simplicity*—The powering system described here is no more burdensome on the end users than the requirements of 10BASE-T, 100BASE-TX, or 1000BASE-T.

33.1.2 Compatibility considerations

All implementations of PD and PSE systems shall be compatible at their respective Power Interfaces (PIs) when used in accordance with the restrictions of Clause 33 where appropriate. Designers are free to implement circuitry within the PD and PSE in an application-dependent manner provided that the respective PI specifications are satisfied.

33.1.3 Relationship of DTE Power via MDI to the IEEE 802.3 Architecture

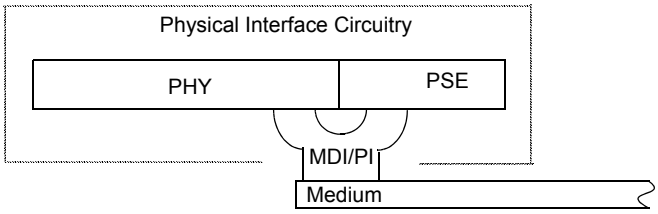
DTE Power via MDI comprises an optional non-data entity. As a non-data entity, it does not appear in a depiction of the OSI Reference Model. Figure 33–1 depicts the positioning of DTE Power via MDI in the case of the PD.



MDI = Medium Dependent Interface
PD = Powered Device
PHY = Physical Layer Device
PI = Power Interface

Figure 33–1—DTE Power via MDI powered device relationship to the physical interface circuitry and the IEEE 802.3 CSMA/CD LAN model

Figure 33–2 and Figure 33–3 depict the positioning of DTE Power via MDI in the cases of the Endpoint PSE and the Midspan PSE, respectively.



MDI = Medium Dependent Interface
PHY = Physical Layer Device
PI = Power Interface
PSE = Power Sourcing Equipment

Figure 33–2—DTE Power via MDI Endpoint power sourcing equipment relationship to the physical interface circuitry and the IEEE 802.3 CSMA/CD LAN model

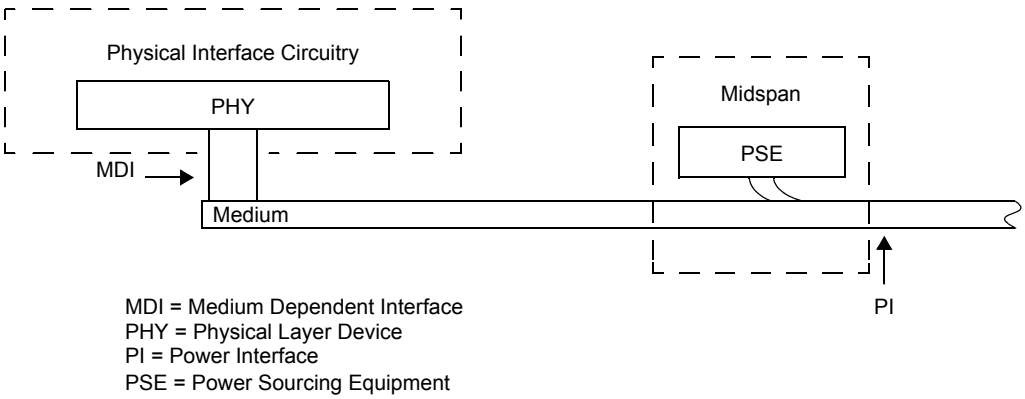


Figure 33–3—DTE Power via MDI Midspan power sourcing equipment relationship to the physical interface circuitry and the IEEE 802.3 CSMA/CD LAN model

The Power Interface (PI) is the generic term that refers to the mechanical and electrical interface between the PSE or PD and the transmission medium.

In an Endpoint PSE and in a PD, the PI is encompassed within the MDI.

PSE power interface specifications that are defined at the MDI apply to an Endpoint PSE. They may or may not apply to a Midspan PSE PI.

33.1.4 Type 1 and Type 2 system parameters

A power system, consisting of a single PSE, link segment, and a single PD, defined as either Type 1 or Type 2, has certain basic parameters defined according to Table 33–1. These parameters define not only certain performance characteristics of the system, but are also used in calculating the various electrical characteristics of PSEs and PDs as described in 33.2 and 33.3.

Table 33–1—Type 1 and Type 2 system parameters

Parameter	Symbol	Units	Type 1 value	Type 2 value	Additional information
Nominal highest DC current per pair	I_{Cable}	A	0.350	0.600	
Channel maximum DC pair loop resistance	R_{Ch}	Ω	20.0	12.5	
Minimum cable type			UTP per 14.4 and 14.5[a]	Class D	See 33.1.4.1, 33.1.4.2

[a]Class D recommended.

I_{Cable} is the current on one twisted pair in the multi-twisted pair cable. Two twisted pairs are required to source I_{Cable}—one carrying (+ I_{Cable}) and one carrying (– I_{Cable}), from the perspective of the PI.

It should be noted that the cable references use “DC loop resistance,” which refers to a single conductor. This clause uses “DC pair loop resistance,” which refers to a pair of conductors in parallel. Therefore, R_{Ch} is related to, but not equivalent to, the “DC loop resistance” called out in the cable references.

33.1.4.1 Type 2 cabling requirement

Type 2 operation requires Class D, or better, cabling as specified in ISO/IEC 11801:1995 with the additional requirement that channel DC loop resistance shall be 25 Ω or less. These requirements are also met by Category 5e or better cable and components as specified in ANSI/TIA/EIA-568-B.2, ANSI/TIA/EIA-568-B.2-1, and ANSI/TIA/EIA-568-B.2-10; or Category 5 cable and components as specified in ANSI/TIA/EIA-568-A-1995.

Under worst-case conditions, Type 2 operation requires a 10 °C reduction in the maximum ambient operating temperature of the cable when all cable pairs are energized at I_{Cable} (see Table 33–1), or a 5 °C reduction in the maximum ambient operating temperature of the cable when half of the cable pairs are energized at I_{Cable}. Additional cable ambient operating temperature guidelines for Type 2 operation are provided in ISO/IEC TR 29125 [Bxx1][3] and TIA TSB-184 [Bxx2].

33.1.4.2 Type 1 and Type 2 channel requirement

Type 1 and Type 2 operation requires that the resistance unbalance shall be 3 % or less. Resistance unbalance is a measure of the difference between the two conductors of a twisted pair in the 100 Ω balanced cabling system. Resistance unbalance is defined as in Equation (33–1):

$$\left\{ \frac{(R_{max} - R_{min})}{(R_{max} + R_{min})} \times 100 \right\}_{\%} \quad (33–1)$$

where

R_{max} is the resistance of the channel conductor with the highest resistance

R_{min} is the resistance of the channel conductor with the lowest resistance

33.2 Power sourcing equipment (PSE)

The PSE is the portion of the end station or midspan equipment that provides the power to a single PD. The PSE's main functions are as follows:

— To search the link section for a PD
— To supply power to the detected PD through the link section
— To monitor the power on the link section
— To remove power when no longer requested or required, returning to the searching state

An unplugged link section is one instance when power is no longer required. In addition, power classification mechanisms exist to provide the PSE with detailed information regarding the power needs of the PD.

A PSE is electrically specified at the point of the physical connection to the cabling.

33.2.1 PSE location

PSEs may be placed in two locations with respect to the link segment, either coincident with the DTE/Repeater or midspan. A PSE that is coincident with the DTE/Repeater is an "Endpoint PSE." A PSE that is located within a link segment that is distinctly separate from and between the MDIs is a "Midspan PSE." The requirements of this document shall apply equally to Endpoint and Midspan PSEs unless the requirement contains an explicit statement that it applies to only one implementation. The location of

[3]The numbers in brackets correspond to those of the bibliography in Annex A.

Alternative A and Alternative B Endpoint PSEs and Midspan PSEs are illustrated in Figure 33–4, Figure 33–5, Figure 33–6, and Figure 33–7.

PSEs can be compatible with 10BASE-T, 100BASE-TX, and/or 1000BASE-T. PSEs may support either Alternative A, Alternative B, or both.

33.2.2 Midspan PSE types

There are two types of Midspan PSEs defined.

10BASE-T/100BASE-TX Midspan PSE:
: A Midspan PSE that results in a link that can support only 10BASE-T and 100BASE-TX operation (see Figure 33–6). Note that this limitation is due to the presence of the Midspan PSE whether it is supplying power or not.

1000BASE-T Midspan PSE:
: A Midspan PSE that results in a link that can support 10BASE-T, 100BASE-TX, and 1000BASE-T operation (see Figure 33–7).

NOTE—See 33.4.9.2 for Alternative A Midspan PSEs.

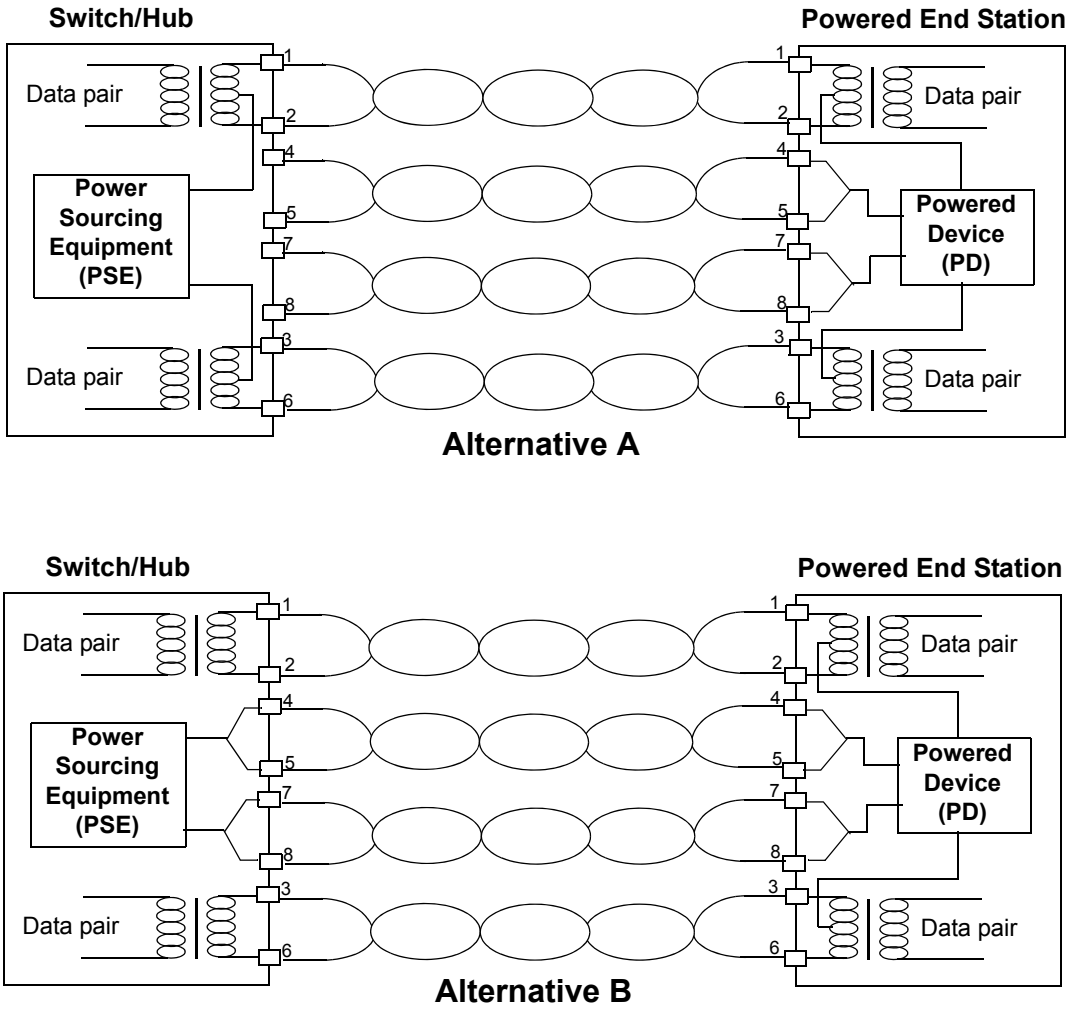


Figure 33–4—10BASE-T/100BASE-TX Endpoint PSE location overview

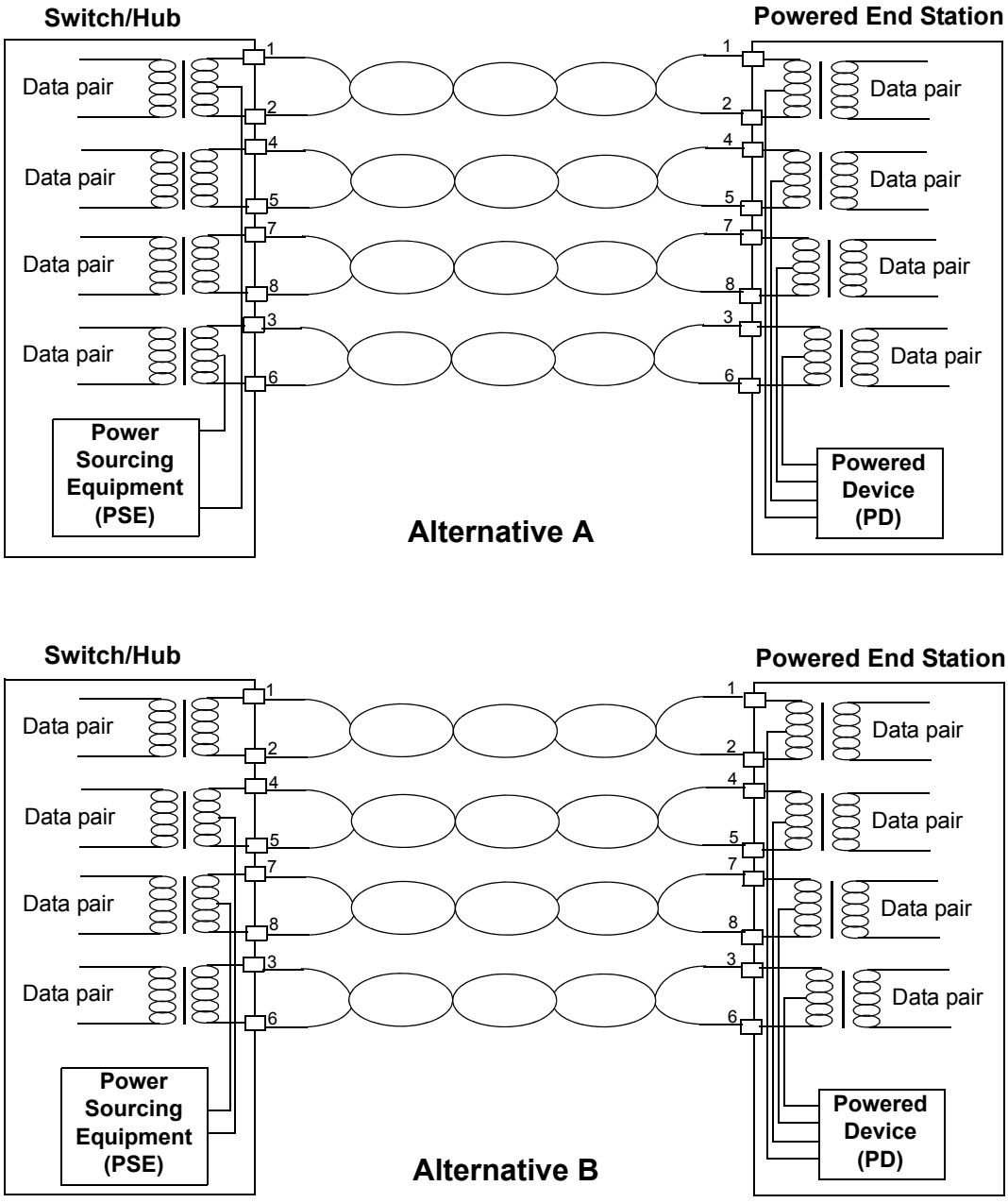


Figure 33–5—1000BASE-T Endpoint PSE location overview

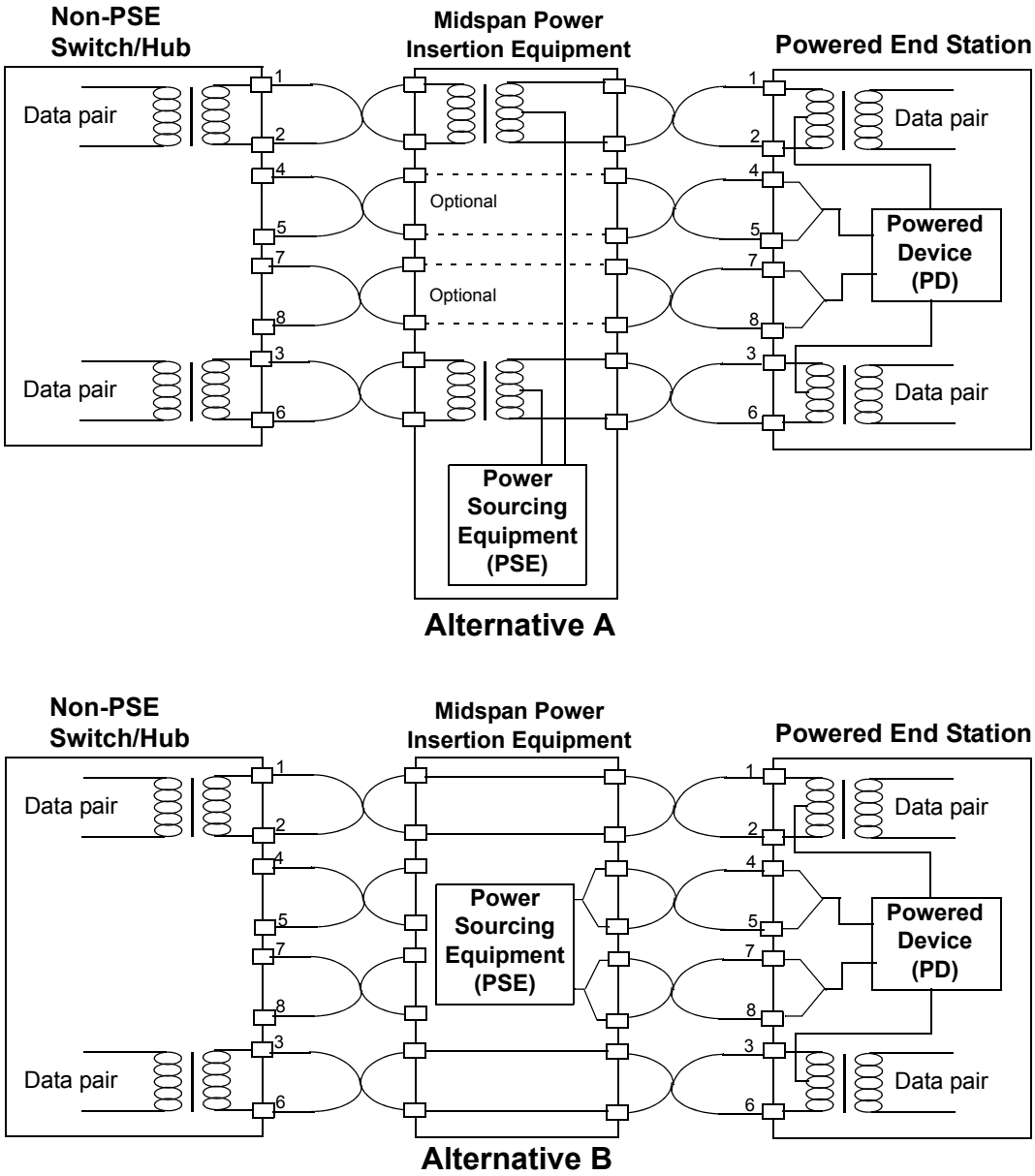


Figure 33–6—10BASE-T/100BASE-TX Midspan PSE location overview

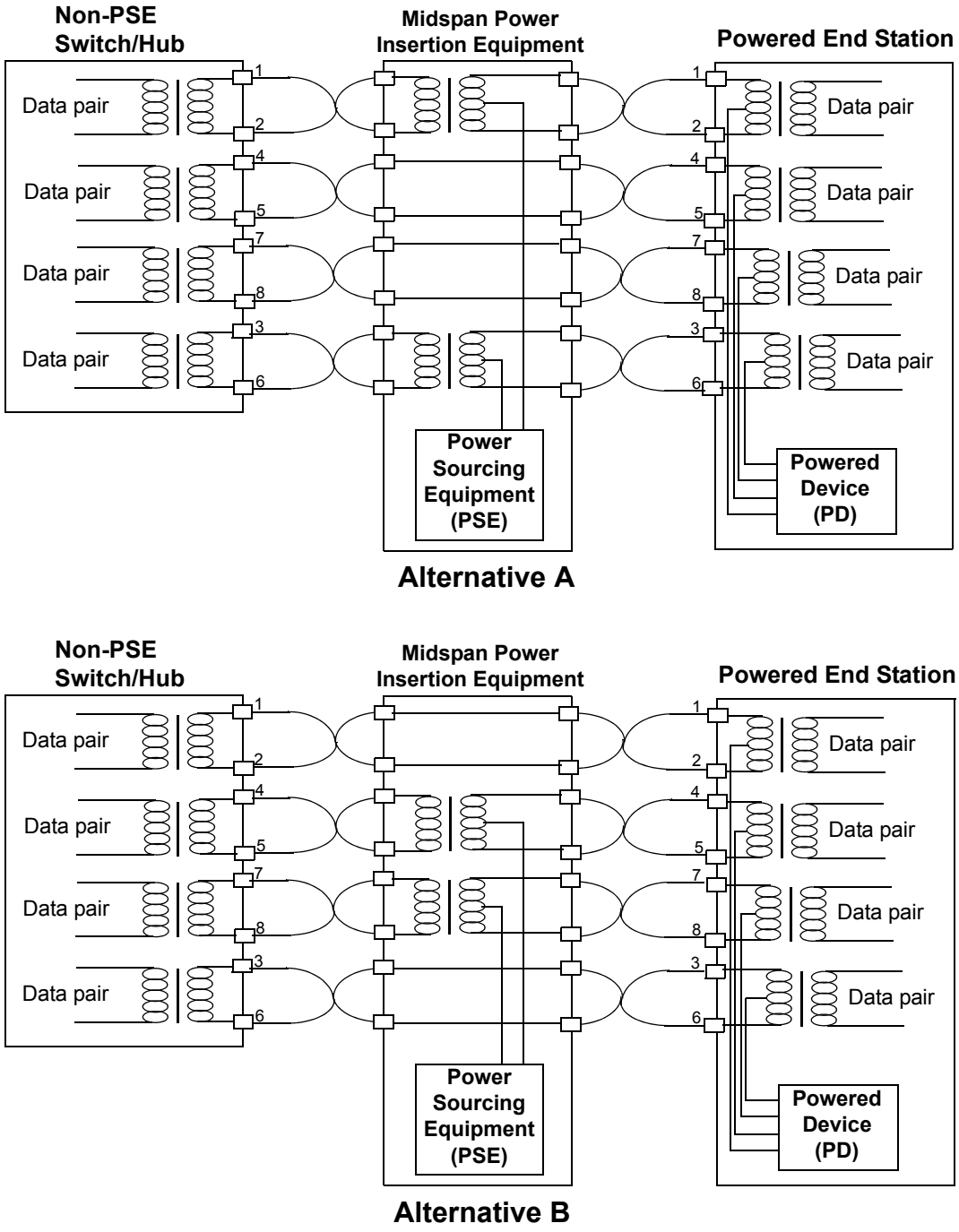


Figure 33–7—1000BASE-T Midspan PSE location overview

33.2.3 PI pin assignments

A PSE device may provide power via one of two valid four-wire connections. In each four-wire connection, the two conductors associated with a pair each carry the same nominal current in both magnitude and polarity. Figure 33–8, in conjunction with Table 33–2, illustrates the valid alternatives.

Table 33–2—PSE Pinout alternatives

Conductor	Alternative A (MDI-X)	Alternative A (MDI)	Alternative B (All)
1	Negative V_{PSE}	Positive V_{PSE}	
2	Negative V_{PSE}	Positive V_{PSE}	
3	Positive V_{PSE}	Negative V_{PSE}	
4			Positive V_{PSE}
5			Positive V_{PSE}
6	Positive V_{PSE}	Negative V_{PSE}	
7			Negative V_{PSE}
8			Negative V_{PSE}

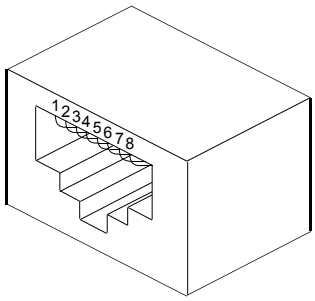


Figure 33–8—PD and PSE eight-pin modular jack

For the purposes of data transfer, the type of PSE data port is relevant to the far-end PD, and in some cases, to the cabling system between them. Therefore, Alternative A matches the positive voltage to the transmit pair of the PSE. PSEs that use automatically-configuring MDI/MDI-X ("Auto MDI-X") ports may choose either polarity choice associated with Alternative A configurations. For further information on the placement of MDI vs. MDI-X, see 14.5.2.

A PSE shall implement Alternative A, Alternative B, or both. While a PSE may be capable of both Alternative A and Alternative B, PSEs shall not operate both Alternative A and Alternative B on the same link segment simultaneously.

33.2.4 PSE state diagrams

The PSE shall provide the behavior of the state diagrams shown in Figure 33–9, Figure 33–9, and Figure 33–10.

33.2.4.1 Overview

Detection, classification, and power turn-on timing shall meet the specifications in Table 33–4, Table 33–10, and Table 33–11.

If power is to be applied, the PSE turns on power after a valid detection in less than T_{pon} as specified in Table 33–11. If the PSE cannot supply power within T_{pon}, it initiates and successfully completes a new detection cycle before applying power.

It is possible that two separate PSEs, one that implements Alternative A and one that implements Alternative B (see 33.2.1), may be attached to the same link segment. In such a configuration, and without the required backoff algorithm, the PSEs could prevent each other from ever detecting a PD by interfering with the detection process of the other.

A PSE performing detection using Alternative B may fail to detect a valid PD detection signature. When this occurs, the PSE backs off for at least T_{dbo} as specified in Table 33–11 before attempting another detection. During this backoff, the PSE shall not apply a voltage greater than V_{Off} to the PI.

If a PSE performing detection using Alternative B detects an open circuit (see 33.2.5.5) on the link section, then that PSE may optionally omit the detection backoff.

If a PSE performing detection using Alternative A detects an invalid signature, it should complete a second detection in less than T_{dbo} min after the beginning of the first detection attempt. This allows an Alternative A PSE to complete a successful detection cycle prior to an Alternative B PSE present on the same link section that may have caused the invalid signature.

NOTE—A Type 1 PSE performing detection using Alternative A may need to have its DTE powering ability disabled when it is attached to the same link segment as a Type 2 Midspan PSE performing detection using Alternative B. This allows the Midspan PSE to successfully complete a detection cycle.

33.2.4.2 Conventions

The notation used in the state diagrams follows the conventions of state diagrams as described in 21.5.

33.2.4.3 Constants

The PSE state diagrams use the following constants:

PSE_TYPE
A constant indicating the type of the PSE
Values: 1: Type 1 PSE
2: Type 2 PSE

33.2.4.4 Variables

The PSE state diagrams use the following variables:

class_num_events

A variable indicating the number of classification events performed by the PSE. A variable that is set in an implementation-dependent manner.

Values: 0: PSE does not perform Physical Layer classification.
1: PSE performs 1-Event Physical Layer classification.
2: PSE performs 2-Event Physical Layer classification.

error_condition

A variable indicating the status of implementation-specific fault conditions or optionally other system faults that prevent the PSE from meeting the specifications in Table 33–11 and that require the PSE not to source power. These error conditions are different from those monitored by the state diagrams in Figure 33–10.

Values: FALSE: No fault indication.
TRUE: A fault indication exists.

I_{Inrush}

Output current during POWER_UP (see Table 33–11 and Figure 33–13).

I_{Port}

Output current (see 33.2.7.6).

legacy_powerup

This variable is provided for PSEs that monitor the PI voltage output and use that information to indicate the completion of PD inrush current during POWER_UP operation. Using only the PI voltage information may be insufficient to determine the true end of PD inrush current; use of a fixed T_{Inrush} period is recommended. A variable that is set in an implementation-dependent manner.

Values: TRUE: The PSE supports legacy power up; this value is not recommended.
FALSE: The PSE does not support legacy power up. It is highly recommended that new equipment use this value.

mr_mps_valid

The PSE monitors either the DC or AC Maintain Power Signature (MPS, see 33.2.9.1). This variable indicates the presence or absence of a valid MPS.

Values: FALSE: If monitoring both components of the MPS, the DC component of MPS is absent or the AC component of MPS is absent. If monitoring only one component of MPS, that component of MPS is absent.
TRUE: If monitoring both components of the MPS, the DC component of MPS and the AC component of MPS are both present. If monitoring only one component of MPS, that component of MPS is present.

mr_pse_alternative

This variable indicates which Pinout Alternative the PSE uses to apply power to the link (see Table 33–2). This variable is provided by a management interface that may be mapped to the PSE Control register Pair Control bits (11.3:2) or other equivalent function.

Values: A: The PSE uses PSE pinout Alternative A.
B: The PSE uses PSE pinout Alternative B.

mr_pse_enable

A control variable that selects PSE operation and test functions. This variables is provided by a management interface that may be mapped to the PSE Control register PSE Enable bits (11.1:0), as described below, or other equivalent functions.

Values: disable: All PSE functions disabled (behavior is as if there was no PSE functionality). This value corresponds to MDIO register bits 11.1:0 = '00'.
enable: Normal PSE operation. This value corresponds to MDIO register bits 11.1:0 = '01'.
force_power: Test mode selected that causes the PSE to apply power to the PI when there are no detected error conditions. This value corresponds to MDIO register bits 11.1:0 = '10'.

option_detect_ted

This variable indicates if detection can be performed by the PSE during the ted_timer interval.

Values: FALSE: Do not perform detection during ted_timer interval.
TRUE: Perform detection during ted_timer interval.

option_vport_lim

This optional variable indicates if V_{PSE} is out of the operating range during normal operating state.

Values: FALSE: V_{PSE} is within the V_{Port_PSE} operating range as defined in Table 33–11.
TRUE: V_{PSE} is outside of the V_{Port_PSE} operating range as defined in Table 33–11.

ovld_detected

A variable indicating if the PSE output current has been in an overload condition (see 33.2.7.6) for at least T_{CUT} of a one second sliding time.

Values: FALSE: The PSE has not detected an overload condition.
TRUE: The PSE has detected an overload condition.

pd_dll_power_type

A control variable output by the PSE power control state diagram (Figure 33–27) that indicates the type of PD as advertised through Data Link Layer classification.

Values: 1: PD is a Type 1 PD (default)
2: PD is a Type 2 PD

pi_powered

A variable that controls the circuitry that the PSE uses to power the PD.

Values: FALSE: The PSE is not to apply power to the link (default).
TRUE: The PSE has detected a PD, classified it if applicable, and determined the PD is to be powered; or power is being forced on in TEST_MODE.

power_applied

A variable indicating that the PSE has begun steady state operation by having asserted pi_powered, completed the ramp of voltage, is not in a current limiting mode, and is operating beyond the POWER_UP requirements of 33.2.7.5.

Values: FALSE: The PSE is either not applying power or has begun applying power but is still in POWER_UP.
TRUE: The PSE has begun steady state operation.

power_not_available

Variable that is asserted in an implementation-dependent manner when the PSE is no longer capable of sourcing sufficient power to support the attached PD. Sufficient power is defined by classification; see 33.2.6.

Values: FALSE: PSE is capable to continue to source power to a PD.
TRUE: PSE is no longer capable of sourcing power to a PD.

pse_available_power

This variable indicates the highest power PD Class that could be supported. The value is determined in an implementation-specific manner.

Values: 0: Class 1
1: Class 2
2: Class 0 and Class 3
3: Class 4

pse_dll_capable

This variable indicates whether the PSE is capable of performing optional Data Link Layer classification. See 33.6. This variable is provided by a management interface that may be mapped to the PSE Control register Data Link Layer Classification Capability bit (11.5), as described below, or other equivalent functions. A variable that is set in an implementation-dependent manner.

Values: FALSE: The PSE's Data Link Layer classification capability is not enabled.
TRUE: The PSE's Data Link Layer classification capability is enabled.

pse_dll_enabled

A variable indicating whether the Data Link Layer classification mechanism is enabled. See 33.6.

Values: FALSE: Data Link Layer classification is not enabled.
TRUE: Data Link Layer classification is enabled.

pse_ready

Variable that is asserted in an implementation-dependent manner to probe the link segment.

Values: FALSE: PSE is not ready to probe the link segment.
TRUE: PSE is ready to probe the link segment.

NOTE—Care should be taken when negating this variable in a PSE performing detection using Alternative A after an invalid signature is detected due to the delay it introduces between detection attempts (see 33.2.4.1).

pse_reset

Controls the resetting of the PSE state diagram. Condition that is TRUE until such time as the power supply for the device that contains the PSE overall state diagrams has reached the operating region. It is also TRUE when implementation-specific reasons require reset of PSE functionality.

Values: FALSE: Do not reset the PSE state diagram.
TRUE: Reset the PSE state diagram.

pse_skips_event2

The PSE can choose to bypass a portion of the classification state flow. A variable that is set in an implementation-dependent manner.

Values: FALSE: The PSE does not bypass MARK_EV1.
TRUE: The PSE does bypass MARK_EV1.

short_detected

A variable indicating if the PSE output current has been in a short circuit condition for T_{LIM} within a sliding window (see 33.2.7.7).

Values: FALSE: The PSE has not detected a short circuit condition.
TRUE: The PSE has detected qualified short circuit condition.

temp_var

A temporary variable used to store the value of the state variable mr_pd_class_detected.

PSEs shall meet at least one of the allowable variable definition permutations described in Table 33–3.

Table 33–3—Allowed PSE variable definition permutations

PSE Type	Variables	
	class_num_events	**pse_dll_capable**
Type 2	2	FALSE
		TRUE
	1	TRUE
Type 1	1	FALSE
		TRUE
	0	FALSE
		TRUE

33.2.4.5 Timers

All timers operate in the manner described in 14.2.3.2 with the following addition: a timer is reset and stops counting upon entering a state where "stop x_timer" is asserted.

tcle1_timer
: A timer used to limit the first classification event time in 2-Event classification; see T_{CLE1} in Table 33–10.

tcle2_timer
: A timer used to limit the second classification event time in 2-Event classification; see T_{CLE2} in Table 33–10.

tdbo_timer
: A timer used to regulate backoff upon detection of an invalid signature; see T_{dbo} in Table 33–11.

tdet_timer
: A timer used to limit an attempt to detect a PD; see T_{det} in Table 33–11.

ted_timer
: A timer used to regulate a subsequent attempt to power a PD after an error condition causes power removal; see T_{ed} in Table 33–11. The default state of this timer is ted_timer_done.

tinrush_timer
: A timer used to monitor the duration of the inrush event; see T_{Inrush} in Table 33–11.

tme1_timer
: A timer used to limit the first mark event time in 2-Event classification; see T_{ME1} in Table 33–10.

tme2_timer
: A timer used to limit the second mark event time in 2-Event classification; see T_{ME2} in Table 33–10.

tmpdo_timer
: A timer used to monitor the dropout of the MPS; see T_{MPDO} in Table 33–11.

tpdc_timer
: A timer used to limit the classification time; see T_{pdc} in Table 33–10.

tpon_timer
: A timer used to limit the time for power turn-on; see T_{pon} in Table 33–11.

33.2.4.6 Functions

do_classification
: This function returns the following variables:

  pd_requested_power: This variable indicates the power class requested by the PD. A Type 1 PSE that measures a Class 4 signature assigns that PD to Class 0. See 33.2.6.

  Values:
  - 0: Class 1
  - 1: Class 2
  - 2: Class 0 or Class 3
  - 3: Class 4

  mr_pd_class_detected: The class of the PD associated with the PD classification signature; see Table 33–7 and 33.2.6.

  Values:
  - 0: Class 0
  - 1: Class 1
  - 2: Class 2
  - 3: Class 3
  - 4: Class 4

do_detection

This function returns the following variables:

signature:

This variable indicates the presence or absence of a PD.

Values:	open_circuit:	The PSE has detected an open circuit. This value is optionally returned by a PSE performing detection using Alternative B.
	valid:	The PSE has detected a PD requesting power.
	invalid:	Neither open_circuit, nor valid PD detection signature has been found.

mr_valid_signature:

This variable indicates that the PSE has detected a valid signature.

Values:	FALSE:	No valid signature detected.
	TRUE:	Valid signature detected.

do_mark

This function produces the classification mark event voltage. This function does not return any variables.

set_parameter_type

This function is used by a Type 2 PSE to evaluate the type of PD connected to the link based on Physical Layer classification or Data Link Layer classification results. The PSE's PI electrical requirements defined in Table 33–11 are set to values corresponding to either a Type 1 or Type 2 PSE. This function returns the following variable:

parameter_type: A variable used by a Type 2 PSE to pick between Type 1 and Type 2 PI electrical requirement parameter values defined in Table 33–11.

Values:	1:	Type 1 PSE parameter values (default)
	2:	Type 2 PSE parameter values

When a Type 2 PSE powers a Type 2 PD, the PSE may choose to assign a value of '1' to parameter_type if mutual identification is not complete (see 33.2.6) and shall assign a value of '2' to parameter_type if mutual identification is complete.

When a Type 2 PSE powers a Type 1 PD, the PSE shall meet the PI electrical requirements of a Type 1 PSE, but may choose to meet the electrical requirements of a Type 2 PSE for I_{Con}, I_{LIM}, T_{LIM}, and P_{Type} (see Table 33–11).

33.2.4.7 State diagrams

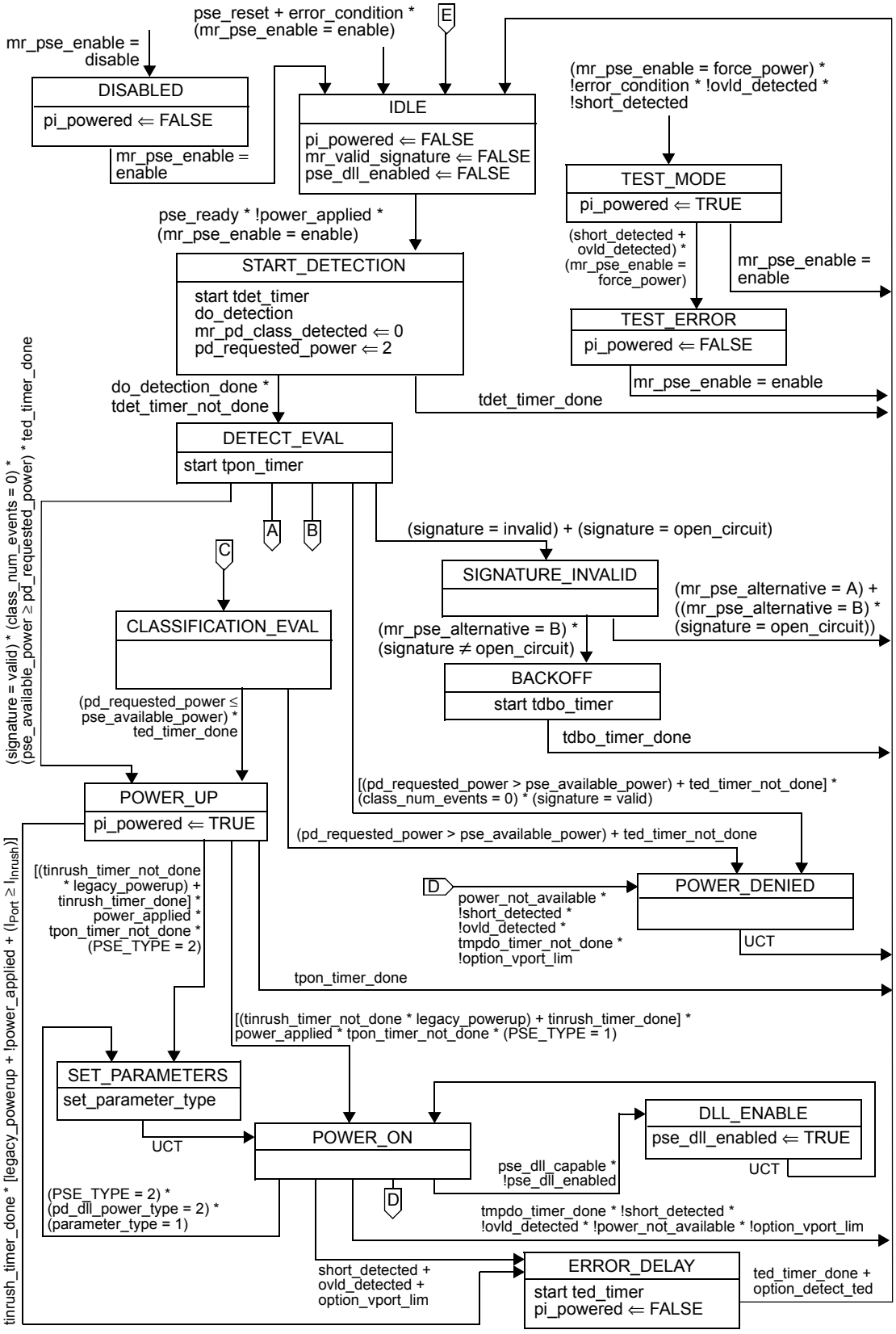


Figure 33–9—PSE state diagram

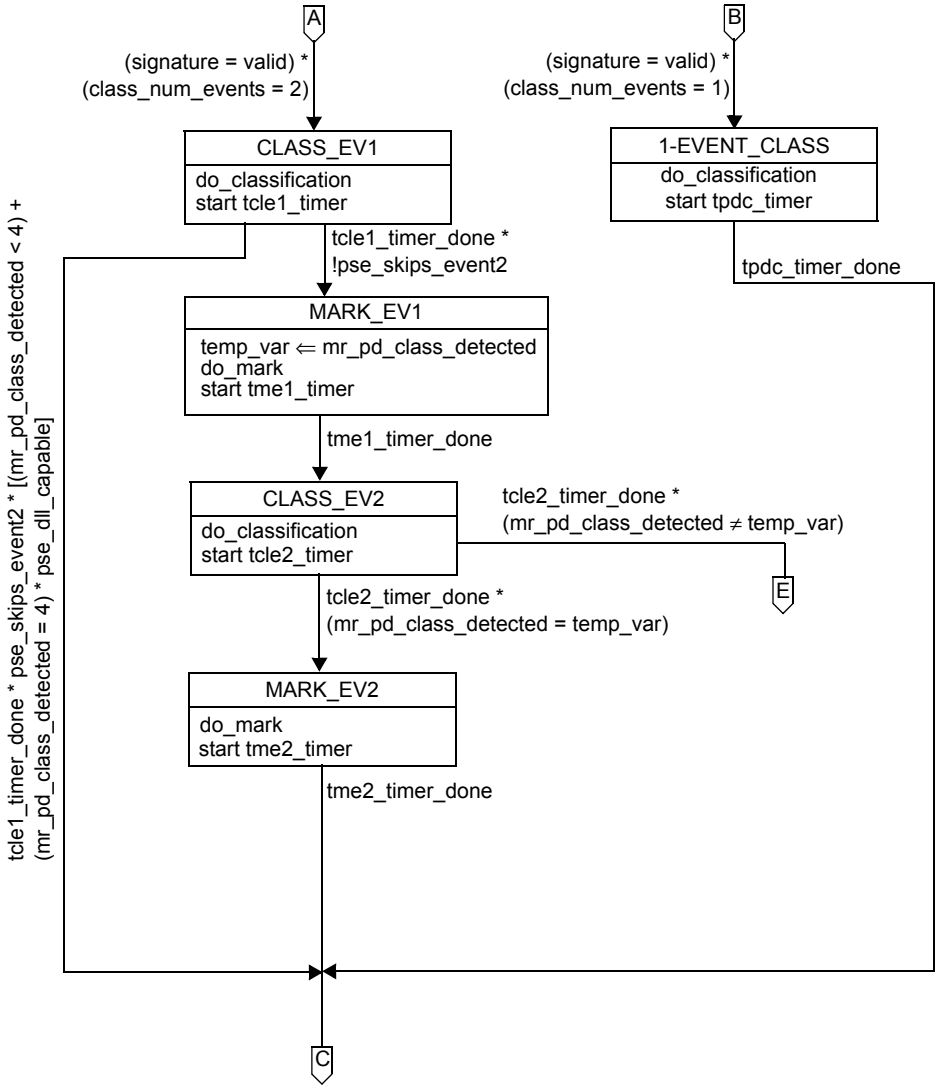


Figure 33–9—PSE state diagram *(continued)*

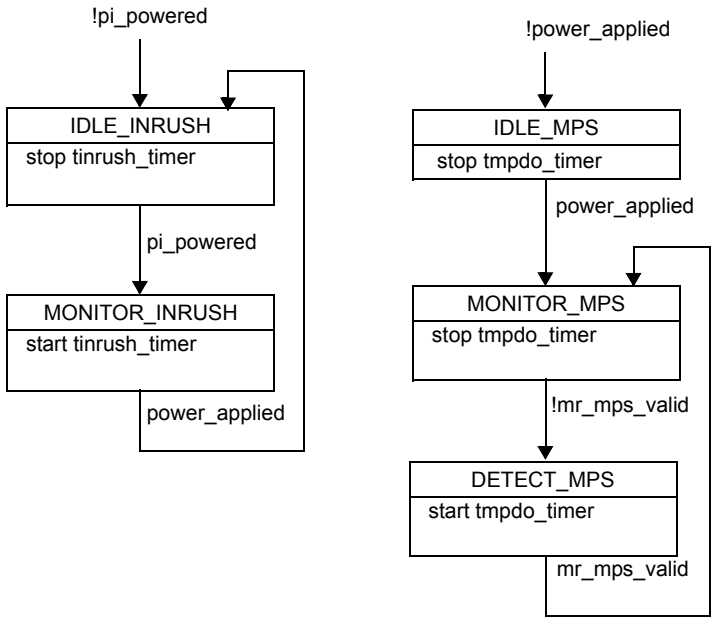


Figure 33–10—PSE monitor inrush and monitor MPS state diagrams

33.2.5 PSE detection of PDs

In any operational state, the PSE shall not apply operating power to the PI until the PSE has successfully detected a PD requesting power.

The PSE probes the link section in order to detect a valid PD detection signature. The PSE PI is connected to a PD through a link segment. In the following subclauses, the link is not called out to preserve clarity.

The PSE is not required to continuously probe to detect a PD signature. The period of time when a PSE is not attempting to detect a PD signature is implementation dependent. Also, a PSE may successfully detect a PD but then opt not to power the detected PD.

The PSE shall turn on power only on the same pairs as those used for detection.

33.2.5.1 PSE detection validation circuit

The PSE shall detect the PD by probing via the PSE PI. The PSE shall present a non-valid PD detection signature as defined in Table 33–15 when probed in either polarity by another PSE. An illustrative embodiment of a detection circuit is shown in Figure 33–11.

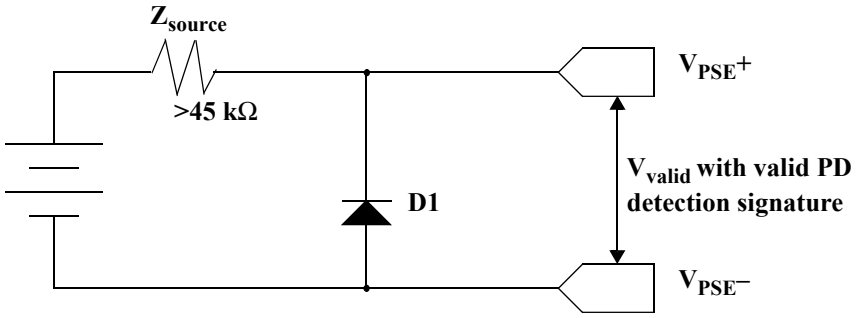


Figure 33–11—PSE detection source

A functional equivalent of the detection circuit that has no source impedance limitation but restricts the PSE detection circuit to the first quadrant is shown in Figure 33–12.

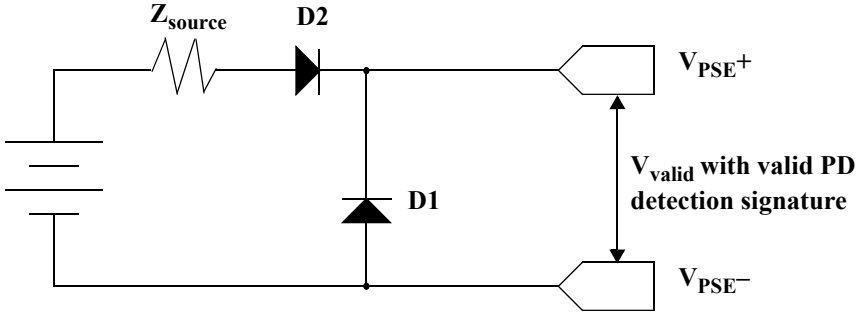


Figure 33–12—Alternative PSE detection source

In Figure 33–11 and Figure 33–12, the diode D1 presents a non-valid PD detection signature for a reversed voltage PSE to PSE connection.

The open circuit voltage and short circuit current shall meet the specifications in Table 33–4. The PSE shall not be damaged by up to 5 mA backdriven current over the range of V_{oc} as specified in Table 33–4. Output capacitance shall be as specified in Table 33–11.

Table 33–4—PSE PI detection state electrical requirements

Item	Parameter	Symbol	Unit	Min	Max	Additional information
1	Open circuit voltage	V_{oc}	V		30.0	In detection state only
2	Short circuit current	I_{sc}	A		0.005	In detection state only
3	Valid test voltage	V_{valid}	V	2.80	10.0	—
4	Voltage difference between test points	ΔV_{test}	V	1.00		—
5	Slew rate	V_{slew}	V/µs		0.100	—

33.2.5.2 Detection probe requirements

The detection voltage at the PSE PI shall be within the V_{valid} voltage range (as specified in Table 33–4) with a valid PD detection signature connected (as specified in Table 33–14).

In evaluating the presence of a valid PD, the PSE shall make at least two measurements with V_{PSE} values that create at least a ΔV_{test} difference as specified in Table 33–4. An effective resistance is calculated from two voltage/current measurements made during the detection process.

The resistance is calculated with Equation (33–2):

$$R = \left\{ \frac{(V_2 - V_1)}{(I_2 - I_1)} \right\}_{\Omega} \quad (33–2)$$

where

V_1 and V_2 are the first and second voltage measurements made at the PSE PI, respectively
I_1 and I_2 are the first and second current measurements made at the PSE PI, respectively
R is the effective resistance

Attached PI capacitance may be determined using these measurements and the port RC time-constant charging characteristics.

NOTE—Settling time before voltage or current measurement: the voltage or current measurement should be taken after V_{PSE} has settled to within 1 % of its steady state condition with a valid PD detection signature connected (as specified in Table 33–14).

The PSE shall control the slew rate of the probing detection voltage when switching between detection voltages to be less than V_{slew} as specified in Table 33–4.

33.2.5.3 Detection criteria

A PSE shall accept as a valid signature a link section with both of the following characteristics between the powering pairs with an offset voltage up to V_{os} max and an offset current up to I_{os} max, as specified in Table 33–5:

a) Signature resistance R_{good}, and
b) Parallel signature capacitance C_{good}.

Table 33–5—Valid PD detection signature electrical characteristics

Item	Parameter	Symbol	Unit	Min	Max	Additional information
1	Accept signature resistance	R_{good}	kΩ	19.0	26.5	—
2	Accept signature capacitance	C_{good}	µF		0.150	—
3	Signature offset voltage tolerance	V_{os}	V	0	2.00	—
4	Signature offset current tolerance	I_{os}	µA	0	12.0	—

CAUTION

In a multiport system, the implementor should maintain DC isolation through the termination circuitry to eliminate cross-port leakage currents.

33.2.5.4 Rejection criteria

The PSE shall reject link sections as having an invalid signature, when those link sections exhibit any of the following characteristics between the powering pairs, as specified in Table 33–6:

a) Resistance less than or equal to R_{bad} min, or
b) Resistance greater than or equal to R_{bad} max, or
c) Capacitance greater than or equal to C_{bad} min.

A PSE may accept or reject a signature resistance in the band between R_{good} min and R_{bad} min, and in the band between R_{good} max and R_{bad} max. A PSE may accept or reject a parallel signature capacitance in the band between C_{good} max and C_{bad} min.

In instances where the resistance and capacitance meet the detection criteria, but one or both of the offset tolerances are exceeded, the detection behavior of the PSE is undefined.

Table 33–6—Invalid PD detection signature electrical characteristics

Item	Parameter	Symbol	Unit	Min	Max	Additional information
1	Reject signature resistance	R_{bad}	kΩ	15.0	33.0	—
2	Reject signature capacitance	C_{bad}	µF	10.0		—
3	Open circuit resistance	R_{open}	MΩ	0.500		—

33.2.5.5 Open circuit criteria

If a PSE that is performing detection using Alternative B (see 33.2.3) determines that the impedance at the PI is greater than R_{open} as defined in Table 33–4, it may optionally consider the link to be open circuit and omit the tdbo_timer interval.

33.2.6 PSE classification of PDs and mutual identification

The ability for the PSE to query the PD in order to determine the power requirements of that PD is called classification. The interrogation and power classification function is intended to establish mutual identification and is intended for use with advanced features such as power management.

Mutual identification is the mechanism that allows a Type 2 PD to differentiate Type 1 PSEs from Type 2 PSEs. Additionally, mutual identification allows Type 2 PSEs to differentiate between Type 1 and Type 2 PDs. PDs or PSEs that do not implement classification will not be able to complete mutual identification and can only perform as Type 1 devices.

There are two forms of classification: Physical Layer classification and Data Link Layer classification.

Physical Layer classification occurs before a PSE supplies power to a PD when the PSE asserts a voltage onto the PI and the PD responds with a current representing a limited number of power classifications. Based on the response of the PD, the minimum power level at the output of the PSE is P_{Class} as shown in Equation (33–3). Physical Layer classification encompasses two methods, known as 1-Event Physical Layer classification (see 33.2.6.1) and 2-Event Physical Layer classification (see 33.2.6.2).

The minimum power output by the PSE for a particular PD class is defined by Equation (33–3). Alternatively, PSE implementations may use $V_{PSE} = V_{Port\_PSE}$ min and $R_{Chan} = R_{Ch}$ max to arrive at over-margined values as shown in Table 33–7.

$$P_{Class} = \left\{ V_{PSE} \times \left(\frac{V_{PSE} - \sqrt{V_{PSE}^2 - 4 \times R_{Chan} \times P_{Class\_PD}}}{2 \times R_{Chan}} \right) \right\}_W \quad (33\text{–}3)$$

where

V_{PSE} is the voltage at the PSE PI as defined in 1.4

R_{Chan} is the channel DC pair loop resistance

P_{Class_PD} is the PD's power classification (see Table 33–18)

Table 33–7—Physical Layer power classifications (P_{Class})

Class	Minimum power levels at output of PSE (P_{Class})
0	15.4 Watts
1	4.00 Watts
2	7.00 Watts
3	15.4 Watts
4	P_{Type} as defined in Table 33–11
NOTE 1—This is the minimum power at the PSE PI. For maximum power available to PDs, see Table 33–18. NOTE 2—Data Link Layer classification takes precedence over Physical Layer classification.	

With Data Link Layer classification, the PSE and PD communicate using the Data Link Layer Protocol (see 33.6) after the data link is established. The Data Link Layer classification has finer power resolution and the ability for the PSE and PD to participate in dynamic power allocation wherein allocated power to the PD may change one or more times during PD operation.

A PSE shall meet one of the allowable classification permutations listed in Table 33–8.

Subsequent to successful detection, a Type 1 PSE may optionally classify a PD using 1-Event Physical Layer classification. Valid classification results are Classes 0, 1, 2, 3, and 4, as listed in Table 33–7. If a Type 1 PSE does not implement classification, then the Type 1 PSE shall assign all PDs to Class 0. A Type 1 PSE may optionally implement Data Link Layer classification.

Table 33–8—PSE and PD classification permutations

Permutations			PSE allowed?	PD allowed?
PSE/PD Type	Physical Layer classification	Data Link Layer classification		
Type 2	2-Event	No	Yes	No
		Yes	Yes	Yes
	1-Event	No	No	No
		Yes	Yes	No
	None	No	No	No
		Yes	No	No
Type 1	2-Event	No	No	Yes
		Yes	No	Yes
	1-Event	No	Yes	Yes
		Yes	Yes	Yes
	None	No	Yes	No
		Yes	Yes	No

Subsequent to successful detection, all Type 2 PSEs perform classification using at least one of the following: 2-Event Physical Layer classification; 2-Event Physical Layer classification and Data Link Layer classification; or 1-Event Physical Layer classification and Data Link Layer classification.

If a PSE successfully completes detection of a PD, but the PSE fails to complete classification of a PD, then a Type 1 PSE shall either return to the IDLE state or assign the PD to Class 0; a Type 2 PSE shall return to the IDLE state.

33.2.6.1 PSE 1-Event Physical Layer classification

When 1-Event Physical Layer classification is implemented, classification consists of the application of V_{Class} and the measurement of I_{Class} in a single classification event—1-EVENT_CLASS—as defined in the state diagram in Figure 33–9.

The PSE shall provide to the PI V_{Class} with a current limitation of I_{Class_LIM}, as defined in Table 33–10. Polarity shall be the same as defined for V_{Port_PSE} in 33.2.3 and timing specifications shall be as defined by T_{pdc} in Table 33–10.

The PSE shall measure the resultant I_{Class} and classify the PD based on the observed current according to Table 33–9. All measurements of I_{Class} shall be taken after the minimum relevant class event timing in Table 33–10. This measurement is referenced from the application of V_{Class} min to ignore initial transients.

If the result of the class event is Class 4, a Type 1 PSE shall assign the PD to Class 0; a Type 2 PSE treats the PD as a Type 2 PD but may provide Class 0 power until mutual identification is complete.

If the measured I_{Class} is within the range of I_{Class_LIM}, a Type 1 PSE shall either return to the IDLE state or classify the PD as Class 0; a Type 2 PSE shall return to the IDLE state.

33.2.6.2 PSE 2-Event Physical Layer classification

When 2-Event Physical Layer classification is implemented, classification consists of the application of V_{Class} and the measurement of I_{Class} in a series of classification and mark events—CLASS_EV1, MARK_EV1, CLASS_EV2, and MARK_EV2—as defined in the state diagram in Figure 33–9.

The PSE in the state CLASS_EV1 shall provide to the PI V_{Class} as defined in Table 33–10. The timing specification shall be as defined by T_{CLE1} in Table 33–10. The PSE shall measure I_{Class} and classify the PD based on the observed current according to Table 33–9.

When the PSE is in the state MARK_EV1, the PSE shall provide to the PI V_{Mark} as defined in Table 33–10. The timing specification shall be as defined by T_{ME1} in Table 33–10.

When the PSE is in the state CLASS_EV2, the PSE shall provide to the PI V_{Class}, subject to the T_{CLE2} timing specification, as defined in Table 33–10. The PSE shall measure I_{Class} and classify the PD based on the observed current according to Table 33–9.

When the PSE is in the state MARK_EV2, the PSE shall provide to the PI V_{Mark} as defined in Table 33–10. The timing specification shall be as defined by T_{ME2} in Table 33–10.

The mark event states, MARK_EV1 and MARK_EV2, commence when the PI voltage falls below V_{Class} min and end when the PI voltage exceeds V_{Class} min. The V_{Mark} requirement is to be met with load currents in the range of I_{Mark} as defined in Table 33–17.

NOTE—In a properly operating system, the port may or may not discharge to the V_{Mark} range due to the combination of channel and PD capacitance and PD current loading. This is normal and acceptable system operation. For compliance testing, it is necessary to discharge the port in order to observe the V_{Mark} voltage. Discharge can be accomplished with a 2 mA load for 3 ms, after which V_{Mark} can be observed with minimum and maximum load current.

If any measured I_{Class} is equal to or greater than I_{Class_LIM} min as defined in Table 33–10, a Type 2 PSE shall return to the IDLE state. The class events shall meet the I_{Class_LIM} current limitation. The mark events shall meet the I_{Mark_LIM} current limitation. All measurements of I_{Class} shall be taken after the minimum relevant class event timing of Table 33–10. This measurement is referenced from the application of V_{Class} min to ignore initial transients.

All class event voltages and mark event voltages shall have the same polarity as defined for V_{Port_PSE} in 33.2.3. The PSE shall complete 2-Event Physical Layer classification and transition to the POWER_ON state without allowing the voltage at the PI to go below V_{Mark} min. If the PSE returns to the IDLE state, it shall maintain the PI voltage at V_{Reset} for a period of at least T_{Reset} min before starting a new detection cycle.

If the result of the first class event is Class 4, the PSE may omit the subsequent mark and class events only if the PSE implements Data Link Layer classification. In this case, a Type 2 PSE treats the PD as a Type 2 PD but may provide Class 0 power until mutual identification is complete.

If the result of the first class event is any of Classes 0, 1, 2, or 3, the PSE treats the PD as a Type 1 PD and may omit the subsequent mark and class events and classify the PD according to the result of the first class event.

Table 33–9—PD classification

Measured I_{Class}	Classification
0 mA to 5.00 mA	Class 0
> 5.00 mA and < 8.00 mA	May be Class 0 or 1
8.00 mA to 13.0 mA	Class 1
> 13.0 mA and < 16.0 mA	Either Class 1 or 2
16.0 mA to 21.0 mA	Class 2
> 21.0 mA and < 25.0 mA	Either Class 2 or 3
25.0 mA to 31.0 mA	Class 3
> 31.0 mA and < 35.0 mA	Either Class 3 or 4
35.0 mA to 45.0 mA	Class 4
> 45.0 mA and < 51.0 mA	Either Class 4 or invalid class

NOTE—A Type 1 PSE may ignore I_{Class} and report Class 0.

Table 33–10—PSE Physical Layer classification electrical requirements

Item	Parameter	Symbol	Units	Min	Max	1- or 2-Event	Additional information
1	Class event voltage	V_{Class}	V	15.5	20.5	1, 2	
2	Class event current limitation	I_{Class_LIM}	A	0.051	0.100	1, 2	
3	Mark event voltage	V_{Mark}	V	7.00	10.0	2	
4	Mark event current limitation	I_{Mark_LIM}	A	0.005	0.100	2	
5	1^{st} class event timing	T_{CLE1}	ms	6.00	30.0	2	
6	1^{st} mark event timing	T_{ME1}	ms	6.00	12.0	2	
7	2^{nd} class event timing	T_{CLE2}	ms	6.00	30.0	2	
8	2^{nd} mark event timing	T_{ME2}	ms	6.00		2	Time from end of detection until power-on is limited by 33.2.7.12.
9	Classification reset voltage	V_{Reset}	V	0	2.80	2	
10	Classification reset timing	T_{Reset}	ms	15.0		2	
11	1-Event Physical Layer classification timing	T_{pdc}	ms	6.00	75.0	1	

33.2.7 Power supply output

PSE behavior conforms to the state diagrams in Figure 33–9, Figure 33–9, and Figure 33–10. When the PSE provides power to the PI, it shall conform with Table 33–11.

Table 33–11 limits show values that support worst-case operating limits. These ranges may be narrowed when additional information is known and applied in accordance with this specification.

Table 33–11—PSE output PI electrical requirements for all PD classes, unless otherwise specified

Item	Parameter	Symbol	Unit	Min	Max	PSE Type	Additional information
1	Output voltage in the POWER_ON state	V_{Port_PSE}	V	44.0	57.0	1	See 33.2.7.1.
				50.0	57.0	2	
2	Voltage transient below V_{Port_PSE} min	K_{Tran_lo}	%		7.6	2	See 33.2.7.2.
3	Power feeding ripple and noise:						
	f < 500 Hz		V_{pp}		0.500	1, 2	See 33.2.7.3.
	500 Hz to 150 kHz				0.200		
	150 kHz to 500 kHz				0.150		
	500 kHz to 1 MHz				0.100		
4	Continuous output current capability in POWER_ON state	I_{Con}	A	P_{Class} / V_{Port_PSE}		1, 2	See 33.2.7.4.
5	Output current in POWER_UP state	I_{Inrush}	A	0.400	See info	1, 2	See 33.2.7.5. Max value defined by Figure 33–13.
6	Inrush time	T_{Inrush}	s	0.050	0.075	1, 2	See 33.2.7.5
7	Overload current detection range	I_{CUT}	A	P_{Class} V_{Port_PSE}	I_{LIM}	1,2	Optional limit; see 33.2.7.6, Table 33–7.
8	Overload time limit	T_{CUT}	s	0.050	0.075	1, 2	See 33.2.7.7
9	Output current – at short circuit condition	I_{LIM}	A	0.400	See info	1	See 33.2.7.7. Max value defined by Figure 33–14.
				1.14 × I_{Cable}		2	
10	Short circuit time limit	T_{LIM}	s	0.050	See info	1	See 33.2.7.7.
				0.010		2	
11	Continuous output power capability in POWER_ON state	P_{Con}	W	P_{Class}		1, 2	See 33.2.7.10, Table 33–7.
12	PSE Type power minimum	P_{Type}	W	I_{Cable} × (V_{Port_PSE} min)		1, 2	See 33.1.4.
13	Power turn on time	T_{pon}	s		0.400	1, 2	See 33.2.7.12.

Table 33–11—PSE output PI electrical requirements for all PD classes, unless otherwise specified *(continued)*

Item	Parameter	Symbol	Unit	Min	Max	PSE Type	Additional information
14	Turn on rise time	T_{Rise}	µs	15.0		1, 2	From 10 % to 90 % of the voltage difference at the PI in POWER_ON state from the beginning of POWER_UP.
15	Turn off time	T_{Off}	s		0.500	1, 2	See 33.2.7.8.
16	Turn off voltage	V_{Off}	V		2.80	1, 2	See 33.2.7.9.
17	DC MPS current	I_{Hold}	A	0.005	0.010	1, 2	See 33.2.9.1.2.
18	PD Maintain Power Signature dropout time limit	T_{MPDO}	s	0.300	0.400	1, 2	See 33.2.9.
19	PD Maintain Power Signature time for validity	T_{MPS}	s	0.060		1, 2	See 33.2.9.
20	Current unbalance	I_{unb}	A		3 % × I_{Cable}	1	See 33.2.7.11, 33.4.8. NOTE—For practical implementations, it is recommended that Type 1 PSEs support Type 2 I_{unb} requirements.
					3 % × I_{Peak}	2	
21	Alternative B detection backoff time	T_{dbo}	s	2.00		1, 2	
22	Output capacitance during detection state	C_{out}	µF		0.520	1, 2	
23	Detection timing	T_{det}	s		0.500	1, 2	Time to complete detection of a PD.
24	Error delay timing	T_{ed}	s	0.750		1, 2	Delay before PSE may attempt subsequent powering after power removal because of error condition.

33.2.7.1 Output voltage in the POWER_ON state

The specification for V_{Port_PSE} in Table 33–11 shall be met with a (I_{Hold} max × V_{Port_PSE} min) to P_{Type} min load step at a rate of change of at least 15 mA/µs. The voltage transients as a result of load changes up to 35 mA/µs shall be limited to 3.5 V/µs max.

A PSE in the POWER_ON state may remove power from the PI when the PI voltage no longer meets the V_{Port_PSE} specification.

33.2.7.2 Voltage transients

A Type 2 PSE shall maintain an output voltage no less than K_{Tran_lo} below V_{Port_PSE} min for transient conditions lasting more than 30 µs and less than 250 µs, and meet the requirements of 33.2.7.7.

Transients less than 30 µs in duration may cause the voltage at the PI to fall more than K_{Tran_lo}. The minimum PD input capacitance allows the PD to operate for any input voltage transient lasting less than 30 µs. Transients lasting more than 250 µs shall meet the V_{Port_PSE} specification.

33.2.7.3 Power feeding ripple and noise

The specification for power feeding ripple and noise in Table 33–11 shall be met for common-mode and/or pair-to-pair noise values for power outputs from (I_{Hold} max × V_{Port_PSE} min) to P_{Type} min for PSEs at static operating V_{Port_PSE}. The limits are meant to preserve data integrity. To meet EMI standards, lower values may be needed. For higher frequencies, see 33.4.4 and 33.4.5.

33.2.7.4 Continuous output current capability in the POWER_ON state

In addition to I_{Con} as specified in Table 33–11, the PSE shall support the following AC current waveform parameters, while within the operating voltage range of V_{Port_PSE}:

I_{Peak} minimum for T_{CUT} minimum and 5 % duty cycle minimum, where

$$I_{Peak} = \left\{ \frac{V_{PSE} - \sqrt{V_{PSE}^2 - 4(R_{Chan})(P_{Peak\_PD})}}{2(R_{Chan})} \right\}_A \quad (33\text{–}4)$$

where

V_{PSE} is the voltage at the PSE PI as defined in 1.4

R_{Chan} is the channel loop resistance as defined in 33.1.4; this parameter has a worst-case value of R_{Ch}, defined in Table 33–1

P_{Peak_PD} is the peak power a PD may draw for its class; see Table 33–18

33.2.7.5 Output current in POWER_UP mode

POWER_UP mode occurs between the PSE's transition to the POWER_UP state and either the expiration of T_{Inrush} or the conclusion of PD inrush currents (see 33.3.7.3). However, for practical implementations, it is recommended that the POWER_UP mode persist for the complete duration of T_{Inrush}, as the PSE may not be able to correctly ascertain the conclusion of a PD's inrush behavior.

The PSE shall limit the maximum current sourced at the PI during POWER_UP. The maximum inrush current sourced by the PSE shall not exceed the PSE inrush template in Figure 33–13.

a) During POWER_UP, for PI voltages between 0 V and 10 V, the minimum I_{Inrush} requirement is 5 mA.
b) During POWER_UP, for PI voltages between 10 V and 30 V, the minimum I_{Inrush} requirement is 60 mA.
c) During POWER_UP, for PI voltages above 30 V, the minimum I_{Inrush} requirement is as specified in Table 33–11.

The PSE inrush template, I_{PSEIT}, is defined by the following segments:

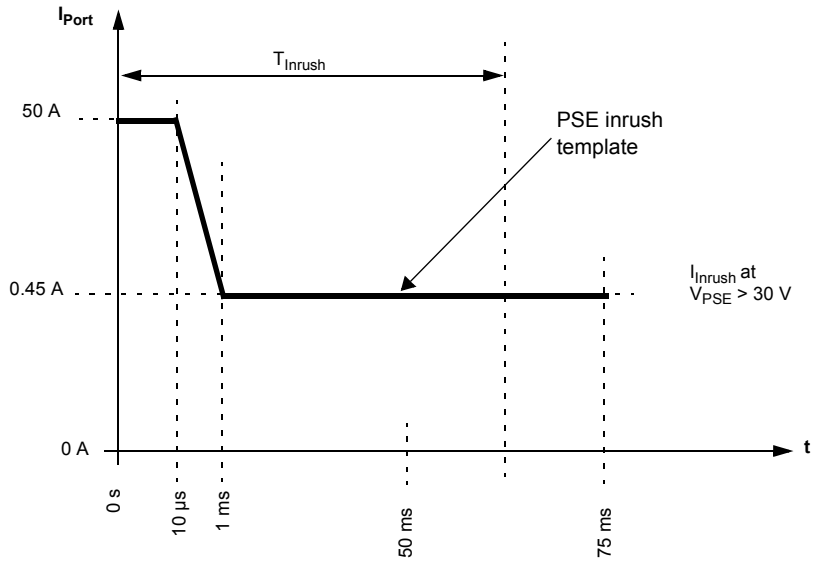


Figure 33–13—I_{Inrush} current and timing limits in POWER_UP state

$$I_{PSEIT}(t) = \left\{ \begin{array}{ll} 50.0 & \text{for } 0 < t < 10.0\times10^{-6} \\ 50.0 - \dfrac{(t - 10.0\times10^{-6}) \times 49.6}{0.990\times10^{-6}} & \text{for } 10.0\times10^{-6} \le t < 0.001 \\ 0.450 & 0.001 \le t < 0.075 \end{array} \right\}_{A} \quad (33\text{–}5)$$

where

t is the time in seconds

33.2.7.6 Overload current

If I_{Port}, the current supplied by the PSE to the PI, exceeds I_{CUT} for longer than T_{CUT}, the PSE may remove power from the PI. The cumulative duration of T_{CUT} is measured with a sliding window of at least 1 second width.

The I_{CUT} threshold may equal the I_{Peak} value determined by Equation (33–4).

33.2.7.7 Output current—at short circuit condition

A PSE may remove power from the PI if the PI current meets or exceeds the “PSE lowerbound template” in Figure 33–14. Power shall be removed from the PI of a PSE before the PI current exceeds the “PSE upperbound template” in Figure 33–14.

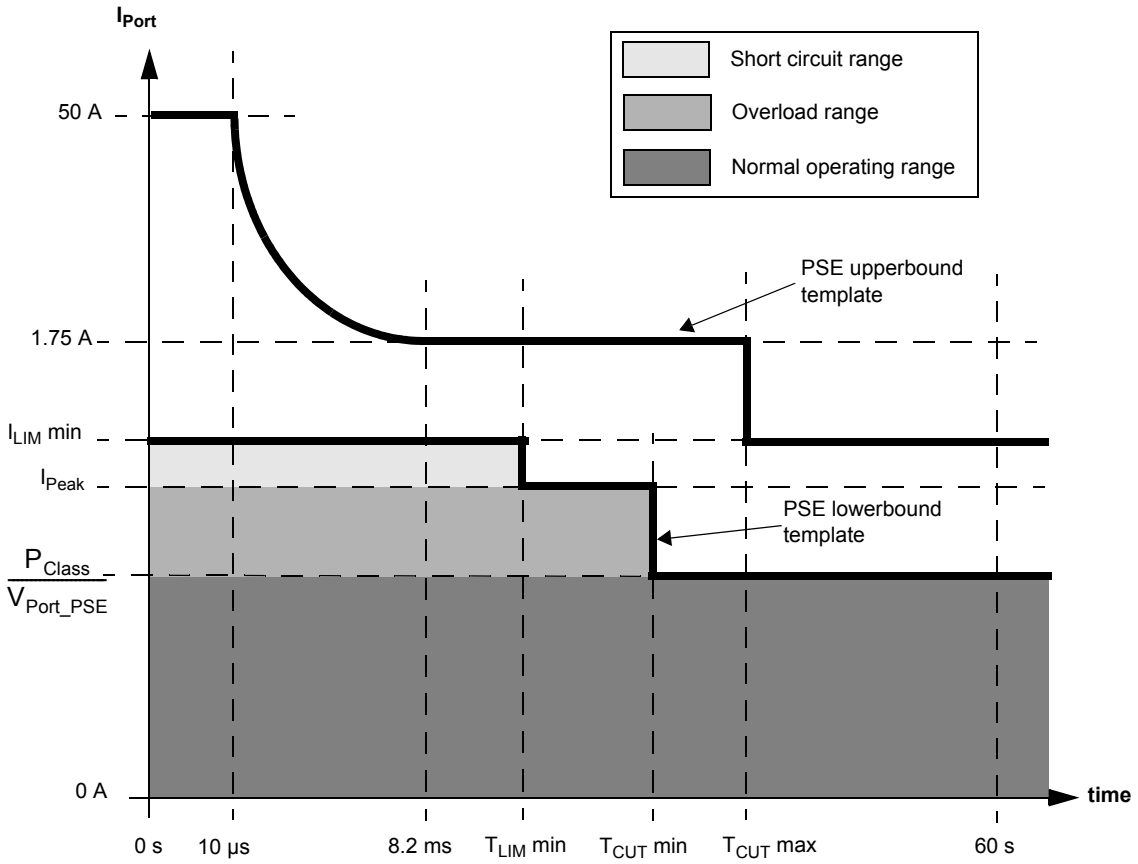


Figure 33–14—POWER_ON state PI operating current templates

The maximum value of I_{LIM} is the PSE upperbound template described by Equation (33–6) and Figure 33–14.

The PSE upperbound template, I_{PSEUT}, is defined by the following segments:

$$I_{\mathrm{PSEUT}}(t) = \left\{ \begin{array}{ll} 50.0 & \text{for } (0 \le t < 10.0\times10^{-6}) \\ \sqrt{\frac{K}{t}} & \text{for } (10.0\times10^{-6} \le t < 8.20\times10^{-3}) \\ 1.75 & \text{for } (8.20\times10^{-3} \le t < T_{\mathrm{cutmax}}) \\ I_{\mathrm{limmin}} & \text{for } (T_{\mathrm{cutmax}} \le t) \end{array} \right\}_{\mathrm{A}} \qquad (33\text{–}6)$$

where

t	is the duration in seconds that the PSE sources I_{Port}
K	is 0.025 A^2s, an energy limitation constant for the port current when it is not in steady state normal operation
T_{cutmax}	is T_{CUT} max, as defined in Table 33–11
I_{limmin}	is I_{LIM} min, as defined in Table 33–11

The PSE shall limit the current to I_{LIM} for a duration of up to T_{LIM} in order to account for PSE dV/dt transients at the PI. The cumulative duration of T_{LIM} may be measured with a sliding window.

The PSE lowerbound template, I_{PSELT}, is defined by the following segments:

$$I_{PSELT}(t) = \left\{ \begin{array}{ll} I_{LIMmin} & \text{for } (0 \le t < T_{limmin}) \\ I_{Peak} & \text{for } (T_{limmin} \le t < T_{cutmin}) \\ \dfrac{P_{Class}}{V_{PSE}} & \text{for } (T_{cutmin} \le t) \end{array} \right\}_{A} \quad (33\text{–}7)$$

where

I_{LIMmin} is the I_{LIM} min value for the PSE (see Table 33–11)
t is the duration that the PI sources I_{Port}
T_{limmin} is T_{LIM} min as defined in Table 33–11
T_{cutmin} is T_{CUT} min, as defined in Table 33–11
I_{Peak} is I_{Peak}, as defined in Equation (33–4)
P_{Class} is P_{Class}, as defined in Table 33–7
V_{PSE} is the voltage at the PSE PI

If a short circuit condition is detected, power removal from the PI shall begin within T_{LIM} as specified in Table 33–11. If I_{Port} exceeds the PSE lowerbound template, the PSE output voltage may drop below V_{Port_PSE} min.

33.2.7.8 Turn off time

The specification for T_{Off} in Table 33–11 shall apply to the discharge time from V_{Port_PSE} to V_{Off} with a test resistor of 320 kΩ attached to the PI. In addition, it is recommended that the PI be discharged when turned off. T_{Off} starts when V_{PSE} drops 1 V below the steady-state value after the pi_powered variable is cleared (see Figure 33–9). T_{Off} ends when $V_{PSE} \le V_{Off}$ max. The PSE remains in the IDLE state as long as the average voltage across the PI is V_{Off}. The IDLE state is the state when the PSE is not in detection, classification, or normal powering states.

33.2.7.9 Turn off voltage

The specification for V_{Off} in Table 33–11 shall apply to the PI voltage in the IDLE State.

33.2.7.10 Continuous output power capability in POWER_ON state

P_{Class} is the class power defined in 33.2.6 and Equation (33–3), or PSE allocated power (as defined in 79.3.2.6) added to the channel power loss.

P_{Con} is valid over the range of V_{Port_PSE} defined in Table 33–11. Measurement of P_{Con} should be averaged using any sliding window with a width of 1 s.

A PSE may remove power from a PD that causes the PSE to source more than P_{Class}.

33.2.7.11 Current unbalance

The specification for I_{unb} in Table 33–11 shall apply to the current unbalance between the two conductors of a power pair over the current load range.

Type 2 Endpoint PSEs shall meet the requirements of 25.4.4a in the presence of (I_{unb} / 2).

33.2.7.12 Power turn on time

The specification for T_{pon} in Table 33–11 applies to the PSE power up time for a PD after completion of detection. If power is not applied as specified, a new detection cycle is initiated (see 33.2.4.1).

33.2.7.13 PSE stability

When connected together as a system, the PSE and PD might exhibit instability at the PSE side or the PD side or both due to the presence of negative impedance at the PD input. See Annex 33A for PSE design guidelines for stable operation.

33.2.8 Power supply allocation

A PSE does not initiate power provision to a link if the PSE is unable to provide the maximum power level requested by the PD based on the PD's class.

The PSE may manage the allocation of power based on additional information beyond the classification of the attached PD. Allocating power based on additional information about the attached PD, and the mechanism for obtaining that additional information, is beyond the scope of this standard with the exception that the allocation of power shall not be based solely on the historical data of the power consumption of the attached PD.

See 33.6 for a description of Data Link Layer classification.

If the system implements a power allocation algorithm, no additional behavioral requirement is placed on the system as it approaches or reaches its maximum power subscription. Specifically, the interaction between one PSE PI and another PSE PI in the same system is beyond the scope of this standard.

33.2.9 PSE power removal

Figure 33–10 shows the PSE monitor state diagrams. These state diagrams monitor for inrush current and the absence of the Maintain Power Signature (MPS).

If any of these conditions exist for longer than its related time limit, the power is removed from the PI.

33.2.9.1 PSE Maintain Power Signature (MPS) requirements

The MPS consists of two components, an AC MPS component and a DC MPS component.

The PSE shall monitor either the DC MPS component, the AC MPS component, or both.

33.2.9.1.1 PSE AC MPS component requirements

A PSE that monitors the AC MPS component shall meet the "AC Signal parameters" and "PSE PI voltage during AC disconnect detection" parameters in Table 33–12.

A PSE shall consider the AC MPS component to be present when it detects an AC impedance at the PI equal to or lower than $|Z_{ac1}|$ as defined in Table 33–12.

A PSE shall consider the AC MPS component to be absent when it detects an AC impedance at the PI equal to or greater than $|Z_{ac2}|$ as defined in Table 33–12. Power shall be removed from the PI when AC MPS has been absent for a time duration greater than T_{MPDO}.

A PSE may consider the AC MPS component to be either present or absent when it detects a AC impedance between the values $|Z_{ac1}|$ max and $|Z_{ac2}|$ min.

33.2.9.1.2 PSE DC MPS component requirements

A PSE shall consider the DC MPS component to be present if I_{Port} is greater than or equal to I_{Hold} max for a minimum of T_{MPS}. A PSE shall consider the DC MPS component to be absent if I_{Port} is less than or equal to I_{Hold} min. A PSE may consider the DC MPS component to be either present or absent if I_{Port} is in the range of I_{Hold}.

Power shall be removed from the PI when DC MPS has been absent for a duration greater than T_{MPDO}.

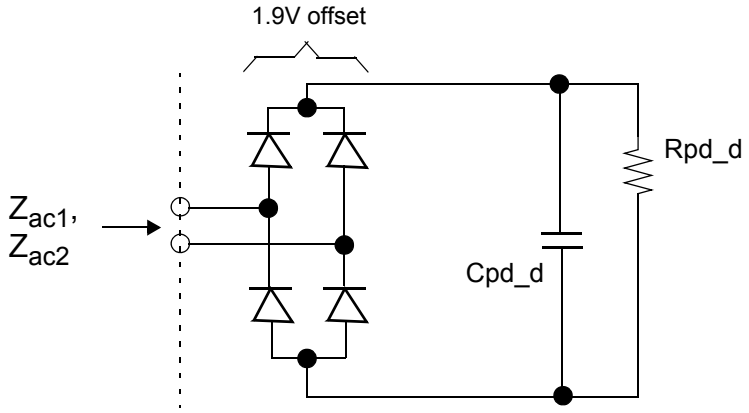
The specification for T_{MPS} in Table 33–11 applies only to the DC MPS component. The PSE shall not remove power from the port when I_{Port} is greater than or equal to I_{Hold} max continuously for at least T_{MPS} every $T_{MPS} + T_{MPDO}$, as defined in Table 33–11. This allows a PD to minimize its power consumption.

Table 33–12—PSE PI parameters for AC disconnect-detection function

Item	Parameter	Symbol	Unit	Min	Max	Additional information
	AC signal parameters					
1a	PI probing AC voltage	V_open	V_{pp}	1.90	10% of the average value of V_{Port_PSE} within the limits of Table 33–11	Includes noise, ripple, etc. V_open is the AC voltage across the PI when the PD is not connected to the PI and before the detection of this condition by the PSE.
		V_open1	V_p		30.0 V, $V_{PSE} \leq$ 44.0 V	V_open1 is the AC voltage across the PI when the PD is not connected to the PI and after the detection of this condition by the PSE and the removal of power from the PI.
1b	AC probing signal frequency	F_p	kHz		0.500	
1c	AC probing signal slew rate	SR	V/µs		0.100	Positive or negative.
	AC source output impedance					
2a	Source output current during the operation of the AC disconnect detection function	I_sac	mA		5.00	During operation of the AC disconnect detection function.
2b	PSE PI impedance during PD detection when measured at the PSE PI	R_rev	kΩ	45.0		Specified in 33.2.5.1 and Figure 33–11. Shown here to clarify the difference in PI impedance during the signature detection function.
	PSE PI voltage during AC disconnect detection					
3a	PI AC voltage when PD is connected	V_{CLOSE}	V_{pp}			See Table 33–11, item 3.

Table 33–12—PSE PI parameters for AC disconnect-detection function *(continued)*

Item	Parameter	Symbol	Unit	Min	Max	Additional information
3b	PI voltage when PD is disconnected	V_{PSE}	V_p		60.0	
	AC Maintain Power Signature					
4a	Valid impedance	$\lvert Z_{ac1} \rvert$	kΩ		27.0	F_p = 5 Hz, Testing voltage >2.5 V. See Figure 33–15.
4b	Invalid impedance	$\lvert Z_{ac2} \rvert$	kΩ	1980		See Figure 33–15.



NOTE—Rpd_d and Cpd_d are specified in Table 33–19. Cpd_d may be located either in parallel with Z_{ac1} or as shown above.

Figure 33–15—Z_{ac1} and Z_{ac2} definition as indicated in Table 33–12

33.3 Powered devices (PDs)

A PD is the portion of a device that is either drawing power or requesting power by participating in the PD detection algorithm. A device that is capable of becoming a powered device may or may not have the ability to draw power from an alternate power source and, if doing so, may or may not require power from the PI. PD capable devices that are neither drawing nor requesting power are also covered in this subclause.

A PD is specified at the point of the physical connection to the cabling. Characteristics such as the losses due to voltage correction circuits, power supply inefficiencies, separation of internal circuits from external ground or other characteristics induced by circuits after the PI connector are not specified. Limits defined for the PD are specified at the PI, not at any point internal to the PD, unless specifically stated.

33.3.1 PD PI

The PD shall be capable of accepting power on either of two sets of PI conductors. The two conductor sets are named Mode A and Mode B. In each four-wire connection, the two wires associated with a pair are at the same nominal average voltage. Figure 33–8 in conjunction with Table 33–13 illustrates the two power modes.

Table 33–13—PD pinout

Conductor	Mode A	Mode B
1	Positive V_{PD}, Negative V_{PD}	
2	Positive V_{P}, Negative V_{PD}	
3	Negative V_{PD}, Positive V_{PD}	
4		Positive V_{PD}, Negative V_{PD}
5		Positive V_{PD}, Negative V_{PD}
6	Negative V_{PD}, Positive V_{PD}	
7		Negative V_{PD}, Positive V_{PD}
8		Negative V_{PD}, Positive V_{PD}

The PD shall be implemented to be insensitive to the polarity of the power supply and shall be able to operate per the PD Mode A column and the PD Mode B column in Table 33–13.

NOTE—PDs that implement only Mode A or Mode B are specifically not allowed by this standard. PDs that simultaneously require power from both Mode A and Mode B are specifically not allowed by this standard.

The PD shall not source power on its PI.

The PD shall withstand any voltage from 0 V to 57 V at the PI indefinitely without permanent damage.

33.3.2 PD type descriptions

PDs can be categorized as either Type 1 or Type 2.

Type 1 PDs implement a minimum of 1-Event Physical Layer classification and advertise a 1-Event class signature of 0, 1, 2, or 3.

Type 2 PDs implement both 2-Event Physical Layer classification (see 33.3.5.2) and Data Link Layer classification (see 33.6) and advertise a 2-Event class signature of 4.

The maximum power a PD expects to draw from a PSE is P_{Class_PD} max as defined in Table 33–18.

A Type 2 PD that does not successfully observe a 2-Event Physical Layer classification or Data Link Layer classification shall conform to Type 1 PD power restrictions and shall provide the user with an active indication if underpowered. The method of active indication is left to the implementor.

Type 2 PDs shall meet the requirements of 25.4.4a in the presence of (I_{unb} / 2).

33.3.3 PD state diagram

The PD state diagram specifies the externally observable behavior of a PD. The PD shall provide the behavior of the state diagram shown in Figure 33–16.

33.3.3.1 Conventions

The notation used in the state diagram follows the conventions of state diagrams as described in 21.5.

33.3.3.2 Constants

The PD state diagram uses the following constants:

V_{Reset_th}
: Reset voltage threshold (see Table 33–17)

V_{Mark_th}
: Mark event voltage threshold (see Table 33–17)

class_sig
: PD classification, one of either 0, 1, 2, 3, or 4 (see Table 33–16)

33.3.3.3 Variables

The PD state diagram uses the following variables:

mdi_power_required
: A control variable indicating the PD is enabled and should request power from the PSE by applying a PD detection signature to the link, and when the PSE sources power to apply the MPS to keep the PSE sourcing power. A variable that is set in an implementation-dependent manner.
  Values: FALSE: PD functionality is disabled.
  TRUE: PD functionality is enabled.

pd_2-event
: A control variable indicating whether the PD presents a 2-Event class signature.
  Values: FALSE: PD does not present a 2-Event class signature.
  TRUE: PD does present a 2-Event class signature.

pd_dll_capable
: This variable indicates whether the PD implements Data Link Layer classification.
  Values: FALSE: The PD does not implement Data Link Layer classification.
  TRUE: The PD does implement Data Link Layer classification.

pd_dll_enabled
: A variable indicating whether the Data Link Layer classification mechanism is enabled.
  Values: FALSE: Data Link Layer classification is not enabled.
  TRUE: Data Link Layer classification is enabled.

pd_max_power
: A control variable indicating the max power that the PD may draw from the PSE. See power classifications in Table 33–18.
  Values: 0: PD may draw Class 0 power
  1: PD may draw Class 1 power
  2: PD may draw Class 2 power
  3: PD may draw Class 3 power
  4: PD may draw Class 4 power

pd_reset
: An implementation-specific control variable that unconditionally resets the PD state diagram to the OFFLINE state.
  Values: FALSE: The device has not been reset (default).
  TRUE: The device has been reset.

power_received
: An indication from the circuitry that power is present on the PD's PI.
  Values: FALSE: The input voltage does not meet the requirements of V_{Port_PD} in Table 33–18.
  TRUE: The input voltage meets the requirements of V_{Port_PD}.

present_class_sig
: Controls presenting the classification signature (see 33.3.5) by the PD.

Values: FALSE: The PD classification signature is not to be applied to the link.
TRUE: The PD classification signature is to be applied to the link.

present_det_sig

Controls presenting the detection signature (see 33.3.4) by the PD.

Values: FALSE: A non-valid PD detection signature is to be applied to the link.
TRUE: A valid PD detection signature is to be applied to the link.

present_mark_sig

Controls presenting the mark event current and impedance (see 33.3.5.2.1) by the PD.

Values: FALSE: The PD does not present mark event behavior.
TRUE: The PD does present mark event behavior.

present_mps

Controls applying MPS (see 33.3.8) to the PD's PI.

Values: FALSE: The Maintain Power Signature (MPS) is not to be applied to the PD's PI.
TRUE: The MPS is to be applied to the PD's PI.

pse_dll_power_type

A control variable output by the PD power control state diagram (Figure 33–28) that indicates the type of PSE by which the PD is being powered.

Values: 1: The PSE is a Type 1 PSE (default).
2: The PSE is a Type 2 PSE.

pse_power_type

A control variable that indicates to the PD the type of PSE by which it is being powered.

Values: 1: The PSE is a Type 1 PSE.
2: The PSE is a Type 2 PSE.

V_{PD}

Voltage at the PD PI as defined in 1.4.

33.3.3.4 Timers

All timers operate in the manner described in 14.2.3.2 with the following addition. A timer is reset and stops counting upon entering a state where "stop x_timer" is asserted.

tpowerdly_timer

A timer used to prevent the Type 2 PD from drawing more than inrush current during the PSE's inrush period; see T_{delay} in Table 33–18.

33.3.3.5 State diagrams

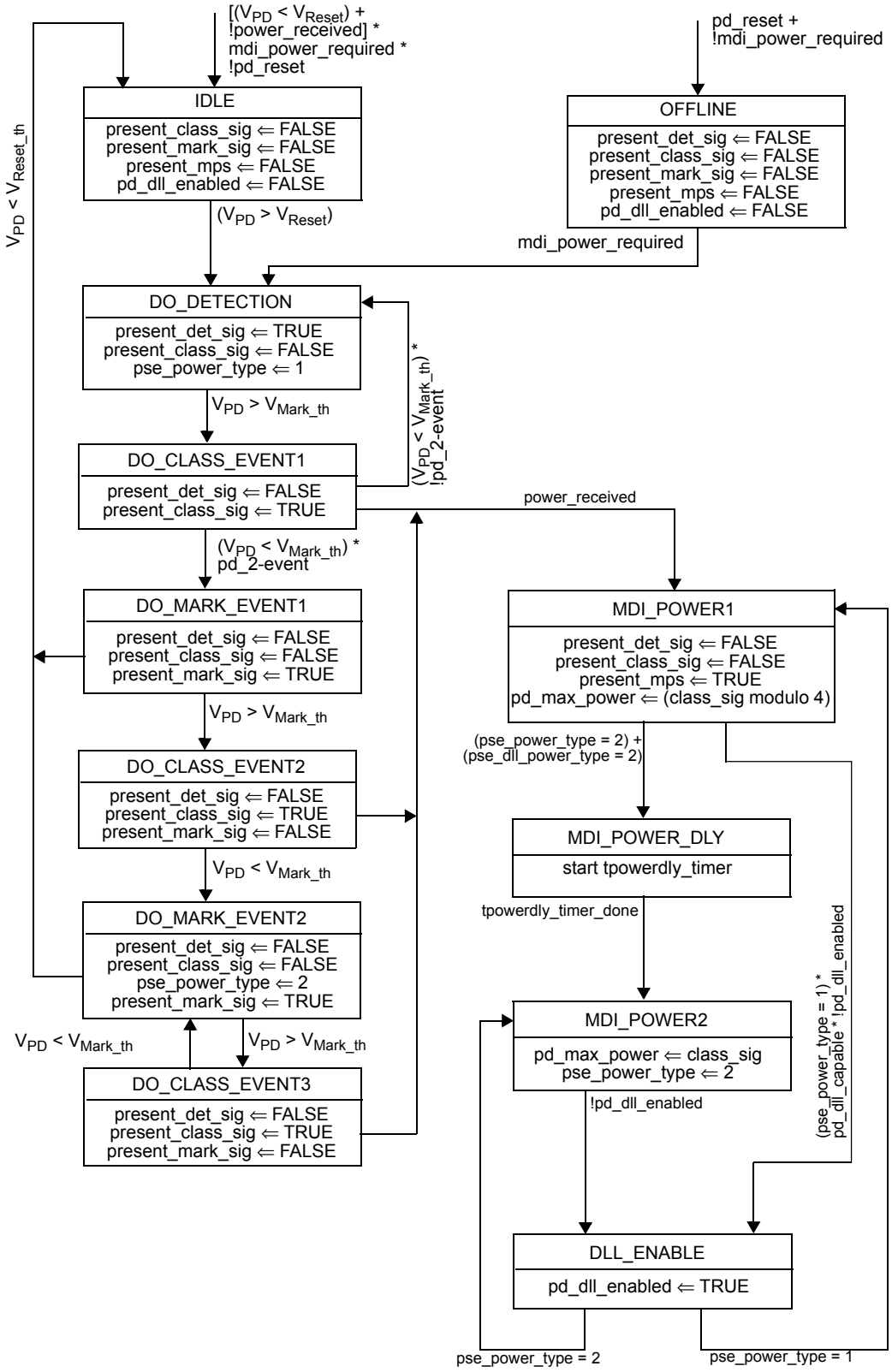


Figure 33–16—PD state diagram

NOTE 1—DO_CLASS_EVENT3 creates a defined behavior for a Type 2 PD that is brought into the classification range repeatedly.

NOTE 2—In general, there is no requirement for a PD to respond with a valid classification signature for any DO_CLASS_EVENT duration less than T_{class}.

33.3.4 PD valid and non-valid detection signatures

A PD presents a valid detection signature while it is in a state where it accepts power via the PI, but is not powered via the PI per Figure 33–16.

A PD presents a non-valid detection signature at the PI while it is in a state where it does not accept power via the PI per Figure 33–16.

A Type 2 PD presents a non-valid detection signature when in a mark event state per Figure 33–16.

When a PD presents a valid or non-valid detection signature, it shall present the detection signature at the PI between Positive V_{PD} and Negative V_{PD} of PD Mode A and PD Mode B as defined in 33.3.1. When a PD becomes powered via the PI, it shall present a non-valid detection signature on the set of pairs from which it is not drawing power.

A PD may or may not present a valid detection signature when in the IDLE state.

The detection signature is a resistance calculated from two voltage/current measurements made during the detection process.

$$R_{\text{detect}} = \left\{ \frac{(V_2 - V_1)}{(I_2 - I_1)} \right\}_{\Omega} \tag{33–8}$$

where

V_1 and V_2	are the first and second voltage measurements made at the PD PI, respectively
I_1 and I_2	are the first and second current measurements made at the PD PI, respectively
R_{detect}	is the effective resistance

A valid PD detection signature shall have the characteristics of Table 33–14.

A non-valid detection signature shall have one or both of the characteristics in Table 33–15.

A PD that presents a signature outside of Table 33–14 is non-compliant, while a PD that present the signature of Table 33–15 is assured to fail detection.

Table 33–14—Valid PD detection signature characteristics, measured at PD input connector

Parameter	Conditions	Minimum	Maximum	Unit
R_{detect} (at any 1 V or greater chord within the voltage range conditions)	2.70 V to 10.1 V	23.7	26.3	kΩ
V offset	See Figure 33–17	0	1.90	V
Voltage at the PI	I_{Port} = 124 μA	2.70		V
Input capacitance	2.70 V to 10.1 V	0.050	0.120	μF
Series input inductance	2.70 V to 10.1 V		0.100	mH

Table 33–15—Non-valid PD detection signature characteristics, measured at PD input connector

Parameter	Conditions	Range of values	Unit
R_{detect}	V < 10.1 V	Either greater than 45.0 or less than 12.0	kΩ
Input capacitance	V < 10.1 V	Greater than 10.0	μF

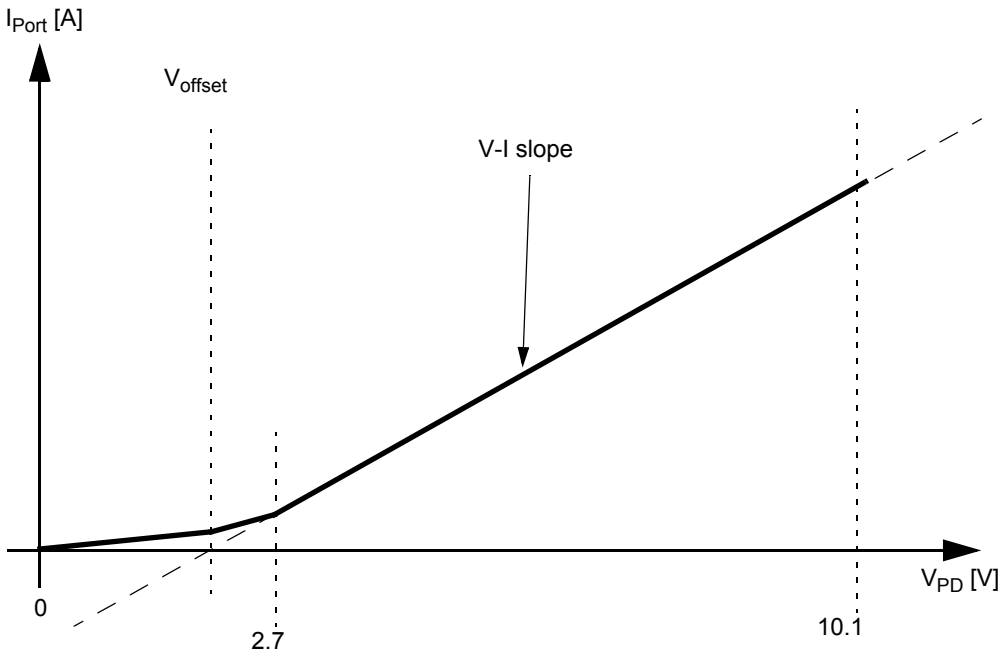


Figure 33–17—Valid PD detection signature offset

33.3.5 PD classifications

See 33.2.6 for a general description of classification mechanisms.

A PD may be classified by the PSE based on the Physical Layer classification information, Data Link Layer classification, or a combination of both provided by the PD. The intent of PD classification is to provide information about the maximum power required by the PD during operation. Additionally, classification is used to establish mutual identification between Type 2 PSEs and Type 2 PDs.

The method of classification depends on the type of the PD and the type of the attached PSE.

A PD shall meet at least one of the allowable classification permutations listed in Table 33–8.

A Type 1 PD may implement any of the class signatures in 33.3.5 and 33.6.

Type 2 PDs implement both 2-Event class signature (see 33.3.5.2) and Data Link Layer classification (see 33.6).

PD classification behavior conforms to the state diagram in Figure 33–16.

33.3.5.1 PD 1-Event class signature

Class 0 is the default for PDs. However, to improve power management at the PSE, a Type 1 PD may opt to provide a signature for Class 1 to 3.

The PD is classified based on power. The Physical Layer classification of the PD is the maximum power that the PD draws across all input voltages and operational modes.

PDs implementing a 2-Event class signature shall return Class 4 in accordance with the maximum power draw, P_{Class_PD}, as specified in Table 33–18. Since 1-Event classification is a subset of 2-Event classification, Type 2 PDs respond to 1-Event classification with a Class 4 signature. Type 1 PDs may choose to implement a 2-Event class signature and return Class 0, 1, 2, or 3 in accordance with the maximum power draw, P_{Class_PD}. The Type 2 PD's classification behavior shall conform to the electrical specifications defined by Table 33–17.

In addition to a valid detection signature, PDs shall provide the characteristics of a classification signature as specified in Table 33–16. A PD shall present one, and only one, classification signature during classification.

Table 33–16—Classification signature, measured at PD input connector

Parameter	Conditions	Minimum	Maximum	Unit
Current for Class 0	14.5 V to 20.5 V	0	4.00	mA
Current for Class 1	14.5 V to 20.5 V	9.00	12.0	mA
Current for Class 2	14.5 V to 20.5 V	17.0	20.0	mA
Current for Class 3	14.5 V to 20.5 V	26.0	30.0	mA
Current for Class 4	14.5 V to 20.5 V	36.0	44.0	mA

33.3.5.2 PD 2-Event class signature

PDs implementing a 2-Event class signature shall return a Class 4 classification signature in accordance with the maximum power draw, P_{Class_PD}, as specified by Table 33–18. The PD's classification behavior shall conform to the electrical specifications defined by Table 33–17.

Until successful 2-Event Physical Layer classification or Data Link Layer classification has completed, a Type 2 PD's pse_power_type state variable is set to '1.' A Type 2 PD shall conform to the electrical requirements as defined by Table 33–18 for the type defined in its pse_power_type state variable.

Table 33–17—2-Event Physical Layer classification electrical requirements

Item	Parameter	Symbol	Units	Min	Max	Additional information
1	Class event voltage	V_{Class}	V	14.5	20.5	
2	Mark event voltage	V_{Mark}	V	6.90	10.1	
3	Mark event current	I_{Mark}	mA	0.250	4.00	See 33.3.5.2.1
4	Mark event threshold	V_{Mark_th}	V	10.1	14.5	See 33.3.5.2.1
5	Classification reset threshold	V_{Reset_th}	V	2.81	6.90	See 33.3.5.2.1
6	Classification reset voltage	V_{Reset}	V	0	2.81	See 33.3.5.2.1

33.3.5.2.1 Mark Event behavior

When the PD is presenting a mark event signature as shown in the state diagram of Figure 33–16, the PD shall draw I_{Mark} as defined in Table 33–17 and present a non-valid detection signature as defined in Table 33–15.

The PD shall not exceed the I_{Mark} current limits when voltage at the PI enters the V_{Mark} specification as defined in Table 33–17.

V_{Mark_th} is the PI voltage threshold at which the PD implementing 2-Event class signature transitions into and out of the DO_CLASS_EVENT1 or DO_CLASS_EVENT2 states as shown in Figure 33–16.

The PD shall draw I_{Mark} until the PD transitions from a DO_MARK_EVENT state to the IDLE state.

V_{Reset_th} is the PI voltage threshold at which the PD implementing 2-Event class signature transitions from a DO_MARK_EVENT state to the IDLE state as shown in Figure 33–16.

33.3.6 PSE Type identification

A Type 2 PD shall identify the PSE Type as either Type 1 or Type 2 (see Figure 33–16).

The default value of pse_power_type is 1. After a successful 2-Event Physical Layer classification or Data Link Layer classification has completed, the pse_power_type is set to 2.

The PD resets the pse_power_type to '1' when the PD enters the DO_DETECTION state.

33.3.7 PD power

The power supply of the PD shall operate within the characteristics in Table 33–18.

The PD may be capable of drawing power from a local power source. When a local power source is provided, the PD may draw some, none, or all of its power from the PI.

Table 33–18—PD power supply limits

Item	Parameter	Symbol	Unit	Min	Max	PD Type	Additional information
1	Input voltage	V_{Port_PD}	V	37.0	57.0	1	See 33.3.7.1, Table 33–1
				42.5	57.0	2	
2	Transient operating input voltage	V_{Tran_lo}	V	36.0		2	For time duration defined in 33.2.7.2
3	Input voltage range during overload	$V_{Overload}$	V	36.0	57.0	1	See 33.3.7.4, Table 33–1
				41.4	57.0	2	
4	Input average power, Class 0 and Class 3	P_{Class_PD}	W		13.0	1	See 33.3.7.2, Table 33–1
	Input average power, Class 1				3.84	1	
	Input average power, Class 2				6.49	1	
	Input average power, Class 4				25.5	2	
5	Input inrush current	I_{Inrush_PD}	A		0.400	1, 2	Peak value—See 33.3.7.3
6	Inrush to operating state delay	T_{delay}	s	0.080		2	See 33.3.7.3
7	Peak operating power, Class 0 and Class 3	P_{Peak_PD}	W		14.4	1	See 33.3.7.4
	Peak operating power, Class 1				5.00	1	
	Peak operating power, Class 2				8.36	1	
	Peak operating power, Class 4				$1.11 \times P_{Class\_PD}$	2	
8	Input current transient (absolute value)		mA/µs		4.70	1, 2	See 33.3.7.5
9	PI capacitance during MDI_POWER states	C_{Port}	µF	5.00		1, 2	See 33.3.7.6, 33.3.7.3

Table 33–18—PD power supply limits *(continued)*

Item	Parameter	Symbol	Unit	Min	Max	PD Type	Additional information
10	Ripple and noise, < 500 Hz		V_{PP}		0.500	1, 2	See 33.3.7.7. Balanced source impedance: R_{Ch}
	Ripple and noise, 500 Hz to 150 kHz				0.200		
	Ripple and noise, 150 kHz to 500 kHz				0.150		
	Ripple and noise, 500 kHz to 1 MHz				0.100		
11	a) PD Power supply turn on voltage	V_{On}	V		42.0	1, 2	See 33.3.7.1
	b) PD power supply turn off voltage	V_{Off}	V	30.0		1, 2	
12	PD classification stability time	T_{class}	s		0.005		See 33.3.7.8
13	Backfeed voltage	V_{bfd}	V		2.80		See 33.3.7.9

33.3.7.1 Input voltage

The specification for V_{Port_PD} in Table 33–18 is for the input voltage range after startup (see 33.3.7.3), and accounts for loss in the cabling plant. Note, $V_{PD} = V_{PSE} - (R_{Chan} \times I_{Port})$.

The PD shall turn on at a voltage less than or equal to V_{On}. After the PD turns on, the PD shall stay on over the entire V_{Port_PD} range. The PD shall turn off at a voltage less than V_{Port_PD} minimum and greater than or equal to V_{Off}.

The PD shall turn on or off without startup oscillation and within the first trial at any load value when fed by V_{Port_PSE} min to V_{Port_PSE} max (as defined in Table 33–11) with a series resistance within the range of valid Channel Resistance.

33.3.7.2 Input average power

The maximum average power, P_{Class_PD} in Table 33–18 or PDMaxPowerValue in 33.6.3.3, is calculated over a 1 second interval. PDs may dynamically adjust their maximum required operating power below P_{Class_PD} as described in 33.6.

NOTE—Average power is calculated using any sliding window with a width of 1 s.

33.3.7.2.1 System stability test conditions during startup and steady state operation

When the PD is fed by V_{Port_PSE} min to V_{Port_PSE} max with R_{Ch} (as defined in Table 33–1) in series, P_{Port_PD} shall be defined as shown in Equation (33–9):

$$P_{Port\_PD} = \{V_{Port\_PD} \times I_{Port}\}_W \quad (33–9)$$

where

P_{Port_PD} is the average input power at the PD PI

V_{Port_PD} is the static input voltage at the PD PI
I_{Port} is the input current, either DC or RMS

NOTE—When connected together as a system, the PSE and PD might exhibit instability at the PSE side, the PD side, or both due to the presence of negative impedance at the PD input. See Annex 33A for PD design guidelines for stable operation.

33.3.7.3 Input inrush current

Inrush current is drawn during the startup period beginning with the application of input voltage at the PI compliant with V_{Port_PD} requirements as defined in Table 33–18, and ending when C_{Port} is charged to 99 % of its final value. This period should be less than T_{Inrush} min per Table 33–11.

Type 2 PDs with pse_power_type state variable set to 2 prior to power-on shall behave like a Type 1 PD for at least T_{delay} min. T_{delay} starts when V_{PD} crosses the PD power supply turn on voltage, V_{On}. This delay is required so that the Type 2 PD does not enter a high power state before the PSE has had time to switch current limits from I_{Inrush} to I_{LIM}.

Input inrush current at startup is limited by the PSE if $C_{Port} < 180$ µF, as specified in Table 33–11.

If $C_{Port} \geq 180$ µF, input inrush current shall be limited by the PD so that I_{Inrush_PD} max is satisfied.

33.3.7.4 Peak operating power

$V_{Overload}$ is the PD PI voltage when the PD is drawing the permissible P_{Peak_PD}.

At any static voltage at the PI, and any PD operating condition, the peak power shall not exceed P_{Class_PD} max for more than T_{CUT} min, as defined in Table 33–11 and 5% duty cycle. Peak operating power shall not exceed P_{Peak} max.

Ripple current content (I_{Port_ac}) superimposed on the DC current level (I_{Port_dc}) is allowed if the total input power is less than or equal to P_{Class_PD} max.

The RMS, DC and ripple current shall be bounded by Equation (33–10):

$$I_{Port} = \{\sqrt{(I_{Port\_dc})^2 + (I_{Port\_ac})^2}\}_A \quad (33–10)$$

where
I_{Port} is the RMS input current
I_{Port_dc} is the DC component of the input current
I_{Port_ac} is the RMS value of the AC component of the input current

The maximum I_{Port} value for all operating V_{Port_PD} range shall be defined by the following equation:

$$I_{portmax} = \left\{\frac{P_{Class\_PD}}{V_{Port\_PD}}\right\}_A \quad (33–11)$$

where
$I_{portmax}$ is the maximum DC and RMS input current
V_{Port_PD} is the static input voltage at the PD PI

P_{Class_PD} is the maximum power, P_{Class_PD} max, as defined in Table 33–18

Peak power, P_{Peak_PD}, for Class 4 is based on Equation (33–12), which approximates the ratiometric peak powers of Class 0 through Class 3. This equation may be used to calculate peak operating power for P_{Peak_PD} values obtained via Data Link Layer classification.

$$P_{Peak\_PD} = \{1.11 \times P_{Class\_PD}\}_W \quad (33–12)$$

where

P_{Peak_PD} is the peak operating power
P_{Class_PD} is the input average power

NOTE—The duty cycle of the peak current is calculated using any sliding window with a width of 1 s.

33.3.7.5 Peak transient current

When the input voltage at the PI is static and in the range of V_{Port_PD} defined by Table 33–18, the transient current drawn by the PD shall not exceed 4.70 mA/μs in either polarity. This limitation applies after inrush has completed (33.3.7.3) and before the PD has disconnected.

Under normal operating conditions when there are no transients applied at the PD PI, the PD shall operate below the PD upperbound template defined in Figure 33–18.

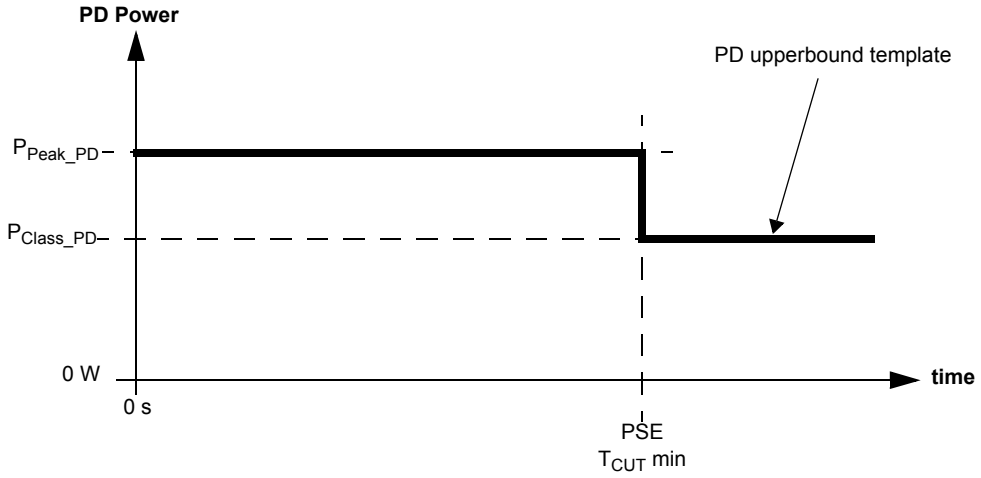


Figure 33–18—PD static operating mask

The PD upperbound template in Figure 33–18, P_{PDUT}, is described by Equation (33–13):

$$P_{PDUT}(t) = \left\{ \begin{array}{ll} P_{Peak\_PD} & \text{for } (0 \le t < T_{cutmin}) \\ P_{Class\_PD} & \text{for } (T_{cutmin} \le t) \end{array} \right\}_W \quad (33–13)$$

where

t is the duration in seconds that the PD sinks I_{Port}
P_{Peak_PD} is the peak operating power, P_{Peak_PD} max, as defined in Table 33–18
P_{Class_PD} is the maximum power, P_{Class_PD} max, as defined in Table 33–18
T_{cutmin} is T_{CUT} min, as defined in Table 33–11

During PSE transient conditions in which the voltage at the PI is undergoing dynamic change, the PSE is responsible for limiting the transient current drawn by the PD for at least T_{LIM} min as defined in Table 33–11.

33.3.7.6 PD behavior during transients at the PSE PI

A Type 1 PD with input capacitance of 180 µF or less requires no special considerations with regard to transients at the PD PI. A Type 2 PD with peak power draw that does not exceed P_{Class_PD} max and has an input capacitance of 180 µF or less requires no special considerations with regard to transients at the PD PI. PDs that do not meet these requirements shall comply with the following:

— A Type 1 PD input current shall not exceed the PD upperbound template (see Figure 33–18) after T_{LIM} min (see Table 33–11 for a Type 1 PSE) when the following input voltage is applied. A current limited voltage source is applied to the PI through a R_{Ch} resistance (see Table 33–1). The current limit meets Equation (33–14) and the voltage ramps from V_{Port_PSE} min to V_{Port_PSE} max at 2250 V/s.

A Type 2 PD shall meet both of the following:

a) The PD input current spike shall not exceed 2.5 A and shall settle below the PD upperbound template (see Figure 33–18) within 4 ms. During this test, the PD PI voltage is driven from 50 V to 52.5 V at greater than 3.5 V/µs, a source impedance of 1.5 Ω, and a source that supports a current greater than 2.5 A.
b) The PD shall not exceed the PD upperbound template beyond T_{LIM} min under worst-case current draw under the following conditions. The input voltage source drives V_{PD} from V_{Port_PSE} min to 56 V at 2250 V/s, the source impedance is R_{Ch} (see Table 33–1), and the voltage source limits the current to MDI I_{LIM} per Equation (33–14).

The current limit at the MDI (MDI I_{LIM}) is defined by Equation (33–14):

$$\{pse_{\mathrm{ILIMmin}}\}_{\mathrm{mA}} < \{mdi_{\mathrm{ILIM}}\}_{\mathrm{mA}} \leq \{pse_{\mathrm{ILIMmin}}\}_{\mathrm{mA}} + 5.00 \qquad (33\text{–}14)$$

where

pse_{ILIMmin} is the PSE I_{LIM} min as defined in Table 33–11
mdi_{ILIM} is the current limit at the MDI (MDI I_{LIM})

33.3.7.7 Ripple and noise

The specification for ripple and noise in Table 33–18 shall be for the common-mode and/or differential pair-to-pair noise at the PD PI generated by the PD circuitry. The ripple and noise specification shall be for all operating voltages in the range of V_{Port_PD}, and over the range of input power of the device.

The PD shall operate correctly in the presence of ripple and noise generated by the PSE that appears at the PD PI. These levels are specified in Table 33–11, item 3.

Limits are provided to preserve data integrity. To meet EMI standards, lower values may be needed.

The system designer is advised to assume the worst-case condition in which both PSE and PD generate the maximum noise allowed by Table 33–11 and Table 33–18, which may cause a higher noise level to appear at the PI than the standalone case as specified by this clause.

33.3.7.8 PD classification stability time

The PD Physical Layer classification signature shall be valid within T_{class} as specified in Table 33–18 and remain valid for the duration of the classification period.

33.3.7.9 Backfeed voltage

When V_{Port_PD} max is applied across the PI at either polarity specified on the conductors for Mode A according to Table 33–13, the voltage measured across the PI for Mode B with a 100 kΩ load resistor connected shall not exceed V_{bfd} max as specified in Table 33–18. When V_{Port_PD} max is applied across the PI at either polarity specified on the conductors for Mode B according to Table 33–13, the voltage measured across the PI for Mode A with a 100 kΩ load resistor connected shall not exceed V_{bfd} max.

33.3.8 PD Maintain Power Signature

In order to maintain power, the PD shall provide a valid Maintain Power Signature (MPS) at the PI. The MPS shall be both:

a) Current draw equal to or above the minimum input current (I_{Port_MPS} min) as specified in Table 33–19 for a minimum duration of 75 ms followed by an optional MPS dropout for no longer than 250 ms, and
b) Input impedance with resistive and capacitive components as defined in Table 33–19.

A PD that does not maintain the MPS components in a) and b) above may have its power removed within the limits of T_{MPDO} as specified in Table 33–11.

Powered PDs that no longer require power shall remove both components a) and b) of the MPS. To cause PSE power removal, the impedance of the PI should rise above Z_{ac2} as specified in Table 33–12.

Table 33–19—PD Maintain Power Signature

Item	Parameter	Symbol	Unit	Min	Max	Additional information
1	Input current	I_{Port_MPS}	A	0.010		See 33.3.8
2	Input resistance	R_{pd_d}	kΩ		26.3	
3	Input capacitance	C_{pd_d}	μF	0.050		See Table 33–12

NOTE—A PD with $C_{port} > 180$ μF may not be able to meet the I_{Port_MPS} specification in Table 33–19 during the maximum allowed port voltage droop (V_{Port_PSE} max to V_{Port_PSE} min with series resistance R_{Ch}). Such a PD should increase its I_{Port} min or make other such provisions to meet the Maintain Power Signature.

33.4 Additional electrical specifications

This clause defines additional electrical specifications for both the PSE and PD. The specifications apply for all PSE and PD operating conditions at the cabling side of the mated connection of the PI. The requirements apply during data transmission only when specified as an operating condition.

The requirements of 33.4 are consistent with the requirements of the 10BASE-T MAU and the 100BASE-TX and 1000BASE-T PHYs.

33.4.1 Isolation

PDs and PSEs shall provide isolation between all accessible external conductors, including frame ground (if any), and all MDI leads including those not used by the PD or PSE. Any equipment that can be connected to a PSE or PD through a non-MDI connector that is not isolated from the MDI leads needs to provide isolation between all accessible external conductors, including frame ground (if any), and the non-MDI connector. Accessible external conductors are specified in subclause 6.2.1 b) of IEC 60950-1:2001.

This electrical isolation shall withstand at least one of the following electrical strength tests:

a) 1500 V rms at 50 Hz to 60 Hz for 60 s, applied as specified in subclause 5.2.2 of IEC 60950-1:2001.
b) 2250 V dc for 60 s, applied as specified in subclause 5.2.2 of IEC 60950-1:2001.
c) An impulse test consisting of a 1500 V, 10/700 µs waveform, applied 10 times, with a 60 s interval between pulses. The shape of the impulses shall be 10/700 µs (10 µs virtual front time, 700 µs virtual time of half value), as defined in IEC 60950-1:2001 Annex N.

There shall be no insulation breakdown, as defined in subclause 5.2.2 of IEC 60950-1:2001, during the test. The resistance after the test shall be at least 2 MΩ, measured at 500 V dc.

Conductive link segments that have differing isolation and grounding requirements shall have those requirements provided by the port-to-port isolation of network interface devices (NID).

33.4.1.1 Electrical isolation environments

There are two electrical power distribution environments to be considered that require different electrical isolation properties. They are as follows:

— **Environment A:** When a LAN or LAN segment, with all its associated interconnected equipment, is entirely contained within a single low-voltage power distribution system and within a single building.
— **Environment B:** When a LAN crosses the boundary between separate power distribution systems or the boundaries of a single building.

33.4.1.1.1 Environment A requirements

Attachment of network segments via NIDs that have multiple instances of a twisted pair MDI requires electrical isolation between each segment and the protective ground of the NID.

For NIDs, the requirement for isolation is encompassed within the isolation requirements of the MAU or PHY (see 14.3.1.1, 25.4.5, and 40.6.1.1.). Equipment with multiple instances of PSE, PD, or both shall meet or exceed the isolation requirement of the MAU/PHY with which they are associated.

A multiport NID complying with Environment A requirements does not require electrical power isolation between link segments.

An Environment A PSE shall switch the more negative conductor. It is allowable to switch both conductors.

33.4.1.1.2 Environment B requirements

The attachment of network segments that cross Environment A boundaries requires electrical isolation between each segment and all other attached segments as well as to the protective ground of the NID.

For NIDs, the requirement for isolation is encompassed within the isolation requirements of the MAU or PHY (see 14.3.1.1, 25.4.5, and 40.6.1.1.). Equipment with multiple instances of PSE, PD, or both shall meet or exceed the isolation requirement of the MAU/PHY with which each is associated.

The requirements for interconnected electrically conducting link segments that are partially or fully external to a single building environment may require additional protection against lightning strikes or other hazards. Protection requirements for such hazards are beyond the scope of this standard. Guidance on these requirements may be found in Section 6 of IEC 60950-1:2001, as well as any local and national codes related to safety.

33.4.2 Fault tolerance

Each wire pair of the PI, when it is also an MDI (e.g., an Endpoint PSE or PD), shall meet the fault tolerance requirements of the appropriate specifying clause. (See 14.3.1.2.7, 25.4, and 40.8.3.4.) When a PI is not an MDI (e.g., a Midspan PSE), the PSE PI shall meet the fault tolerance requirements of this subclause.

The PSE PI shall withstand without damage the application of short circuits of any wire to any other wire within the cable for an indefinite period of time. The magnitude of the current through such a short circuit shall not exceed I_{LIM} max as defined in Table 33–11.

Each wire pair shall withstand, without damage, a 1000 V common-mode impulse applied at E_{cm} of either polarity. The shape of the impulse shall be (0.3/50) μs (300 ns virtual front time, 50 μs virtual time of half value), as defined in IEC 60060, where E_{cm} is an externally applied AC voltage as shown in Figure 33–19.

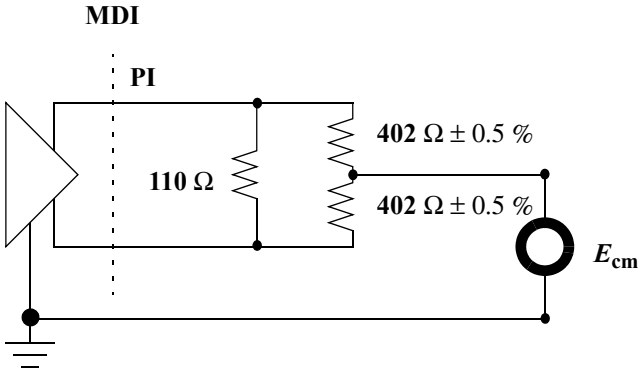


Figure 33–19—PI fault tolerance test circuit

33.4.3 Impedance balance

Impedance balance is a measurement of the common-mode-to-differential-mode offset of the PI. The common-mode-to-differential-mode impedance balance for the transmit and receive pairs shall exceed:

$$\left\{29.0 - 17.0 \times \log_{10}\left(\frac{f}{10.0}\right)\right\}_{dB} \quad (33\text{–}15)$$

where

f is the frequency in MHz from 1.00 MHz to 20.0 MHz for a 10 Mb/s MAU

$$\left\{34.0 - 19.2 \times \log_{10}\left(\frac{f}{50.0}\right)\right\}_{\text{dB}} \quad (33\text{–}16)$$

where

f is the frequency in MHz from 1.00 MHz to 100. MHz for a 100 Mb/s or greater PHY

The impedance balance is defined as shown in Equation (33–17):

$$\left\{20.0 \times \log_{10}\left(\frac{E_{\text{cm}}}{E_{\text{dif}}}\right)\right\}_{\text{dB}} \quad (33\text{–}17)$$

where

E_{cm} is an externally applied sinusoidal voltage as shown in Figure 33–20

E_{dif} is the voltage of the resulting waveform due only to the applied sine wave measured as shown in Figure 33–20

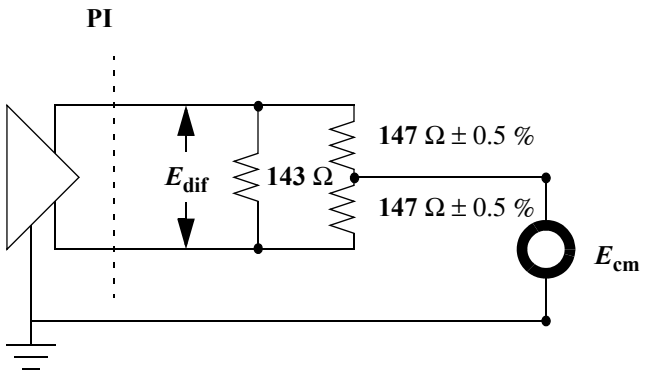
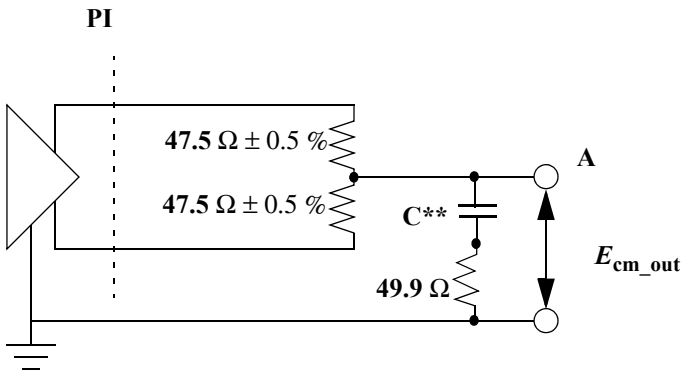


Figure 33–20—PI impedance balance test circuit

33.4.4 Common-mode output voltage

The magnitude of the common-mode AC output voltage measured according to Figure 33–21 and Figure 33–22 at the transmit PI while transmitting data and with power applied, $E_{\text{cm\_out}}$, shall not exceed 50 mV peak when operating at 10 Mb/s, and 50 mV peak-to-peak when operating at 100 Mb/s or greater. The frequency of the measurement shall be from 1 MHz to 100 MHz.



**Capacitor impedance less than 1 Ω
from 1 MHz to 100 MHz

Figure 33–21—Common-mode output voltage test

The common-mode AC output voltage shall be measured while the PHY is transmitting data, the PSE or PD is operating with the following PSE load or PD source:

1) For a PSE, the PI that supplies power is terminated as illustrated in Figure 33–22. The PSE load, R, in Figure 33–22 is adjusted so that the PSE output current, I_{out}, is 10 mA and then 350 mA, while measuring E_{cm_out} on the PI.
2) For a PD, the PI that requires power shall be terminated as illustrated in Figure 33–22. V_{source} in Figure 33–22 is adjusted to 36 Vdc and 57 Vdc, while measuring E_{cm_out} on the PI.

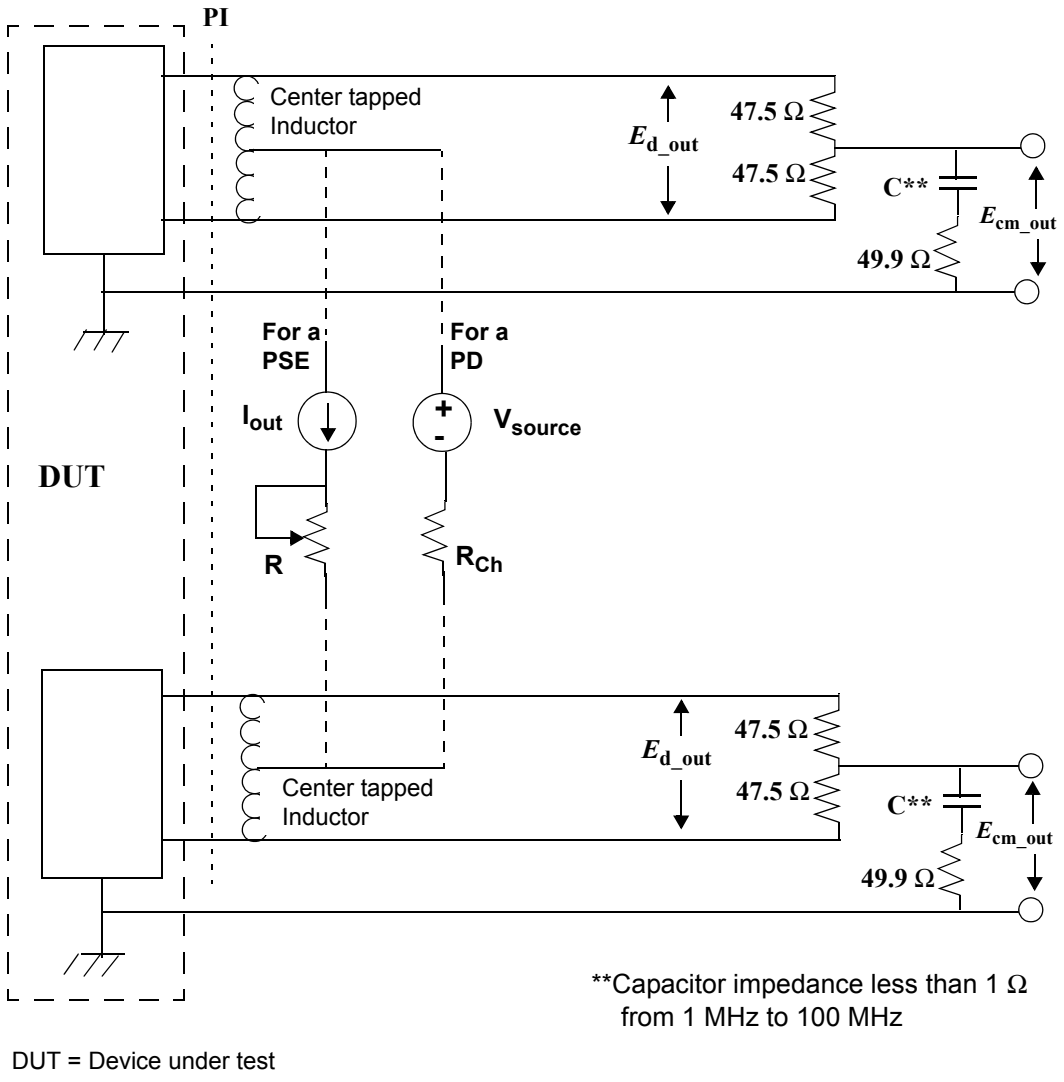


Figure 33–22—PSE and PD terminations for common-mode output voltage test

NOTE—The implementor should consider any applicable local, national, or international regulations that may require more stringent specifications. One such specification can be found in the European Standard EN 55022:1998.

33.4.5 Pair-to-pair output noise voltage

The pair-to-pair output noise voltage (see Figure 33–23) is limited by the resulting electromagnetic interference due to this AC voltage. This AC voltage can be ripple from the power supply (Table 33–11, item 3) or from any other source. A system integrating a PSE shall comply with applicable local and national codes for the limitation of electromagnetic interference.

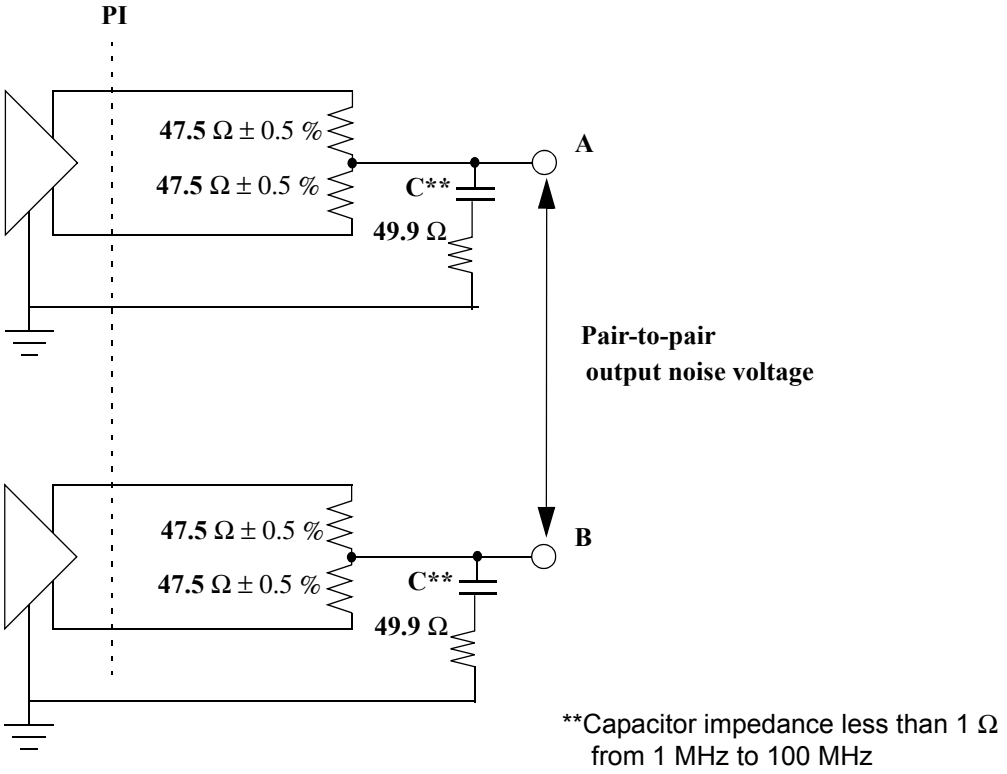


Figure 33–23—Pair-to-pair output noise voltage test

33.4.6 Differential noise voltage

The coupled noise, E_{d_out} in Figure 33–22, from a PSE or PD to the differential transmit and receive pairs shall not exceed 10 mV peak-to-peak when measured from 1 MHz to 100 MHz under the conditions specified in 33.4.4, item 1) and item 2).

33.4.7 Return loss

The differential impedance of the transmit and receive pairs at the PHY's MDI shall be such that any reflection shall meet the return loss requirements as specified in 14.3.1.3.4 for a 10 Mb/s PHY, in ANSI X3.263:1995 for a 100 Mb/s PHY, and 40.8.3.1 for a 1000 Mb/s PHY. In addition, all pairs terminated at an MDI should maintain a nominal common-mode impedance of 75 Ω. The common-mode termination is affected by the presence of the power supply, and this should be considered to determine proper termination.

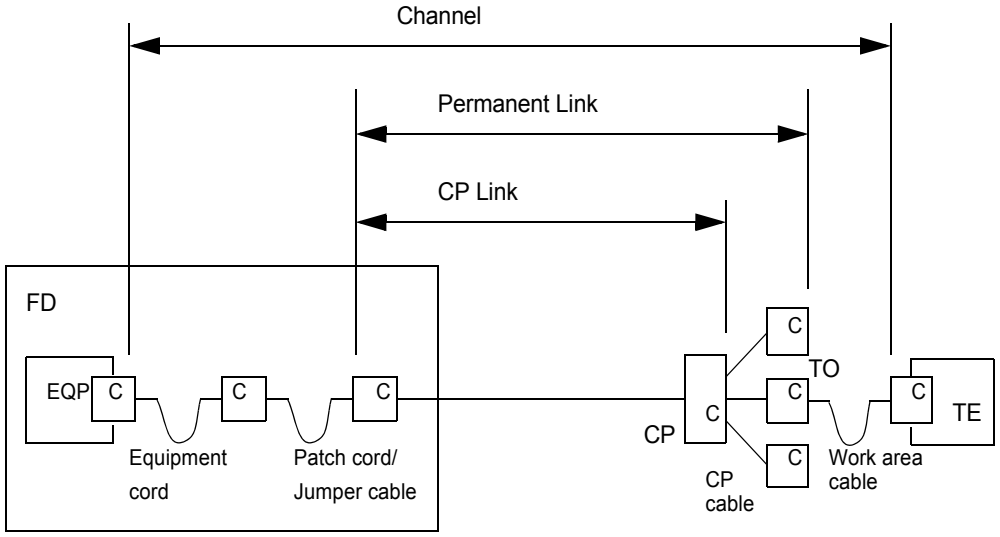
33.4.8 100BASE-TX transformer droop

100BASE-TX systems may contain a legacy PHY receiver that expects to be connected to a PHY transmitter with 350 μH open circuit inductance (OCL). Alternative A Type 2 Midspan PSEs that support 100BASE-TX shall enforce channel unbalance currents less than or equal to Type 1 I_{unb} (see Table 33–11) or meet 33.4.9.2.

100BASE-TX Type 2 Endpoint PSEs and 100BASE-TX Type 2 PDs shall meet the requirements of Clause 25 in the presence of (I_{unb}/2).

33.4.9 Midspan PSE device additional requirements

The cabling specifications for 100 Ω balanced cabling are described in ISO/IEC 11801-2002. Cable conforming to ANSI/TIA-568-C.2 also meets these requirements. Some cable category specifications that only appear in earlier editions are also supported. The configuration of "channel" and "permanent link" is defined in Figure 33–24. Type 2 Midspan PSE cabling system requirements are specified in 33.1.4.1.



FD = floor distributor; EQP = equipment; C = connection (mated pair);
CP = consolidation point; TO = telecommunications outlet;
TE = terminal equipment

Figure 33–24—Floor distributor channel configuration

ISO/IEC 11801 defines in 5.6.1 two types of Equipment interface to the cabling system: "Interconnect model" and the "cross-connect model." An equivalent "Interconnect model" and "cross-connect model" can be found in ANSI/TIA-568-C.0, 4.2. See Figure 33–25.

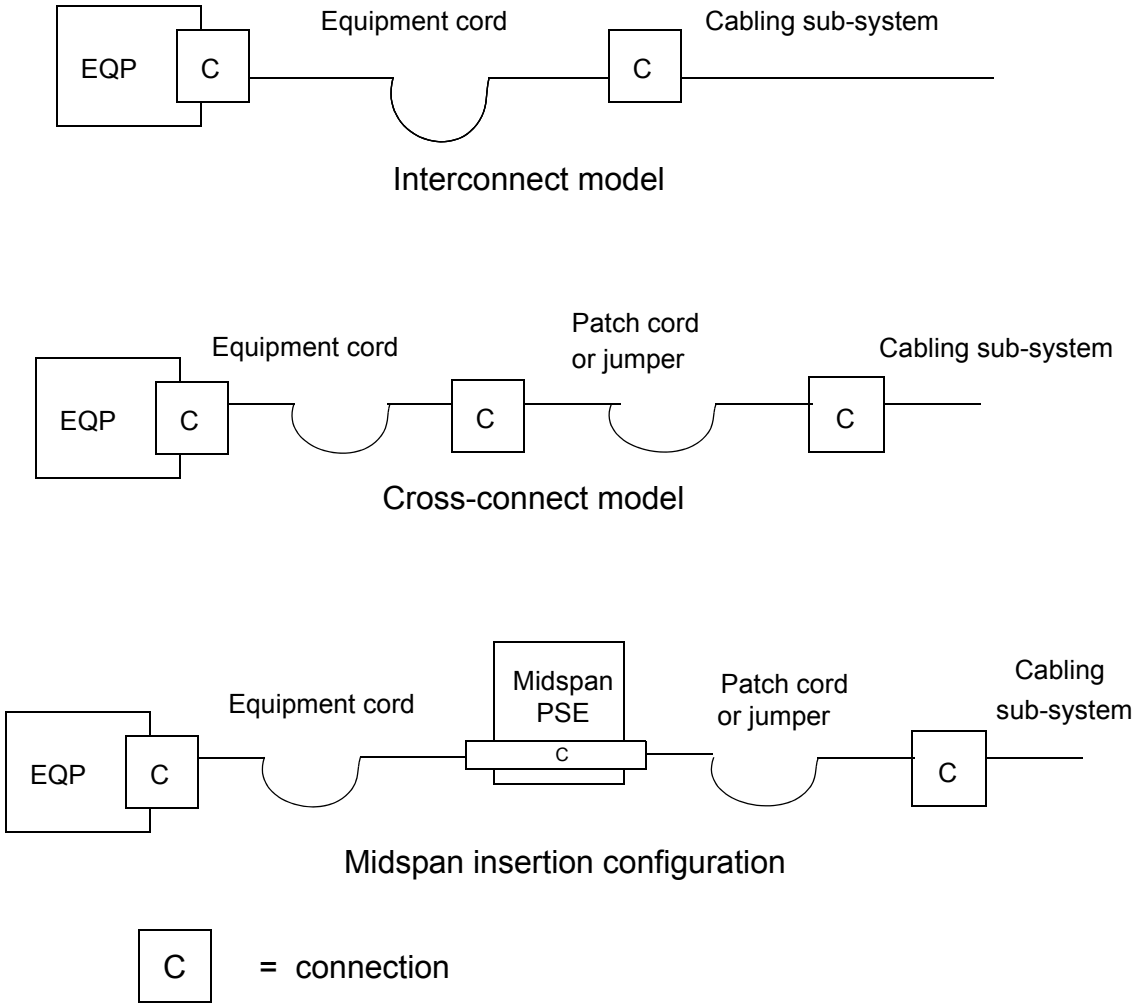


Figure 33–25—Interconnect model, cross-connect model, and midspan insertion configuration

The insertion of a Midspan PSE at the Floor Distributor (FD) shall comply with the following guidelines:

a) If the existing FD configuration is of the "Interconnect model" type, the Midspan PSE can be added, provided it does not increase the length of the resulting "channel" to more than specified 100 m as defined in ISO/IEC 11801 or ANSI/TIA-568-C.0.

b) If the existing FD configuration is of the "Cross-connect model" type, the Midspan PSE needs to be installed instead of one of the connection pairs in the FD. In addition, the installation of the Midspan PSE shall not increase the length of the resulting "channel" to more than specified 100 m as defined in ISO/IEC 11801 or ANSI/TIA-568-C.0.

Configurations with the Midspan PSE in the cabling channel shall not alter the transmission requirements of the "permanent link." A Midspan PSE shall not provide DC continuity between the two sides of the segment for the pairs that inject power.

The requirements for the two pair Category 5 channel are found in 25.4.6. The specification of Midspan PSE operation on a two pair cable is beyond the scope of this document.

NOTE—Appropriate terminations may be applied to the interrupted pairs on both sides of the Midspan device.

33.4.9.1 "Connector" or "telecom outlet" Midspan PSE device transmission requirements

The Midspan PSE equipment to be inserted as "connector" or "telecom outlet" shall meet the following transmission parameters. These parameters should be measured using the test procedures of ISO 11801:2002 or ANSI/TIA-568-C.2 for connecting hardware.

There are four types of Midspan PSEs defined with respect to transmission requirements:

1) 10BASE-T/100BASE-TX connector or telecom outlet Midspan PSE
2) 10BASE-T/100BASE-TX work area or equipment cable Midspan PSE
3) 1000BASE-T connector or telecom outlet Midspan PSE
4) 1000BASE-T work area of equipment cable Midspan PSE

33.4.9.1.1 Near End Crosstalk (NEXT)

NEXT loss is a measure of the unwanted signal coupling from a transmitter at the near-end into neighboring pairs measured at the near-end. NEXT loss is expressed in dB relative to the received signal level. NEXT loss for Midspan PSE devices shall meet the values determined by Equation (33–18) when measured for the transmit and receive pairs from 1 MHz to 100 MHz. However, for frequencies that correspond to calculated values greater than 65 dB, the requirement reverts to the minimum requirement of 65 dB.

$$\{NEXTconn\}_{\mathrm{dB}} \geq 40.0 - 20.0 \times \log_{10}\left(\frac{f}{100.}\right) \qquad (33\text{–}18)$$

where

NEXTconn is the Near End Crosstalk loss
f is the frequency expressed in MHz

33.4.9.1.2 Insertion loss

Insertion loss is a measure of the signal loss between the transmitter and receiver, expressed in dB relative to the received signal level. Insertion loss for Midspan PSE devices shall meet the values determined by Equation (33–19) when measured for the transmit and receive pairs from 1 MHz to 100 MHz. However, for frequencies that correspond to calculated values less than 0.1 dB, the requirement reverts to the maximum requirement of 0.1 dB.

$$\{ILconn\}_{\mathrm{dB}} \leq 0.040 \times \sqrt{f} \qquad (33\text{–}19)$$

where

ILconn is the insertion loss
f is the frequency expressed in MHz

33.4.9.1.3 Return loss

Return loss is a measure of the reflected energy caused by impedance mismatches in the cabling system and is expressed in dB relative to the reflected signal level. Return loss for Midspan PSE devices shall meet or exceed the values specified in Table 33–20 when measured for the transmit and receive pairs from 1 MHz to 100 MHz.

Table 33–20—Connector return loss

Frequency	Return loss
1 MHz ≤ f < 20 MHz	23 dB
20 MHz ≤ f ≤ 100 MHz	14 dB

33.4.9.1.4 Work area or equipment cable Midspan PSE

Replacing the work area or equipment cable with a cable that includes a Midspan PSE should not alter the requirements of the cable. This cable shall meet the requirements of this clause and the specifications for a Category 5 (jumper) cord as specified in ISO/IEC 11801:2002 or ANSI/TIA-568-C.2 for insertion loss, NEXT, and return loss for the transmit and receive pairs.

33.4.9.2 Midspan signal path requirements

An Alternative A Midspan PSE transfer function gain shall be greater than that expressed by Equation (33–20) for the frequency range from 0.1 MHz to 1 MHz, at the pins of the PI used as 100BASE-TX transmit pins.

$$\left\{ -0.100 + 37.5 \times \log_{10}\left(\frac{22.4 \times f}{\sqrt{1.00 + 521 \times f^2}} \right) \right\}_{\text{dB}} \qquad (33\text{–}20)$$

where

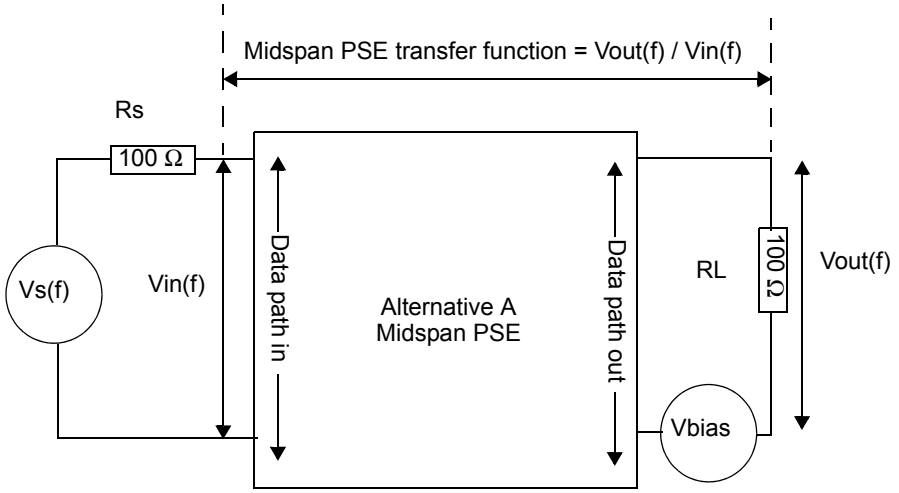
f is the frequency expressed in MHz.

The requirements shall be met with a DC bias current, I_{bias}, between 0 mA and (I_{unb}/2) mA (I_{unb} is defined in Table 33–11).

33.4.9.2.1 Alternative A Midspan PSE signal path transfer function

The transfer function is measured by applying a test signal to the Midspan PSE signal input through a source impedance of 100 Ω ± 1 %. The Midspan PSE signal input and output may be connected to a 0.5 m maximum length of cable, meeting the requirements of 25.4.7, terminated with 100 Ω ± 1 %.

The transfer function is defined from the output termination to the Midspan PSE input. See Figure 33–26.



Vin(f) is the sine wave signal to be used to measure the Midspan PSE transfer function.
Vbias is the DC offset voltage to be applied in series with RL in order to generate I_{bias}.
Vout(f) is the Midspan PSE response to Vin(f).
Some test equipment may require isolation between measurement ports.

Figure 33–26—Measurement setup for Alternative A Midspan PSE transfer function

33.5 Management function requirements

If the PSE is implemented with a management interface described in 22.2.4 or 45.2 (MDIO), then the management access shall use the PSE register definitions shown in 33.5.1. Where no physical embodiment of the Clause 22 or Clause 45 management is supported, equivalent management capability shall be provided. Managed objects corresponding to PSE and PD control parameters and states are described in Clause 30.

33.5.1 PSE registers

A PSE implementing either Clause 22 or Clause 45 management interface shall use register address 11 for its control and register address 12 for its status functions. The full set of management registers is listed in Table 22–6.

Some of the bits within registers are defined as latching high (LH). When a bit is defined as latching high and the condition for the bit to be high has occurred, the bit shall remain high until after it has been read via the management interface. Once such a read has occurred, the bit shall assume a value based on the current state of the condition it monitors.

33.5.1.1 PSE Control register (Register 11) (R/W)

The assignment of bits in the PSE Control register is shown in Table 33–21. The default value for each bit of the PSE Control register should be chosen so that the initial state of the PSE upon power up or reset is a normal operational state without management intervention.

Table 33–21—PSE Control register bit definitions

Bit(s)	Name	Description	R/W[a]
11.15:6	Reserved	Ignore when read	RO
11.5	Data Link Layer Classification Capability	1 = Data Link Layer classification capability enabled 0 = Data Link Layer classification capability disabled	R/W
11.4	Enable Physical Layer Classification	1 = Physical Layer classification enabled 0 = Physical Layer classification disabled	R/W
11.3:2	Pair Control	(11.3) (11.2) 1 1 = Reserved 1 0 = PSE pinout Alternative B 0 1 = PSE pinout Alternative A 0 0 = Reserved	R/W
11.1:0	PSE Enable	(11.1) (11.0) 1 1 = Reserved 1 0 = Force Power Test Mode 0 1 = PSE Enabled 0 0 = PSE Disabled	R/W

[a]R/W = Read/Write, RO = Read Only

33.5.1.1.1 Reserved bits (11.15:6)

Bits 11.15:6 are reserved for future standardization. They shall not be affected by writes and shall return a value of zero when read. For compatibility with future use of reserved bits and registers, if the management entity writes to a reserved bit, it should use a value of zero. If it reads a reserved bit, it should ignore the results.

33.5.1.1.2 Data Link Layer Classification capability (11.5)

Bit 11.5 controls a PSEs capability of performing Data Link Layer classification as specified in 33.6.

A PSE that does not support Data Link Layer classification shall ignore writes to bit 11.5 and shall return a value of zero when read. A PSE that supports Data Link Layer classification, but does not allow the capability to be disabled, shall ignore writes to bit 11.5 and shall return a value of one when read.

A PSE that supports Data Link Layer classification and supports the ability to enable and disable it shall enable Data Link Layer classification by setting bit 11.5 to one and disable it by setting bit 11.5 to zero.

33.5.1.1.3 Enable Physical Layer classification (11.4)

Bit 11.4 controls Physical Layer classification as specified in 33.2.6. A PSE that indicates support for Physical Layer classification in register 12.13 may also provide the option of disabling Physical Layer classification through bit 11.4.

A PSE that does not support Physical Layer classification shall ignore writes to bit 11.4 and shall return a value of zero when read. A PSE that supports Physical Layer classification, but does not allow the function to be disabled, shall ignore writes to bit 11.4 and shall return a value of one when read.

The Physical Layer classification function shall be enabled by setting bit 11.4 to one and disabled by setting bit 11.4 to zero.

33.5.1.1.4 Pair Control (11.3:2)

Bits 11.3:2 report the supported PSE Pinout Alternative specified in 33.2.1. A PSE may also provide the option of controlling the PSE Pinout Alternative through these bits. Provision of this option is indicated through the Pair Control Ability (12.0) bit. A PSE that does not support this option shall ignore writes to these bits and shall return the value that reports the supported PSE Pinout Alternative.

When read as '01', bits 11.3:2 indicate that only PSE Pinout Alternative A is supported by the PSE. When read as '10', bits 11.3:2 indicate that only PSE Pinout Alternative B is supported by the PSE.

Where the option of controlling the PSE Pinout Alternative through these bits is provided, setting bits 11.3:2 to '01' shall force the PSE to use only PSE Pinout Alternative A and setting bits 11.3:2 to '10' shall force the PSE to use only PSE Pinout Alternative B.

If bit 12.0 is one, writing to these register bits shall set mr_pse_alternative to the corresponding value: '01' = A and '10' = B. The combinations '00' and '11' for bits 11.3:2 are reserved and will never be assigned. Reading bits 11.3:2 returns an unambiguous result of '01' or '10' that may be used to determine the presence of the PSE Control register.

33.5.1.1.5 PSE enable (11.1:0)

The PSE function shall be disabled by setting bit 11.1 to zero and bit 11.0 to zero. When the PSE function is disabled, the MDI shall function as it would if it had no PSE function. The PSE function shall be enabled by setting bits 11.1 to a zero and 11.0 to a one. When bit 11.1 is a one, and bit 11.0 is a zero, a test mode is enabled. This test mode supplies power without regard to PD detection.

Writing to these register bits shall set mr_pse_enable to the corresponding value: '00' = disable, '01' = enable and '10' = force power. The combination '11' for bits 11.1:0 has been reserved for future use.

CAUTION

Test mode may damage connected non-PD, legacy, twisted pair Ethernet devices, or other non-Ethernet devices, especially in split application wiring schemes.

33.5.1.2 PSE Status register (Register 12) (R/W)

The assignment of bits in the PSE Status register is shown in Table 33–22.

Table 33–22—PSE Status register bit definitions

Bit(s)	Name	Description	R/W[a]
12.15	PSE Type Electrical Parameters	1 = PSE is using Type 2 PSE electrical parameters 0 = PSE is using Type 1 PSE electrical parameters	RO
12.14	Data Link Layer Classification Enabled	1 = Data Link Layer classification is enabled 0 = Data Link Layer classification is not supported or is not enabled	RO
12.13	Physical Layer Classification Supported	1 = PSE supports Physical Layer classification 0 = PSE does not support Physical Layer classification	RO

Table 33–22—PSE Status register bit definitions *(continued)*

Bit(s)	Name	Description	R/W[a]
12.12	Power Denied or Removed	1 = Power has been denied or removed due to fault 0 = Power has not been denied or removed	RO/ LH
12.11	Valid Signature	1 = Valid PD signature detected 0 = No valid PD signature detected	RO/ LH
12.10	Invalid Signature	1 = Invalid PD signature detected 0 = No invalid PD signature detected	RO/ LH
12.9	Short Circuit	1 = Short circuit condition detected 0 = No short circuit condition detected	RO/ LH
12.8	Overload	1 = Overload condition detected 0 = No overload condition detected	RO/ LH
12.7	MPS Absent	1 = MPS absent condition detected 0 = No MPS absent condition detected	RO/ LH
12.6:4	PD Class	(12.6) (12.5) (12.4) 1 1 1 = Reserved 1 1 0 = Reserved 1 0 1 = Invalid Class 1 0 0 = Class 4 0 1 1 = Class 3 0 1 0 = Class 2 0 0 1 = Class 1 0 0 0 = Class 0	RO
12.3:1	PSE Status	(12.3) (12.2) (12.1) 1 1 1 = Reserved 1 1 0 = Reserved 1 0 1 = implementation-specific fault 1 0 0 = Test error 0 1 1 = Test mode 0 1 0 = Delivering power 0 0 1 = Searching 0 0 0 = Disabled	RO
12.0	Pair Control Ability	1 = PSE pinout controllable by Pair Control bits 0 = PSE Pinout Alternative fixed	RO

[a]RO = Read Only, LH = Latched High

33.5.1.2.1 PSE Type electrical parameters (12.15)

When read as a zero, bit 12.15 indicates that the PSE is operating with Type 1 PSE electrical parameters. When read as a one, bit 12.15 indicates that the PSE is operating with Type 2 PSE electrical parameters. This bit shall be set to zero when the PSE state diagram sets the state variable set_parameter_type to 1. This bit shall be set to one when the PSE state diagram sets set_parameter_type to 2.

33.5.1.2.2 Data Link Layer Classification Enabled (12.14)

When read as a one, bit 12.14 indicates the PSE supports Data Link Layer classification as defined in 33.2.6 and that it is enabled. When read as a zero, bit 12.14 indicates that the PSE lacks support for Data Link

Layer classification or that Data Link Layer classification is not enabled. If supported, the Data Link Layer classification may be enabled or disabled through the state diagram variable pse_dll_enabled (see 33.2.4.4).

This bit shall be set to one when the PSE state diagram (Figure 33–9) sets true the state variable pse_dll_enabled. This bit shall be set to zero when the PSE state diagram sets false the state variable pss_dll_enabled.

33.5.1.2.3 Physical Layer Classification Supported (12.13)

When read as a one, bit 12.13 indicates that the PSE supports Physical Layer classification as defined in 33.2.6. When read as a zero, bit 12.13 indicates that the PSE lacks support for Physical Layer classification. If supported, the function may be enabled or disabled through the Enable Physical Layer Classification bit (11.4).

33.5.1.2.4 Power Denied or Removed (12.12)

When read as a one, bit 12.12 indicates that power has been denied or has been removed due to a fault condition. This bit shall be set to one when the PSE state diagram (Figure 33–9) enters the states 'POWER_DENIED' or 'ERROR_DELAY.' The Power Denied bit shall be implemented with latching high behavior as defined in 33.5.1.

33.5.1.2.5 Valid Signature (12.11)

When read as a one, bit 12.11 indicates that a valid signature has been detected. This bit shall be set to one when mr_valid_signature transitions from FALSE to TRUE. The Valid Signature bit shall be implemented with latching high behavior as defined in 33.5.1.

33.5.1.2.6 Invalid Signature (12.10)

When read as a one, bit 12.10 indicates that an invalid signature has been detected. This bit shall be set to one when the PSE state diagram (Figure 33–9) enters the state 'SIGNATURE_INVALID'. The Invalid Signature bit shall be implemented with latching high behavior as defined in 33.5.1.

33.5.1.2.7 Short Circuit (12.9)

When read as a one, bit 12.9 indicates that a short circuit condition has been detected. This bit shall be set to one when the PSE state diagram (Figure 33–9) enters the state 'ERROR_DELAY.' The Short Circuit bit shall be implemented with latching high behavior as defined in 33.5.1.

33.5.1.2.8 Overload (12.8)

When read as a one, bit 12.8 indicates that an overload condition has been detected. This bit shall be set to one when the PSE state diagram (Figure 33–9) enters the state 'ERROR_DELAY_OVER'. The Overload bit shall be implemented with latching high behavior as defined in 33.5.1.

33.5.1.2.9 MPS Absent (12.7)

When read as a one, bit 12.7 indicates that an MPS Absent condition has been detected. The MPS Absent bit shall be set to one when the PSE state diagram (Figure 33–9) transitions directly from the state POWER_ON to IDLE due to tmpdo_timer_done being asserted. The MPS Absent bit shall be implemented with latching high behavior as defined in 33.5.1.

33.5.1.2.10 PD Class (12.6:4)

Bits 12.6:4 report the PD Class of a detected PD as specified in 33.2.5 and 33.2.6. The value in this register is valid while a PD is connected, i.e., while the PSE Status (12.3:1) bits are reporting "delivering power." The combinations '110' and '111' for bits 12.6:4 have been reserved for future use.

33.5.1.2.11 PSE Status (12.3:1)

Bits 12.3:1 report the current status of the PSE. When read as '000', bits 12.3:1 indicate that the PSE state diagram (Figure 33–9) is in the state DISABLED. When read as '010', bits 12.3:1 indicate that the PSE state diagram is in the state POWER_ON. When read as '011', bits 12.3:1 indicate that the PSE state diagram is in the state TEST_MODE. When read as '100', bits 12.3:1 indicate that the PSE state diagram is in the state TEST_ERROR. When read as '101', bits 12.3:1 indicate that the PSE state diagram is in the state IDLE due to the variable error_condition = true. When read as '001', bits 12.3:1 indicate that the PSE state diagram is in a state other than those listed above.

The combinations '111' and '110' for bits 12.3:1 have been reserved for future use.

33.5.1.2.12 Pair Control Ability (12.0)

When read as a one, bit 12.0 indicates that the PSE supports the option to control which PSE Pinout Alternative (see 33.2.1) is used for PD detection and power through the Pair Control (11.3:2) bits. When read as a zero, bit 12.0 indicates that the PSE lacks support of the option to control which PSE Pinout Alternative is used for PD detection and power through the Pair Control (11.3:2) bits.

33.6 Data Link Layer classification

Additional control and classification functions are supported using Data Link Layer classification using frames based on the IEEE 802.3 Organizationally Specific TLVs defined in Clause 79. Type 2 PDs that require more than 13.0 W support Data Link Layer classification (see 33.3.5). Data Link Layer classification is optional for all other devices.

All reserved fields in transmitted Power via MDI TLVs shall contain zero, and all reserved fields in received Power via MDI TLVs shall be ignored.

33.6.1 TLV frame definition

Implementations that support Data Link Layer classification shall comply with all mandatory parts of IEEE Std 802.1AB-20XX; shall support the Power via MDI Type, Length, Value (TLV) defined in 79.3.2; and shall support the control state diagrams defined in 33.6.3.

33.6.2 Data Link Layer classification timing requirements

A Type 2 PSE shall send an LLDPDU containing a Power via MDI TLV within 10 seconds of Data Link Layer classification being enabled in the PSE as indicated by the variable pse_dll_enabled (33.2.4.4, 33.6.3.3).

A Type 1 PSE that implements Data Link Layer classification shall send an LLDPDU containing a Power via MDI TLV when the PSE Data Link Layer classification engine is ready as indicated by the variable pse_dll_ready (33.6.3.3).

All Type 1 PDs that implement Data Link Layer classification and Type 2 PDs shall set the state variable pd_dll_ready within 5 minutes of Data Link Layer classification being enabled in a PD as indicated by the variable pd_dll_enabled (33.3.3.3, 33.6.3.3).

Under normal operation, an LLDPDU containing a Power via MDI TLV with an updated value for the "PSE allocated power value" field shall be sent within 10 seconds of receipt of an LLDPDU containing a Power via MDI TLV where the "PD requested power value" field is different from the previously communicated value.

Under normal operation, an LLDPDU containing a Power via MDI TLV with an updated value for the "PD requested power value" field shall be sent within 10 seconds of receipt of an LLDPDU containing a Power via MDI TLV where the "PSE allocated power value" field is different from the previously communicated value.

33.6.3 Power control state diagrams

The power control state diagrams for PSEs and PDs specify the externally observable behavior of a PSE and PD Data Link Layer classification respectively. PSE Data Link Layer classification shall provide the behavior of the state diagram as shown in Figure 33–27. PD Data Link Layer classification shall provide the behavior of the state diagram as shown in Figure 33–28.

33.6.3.1 Conventions

The body of this subclause is comprised of state diagrams, including the associated definitions of variables, constants, and functions. Should there be a discrepancy between a state diagram and descriptive text, the state diagram prevails.

The notation used in the state diagrams follows the conventions of state diagrams as described in 21.5.

33.6.3.2 Constants

PD_DLLMAX_VALUE

This value is derived from pd_max_power variable (33.3.3.3) described as follows:

pd_max_power	PD_DLLMAX_VALUE
0	130
1	39
2	65
3	130
4	255

PD_INITIAL_VALUE

This value is derived as follows from the pd_max_power (33.3.3.3) variable used in the PD state diagram (Figure 33–16):

pd_max_power	PD_INITIAL_VALUE
0	≤ 130
1	≤ 39
2	≤ 65
3	≤ 130
4	≤ 255

PSE_INITIAL_VALUE

This value is derived as follows from parameter_type and the mr_pd_class_detected (33.2.4.6) variable used in the PSE state diagram (Figure 33–9):

parameter_type	mr_pd_class_detected	PSE_INITIAL_VALUE

1	0	130
1	1	39
1	2	65
1	3	130
1	4	130
2	4	255

33.6.3.3 Variables

The PSE power control state diagram (Figure 33–27) and PD power control state diagram (Figure 33–28) use the following variables:

MirroredPDRequestedPowerValue
: The copy of PDRequestedPowerValue that the PSE receives from the remote system. This variable is mapped from the aLldpXdot3RemPDRequestedPowerValue attribute (30.12.3.1.17). Actual power numbers are represented using an integer value that is encoded according to Equation (79–1), where *X* is the decimal value of MirroredPDRequestedPowerValue.
Values: 0 through 255

MirroredPSEAllocatedPowerValue
: The copy of PSEAllocatedPowerValue that the PD receives from the remote system. This variable is mapped from the aLldpXdot3RemPSEAllocatedPowerValue attribute (30.12.3.1.18). Actual power numbers are represented using an integer value that is encoded according to Equation (79–2), where *X* is the decimal value of MirroredPSEAllocatedPowerValue.
Values: 0 through 255

MirroredPSEAllocatedPowerValueEcho
: The copy of PSEAllocatedPowerValue that the PSE receives from the remote system. This variable is mapped from the aLldpXdot3RemPSEAllocatedPowerValue attribute (30.12.3.1.18).

PDRequestedPowerValueEcho
: This variable is updated by the PSE state diagram. This variable maps into the aLldpXdot3LocPDRequestedPowerValue attribute (30.12.2.1.17).
Values: 0 through 255

PDMaxPowerValue
: Integer that indicates the actual PD power value of the local system. The actual PD power value for a PD is the maximum input average power (see 33.3.7.2) the PD ever draws under the current power allocation. Actual power numbers are represented using an integer value that is encoded according to Equation (79–1), where *X* is the decimal value of PDMaxPowerValue.

PDRequestedPowerValue
: Integer that indicates the PD requested power value in the PD. The value is the maximum input average power (see 33.3.7.2) the PD requests. This power value is encoded according to Equation (79–1), where *X* is the decimal value of PDRequestedPowerValue. This variable is mapped from the aLldpXdot3LocPDRequestedPowerValue attribute (30.12.2.1.17).
Values: 0 through PD_DLLMAX_VALUE

PSEAllocatedPowerValue
: Integer that indicates the PSE allocated power value in the PSE. The value is the maximum input average power (see 33.3.7.2) the PD ever draws. The power value for a PSE is the maximum input average power the PD may ever draw. This power value is encoded according to Equation (79–2), where *X* is the decimal value of PSEAllocatedPowerValue. This variable is mapped from the aLldpXdot3LocPSEAllocatedPowerValue attribute (30.12.2.1.18).
Values: 0 through 255

PSEAllocatedPowerValueEcho
: This variable is updated by the PD state diagram. This variable maps into the aLldpXdot3LocPSEAllocatedPowerValue attribute (30.12.2.1.18).
Values: 0 through 255

TempVar

A temporary variable used to store Power Value. Actual power numbers are represented using an integer value that is encoded according to Equation (79–1) or Equation (79–2), where *X* is the decimal value of TempVar.

local_system_change

An implementation-specific control variable that indicates that the local system wants to change the allocated power value. In a PSE, this indicates it is going to change the power allocated to the PD. In a PD, this indicates it is going to request a new power allocation from the PSE.

Values: FALSE: The local system does not wants to change the power allocation.
TRUE: The local system wants to change the power allocation.

parameter_type

A control variable output by the PSE state diagram (Figure 33–9) used by a Type 2 PSE to choose operation with Type 1 or Type 2 PSE output PI electrical requirement parameter values defined in Table 33–11.

Values: 1: Type 1 PSE parameter values (default).
2: Type 2 PSE parameter values.

pd_dll_enabled

A variable output by the PD state diagram (Figure 33–16) to indicate if the PD Data Link Layer classification mechanism is enabled.

Values: FALSE: PD Data Link Layer classification is not enabled.
TRUE: PD Data Link Layer classification is enabled.

pd_dll_power_type

A control variable that indicates the type of PD that is connected to the PSE as advertised through Data Link Layer classification.

Values: 1: PD is a Type 1 PD (default).
2: PD is a Type 2 PD.

pd_dll_ready

An implementation-specific control variable that indicates that the PD has initialized Data Link Layer classification. This variable maps into the aLldpXdot3LocReady attribute (30.12.2.1.20).

Values: FALSE: Data Link Layer classification has not completed initialization.
TRUE: Data Link Layer classification has completed initialization.

pse_dll_enabled

A variable output by the PSE state diagram (Figure 33–9) to indicate if the PSE Data Link Layer classification mechanism is enabled.

Values: FALSE: PSE Data Link Layer classification is not enabled.
TRUE: PSE Data Link Layer classification is enabled.

pse_dll_power_type

A control variable that indicates the type of the PSE by which the PD is being powered.

Values: 1: PSE is a Type 1 PSE (default).
2: PSE is a Type 2 PSE.

pse_dll_ready

An implementation-specific control variable that indicates that the PSE has initialized Data Link Layer classification. This variable maps into the aLldpXdot3LocReady attribute (30.12.2.1.20).

Values: FALSE: Data Link Layer classification has not completed initialization.
TRUE: Data Link Layer classification has completed initialization.

pse_power_type

A control variable output by the PD state diagram (Figure 33–16) to indicate the type of PSE by which it is being powered.

A summary cross-references between the DTE Power via MDI classification local and remote object class attributes and the PSE and PD power control state diagrams, including the direction of the mapping, is provided in Table 33–23.

33.6.3.4 Functions

pse_power_review

This function evaluates the power allocation or budget of the PSE based on local system changes. The function returns the following variables:

PSE_NEW_VALUE:

The new max power value that the PSE expects the PD to draw. Actual power numbers are represented using an integer value that is encoded according to Equation (79–2), where *X* is the decimal value of PSE_NEW_VALUE.

pd_power_review

This function evaluates the power requirements of the PD based on local system changes and/or changes in the PSE allocated power value. The function returns the following variables:

PD_NEW_VALUE:

The new max power value that the PD wants to draw. Actual power numbers are represented using an integer value that is encoded according to Equation (79–1), where *X* is the decimal value of PD_NEW_VALUE.

Table 33–23—Attribute to state diagram variable cross-reference

Entity	Attribute	Mapping	State diagram variable
oLldpXdot3LocSystemsGroup Object Class			
PSE	aLldpXdot3LocPDRequestedPowerValue	⇐	PDRequestedPowerValueEcho
	aLldpXdot3LocPSEAllocatedPowerValue	⇐	PSEAllocatedPowerValue
	aLldpXdot3LocReady	⇐	pse_dll_ready
PD	aLldpXdot3LocPDRequestedPowerValue	⇐	PDRequestedPowerValue
	aLldpXdot3LocPSEAllocatedPowerValue	⇐	PSEAllocatedPowerValueEcho
	aLldpXdot3LocReady	⇐	pd_dll_ready
oLldpXdot3RemSystemsGroup Object Class			
PSE	aLldpXdot3RemPDRequestedPowerValue	⇒	MirroredPDRequestedPowerValue
	aLldpXdot3RemPSEAllocatedPowerValue	⇒	MirroredPSEAllocatedPowerValueEcho
	aLldpXdot3RemPowerType Value[a] 11 01	 ⇒ ⇒	pd_dll_power_type Value[a] 01 10
PD	aLldpXdot3RemPSEAllocatedPowerValue	⇒	MirroredPSEAllocatedPowerValue
	aLldpXdot3RemPowerType Value[a] 10 00	 ⇒ ⇒	pse_dll_power_type Value[a] 01 10

[a]Other value combinations mapping from aLldpXdot3RemPowerType to pd_dll_power_type or pse_dll_power_type are not possible.

33.6.3.5 State diagrams

The general state change procedure for PSEs is shown in Figure 33–27.

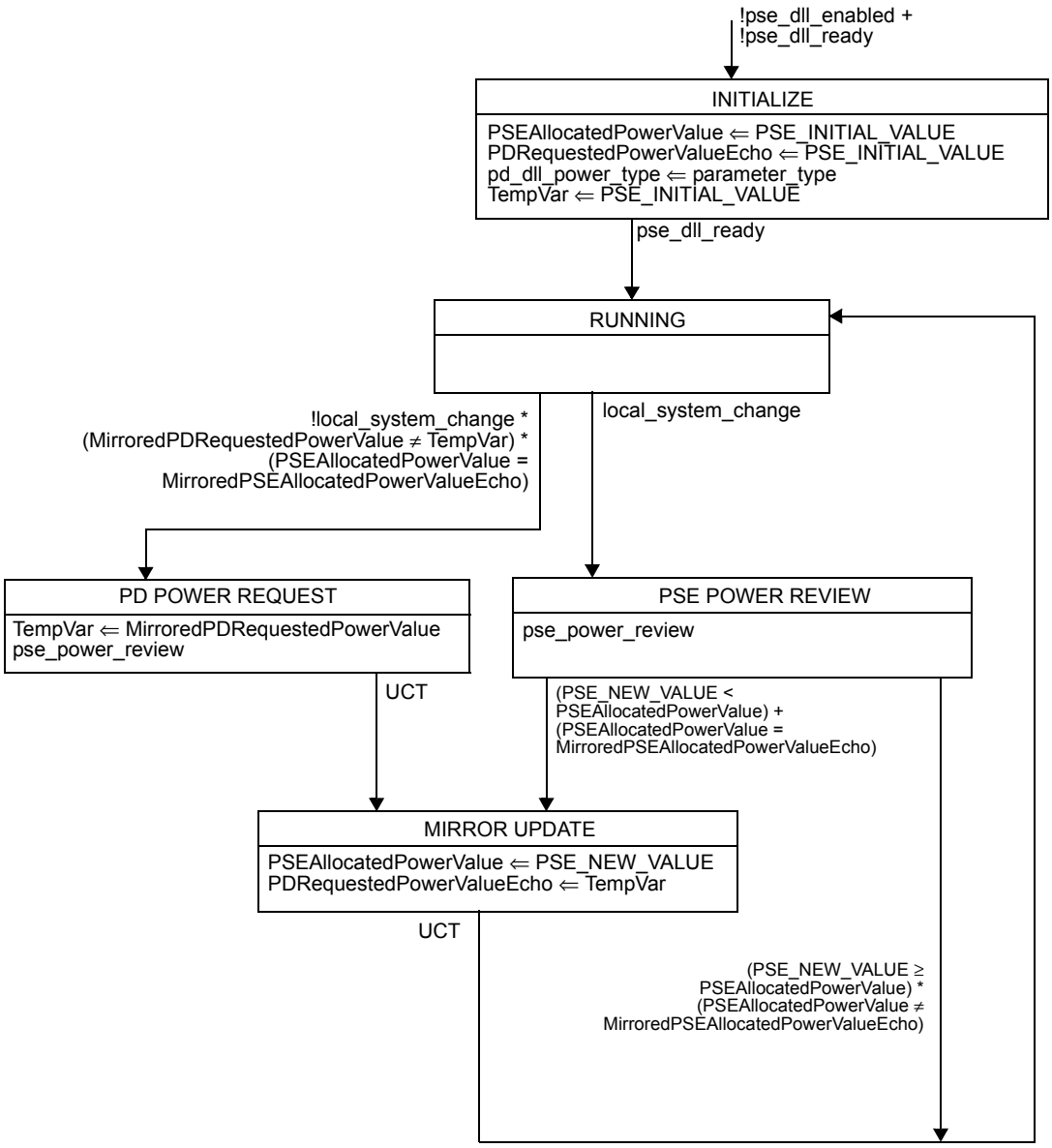


Figure 33–27—PSE power control state diagram

The general state change procedure for PDs is shown in Figure 33–28.

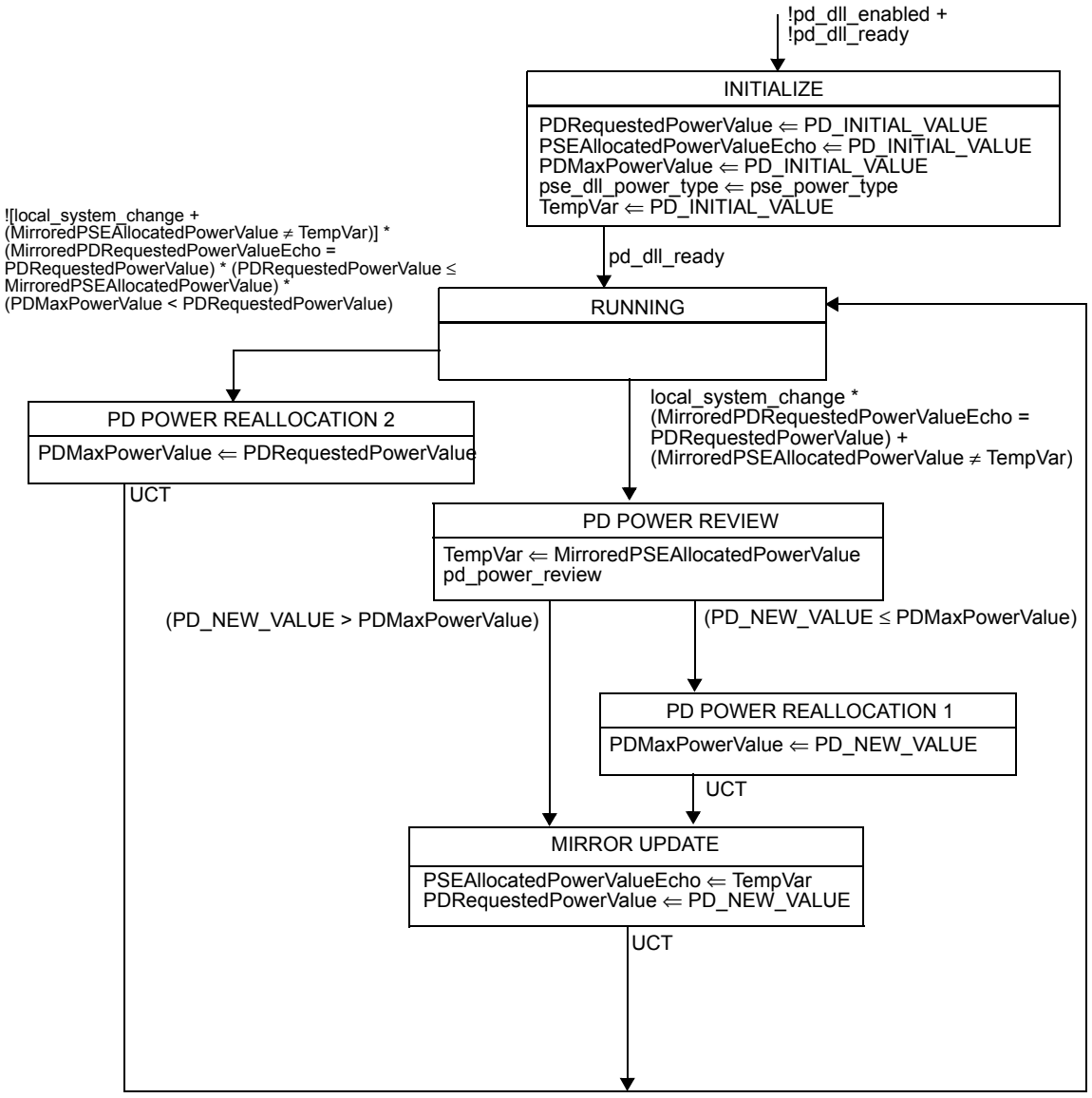


Figure 33–28—PD power control state diagram

33.6.4 State change procedure across a link

The PSE and PD utilize the LLDPDUs to advertise their various attributes to the other entity.

The PD may request a new power value through the aLldpXdot3LocPDRequestedPowerValue (30.12.2.1.17) attribute in the oLldpXdot3LocSystemsGroup object class. The request appears to the PSE as a change to the aLldpXdot3RemPDRequestedPowerValue (30.12.3.1.17) attribute in the oLldpXdot3RemSystemsGroup object class.

The PSE responds to the PD's request through the aLldpXdot3LocPSEAllocatedPowerValue (30.12.2.1.18) attribute in the oLldpXdot3LocSystemsGroup object class. The PSE also copies the value of the aLldpXdot3RemPDRequestedPowerValue (30.12.3.1.17) in the oLldpXdot3RemSystemsGroup object class

to the aLldpXdot3LocPDRequestedPowerValue (30.12.2.1.17) in the oLldpXdot3LocSystemsGroup object class. This appears to the PD as a change to the aLldpXdot3RemPSEAllocatedPowerValue (30.12.3.1.18) attribute in the oLldpXdot3RemSystemsGroup object class.

The PSE may allocate a new power value through the aLldpXdot3LocPSEAllocatedPowerValue (30.12.2.1.18) attribute in the oLldpXdot3LocSystemsGroup object class. The request appears to the PD as a change to the aLldpXdot3RemPSEAllocatedPowerValue (30.12.3.1.18) attribute in the oLldpXdot3RemSystemsGroup object class. The PD responds to a PSE's request through the aLldpXdot3LocPDRequestedPowerValue (30.12.2.1.17) attribute in the oLldpXdot3LocSystemsGroup object class. The PD also copies the value of the aLldpXdot3RemPSEAllocatedPowerValue (30.12.3.1.18) attribute in the oLldpXdot3RemSystemsGroup object class to the aLldpXdot3LocPSEAllocatedPowerValue (30.12.2.1.18) attribute in the oLldpXdot3LocSystemsGroup object class. This appears to the PSE as a change to the aLldpXdot3RemPDRequestedPowerValue (30.12.3.1.17) attribute in the oLldpXdot3RemSystemsGroup object class.

The state diagrams describe the behavior above.

33.6.4.1 PSE state change procedure across a link

A PSE is considered to be in sync with the PD when the value of PSEAllocatedPowerValue matches the value of MirroredPSEAllocatedPowerValueEcho. When the PSE is not in sync with the PD, the PSE is only allowed to decrease its power allocation.

During normal operation, the PSE is in the RUNNING state. If the PSE wants to initiate a change in the PD allocation, the local_system_change is asserted and the PSE enters the PSE POWER REVIEW state, where a new power allocation value, PSE_NEW_VALUE, is computed. If the PSE is in sync with the PD or if PSE_NEW_VALUE is smaller than PSEAllocatedPowerValue, it enters the MIRROR UPDATE state where PSE_NEW_VALUE is assigned to PSEAllocatedPowerValue. It also updates PDRequestedPowerValueEcho and returns to the RUNNING state.

If the PSE sees a change to the previously stored MirroredPDRequestedPowerValue, it recognizes a request by the PD to change its power allocation. It entertains this request only when it is in sync with the PD. The PSE examines the request by entering the PD POWER REQUEST state. A new power allocation value, PSE_NEW_VALUE, is computed. It then enters the MIRROR UPDATE state where PSE_NEW_VALUE is assigned to PSEAllocatedPowerValue. It also updates PDRequestedPowerValueEcho and returns to the RUNNING state.

33.6.4.2 PD state change procedure across a link

A PD is considered to be in sync with the PSE when the value of PDRequestedPowerValue matches the value of MirroredPDRequestedPowerValueEcho. The PD is not allowed to change its maximum power draw or the requested power value when it is not in sync with the PSE.

During normal operation, the PD is in the RUNNING state. If the PD sees a change to the previously stored MirroredPSEAllocatedPowerValue or local_system_change is asserted by the PD so as to change its power allocation, it enters the PD POWER REVIEW state. In this state, the PD evaluates the change and generates an updated power value called PD_NEW_VALUE. If PD_NEW_VALUE is less than PDMaxPowerValue, it updates PDMaxPowerValue in the PD POWER REALLOCATION 1 state. The PD finally enters the MIRROR UPDATE state where PD_NEW_VALUE is assigned to PDRequestedPowerValue. It also updates PSEAllocatedPowerValueEcho and returns to the RUNNING state.

In the above flow, if PD_NEW_VALUE is greater than PDMaxPowerValue, the PD waits until it is in sync with the PSE and the PSE grants the higher power value. When this condition arises, the PD enters the PD

POWER REALLOCATION 2 state. In this state, the PD assigns PDMaxPowerValue to PDRequestedPowerValue and returns to the RUNNING state.

33.7 Environmental

33.7.1 General safety

All equipment subject to this clause shall conform to IEC 60950-1:2001. In particular, the PSE shall be classified as a Limited Power Source in accordance with IEC 60950-1:2001.

Equipment shall comply with all applicable local and national codes related to safety.

33.7.2 Network safety

This subclause sets forth a number of recommendations and guidelines related to safety concerns. The list is neither complete nor does it address all possible safety issues. The designer is urged to consult the relevant local, national, and international safety regulations to verify compliance with the appropriate requirements. LAN cabling systems described in this clause are subject to at least four direct electrical safety hazards during their installation and use. These hazards are as follows:

a) Direct contact between LAN components and power, lighting, or communications circuits.
b) Static charge buildup on LAN cabling and components.
c) High-energy transients coupled onto the LAN cabling system.
d) Voltage potential differences between safety grounds to which various LAN components are connected.

Such electrical safety hazards should be avoided or appropriately protected against for proper network installation and performance. In addition to provisions for proper handling of these conditions in an operational system, special measures should be taken to verify that the intended safety features are not negated during installation of a new network or during modification of an existing network.

33.7.3 Installation and maintenance guidelines

It is a mandatory requirement that sound installation practice, as defined by applicable local codes and regulations, be followed in every instance in which such practice is applicable.

It is a mandatory requirement that, during installation of the cabling plant, care be taken to verify that non-insulated network cabling conductors do not make electrical contact with unintended conductors or ground.

33.7.4 Patch panel considerations

It is possible that the current carrying capability of a cabling cross-connect may be exceeded by a PSE. The designer should consult the manufacturers' specifications to verify compliance with the appropriate requirements.

33.7.5 Telephony voltages

The use of building wiring brings with it the possibility of wiring errors that may connect telephony voltages to a PSE or PD. Other than voice signals, the primary voltages that may be encountered are the "battery" and ringing voltages. Although there is no universal standard, the following maximums generally apply:

Battery voltage to a telephone line is generally 56 Vdc, applied to the line through a balanced 400 Ω source impedance. Ringing voltage is a composite signal consisting of an AC component and a DC component. The

AC component is up to 175 Vp at 20 Hz to 60 Hz with a 100 Ω source resistance. The DC component is 56 Vdc with 300 Ω to 600 Ω source resistance. Large reactive transients can occur at the start and end of each ring interval.

Application of any of the above voltages to the PI of a PSE or a PD shall not result in any safety hazard.

33.7.6 Electromagnetic emissions

The PD and PSE powered cabling link shall comply with applicable local and national codes for the limitation of electromagnetic interference.

33.7.7 Temperature and humidity

The PD and PSE powered cabling link segment is expected to operate over a reasonable range of environmental conditions related to temperature, humidity, and physical handling. Specific requirements and values for these parameters are beyond the scope of this standard.

33.7.8 Labeling

It is recommended that the PSE or PD (and supporting documentation) be labeled in a manner visible to the user with at least the following parameters:

a) Power classification and power level in terms of maximum current drain over the operating voltage range, 36 V to 57 V, applies for PD only
b) Port type (e.g., 100BASE-TX, TIA Category, or ISO Class)
c) Any applicable safety warnings
d) “PSE” or “PD” as appropriate
e) Type (e.g., “Type 1” or “Type 2”)

33.8 Protocol implementation conformance statement (PICS) proforma for Clause 33, DTE Power via MDI[4]

33.8.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 33, DTE Power via MDI, shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

33.8.2 Identification

33.8.2.1 Implementation identification

Supplier[1]	
Contact point for enquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1,3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	
NOTE 1—Required for all implementations NOTE 2—May be completed as appropriate in meeting the requirements for the identification. NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

33.8.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3at-2009, Clause 33, DTE Power via MDI
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3at-2009.)	
Date of Statement	

[4]*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

33.8.2.3 PD Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
*PDT2	Type 2 PD implementation	33.3.2	PD is Type 2	O	Yes [ ] No [ ]
*PDCL	PD Classification	33.3.5	PD supports classification	PDT2:M	Yes [ ] No [ ]
*PDCL2	Implementation supports 2-Event class signature	33.3.5	PD supports 2-Event class signature	PDT2:M	Yes [ ] No [ ]
*DLLC	Implementation supports Data Link Layer classification	33.6	PD supports Data Link Layer classification	PDT2:M	Yes [ ] No [ ]

33.8.2.4 PSE Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
*PSET1	Type 1 PSE implementation	33.1.4	Optional	O	Yes [ ] No [ ]
*PSET2	Type 2 PSE implementation	33.1.4	Optional	O	Yes [ ] No [ ]
*MID	Midspan PSE	33.2.1	PSE implemented as a midspan device	O/1	Yes [ ] No [ ]
*MIDA	Alternative A Midspan PSE	33.2.2	Midspan PSE implements Alternative A	MID:O:2	Yes [ ] No [ ]
*MAN	PSE supports management registers accessed through MII Management Interface	33.5	Optional	O	Yes [ ] No [ ]
*CL	Implementation supports Physical Layer classification	33.2.6	Optional	O/1	Yes [ ] No [ ]
*DLLC	Implementation supports Data Link Layer classification	33.6	PSE supports Data Link Layer classification	O	Yes [ ] No [ ]
*1EPLC	Implementation supports 1-Event Physical Layer classification	33.2.6.1	Optional	O	Yes [ ] No [ ]
*2EPLC	Implementation supports 2-Event Physical Layer classification	33.2.6.2	Optional	O	Yes [ ] No [ ]
*PA	Power Allocation	33.2.8	PSE implements power supply allocation	O	Yes [ ] No [ ]
*PCA	Pair control ability—PSE supports the option to control which PSE Pinout is used	33.5.1.1.5	Optional	O	Yes [ ] No [ ]
*AC	Monitor AC MPS	33.2.9.1.1	PSE monitors for AC MPS	O.3	Yes [ ] No [ ]
*DC	Monitor DC MPS	33.2.9.1.2	PSE monitors for DC MPS	O.3	Yes [ ] No [ ]

33.8.3 PICS proforma tables for DTE Power via MDI

33.8.3.1 Common device features

Item	Feature	Subclause	Value/Comment	Status	Support
COM1	Compatibility considerations.	33.1.2	PDs and PSEs compatible at their PIs	M	Yes [ ]
COM2	Type 2 operation cabling	33.1.4.1	DC loop resistance 25 Ω or less. Requirement satisfied by category 5e components (cables, cords, and connectors)	M	Yes [ ]
COM3	Resistance unbalance	33.1.4.2	3 % or less	M	Yes [ ]

33.8.3.2 Power sourcing equipment

Item	Feature	Subclause	Value/Comment	Status	Support
PSE1	PSE location	33.2.1	Requirements apply equally to Endpoint and Midspan PSE unless otherwise stated	M	Yes [ ]
PSE2	Alternative A and Alternative B	33.2.3	Implement either Alternative A or Alternative B or both but not operate on same link segment simultaneously	M	Yes [ ] N/A [ ]
PSE3	PSE behavior	33.2.4	In accordance with state diagrams shown in Figure 33–9, Figure 33–9, and Figure 33–10	M	Yes [ ]
PSE4	Detection, classification, and turn on timing	33.2.4.1	In accordance with Table 33–4, Table 33–10, and Table 33–11	M	Yes [ ]
PSE5	Backoff voltage	33.2.4.1	Not greater than V_{Off}	M	Yes [ ]
PSE6	PSE variable definition permutations	33.2.4.4	Meet at least one allowable definition described in Table 33–3	M	Yes [ ]
PSE7	Type 2 PSE mutual identification	33.2.4.6	When powering a Type 2 PD, assigns a value of '2' to parameter_type if mutual identification is complete	PSET2: M	Yes [ ] N/A [ ]
PSE8	Type 2 PSE powering a Type 1 PD	33.2.4.6	Meets the PI electrical requirements of a Type 1 PSE, but may choose to meet the electrical requirements of a Type 2 PSE for I_{Con}, I_{LIM}, T_{LIM}, and P_{Type}	PSET2: M	Yes [ ] N/A [ ]
PSE9	Applying power	33.2.5	Not until a PD requesting power has been successfully detected	M	Yes [ ]
PSE10	Power pairs	33.2.5	Power supplied on the same pairs as those used for detection	M	Yes [ ]
PSE11	Detecting PDs	33.2.5.1	Performed via the PSE PI	M	Yes [ ]

Item	Feature	Subclause	Value/Comment	Status	Support
PSE12	PSE presents non-valid signature	33.2.5.1	As defined in Table 33–15	M	Yes [ ]
PSE13	Open circuit voltage and short circuit current	33.2.5.1	Meet specifications for V_{oc} and I_{sc} in Table 33–4	M	Yes [ ]
PSE14	Backdriven current	33.2.5.1	Not be damaged by up to 5 mA over the range of V_{Port_PSE}	M	Yes [ ]
PSE15	Output capacitance	33.2.5.1	C_{out} in Table 33–11	M	Yes [ ]
PSE16	Detection voltage with a valid PD signature connected	33.2.5.2	Meets V_{valid} in Table 33–4	M	Yes [ ]
PSE17	Detection voltage measurements	33.2.5.2	At least two that create at least ΔV_{test} difference	M	Yes [ ]
PSE18	Control slew rate when switching detection voltages	33.2.5.2	Less than V_{slew} in Table 33–4	M	Yes [ ]
PSE19	Accept as a valid signature	33.2.5.3	R_{good} and C_{good}, with up to V_{os} max and I_{os} max as defined in Table 33–5	M	Yes [ ]
PSE20	Reject as an invalid signature	33.2.5.4	Resistance less than R_{bad} min, resistance greater than R_{bad} max, or capacitance greater than C_{bad} min	M	Yes [ ]
PSE21	Classification permutations	33.2.6	Meet one allowable permutation in Table 33–8	M	Yes [ ]
PSE22	Type 1 PSE does not implement Physical Layer classification	33.2.6	Assign all PDs to Class 0	PSET1: M	Yes [ ] N/A [ ]
PSE23	Type 1 PSE failure to complete classification	33.2.6	Return to IDLE state or assign PD to Class 0	PSET1: M	Yes [ ] N/A [ ]
PSE24	Type 2 PSE failure to complete classification	33.2.6	Return to IDLE state	PSET2: M	Yes [ ] N/A [ ]
PSE25	Provide V_{Class} for 1-Event Physical Layer classification	33.2.6.1	Limited to I_{Class_LIM} as defined by Table 33–10	1EPLC: M	Yes [ ] N/A [ ]
PSE26	Classification polarity for 1-Event Physical Layer classification	33.2.6.1	Same as V_{Port_PSE}	1EPLC: M	Yes [ ] N/A [ ]
PSE27	Classification timing for 1-Event Physical Layer classification	33.2.6.1	In accordance with T_{pdc} in Table 33–10	1EPLC: M	Yes [ ] N/A [ ]
PSE28	Measurement result of 1-Event Physical Layer classification I_{Class}	33.2.6.1	Classify PD according to observed current based on Table 33–9	1EPLC: M	Yes [ ] N/A [ ]
PSE29	Measurement timing of 1-Event Physical Layer classification I_{Class}	33.2.6.1	Measurement taken after the minimum relevant class event timing in Table 33–10	1EPLC: M	Yes [ ] N/A [ ]
PSE30	Class 4 result for 1-Event Physical Layer classification with a Type 1 PSE	33.2.6.1	Assign the PD to Class 0	PSET1: M	Yes [ ] N/A [ ]

Item	Feature	Subclause	Value/Comment	Status	Support
PSE31	Type 1 PSE 1-Event Physical Layer classification if I_{Class} is in the range of I_{Class_LIM}	33.2.6.1	Return to IDLE state or assign PD to Class 0	PSET1: M	Yes [ ] N/A [ ]
PSE32	Type 2 PSE 1-Event Physical Layer classification if I_{Class} is in the range of I_{Class_LIM}	33.2.6.1	Return to IDLE state	PSET2: M	Yes [ ] N/A [ ]
PSE33	In the CLASS_EV1 and CLASS_EV2 states, provide V_{Class}	33.2.6.2	As defined in Table 33–10	2EPLC: M	Yes [ ] N/A [ ]
PSE34	Classification timing in CLASS_EV1 state	33.2.6.2	In accordance with T_{CLE1} in Table 33–10	2EPLC: M	Yes [ ] N/A [ ]
PSE35	In the CLASS_EV1 and CLASS_EV2 states, measurement result I_{Class}	33.2.6.2	Classify PD according to Table 33–9	2EPLC: M	Yes [ ] N/A [ ]
PSE36	In the MARK_EV1 and MARK_EV2 states, provide V_{Mark}	33.2.6.2	In accordance with Table 33–10	2EPLC: M	Yes [ ] N/A [ ]
PSE37	Classification timing in MARK_EV1	33.2.6.2	In accordance with T_{ME1} in Table 33–10	2EPLC: M	Yes [ ] N/A [ ]
PSE38	Classification timing in CLASS_EV2 state	33.2.6.2	In accordance with T_{CLE2} in Table 33–10	2EPLC: M	Yes [ ] N/A [ ]
PSE39	Classification timing in MARK_EV2 state	33.2.6.2	In accordance with T_{ME2} in Table 33–10	2EPLC: M	Yes [ ] N/A [ ]
PSE40	Type 2 PSE 2-Event Physical Layer classification if I_{Class} is greater than or equal to I_{Class_LIM} min	33.2.6.2	Returns to IDLE state	2EPLC: M	Yes [ ] N/A [ ]
PSE41	Current limitation during class events	33.2.6.2	Meet I_{Class_LIM}	2EPLC: M	Yes [ ] N/A [ ]
PSE42	Current limitation during mark events	33.2.6.2	Meet I_{Mark_LIM}	2EPLC: M	Yes [ ] N/A [ ]
PSE43	Measurement timing of 2-Event Physical Layer classification I_{Class}	33.2.6.2	Taken after the minimum relevant class event timing in Table 33–10	2EPLC: M	Yes [ ] N/A [ ]
PSE44	Class event and mark event voltages polarity	33.2.6.2	Same as V_{Port_PSE}	2EPLC: M	Yes [ ] N/A [ ]
PSE45	Voltage level at PI when transition to POWER_ON state	33.2.6.2	Completes 2-Event classification and transitions to POWER_ON with PI voltage greater than or equal to V_{Mark} min	2EPLC: M	Yes [ ] N/A [ ]
PSE46	Return to IDLE state	33.2.6.2	Maintains PI voltage at V_{Reset} for at least T_{Reset} min before starting new detection cycle	2EPLC: M	Yes [ ] N/A [ ]
PSE47	Power supply output	33.2.7	When the PSE provides power to the PI, conforms with Table 33–11	M	Yes [ ]

Item	Feature	Subclause	Value/Comment	Status	Support
PSE48	Load regulation	33.2.7.1	Met with (I_{Hold} max × V_{Port_PSE} min) to P_{Type} min load step at a rate of change of at least 15 mA/µs max	M	Yes [ ]
PSE49	Voltage transients	33.2.7.1	Limited to 3.5 V/µs max for load changes up to 35 mA/µs	M	Yes [ ]
PSE50	Voltage transients (30 µs to 250 µs)	33.2.7.2	No less than K_{Tran_lo} below V_{Port_PSE} min and meet requirements of 33.2.7.7.	PSET2: M	Yes [ ]
PSE51	Voltage transients (greater than 250 µs)	33.2.7.2	Meet V_{Port_PSE} specification	M	Yes [ ]
PSE52	Power feeding ripple and noise	33.2.7.3	Met for common-mode and/or pair-to-pair noise values for power outputs from (I_{Hold} max × V_{Port_PSE} min) to P_{Type} min at static operating V_{Port_PSE}	M	Yes [ ]
PSE53	AC current waveform parameters	33.2.7.4	I_{Peak} minimum equals Equation (33–4) for T_{CUT} minimum and 5% duty cycle minimum.	M	Yes [ ]
PSE54	Inrush current limit	33.2.7.5	PSE limits the maximum current sourced at the PI	M	Yes [ ]
PSE55	Inrush current template	33.2.7.5	Current sourced does not exceed the PSE inrush template in Figure 33–13	M	Yes [ ]
PSE56	Short circuit condition	33.2.7.7	Remove power from PI before I_{PSEUT} is exceeded. Equation (33–6) and Figure 33–14.	M	Yes [ ]
PSE57	Short circuit current and time	33.2.7.7	In accordance with I_{LIM} and T_{LIM} in Table 33–11	M	Yes [ ]
PSE58	Short circuit power removal	33.2.7.7	Begins within T_{LIM} in Table 33–11	M	Yes [ ]
PSE59	Turn off time	33.2.7.8	Applies to the discharge time from V_{Port_PSE} to V_{Off} with a test resistor of 320 kΩ attached to the PI.	M	Yes [ ]
PSE60	Turn off voltage	33.2.7.9	Applies to the PI voltage in the IDLE state	M	Yes [ ]
PSE61	Current unbalance	33.2.7.11	Applies to the two conductors of a power pair over the current load range in accordance with I_{unb} in Table 33–11.	M	Yes [ ]
PSE62	Type 2 PSEs in the presence of (I_{unb} / 2)	33.2.7.11	Meet the requirements of 25.4.4a	PSET2: M	Yes [ ]
PSE63	Power allocation	33.2.8	Not be based solely on historical data of power consumption of the attached PD	PA:M	Yes [ ] N/A [ ]

Item	Feature	Subclause	Value/Comment	Status	Support
PSE64	PSE monitoring AC MPS component	33.2.9.1.1	Meets "AC Signal parameters" and "PSE PI voltage during AC disconnect detection" parameters in Table 33–12	AC:M	Yes [ ] N/A [ ]
PSE65	PSE AC MPS component present	33.2.9.1.1	When AC impedance at the PI is equal to or lower than $\|Z_{ac1}\|$ in Table 33–12	AC:M	Yes [ ] N/A [ ]
PSE66	PSE AC MPS component absent	33.2.9.1.1	When AC impedance at the PI equal to or greater than $\|Z_{ac2}\|$ in Table 33–12	AC:M	Yes [ ] N/A [ ]
PSE67	Power removal	33.2.9.1.1	When AC MPS has been absent for a time duration greater than T_{MPDO}	AC:M	Yes [ ] N/A [ ]
PSE68	PSE DC MPS component present	33.2.9.1.2	I_{Port} is greater than or equal to I_{Hold} max for at least T_{MPS} min as specified in Table 33–11	DC:M	Yes [ ] N/A [ ]
PSE69	PSE DC MPS component absent	33.2.9.1.2	I_{Port} is less than or equal to I_{Hold} min as specified in Table 33–11	DC:M	Yes [ ] N/A [ ]
PSE70	Power removal	33.2.9.1.2	When DC MPS has been absent for a time duration greater than T_{MPDO}	DC:M	Yes [ ] N/A [ ]
PSE71	Not remove power	33.2.9.1.2	When the DC current is greater than or equal to I_{Hold} max continuously for at least T_{MPS} every $T_{MPS} + T_{MPDO}$	DC:M	Yes [ ] N/A [ ]

33.8.3.3 Powered devices

Item	Feature	Subclause	Value/Comment	Status	Support
PD1	Accept power	33.3.1	On either set of PI conductors	M	Yes [ ]
PD2	Polarity insensitive	33.3.1	Both Mode A and Mode B per Table 33–13	M	Yes [ ]
PD3	Source power	33.3.1	The PD does not source power on its PI	M	Yes [ ]
PD4	Voltage tolerance	33.3.1	Withstand 0 V to 57 V at the PI indefinitely without permanent damage	M	Yes [ ]
PD5	Underpowered Type 2 PD	33.3.2	If PD does not successfully observe 2-Event Physical Layer classification or Data Link Layer classification, conforms to Type 1 PD power restrictions and provides the user with an active indication if underpowered	PDT2:M	Yes [ ] N/A [ ]
PD6	Current unbalance	33.3.2	Type 2 PDs meet the requirements of 25.4.4a in presence of (I_{unb}/2)	PDT2:M	Yes [ ] N/A [ ]
PD7	PD behavior	33.3.3	According to state diagram shown in Figure 33–16	M	Yes [ ]
PD8	Valid and non-valid detection signatures	33.3.4	Presented between positive V_{PD} and negative V_{PD} on each set of pairs defined in 33.3.1	M	Yes [ ]
PD9	Non-valid detection signature	33.3.4	When powered, present an invalid signature on the set of pairs not drawing power	M	Yes [ ]
PD10	Valid detection signature	33.3.4	Characteristics defined in Table 33–14	M	Yes [ ]
PD11	Non-valid detection signature	33.3.4	Exhibit one or both of the characteristics described in Table 33–15	M	Yes [ ]
PD12	PD classifications	33.3.5	Meets at least one permutation listed in Table 33–8	PDCL:M	Yes [ ]
PD13	PD implementing 2-Event class signature	33.3.5.1	Returns Class 4	PDCL2:M	Yes [ ] N/A [ ]
PD14	Type 2 PD classification behavior	33.3.5.1	Conforms to electrical specifications in Table 33–17	PDT2:M	Yes [ ] N/A [ ]
PD15	Classification signature	33.3.5.1	As defined in Table 33–16	PDCL:M	Yes [ ] N/A [ ]
PD16	Classification signature	33.3.5.1	One classification signature during classification	PDCL:M	Yes [ ] N/A [ ]
PD17	2-Event class signature	33.3.5.2	Class 4 in accordance with the maximum power draw as specified in Table 33–18	PDCL2:M	Yes [ ] N/A [ ]

Item	Feature	Subclause	Value/Comment	Status	Support
PD18	2-Event class signature behavior	33.3.5.2	As defined in Table 33–17	PDCL2:M	Yes [ ] N/A [ ]
PD19	Type 2 PD electrical requirements	33.3.5.2	As defined by Table 33–18 of the Type defined in its pse_power_type state variable	PDT2:M	Yes [ ] N/A [ ]
PD20	Mark event current and 2-Event class signature	33.3.5.2.1	Draw I_{Mark} and present a non-valid detection signature as defined in Table 33–15	PDCL2:M	Yes [ ] N/A [ ]
PD21	Mark event current limits	33.3.5.2.1	Not exceed I_{Mark} when voltage at the PI enters V_{Mark} as defined in Table 33–17	PDCL2:M	Yes [ ] N/A [ ]
PD22	PD current draw	33.3.5.2.1	I_{Mark} until the PD transitions from DO_MARK_EVENT state to the IDLE state	PDCL2:M	Yes [ ] N/A [ ]
PD23	PSE identification	33.3.6	Identify as Type 1 or Type 2 (see Figure 33–16)	PDT2:M	Yes [ ]
PD24	PD power supply	33.3.7	Operate within the characteristics in Table 33–18	M	Yes [ ]
PD25	PD turn on voltage	33.3.7.1	PD turns on at a voltage less than or equal to V_{On}	M	Yes [ ]
PD26	PD stay on voltage	33.3.7.1	Stay on for all voltages in the range of V_{Port_PD}	M	Yes [ ]
PD27	PD turn off voltage	33.3.7.1	Turn off at a voltage less than V_{Port_PD} min and greater than V_{Off}	M	Yes [ ]
PD28	Startup oscillations	33.3.7.1	Shall turn on or off without startup oscillations and within the first trial at any load value	M	Yes [ ]
PD29	P_{Port_PD} definition	33.3.7.2.1	When PD is fed by V_{Port_PD} min to V_{Port_PD} max with R_{Ch} (as defined in Table 33–1) in series	M	Yes [ ]
PD30	Type 2 PD input inrush current	33.3.7.3	With pse_power_type state set to 2 prior to power-on, operate as a Type 1 PD for at least T_{delay} min	PDT2:M	Yes [ ] N/A [ ]
PD31	Input inrush current	33.3.7.3	Limited by the PD if C_{port} is greater than or equal to 180 µF so that I_{Inrush_PD} max is satisfied.	M	Yes [ ]
PD32	Peak power	33.3.7.4	Not to exceed P_{Class_PD} max for more than T_{CUT} min and 5% duty cycle	M	Yes [ ]
PD33	Peak operating power	33.3.7.4	Not to exceed P_{Peak} max	M	Yes [ ]
PD34	RMS, DC, and ripple current	33.3.7.4	Bounded by Equation (33–10)	M	Yes [ ]
PD35	Maximum I_{Port} for all operating V_{Port_PD}	33.3.7.4	Defined by Equation (33–11)	M	Yes [ ]

Item	Feature	Subclause	Value/Comment	Status	Support
PD36	Peak transient current	33.3.7.5	Not to exceed 4.70 mA/μs in either polarity	M	Yes [ ]
PD37	Specifications for I_{PDUT}	33.3.7.5	Operate below upperbound template defined in Figure 33–18	M	Yes [ ]
PD38	Behavior during transients at the PSE PI	33.3.7.6	As specified in 33.3.7.6	M	Yes [ ]
PD39	Ripple and noise	33.3.7.7	As specified in Table 33–18 for the common-mode and/or differential pair-to-pair noise at the PD PI	M	Yes [ ]
PD40	Ripple and noise specification	33.3.7.7	For all operating voltages in the range defined by V_{Port_PD} in Table 33–18	M	Yes [ ]
PD41	Ripple and noise presence	33.3.7.7	Operates in the presence of ripple and noise generated by the PSE that appears at the PD PI	M	Yes [ ]
PD42	Classification stability	33.3.7.8	Class signature valid within T_{class} and remains valid for the duration of the classification period	M	Yes [ ]
PD43	Backfeed voltage	33.3.7.9	Mode A and Mode B per 33.3.7.9	M	Yes [ ]
PD44	Maintain power signature	33.3.8	PD provides a valid MPS at the PI as defined in 33.3.8	M	Yes [ ]
PD45	No longer require power	33.3.8	Remove both components of the Maintain Power Signature	M	Yes [ ]

33.8.3.4 Electrical specifications applicable to the PSE and PD

Item	Feature	Subclause	Value/Comment	Status	Support
EL1	Conductor isolation	33.4.1	Provided between accessible external conductors including frame ground and all MDI leads	M	Yes [ ]
EL2	Strength tests for electrical isolation	33.4.1	Withstand at least one of the electrical strength tests specified in 33.4.1	M	Yes [ ]
EL3	Insulation breakdown	33.4.1	No breakdown of insulation during electrical isolation tests	M	Yes [ ]
EL4	Isolation resistance	33.4.1	At least 2 MΩ, measured at 500 Vdc after electrical isolation tests	M	Yes [ ]
EL5	Isolation and grounding requirements	33.4.1	Conductive link segments that have different requirements have those requirements provided by the port-to-port isolation of the NID	M	Yes [ ]
EL6	Environment A requirements for multiple instances of PSE and/or PD	33.4.1.1.1	Meet or exceed the isolation requirement of the MAU/PHY with which they are associated	!MID:M	Yes [ ] N/A [ ]
EL7	Environment A requirement	33.4.1.1.1	Switch more negative conductor	M	Yes [ ] N/A [ ]
EL8	Environment B requirements for multiple instances of PSE and/or PD	33.4.1.1.2	Meet or exceed the isolation requirement of the MAU/PHY with which they are associated	!MID:M	Yes [ ] N/A [ ]
EL9	Fault tolerance for PIs encompassed within the MDI	33.4.2	Meet requirements of the appropriate specifying clause	!MID:M	Yes [ ] N/A [ ]
EL10	Fault tolerance for PSE PIs not encompassed within an MDI	33.4.2	Meet the requirements of 33.4.2	M	Yes [ ] N/A [ ]
EL11	Common-mode fault tolerance	33.4.2	Each wire pair withstands without damage a 1000 V common-mode impulse applied at E_{cm} of either polarity	M	Yes [ ]
EL12	The shape of the impulse for item common-mode fault tolerance	33.4.2	0.3/50 μs (300 ns virtual front time, 50 μs virtual time of half value)	M	Yes [ ]
EL13	Common-mode to differential-mode impedance balance for transmit and receive pairs	33.4.3	Exceeds Equation (33–15) for 10Mb/s PHYs and Equation (33–16) for 100Mb/s or greater PHYs	M	Yes [ ]
EL14	Common-mode AC output voltage	33.4.4	Magnitude while transmitting data and with power applied does not exceed 50 mV peak when operating at 10 Mb/s and 50 mV peak-to-peak when operating at 100 Mb/s or greater	M	Yes [ ]

Item	Feature	Subclause	Value/Comment	Status	Support
EL15	Frequency range for common-mode AC output voltage measurement	33.4.4	From 1 MHz to 100 MHz	M	Yes [ ]
EL16	Common-mode AC output voltage measurement	33.4.4	While the PHY is transmitting data, the PSE or PD is operating, and with the enumerated PSE load or PD source	M	Yes [ ]
EL17	Noise from an operating PSE or PD to the differential transmit and receive pairs	33.4.6	Does not exceed 10 mV peak-to-peak measured from 1 MHz to 100 MHz under the conditions specified in 33.4.4	M	Yes [ ]
EL18	Return loss requirements	33.4.7	Specified in 14.3.1.3.4 for a 10 Mb/s PHY, in ANSI X3.263:1995 for a 100 Mb/s PHY, and 40.8.3.1 for a 1000 Mb/s PHY	M	Yes [ ]
EL19	100BASE-TX Type 2 End-point PSE and PD channel unbalance	33.4.8	Meet requirements of Clause 25 in the presence of (I_{unb}/2)	M	Yes [ ] N/A [ ]

33.8.3.5 Electrical specifications applicable to the PSE

Item	Feature	Subclause	Value/Comment	Status	Support
PSEEL1	Short circuit fault tolerance	33.4.2	Any wire pair withstands any short circuit to any other pair for an indefinite amount of time	M	Yes [ ]
PSEEL2	Magnitude of short circuit current	33.4.2	Does not exceed I_{LIM} max	M	Yes [ ]
PSEEL3	Limitation of electromagnetic interference.	33.4.5	PSE complies with applicable local and national codes	M	Yes [ ]
PSEEL4	Alternative A Type 2 Midspan PSEs that support 100BASE-TX	33.4.8	Enforce channel unbalance currents less than or equal to Type 1 Iunb (see Table 33–11) or meet 33.4.9.2.	MIDA: M	Yes [ ] N/A [ ]
PSEEL5	Insertion of Midspan at FD	33.4.9	Comply with the guidelines specified in 33.4.9 items a) and b)	MID:M	Yes [ ] N/A [ ]
PSEEL6	Resulting “channel”	33.4.9	Installation of a Midspan PSE does not increase the length to more than 100 m as defined in ISO/IEC 11801.	MID:M	Yes [ ] N/A [ ]
PSEEL7	Configurations with Midspan PSE	33.4.9	Not alter transmission requirements of the “permanent link”	MID:M	Yes [ ] N/A [ ]
PSEEL8	DC continuity in power injecting pairs	33.4.9	Does not provide DC continuity between the two sides of the segment for the pairs that inject power	MID:M	Yes [ ] N/A [ ]

Item	Feature	Subclause	Value/Comment	Status	Support
PSEEL9	Midspan PSE inserted as a "connector" or "telecom outlet"	33.4.9.1	Meet transmission parameters NEXT, insertion loss, and return loss	MID:M	Yes [ ] N/A [ ]
PSEEL10	Midspan PSE NEXT	33.4.9.1.1	Meet values detemined by Equation (33–18) from 1 MHz to 100 MHz, but not greater than 65 dB	MID:M	Yes [ ] N/A [ ]
PSEEL11	Midspan PSE Insertion Loss	33.4.9.1.2	Meet values determined by Equation (33–19) from 1 MHz to 100 MHz, but not less than 0.1 dB	MID:M	Yes [ ] N/A [ ]
PSEEL12	Midspan PSE Return Loss	33.4.9.1.3	Meet or exceed values in Table 33–20 for transmit and receive pairs from 1 MHz to 100 MHz	MID:M	Yes [ ] N/A [ ]
PSEEL13	Work area or equipment cable Midspan PSE	33.4.9.1.4	Meet the requirements of this clause and the specifications for a Category 5 (jumper) cord as specified in ISO/IEC 11801-2002 or ANSI/TIA-568-C.2 for insertion loss, NEXT, and return loss for transmit and receive pairs	MID:M	Yes [ ] N/A [ ]
PSEEL14	Alternative A Midspan PSE signal path requirements	33.4.9.2	Exceed transfer function gain expressed in Equation (33–20) from 0.10 MHz to 1 MHz at the pins of the PI used as 100BASE-TX transmit pins	MIDA: M	Yes [ ] N/A [ ]
PSEEL15	Alternative A Midspan PSE signal path requirements bias current	33.4.9.2	Met with DC bias current between 0 mA and (I_{unb}/2)	MIDA: M	Yes [ ] N/A [ ]

33.8.3.6 Electrical specifications applicable to the PD

Item	Feature	Subclause	Value/Comment	Status	Support
PDEL1	PD common-mode test requirement	33.4.4	The PIs that require power terminated as illustrated in Figure 33–22	M	Yes [ ]

33.8.3.7 Management function requirements

Item	Feature	Subclause	Value/Comment	Status	Support
MF1	Management capability	33.5	Access to register definitions defined in 33.5.1 via interface described in 22.2.4 or 45.2 or equivalent	MAN:M	Yes [ ] N/A [ ]
MF2	PSE registers	33.5.1	Register address 11 for control functions and register address 12 for status functions	MAN:M	Yes [ ] N/A [ ]
MF3	Register bits latching high (LH)	33.5.1	Remain high until read via the management interface	MAN:M	Yes [ ] N/A [ ]
MF4	Latching register bit after read	33.5.1	Assumes a value based on the current state of the condition it monitors	MAN:M	Yes [ ] N/A [ ]
MF5	PSE Control register reserved bits (11.15:6)	33.5.1.1.1	Not affected by writes and return a value of zero when read	MAN:M	Yes [ ] N/A [ ]
MF6	Data Link Layer classification not supported	33.5.1.1.2	Ignore writes to bit 11.5 and return a value of zero when read	MAN* !DLLC: M	Yes [ ] N/A [ ]
MF7	Data Link Layer classification supported	33.5.1.1.2	Ignore writes to bit 11.5 and return a value of one when function cannot be disabled	MAN* DLLC: M	Yes [ ] N/A [ ]
MF8	Enable/disable Data Link Layer classification capability	33.5.1.1.2	Capability enabled by setting bit 11.5 to one and disabled by setting bit 11.5 to zero	MAN* DLLC: M	Yes [ ] N/A [ ]
MF9	Physical Layer classification not supported	33.5.1.1.3	Ignore writes to bit 11.4 and return a value of zero when read	MAN* !CL:M	Yes [ ] N/A [ ]
MF10	Physical Layer classification supported	33.5.1.1.3	Ignore writes to bit 11.4 and return a value of one when function cannot be disabled	MAN* CL:M	Yes [ ] N/A [ ]
MF11	Enable/disable Physical Layer classification	33.5.1.1.3	Function enabled by setting bit 11.4 to one and disabled by setting bit 11.5 to zero	MAN* CL:M	Yes [ ] N/A [ ]
MF12	Pair Control Ability not supported	33.5.1.1.4	Ignore writes to bits 11.3:2	MAN* !PCA:M	Yes [ ] N/A [ ]
MF13	Writes to 11.3:2 when Pair Control Ability not supported	33.5.1.1.4	Return the value that reports the supported PSE Pinout Alternative	MAN* !PCA:M	Yes [ ] N/A [ ]
MF14	Bits 11.3:2 set to '01'	33.5.1.1.4	Forces the PSE to use Alternative A	MAN* PCA:M	Yes [ ] N/A [ ]
MF15	Bits 11.3:2 set to '10'	33.5.1.1.4	Forces the PSE to use Alternative B	MAN* PCA:M	Yes [ ] N/A [ ]
MF16	Pair control ability bit (12.0)	33.5.1.1.4	A value of one sets the mr_pse_alternative variable	MAN* PCA:M	Yes [ ] N/A [ ]

Item	Feature	Subclause	Value/Comment	Status	Support
MF17	PSE function disabled	33.5.1.1.5	Setting PSE Enable bits 11.1:0 to a '00', also the MDI shall function as it would if it had no PSE function	MAN:M	Yes [ ] N/A [ ]
MF18	PSE function enabled	33.5.1.1.5	Setting PSE Enable bits 11.1:0 to a '01'	MAN:M	Yes [ ] N/A [ ]
MF19	PSE enable bits (11.1:0)	33.5.1.1.5	Writing to these register bits shall set mr_pse_enable to the corresponding value: '00' = disable, '01' = enable and '10' = force power	MAN:M	Yes [ ] N/A [ ]
MF20	PSE Type electrical parameters bit (12.15)	33.5.1.2.1	Set to zero when the PSE state diagram sets the state variable set_parameter_type to 1. Set to one when set_parameter_type is set to 2	MAN:M	Yes [ ] N/A [ ]
MF21	Data Link Layer classification enabled bit (12.14)	33.5.1.2.2	Set to one when the PSE state diagram sets true pse_dll_enabled. Set to zero when the PSE state diagram sets false pss_dll_enabled	MAN:M	Yes [ ] N/A [ ]
MF22	Power denied bit (12.12)	33.5.1.2.4	A value of one indicates power has been denied or removed due to an error condition	MAN:M	Yes [ ] N/A [ ]
MF23	Power denied bit implementation	33.5.1.2.4	Implemented with a latching high behavior as defined in 33.5.1	MAN:M	Yes [ ] N/A [ ]
MF24	Valid signature bit (12.11)	33.5.1.2.5	One indicates a valid signature has been detected. Set to one when mr_valid_signature transitions from FALSE to TRUE	MAN:M	Yes [ ] N/A [ ]
MF25	Valid signature bit implementation	33.5.1.2.5	Implemented with a latching high behavior as defined in 33.5.1	MAN:M	Yes [ ] N/A [ ]
MF26	Invalid signature bit (12.10)	33.5.1.2.6	One indicates an invalid signature has been detected. Set to one entering SIGNATURE_INVALID state	MAN:M	Yes [ ] N/A [ ]
MF27	Invalid signature bit implementation	33.5.1.2.6	Implemented with a latching high behavior as defined in 33.5.1	MAN:M	Yes [ ] N/A [ ]
MF28	Short circuit bit (12.9)	33.5.1.2.7	Bit indicates a short circuit condition has been detected. Set to one entering ERROR_DELAY state	MAN:M	Yes [ ] N/A [ ]
MF29	Short circuit bit implementation	33.5.1.2.7	Implemented with a latching high behavior as defined in 33.5.1	MAN:M	Yes [ ] N/A [ ]

Item	Feature	Subclause	Value/Comment	Status	Support
MF30	Overload bit (12.8)	33.5.1.2.8	Bit indicates an overload condition has been detected. Set to one when entering the ERROR_DELAY_OVER state	MAN:M	Yes [ ] N/A [ ]
MF31	Overload bit implementation	33.5.1.2.8	Implemented with a latching high behavior as defined in 33.5.1	MAN:M	Yes [ ] N/A [ ]
MF32	MPS absent bit (12.7)	33.5.1.2.9	Bit indicates an MPS Absent condition has been detected. Set to one when transitions directly from POWER_ON to IDLE state when MPS is absent for a duration greater than T_{MPDO} as specified in 33.2.9	MAN:M	Yes [ ] N/A [ ]
MF33	MPS Absent bit implementation	33.5.1.2.9	Implemented with a latching high behavior as defined in 33.5.1	MAN:M	Yes [ ] N/A [ ]

33.8.3.8 Data Link Layer classification requirements

Item	Feature	Subclause	Value/Comment	Status	Support
DLL1	Reserved fields	33.6	Reserved fields in Power via MDI TLV transmitted as zeroes and ignored upon receipt	M	Yes [ ] N/A [ ]
DLL2	Data Link Layer classification standards compliance	33.6.1	Meet mandatory parts of IEEE Std 802.1AB-2009	DLLC:M	Yes [ ] N/A [ ]
DLL3	TLV frame definitions	33.6.1	Meet requirements for Type, Length, and Value (TLV) defined in 79.3.2	DLLC:M	Yes [ ] N/A [ ]
DLL4	Control state diagrams	33.6.1	Meet state diagrams defined in 33.6.3	DLLC:M	Yes [ ] N/A [ ]
DLL5	Type 2 PSE LLDPDU	33.6.2	Transmitted within 10 seconds of Data Link Layer classification being enabled as indicated by pse_dll_enabled	DLLC:M	Yes [ ] N/A [ ]
DLL6	Type 1 PSE LLDPDU	33.6.2	Transmitted when Data Link Layer classification is ready as indicated by pse_dll_ready	DLLC:M	Yes [ ] N/A [ ]
DLL7	PD Data Link Layer classification ready	33.6.2	Set state variable pd_dll_ready within 5 min of Data Link Layer classification being enabled as indicated by pd_dll_enabled	DLLC:M	Yes [ ] N/A [ ]
DLL8	PD requested power value change	33.6.2	LLDPDU with updated “PSE allocated power value” sent within 10 seconds	DLLC:M	Yes [ ] N/A [ ]
DLL9	PSE allocated power value change	33.6.2	LLDPDU with updated “PD requested power value” sent within 10 seconds	DLLC:M	Yes [ ] N/A [ ]
DLL10	PSE power control state diagrams	33.6.3	Meet the behavior shown in Figure 33–27	DLLC:M	Yes [ ] N/A [ ]
DLL11	PD power control state diagrams	33.6.3	Meet the behavior shown in Figure 33–28	DLLC:M	Yes [ ] N/A [ ]

33.8.3.9 Environmental specifications applicable to PSEs and PDs

Item	Feature	Subclause	Value/Comment	Status	Support
ES1	Safety	33.7.1	Conforms to IEC 60950-1:2001	M	Yes [ ]
ES2	PSE classified as a limited power source	33.7.1	In accordance with IEC 60950-1:2001	M	Yes [ ]
ES3	Safety	33.7.1	Comply with all applicable local and national codes	M	Yes [ ]
ES4	Telephony voltages	33.7.5	Application thereof described in 33.7.5 not result in any safety hazard	M	Yes [ ]
ES5	Limitation of electromagnetic interference	33.7.6	PD and PSE powered cabling comply with applicable local and national codes	M	Yes [ ]

33.8.3.10 Environmental specifications applicable to the PSE

Item	Feature	Subclause	Value/Comment	Status	Support
PSEES1	Safety	33.7.1	Limited Power Source in accordance with IEC 60950-1:2001	M	Yes [ ]

79. IEEE 802.3 Organizationally Specific Link Layer Discovery Protocol (LLDP) type, length, and value (TLV) information elements

79.2 Requirements of the IEEE 802.3 Organizationally Specific TLV set

Change the below paragraph as follows (this subclause was inserted by IEEE Std 802.3bc-2009):

~~If any IEEE 802.3 Organizationally Specific TLV is supported, all IEEE 802.3 Organizationally Specific TLVs shall be supported.~~ All IEEE 802.3 Organizationally Specific TLVs shall conform to the LLDPDU bit and octet ordering conventions of 8.1 of IEEE Std 802.1AB-2009.

79.3 IEEE 802.3 Organizationally Specific TLVs

79.3.2 Power via MDI TLV

Change paragraph as follows (this subclause was inserted by IEEE Std 802.3bc-2009):

Clause 33 defines two option power entities: a Powered Device (PD) and Power Sourcing Equipment (PSE). These entities allow devices to draw/supply power over the sample generic cabling as used for data transmission. ~~DTE power via MDI is intended to provide a 10BASE-T, 100BASE-TX, or 1000BASE-T device with a single interface for both the data it requires and the power to process these data.~~ The Power Via MDI TLV ~~is an optional TLV that~~ allows network management to advertise and discover the MDI power support capabilities of the sending IEEE 802.3 LAN station. This TLV is also required to perform Data Link Layer classification as defined in 33.6. Figure 79–3 shows the format of this TLV.

Replace Figure 79–3 with the following:

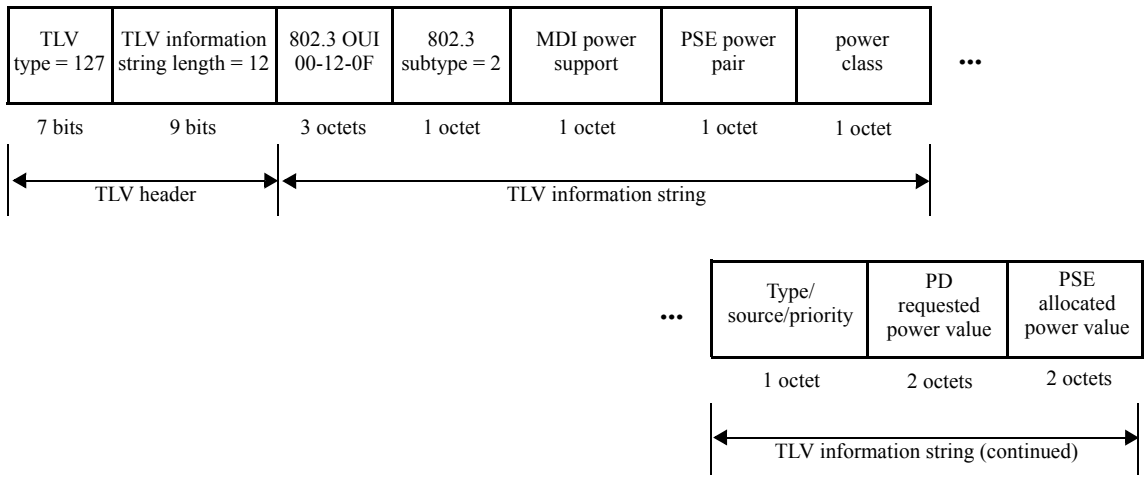


Figure 79–3—Power via MDI TLV format

Insert new paragraph at the end of 79.3.2:

The TLV shown in Figure 79–3 is a revision of the legacy Power via MDI TLV originally defined in IEEE Std 802.1AB-2009 Annex F.3. The legacy TLV had only the first three fields of the TLV shown in the figure. These three fields enable discovery and advertisement of MDI power support capabilities. The newly added fields provide Data Link Layer classification capabilities. The revised TLV can be used by the PSE only when it is supplying power to a PI encompassed within an MDI and by the PD only when it is drawing

power from the PI. Power entities may continue to use the legacy TLV prior to supplying/drawing power to/from the PI. If the power entity implements Data Link Layer classification, it shall use the Power via MDI TLV shown in Figure 79–3 after the PI has been powered.

Renumber existing 79.3.2.4 as 79.3.2.7.

Insert new subclauses 79.3.2.4, 79.3.2.5, and 79.3.2.6 after existing 79.3.2.3:

79.3.2.4 Requested power type/source/priority

The power type/source/priority field shall contain a bit-map of the power type, source and priority defined in Table 79–3a and is reported for the device generating the TLV.

Table 79–3a—Power type/source/priority field

Bit	Function	Value/meaning
7:6	power type	7 6 1 1 = Type 1 PD 1 0 = Type 1 PSE 0 1 = Type 2 PD 0 0 = Type 2 PSE
5:4	power source	Where power type = PD 5 4 1 1 = PSE and local 1 0 = Reserved 0 1 = PSE 0 0 = Unknown Where power type = PSE 5 4 1 1 = Reserved 1 0 = Backup source 0 1 = Primary power source 0 0 = Unknown
3:2	Reserved	Transmit as zero, ignore on receive
1:0	power priority	1 0 1 1 = low 1 0 = high 0 1 = critical 0 0 = unknown (default)

79.3.2.4.1 Power type

This field shall be set according to Table 79–3a.

79.3.2.4.2 Power source

When the power type is PD, this field shall be set to 01 when the PD is being powered only through the PI; to 11 when the PD is being powered from both; and to 00 when this information is not available.

When the power type is PSE, this field shall be set to 01 when the PSE is sourcing its power through the PI from its primary supply; to 10 when the PSE is sourcing its power through the PI from a backup source; and to 00 when this information is not available.

79.3.2.4.3 Power priority

When the power type is PD, this field shall be set to the power priority configured for the device. If a PD is unable to determine its power priority or it has not been configured, then this field shall be set to 00.

When the power type is PSE, this field reflects the PD priority that the PSE advertises to assign to the PD.

79.3.2.5 PD requested power value

The PD requested power value field shall contain the PD's requested power value defined in Table 79–3b.

Table 79–3b—PD requested power value field

Bit	Function	Value/meaning
15:0	PD requested power value	Power = 0.1 × (decimal value of bits) Watts. Valid values for these bits are decimal 1 through 255.

The PD requested power value is encoded according to Equation (79–1):

$$Power = \{0.1 \times X\}_{W} \quad (79–1)$$

where

Power is the effective requested PD power value
X is the decimal value of the power value field, bits 15:0

"PD requested power value" is the maximum input average power (see 33.3.7.2) the PD wants to draw. "PD requested power value" is the power value at the input to the PD's PI.

79.3.2.6 PSE allocated power value

The PSE allocated power value field shall contain the PSE's allocated power value defined in Table 79–3c.

Table 79–3c—PSE allocated power value field

Bit	Function	Value/meaning
15:0	PSE allocated power value	Power = 0.1 × (decimal value of bits) Watts. Valid values for these bits are decimal 1 through 255.

The PSE allocated power value is encoded according to Equation (79–2):

$$Power = \{0.1 \times X\}_{W} \quad (79–2)$$

where

Power is the effective allocated PSE power value
X is the decimal value of the power value field, bits 15:0

"PSE allocated power value" is the maximum input average power (see 33.3.7.2) the PSE expects the PD to draw. "PSE allocated power value" is the power at the input to the PD's PI. The PSE uses this value to compute P_{Class} as defined in 33.2.6.

79.4 IEEE 802.3 Organizationally Specific TLV selection management

79.4.2 IEEE 802.3 Organizationally Specific TLV/LLDP Local and Remote System group managed object class cross references

Replace Table 79–6 and Table 79–7 with the following (79.4 was inserted by IEEE Std 802.3bc-2009):

Table 79–6—IEEE 802.3 Organizationally Specific TLV/LLDP Local System Group managed object class cross references

TLV name	TLV variable	LLDP Local System Group managed object class attribute
MAC/PHY Configuration/Status	Auto-negotiation support	aLldpXdot3LocPortAutoNegSupported
	Auto-negotiation status	aLldpXdot3LocPortAutoNegEnabled
	PMD auto-negotiation advertised capability	aLldpXdot3LocPortAutoNegAdvertisedCap
	Operational MAU type	aLldpXdot3LocPortOperMauType
Power Via MDI	Port class	aLldpXdot3LocPowerPortClass
	PSE MDI power support	aLldpXdot3LocPowerMDISupported
	PSE MDI power state	aLldpXdot3LocPowerMDIEnabled
	PSE pairs control ability	aLldpXdot3LocPowerPairControlable
	PSE power pair	aLldpXdot3LocPowerPairs
	Power class	aLldpXdot3LocPowerClass
	Power type	aLldpXdot3LocPowerType
	Power source	aLldpXdot3LocPowerSource
	Power priority	aLldpXdot3LocPowerPriority
	PD requested power value	aLldpXdot3LocPDRequestedPowerValue
	PSE allocated power value	aLldpXdot3LocPSEAllocatedPowerValue
Link Aggregation (deprecated)	aggregation status	aLldpXdot3LocLinkAggStatus
	aggregated port ID	aLldpXdot3LocLinkAggPortId
Maximum Frame Size	maximum frame size	aLldpXdot3LocMaxFrameSize

Table 79–7—IEEE 802.3 Organizationally Specific TLV/LLDP Remote System Group managed object class cross references

TLV name	TLV variable	LLDP Remote System Group managed object class attribute
MAC/PHY Configuration/Status	Auto-negotiation support	aLldpXdot3RemPortAutoNegSupported
	Auto-negotiation status	aLldpXdot3RemPortAutoNegEnabled
	PMD auto-negotiation advertised capability	aLldpXdot3RemPortAutoNegAdvertisedCap
	Operational MAU type	aLldpXdot3RemPortOperMauType
Power Via MDI	Port class	aLldpXdot3RemPowerPortClass
	PSE MDI power support	aLldpXdot3RemPowerMDISupported
	PSE MDI power state	aLldpXdot3RemPowerMDIEnabled
	PSE pairs control ability	aLldpXdot3RemPowerPairControlable
	PSE power pair	aLldpXdot3RemPowerPairs
	Power class	aLldpXdot3RemPowerClass
	Power type	aLldpXdot3RemPowerType
	Power source	aLldpXdot3RemPowerSource
	Power priority	aLldpXdot3RemPowerPriority
	PD requested power value	aLldpXdot3RemPDRequestedPowerValue
	PSE allocated power value	aLldpXdot3RemPSEAllocatedPowerValue
Link Aggregation (deprecated)	aggregation status	aLldpXdot3RemLinkAggStatus
	aggregated port ID	aLldpXdot3RemLinkAggPortId
Maximum Frame Size	maximum frame size	aLldpXdot3RemMaxFrameSize

79.5 Protocol implementation conformance statement (PICS) proforma for IEEE 802.3 Organizationally Specific Link Layer Discovery Protocol (LLDP) type, length, and values (TLV) information elements

79.5.6 Power via MDI TLV

Replace the table in 79.5.6 with the following (79.5 was inserted by IEEE Std 802.3bc-2009):

Item	Feature	Subclause	Value/Comment	Status	Support
PVT1	MDI power support field	79.3.2.1	Bit map of the MDI power capabilities and status as defined in Table 79–2	PV:M	Yes [ ] N/A [ ]
PVT2	PSE power pair field	79.3.2.2	Integer value as defined by the pethPsePortPowerPairs object in IETF RFC 3621	PV:M	Yes [ ] N/A [ ]
PVT3	power class field	79.3.2.3	Integer value as defined by the pethPsePortPowerClassifications object in IETF RFC 3621	PV:M	Yes [ ] N/A [ ]
PVT4	Power type/source/priority field	79.3.2.4	Contains a bit-map of the power type, source, and priority defined in Table 79–3a	PV:M	Yes [ ] N/A [ ]
PVT5	Power type field	79.3.2.4.1	Set according to Table 79–3a	PV:M	Yes [ ] N/A [ ]
PVT6	Power source field when power type is PD	79.3.2.4.2	Set to ‘01’ when powered only through the PI; set to ‘11’ when powered from both; set to ‘00’ when information is not available	PV:M	Yes [ ] N/A [ ]
PVT7	Power source field when power type is PSE	79.3.2.4.2	When sourcing power through the PI, set to ‘01’ when using primary supply; set to ‘10’ when using backup source; set to ‘00’ when information is not available	PV:M	Yes [ ] N/A [ ]
PVT8	Power priority field when power type is PD	79.3.2.4.3	Set to the power priority configured for the device; set to ‘00’ if power priority is undetermined	PV:M	Yes [ ] N/A [ ]
PVT9	PD requested power value field	79.3.2.5	Contains the PD’s requested power value defined in Table 79–3b	PV:M	Yes [ ] N/A [ ]
PVT10	PSE allocated power value field	79.3.2.6	Contains the PSE’s allocated power value defined in Table 79–3c	PV:M	Yes [ ] N/A [ ]
PVT11	Usage rules	79.3.2.7	LLDPDU contains no more than one Power Via MDI TLV	PV:O	Yes [ ] No [ ] N/A [ ]

Annex A

(informative)

Bibliography

Add the following references alphanumerically and renumber as needed:

[Bxx1] ISO/IEC TR 29125 (draft), Information technology—Telecommunications cabling guidelines for remote powering of data terminal equipment. Draft document number ISO/IEC JTC 1/SC 25 N 874.

[Bxx2] TIA TSB-184 (draft), Guidelines for Supporting Power Delivery over Balanced Twisted-Pair Cabling. Draft document number PN-3-0324A (TIA-TSB 184 D2.0).

Replace all Clause 33 annexes with the following:

Annex 33A

(informative)

PSE-PD stability

33A.1 Recommended PSE design guidelines and test setup

In order to prevent potential oscillations between the PSE and PD, the sum of the PSE port output impedance (Zo_port), the cable impedance (Zc), the PD input port circuitry impedance (Zpd_cir) and the PD EMI output filter impedance (Z_emi) should be lower than the PD power supply input impedance (Zin_ps_pd). This subclause focuses on the PSE part.

Port output impedance consists of two parts:

a) PSE power supply output impedance (Zo_ps), which is a function of the load (P_{Port}), and
b) Series elements (Z_ser) that connect the PSE power supply output to the port.

Therefore, the total Port output impedance during normal powering mode is Zo_port=Zo_ps+Z_ser.

In order to maintain PSE-PD stability, the following guidelines apply:

c) Zo_ps max = 0.3 Ω at frequencies up to 100 kHz at $P_{port} = P_{Type}$ as defined in Table 33–11.
   Zo_ps can be extracted from Z_{port} by measuring V_{Port} / I_{Port} (with an external power dynamic analyzer system) as a function of frequency and subtracting from Z_{port} the value of Zser (f = DC) which is limited by the value of Zser at DC (low frequency).
d) If Zo_ps < Zo_ser and V_{Port} is kept to V_{Port} min and V_{Port} max as defined in Table 33–11 during dynamic load changes from 10 Hz to 100 kHz, then the value of Zo_ps is not limited.

Compliance to the above requirements should be made by measuring the port output impedance from 10 Hz to 100 kHz with a load of P_{Type} as defined in Table 33–11 at short cable length, or by presenting simulation results.

See Figure 33A–1 for the PSE-PD system impedance allocation.

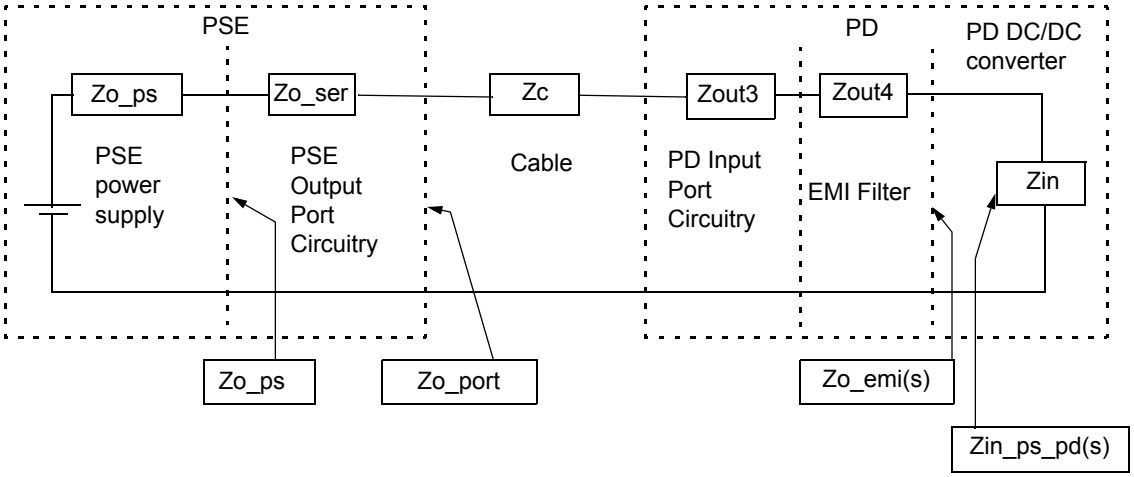


Figure 33A–1—PSE-PD system impedance allocation

See Figure 33A–2 for the test setup and Figure 33A–3 for the test requirements.

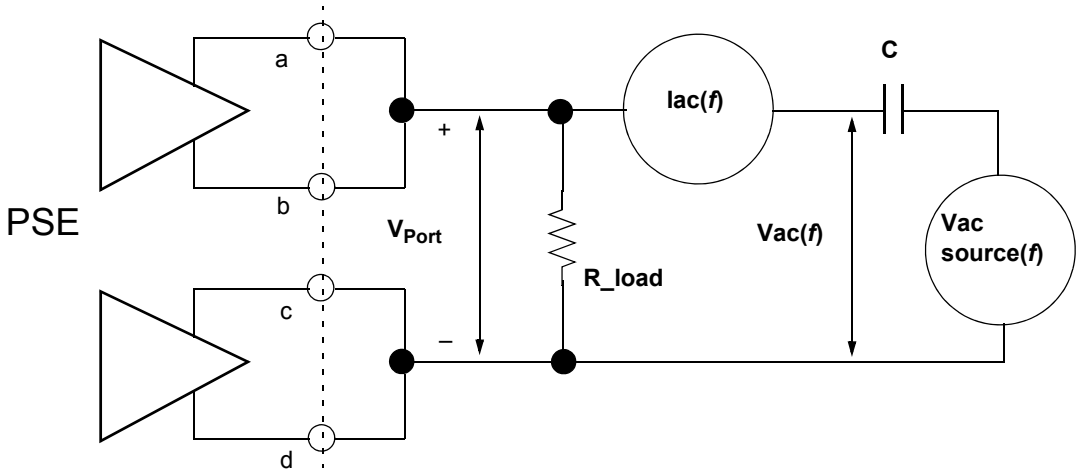


Figure 33A–2—Test setup for measuring Zo_port

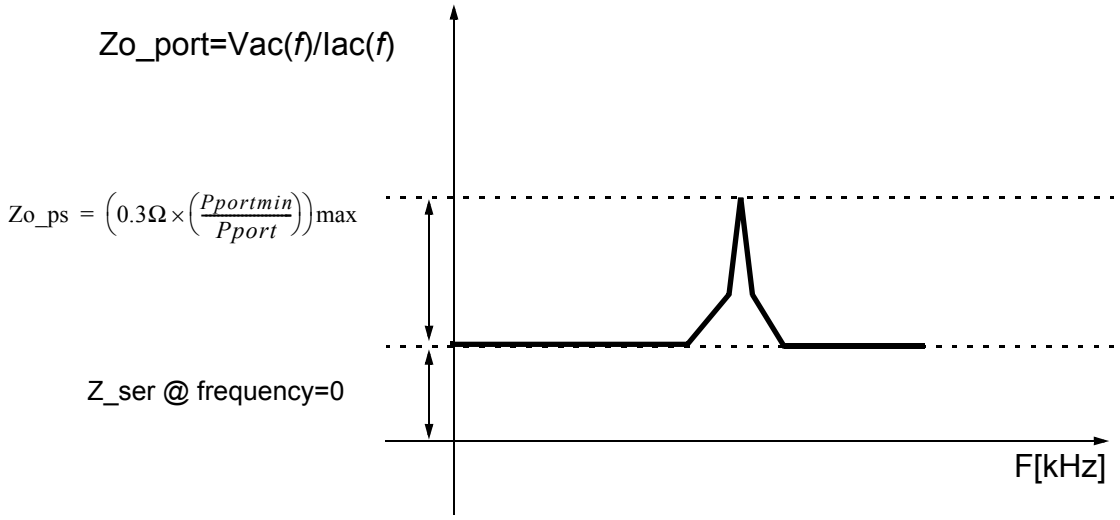


Figure 33A–3—Test requirements for measuring Zo_port

33A.2 Recommended PD design guidelines

PD port input impedance consists of the following two parts:

a) PD port input circuits including the EMI filter (Zin_ser), and
b) PD power supply input impedance (Zin_ps_pd), which is fed by the output of the EMI filter (Zo_emi).

In order to maintain stability with the PSE, the PD power supply input impedance (Zin_ps_pd) should be higher than the output impedance of the total network including the PD EMI output filter impedance fed by the cable (MDI) output impedance, which is fed by the PSE port output impedance.

The worst-case scenario is when the cable (MDI) length is zero (in terms of lower damping factor).

The access to the PD input power supply is not possible through the PD port for evaluating the various impedances and derivation of the above parameters. Because of this, measuring the PD input impedance is a complicated task and the following guidelines should be followed by the PD vendor:

c) The PD power supply input impedance (Zin_ps_pd) at max load of $P_{port} = P_{Port}$ max as defined in Table 33–18 should be higher than 30 Ω at any frequency up to the PD power supply crossover frequency. If the PD power supply is consuming less than $P_{port} = P_{Port}$ max as defined in Table 33–18, then Zin_ps_pd min = $30 \times P_{Port}$ max / P_{port}.
d) The PD power supply EMI filter output impedance should be Zo_emi = 2.7 Ω max. If the PD power supply is consuming less than $P_{port} = P_{Port}$ max, then Zo_emi = $2.7 \times P_{Port}$ max / P_{port}.

See Figure 33A–1 for the PSE-PD system impedance allocation.