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Implementing a 60-W, End-to-End PoE System

Artem Rogachev/Martin Patoka *Power Interface*

ABSTRACT

Specialized applications such as WiMax base stations may require more than 50 W of power, but the current IEEE 802.3at standard defines 25.5-W, two-pair systems. This application report presents a nonstandard Power over Ethernet (PoE) system that can deliver 60 W of processed power to the load. The Powered Device (PD) interface is based on a single TPS2379 and an external hotswap MOSFET, permitting arbitrarily large-load currents. The nonstandard Power Sourcing Equipment (PSE) interface is built around a TPS23851. The document also discusses the use of the commercially available 80-W PSE.

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1 Introduction

A system that complies with the latest PoE standard (IEEE 802.at) can supply up to 25.5 W of power to the PD, which is insufficient for some specialized applications. A nonstandard PoE system can be designed to meet the power requirements and retain the PoE benefits such as protection of non-PoE devices and fault tolerance. Such a solution does not comply with IEEE802.3at and must be designed and operated as a stand-alone system.

Higher power is achieved by feeding current over all four pairs instead of two, and by increasing the current flow through each pair. To ensure proper operation, several design considerations must be taken into account. First, the current limit of both the PD and the PSE must be increased. Second, current-carrying components such as the diode bridges, power transistors, and sense resistors must be scaled up. Finally, the Ethernet data isolation transformers must be capable of carrying the worst-case current without data corruption. It may also be desirable for a high-power PSE or PD to reject its standard compliant counterpart to prevent potential failures.

A 60-W system is designed as an example and can serve as a guide for building systems with higher power requirements. The TPS2379 and the TPS23851 evaluation modules (EVM) are used to build and validate the design. Experimental results are presented and conclusions are drawn.

2 Standard PoE Overview

Selected highlights of the PoE Plus Standard (IEEE 802.3at) are:

- Maximum current of 600 mA per pair in large cable bundles with 10°C temperature derating.
- Current feed over two-pair sets of CAT-5 cable resulting in a 12.5-Ω, power-loop resistance.
- PSE supplies between 50 V and 57 V for a Type-2 PSE (30-W output).
- PD receives at least 42.5 V [50 V – (0.6 A × 12.5 Ω)].
- Only two of the four-pair sets are used for power.
- The PSE follows an intelligent process of:
  - Discovery,
  - Power demand determination (classification),
  - Powering with overload protection, and
  - Power removal when PD is disconnected.
- Only loads with an unpowered, 25-kΩ signature resistance are powered.
- PD operates from either polarity on either of two-pair sets (1,2 and 3,6 or 4,5 and 7,8)
- PSE provides output short and overload protection.
- The load is assumed to have a switching power supply input.

These specifications provide 25.5 W at the PD input. Additional power losses are incurred in the diode bridges, the implicit power switch, and the dc/dc converter. Power levels above 25.5 W require a nonstandard solution. One simple approach doubles the power by feeding current over all four pairs and using two PDs and two PSEs. This solution can be implemented by duplicating the 25.5-W design, but combining the power from the two channels may cause difficulties. Although based on existing standard solutions, it is costly and does not work for applications that require more than 50 W of power. An alternative is to use a single, high-power PSE and a single, high-power PD to feed current over all four pairs. This reduces the component count and can be designed to supply power in excess of 50 W. Such a solution deviates further from the standard implementation and requires more care in component selection.

3 High-Power System Overview

Figure 1 shows a block level diagram of the PoE system implemented in a gigabit Ethernet environment. The 50-V minimum power supply is fed through the 1, 2 and 4, and 5 pair sets in parallel, and the 3, 6 and 7, and 8 pair sets in parallel. The PSE's N-type MOSFET switch is located on the low side of the line. The IEEE 802.3at standard requires the PSE output to be current limited to protect against overloads. The PD does not have this requirement, but most solutions implement current limit to prevent transients and overloads from damaging the power switch. The PD's input diode bridges allow input voltage of either polarity as permitted by the IEEE 802.3 standard. It is possible to define a nonstandard single polarity and protect against reversal with a single diode, but a crossover cable will result in a nonfunctional system (troubleshooting issue). Finally, the output of the PD is fed to the dc/dc converter, which regulates the high-voltage input to the required load voltage(s).

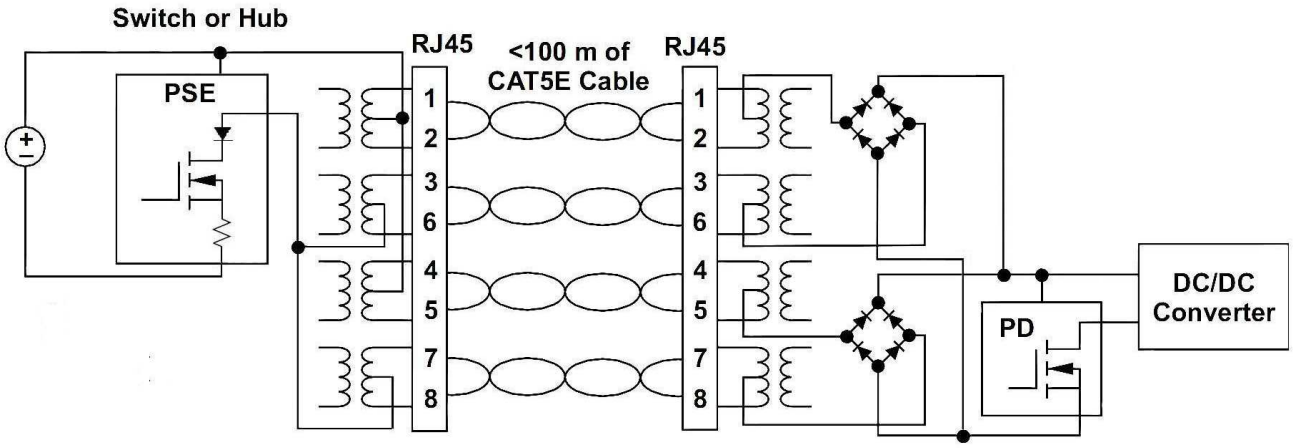

Figure 1. End-to-End PoE System

When the high-power PD and PSE are connected, the following occurs:

1. The PSE periodically performs detection by putting two voltages between 2.8 V and 10 V on the power link.
2. The PD connects its detection resistance of 12.5 kΩ (rather than 25 kΩ) between the input lines, telling the PSE that its special PD is connected rather than a compliant PD.
3. The PSE measures the two currents, and if the incremental resistance is 12.5 kΩ, the PSE proceeds to classification.
4. The PSE performs classification by outputting a voltage between 15.5 V and 20.5 V and measuring the current. The current is decoded into a hardware class by the PSE (0 through 4). This step is optional in a nonstandard implementation.
5. After this handshake is complete, the PSE applies the full 50 V to 57 V between the lines.
6. The PD charges its output capacitor and then turns on the dc/dc converter.

Using a 12.5-kΩ signature instead of a 25-kΩ signature ensures that the special PSE rejects a standard-compliant PD. This is a safety precaution for legacy PDs that do not have an internal current limit and may not be able to handle the large current levels supplied by the high-power PSE.

4 High-Power System Level Design Considerations

4.1 Calculating the Current Requirement of the System

The first step in designing a PoE system is to translate the processed load power requirement (dc/dc

converter output power) to an input current requirement. This is necessary to set the current limits on both the PD and PSE side and to specify the different components. Table 1 shows conservative assumptions that can be made for the power-loss calculations. Schottky diodes are used in the PD input bridge and the PSE. In total, three diodes, two MOSFETs, and a sense resistor (PSE side) are in series with each other. Also, some power losses occur in the dc/dc converter.

Table 1. Assumptions and Specifications

Parameter	Limit
PSE input voltage	53.7 V
Load power requirement	60 W
Converter efficiency	> 90%
Cable resistance	< 6.5 Ω
Schottky diode drop	< 800 mV
Sense resistance	< 300 mΩ
PSE MOSFET R_{dson}	< 200 mΩ
PD MOSFET R_{dson}	< 400 mΩ

Equation 1 computes the required input current based on the processed load power and loop series losses. Here, I_L is the current delivered to the load, V_{IN} is the voltage supplied to the PSE, V_D is the sum of the three diode drops, R_T is the total series resistance (cable, sense resistor, PD, and PSE MOSFET), conv_eff stands for the efficiency of the dc/dc converter, and P_L is the load power. If 60 W of power is specified and the values from Table 1 are used in Equation 1 (computation of loop current), the required load current is 1.73 A.

$$I_L = \frac{(V_{IN} - V_D) - \sqrt{(V_{IN} - V_D)^2 - \left[4 \times R_T \times \left(P_L / conv\_eff\right)\right]}}{2 \times R_T} \quad (1)$$

5 High-Power PD Design Considerations

Once the current requirement is known, the PD can be designed. Figure 2 depicts a recommended design for a high-power PD. The diode bridges combine the current from both sets of pairs to power the single, high-power interface. D_1 and C_1 serve to protect the PD against transients and smooth the PoE protocol waveforms. C_{BULK} is required to present low impedance to the converter input for stability and to buffer the converter input for line and load transients. Q_1 serves as an external auxiliary load switch, increasing the overall current limit and improving efficiency.

The combination of R_{LIM} and Q_2 protects Q_1 by implementing a simple current limit. R_{DEN} sets the detection signature resistance. Finally, the combination of R_{CLASS} and the optional I_{CLASS} boost circuit set the classification current of the PD. Design considerations for component selection are discussed in subsequent text. The TPS2379 evaluation module (EVM) implements this design for a 60-W load.

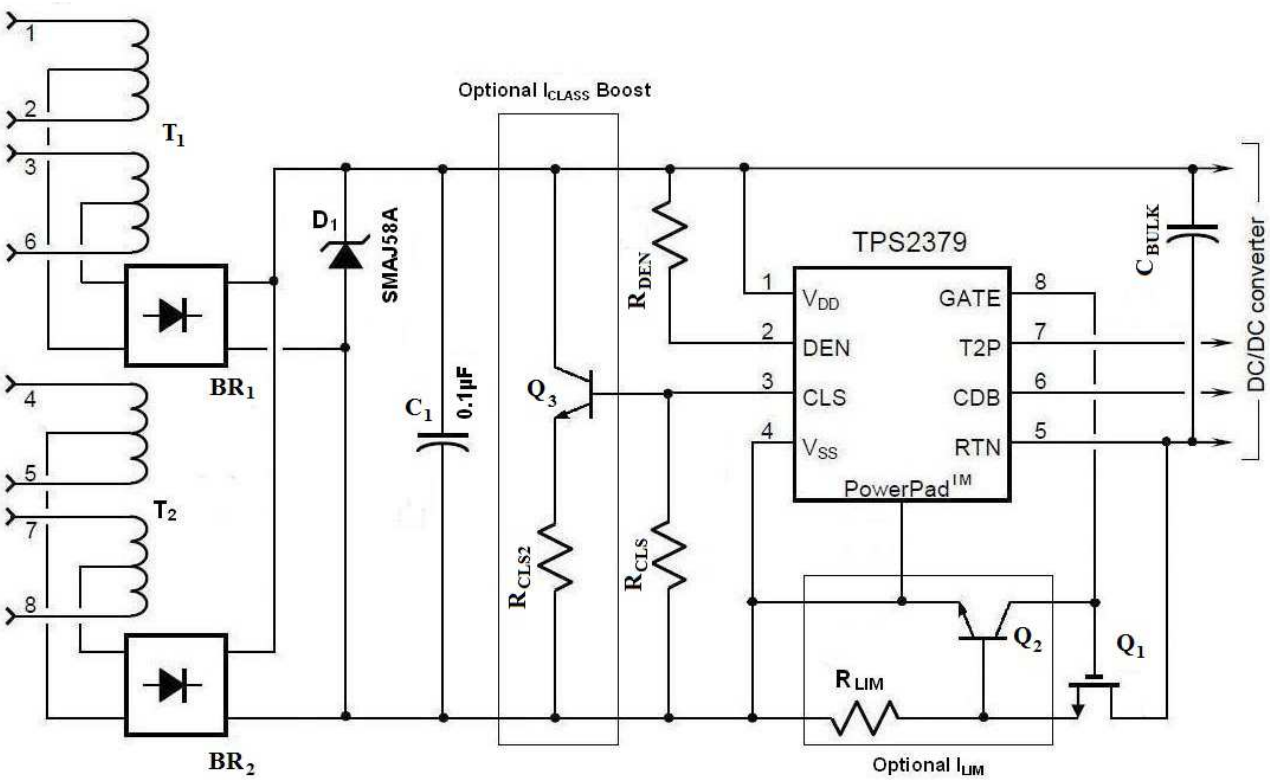

Figure 2. PD Application Circuit

5.1 Selecting R_{DET}

R_{DET} must be set to 24.9 kΩ for an IEEE802.3at-compliant PD. For this example, R_{DET} was set to 12.5 kΩ to achieve operation from only the nonstandard PSE. This simplification avoids having to create user notification of insufficient source power.

5.2 Selecting R_{CLS} to Set the Classification Current

A nonstandard PoE system may not need to use hardware classification, because the user is designing both the PSE and the PD. However, if a system is designed for multiple nonstandard loads (e.g., one is 40 W and one is 60 W) the PSE may use the classification protocol to distinguish them. If classification current is in excess of 40 mA (which is the maximum for TPS2379) are required (more on this in the PSE section), additional boost circuitry can be added as shown in Figure 2. In this case, set R_{CLS} to 63.4 Ω and set R_{CLS2} using Equation 2 (setting R_{CLS2}). In Equation 2, 2.52 V is the regulated CLS voltage, V_{BEON} is the Q3 bias voltage, I_{CLS} is the desired classification current, and 39.7 mA is the current that will flow through R_{CLS}.

$$R_{CLS2} = \frac{2.52\ V - V_{BEON}}{I_{CLS} - 39.7\ mA} \quad (2)$$

5.3 Selecting R_{LIM} and Q_1

The IEEE 802.3at standard requires the PSE to have a current limit and does not require a PD to have one. However, the PSE current limit may not react immediately to a fault, and IEEE 802.3at permits up to 50-A transients. In one test, a commercially available PSE supplied 25 A of current for 200 µs before turning off. Such a transient may cause damaging stress to the current-carrying components, and it is often desirable to provide protection in the PD. The TPS23851 reacts much quicker and does not cause this large overcurrent condition.

When the external current limit is implemented, the load current divides between the TPS2379 and Q1 based on the ratio of R_{2379} (resistance of TPS2379) and R_{EXT} (R_{LIM} + R_{dson} of Q_1) as shown in Equation 3 (current division). Here, I_L is the load current and I_{2379} is the current through the TPS2379.

$$I_{2379} = I_L \times \frac{R_{EXT}}{R_{EXT} + R_{2379}} \tag{3}$$

When I_{2379} exceeds the current limit of the TPS2379 for over 300 µs, the external MOSFET is shut off. For a given load current, the upper bound for R_{EXT} can be computed with Equation 4 (finding an upper bound for R_{EXT}). $I_{2379,LIM}$ is the lowest current limit of the TPS2379, and $R_{2379,MIN}$ is the minimum R_{dson} of the TPS2379. $R_{2379,MIN}$ can be as low as 250 mΩ, but is at least 350 mΩ for temperatures above 0°C. Because the chip heats up during a current-limit condition, setting $R_{2379,MIN}$ to 350 mΩ is a reasonable assumption. For the 60-W design example, R_{EXT} must be kept under 338 mΩ.

$$R_{EXT} \le \frac{I_{2379,LIM} \times R_{2379,MIN}}{I_L - I_{2379,LIM}} = \frac{850\ mA \times 350\ m\Omega}{1730\ mA - 850\ mA} = 338\ m\Omega \tag{4}$$

Once the upper threshold for R_{EXT} is established, the designer can choose R_{LIM} and Q_1. First, pick a MOSFET, then set R_{LIM} to satisfy Equation 4 (finding an upper bound for R_{EXT}). BUK7275 from NXP semiconductor can be used for the design example. At room temperature, its maximum R_{dson} is 75 mΩ, so R_{LIM} must be at least 261 mΩ. Assuming a Q2 $V_{BE\text{-}ON}$ of 0.6 V, the current limit of the external MOSFET is set to 2.3 A.

The TPS2379 turns off the external MOSFET 300 µs after an overload starts. During this condition, the MOSFET has a maximum V_{DS} of 50 V and IDS of 2.3 A, which must be within its safe operating area (SOA). SOA represents the power and duration that leads to a junction temperature rise from 25°C to 150°C or 175°C, depending on the manufacturer. Because the junction may start above 25°C, the SOA curve must be derated. A simple method is to ensure that the MOSFET can handle this transient for 1 ms instead of 300 µs (derate temperature rise by a factor of 3 permitting junction operation to 100°C). In the case of the BUK7275, the SOA curve for 1 ms can handle 8 A at 50 V. Thus, it will work for this 60-W application.

If the PSE current limit is below 2.3 A, and considering worst-case current imbalance between TPS2379 and Q_2, the maximum current through R_{LIM} is (Equation 3) [2.3 A × (750 mΩ / (750 mΩ + 336 mΩ))] = 1.6 A. With this assumption, the power in R_{LIM} is $(1.6\ A)^2 \times 0.261\ \Omega = 0.67$ W. Use a 1-W device with a great deal of heatsinking or a 1.5-W device.

Regardless of the PSE current limit, the worst-case power dissipation of R_{LIM} is limited by Equation 5 (maximum power dissipation of R_{LIM}). P_{RLIM} is the power dissipated by R_{LIM}, and V_{BEON} is the turnon voltage of Q_2.

$$P_{R\_LIM} < \frac{V_{BEON}^2}{R_{LIM}} = \frac{0.6\ V^2}{0.261\ \Omega} = 1.38\ W \tag{5}$$

5.4 Selecting the Data Transformers

This high-power system requires the Ethernet data transformers to carry more current than the 600-mA rating of those built for the IEEE 802.3at standard. In this design, the transformers operate in parallel, sharing the load current. However, some current imbalance is caused by variations in the loop resistance and other small offsets like diode forward voltages. If the diodes and connectors are reasonably well matched, the wire resistance tolerance (based on the cabling standard 3% wire-wire mismatch) between parallel pair sets can be assumed to be 6% in the worst case.

Based on the current rating of the transformers, the maximum allowed load current can be computed with Equation 6. Here, I_{TOTAL} is the maximum load current, I_{MAX} is the maximum current allowed for each transformer, and R_{MM} is the total mismatch in the two current paths. Equation 6 suggests that standard compliant transformers can be used for load currents below 1132 mA, which is less than the 1.73 A required for the 60-W system. For this example, Coilcraft's ETH1-230 transformers (each can handle 1 A of current) can be used.

$$I_{TOTAL} = I_{MAX} \times \frac{2}{1 + R_{MM}} = 600\ mA \times \frac{2}{1 + 0.06} = 1132\ mA \tag{6}$$

6 PSE Design Considerations

Figure 3 shows a diagram of a PSE power section using a TPS23851. Changes from a standard implementation include: reducing R_{SENSE}, adding R_{DET}, enlarging D1, and enlarging Q1.

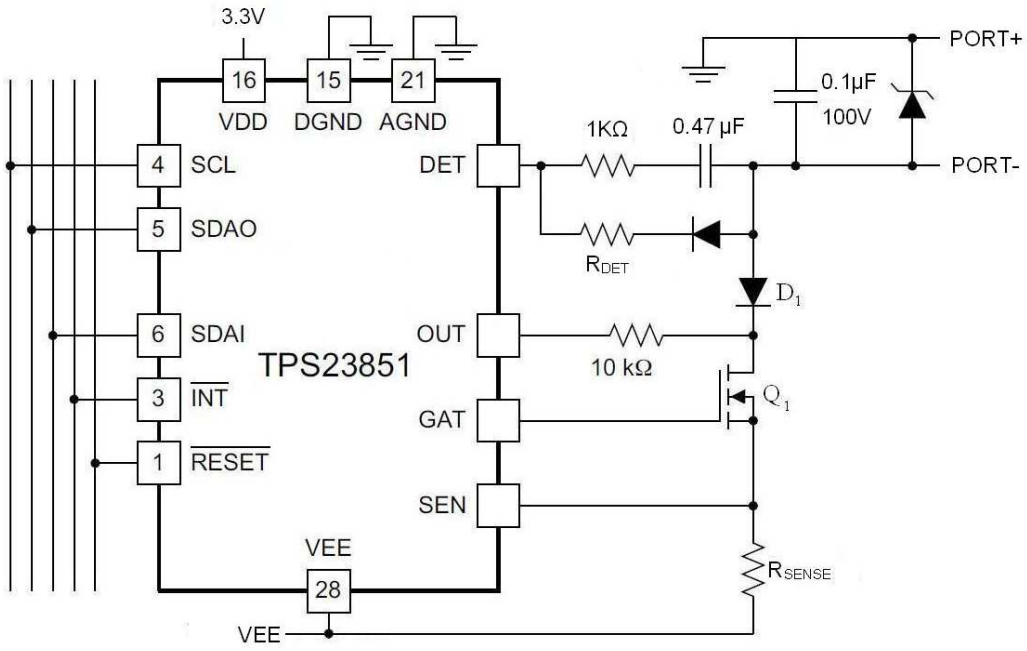

Figure 3. Custom PSE Design Using TPS23851

6.1 Selecting R_{SENSE}

The PSE monitors and controls output current by sensing the voltage across R_{SENSE} (V_{SENSE}). The PSE starts a timed overload algorithm when V_{SENSE} is above a threshold level V_{CUT}. The PSE shuts off once the timer has reached its limit. With the TPS23851 set to the highest current-limit setting, V_{CUT} is at least 385 mV. For I_L = 1.73 A, R_{SENSE} must be less than 385 mV / 1.73 A = 223 mΩ. The maximum continuous power dissipation of R_{SENSE} is determined by Equation 7 . Here, $V_{CUT,MAX}$ is the maximum V_{CUT} over temperature and all process corners. Based on $V_{CUT,MA,X}$ = 430 mV and R_{SENSE} = 200 mΩ, the maximum power dissipation is 0.92 W. Use a 1-W resistor with a great deal of heatsinking or a 1.5-W device.

$$P_{SENSE} < \frac{V_{CUT,MAX}^2}{R_{SENSE}} = \frac{0.43\ V^2}{0.2\ \Omega} = 0.92\ W \quad (7)$$

6.2 Selecting R_{DET}

For this system, it was decided that the PSE must reject standard PDs. This is accomplished by using an R_{DET} value of 12.4 kΩ (see Figure 3). Because the TPS23851 looks for a 24.9-kΩ detection signature, this added resistance causes the PSE to measure a standard PD as an unsatisfactory ~37.4 kΩ. This designed PD with its 12.5-kΩ detection signature satisfies this PSE design.

6.3 Selecting D_1

Based on the R_{SENSE} selection, the maximum continuous current can be calculated. It occurs when V_{SENSE} = V_{CUT_MAX} = 430 mV and I_{CUT_MAX} = 430 mV / 200 mΩ = 2.15 A. A suitable part is a 3-A, 100-V Schottky diode, available from multiple sources.

6.4 Selecting Q_1

The hotswap transistor must have a low R_{DSON} for high efficiency. A good initial choice is a device with an R_{DSON} below 200 mΩ (< 100 mΩ is ideal). Q_1 experiences the most stress in an overcurrent condition when V_{DS} equals 25 V and $I_{DS} = I_{LIM}$. The TPS23851 controls the current to ensure that V_{SENSE} is below V_{LIM}. Based on the maximum V_{LIM} of 452 mV, the worst-case I_{LIM} can be computed as 452 mV / 200 mΩ = 2.26 A. The duration of this power surge is set by the TPS23851 t_{ICUT} parameter, which is 50 ms to 70 ms for the default setting. A suitable device for this applications is the BUK7275, that was used for the PD, which is rated at 4 A and 25 V for 100 ms.

6.5 Modifying the Port Output

The TPS23851 EVM's PoE connector only allows for power transmission over two-pair sets. All four pairs must be used for conduction in this 60-W, high-power PoE example. The ETH1-230LD transformers can be used along with nonintegrated Ethernet connectors.

6.6 Register Changes

To operate the TPS23851 in the high-current-limit mode, the internal registers must be modified via the I2C interface. Specifically, the I_{CUT} bits must be set to 0111b. This must be done for registers 0x2ah or 0x2bh, depending on the port being used. In addition, the current limit must be set to the 2x mode by changing the corresponding port bit to 1. For more detail, see the Electrical Characteristics table of the TPS23851 data sheet (SLUSAB3).

6.7 Current Monitoring Considerations

The TPS23851 measures the classification current and instantaneous current by measuring the voltage across R_{SENSE}. Modifying this value results in incorrectly reported measurements. For the instantaneous current, this can be corrected by multiplying the reported current value by 500 mΩ / R_{SENSE}.

As previously stated, the classification feature is unnecessary for custom systems. If it is used, the classification currents of the PD must be multiplied by 500 mΩ / R_{SENSE}. For the 60-W design example, the PD must draw 99.25 mA to be classified as Type 2.

6.8 Using the Phihong PSE

The user may choose to purchase an off-the-shelf Phihong PSE (POE80U-560G). It looks for a 12.5-kΩ detection signature and ensures that 720 mA of current are provided in each of the pair sets. This PSE shuts down if one of the currents exceeds 720 mA. Thus, the total load current must not exceed 1400 mA (due to cabling mismatch). Although this is not suitable for the 60-W application, it is a great choice for applications that require less than 50 W. The TPS2379 EVM is compatible to this PSE.

7 Experimental Results

7.1 Efficiency and Power Losses

Figure 4 shows the topology for testing the efficiency of the end-to-end PoE system designed and discussed in this document. Input power is measured based on the input current and the input voltage. At every stage, the power loss is calculated based on the voltage drop. The actual experimental setup did not include a dc/dc converter, so, the reported data assumes that the dc/dc converter can convert the power from the PD at 90% efficiency. A 6.5-Ω resistor was placed between the PSE and the diode bridges to account for the maximum length cable loss.

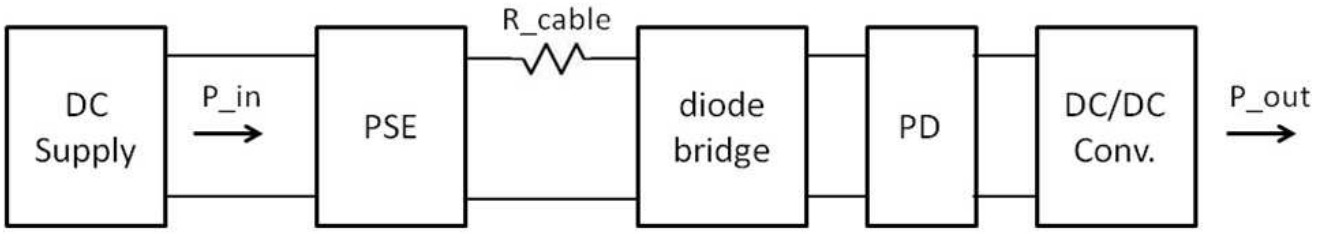

Figure 4. Experimental Setup

Table 2 provides a summary of the system performance under different load conditions. The efficiency decreases as the power is increased due to I x V and I^2 x R losses. A converter's improved efficiency at higher load offsets some of this decrease until the I^2 x R losses dominate. Supplying a load above 60 W becomes quite inefficient due to this loss.

Table 2. System Performance Summary

I_load	P_in (W)	P_out (W)	Efficiency (%)
0.10	5.4	4.7	86.6
0.35	18.8	15.6	83.2
1.00	53.7	39.7	73.9
1.75	94.0	61.2	65.2

Figure 5 shows the power losses in the different stages of the power loop. The cable losses dominate at load currents above 1 A. The second largest source of power loss is the dc/dc converter followed by the diode bridges and the internal switches of the PD and the PSE. The 6.5-Ω cable resistance is for the longest cable or worst case. For a typical 100-meter cable, the resistance is below 4.5 Ω. In addition, systems with a shorter cable are more efficient. Thus, a typical PoE system performs better than the results in Table 2.

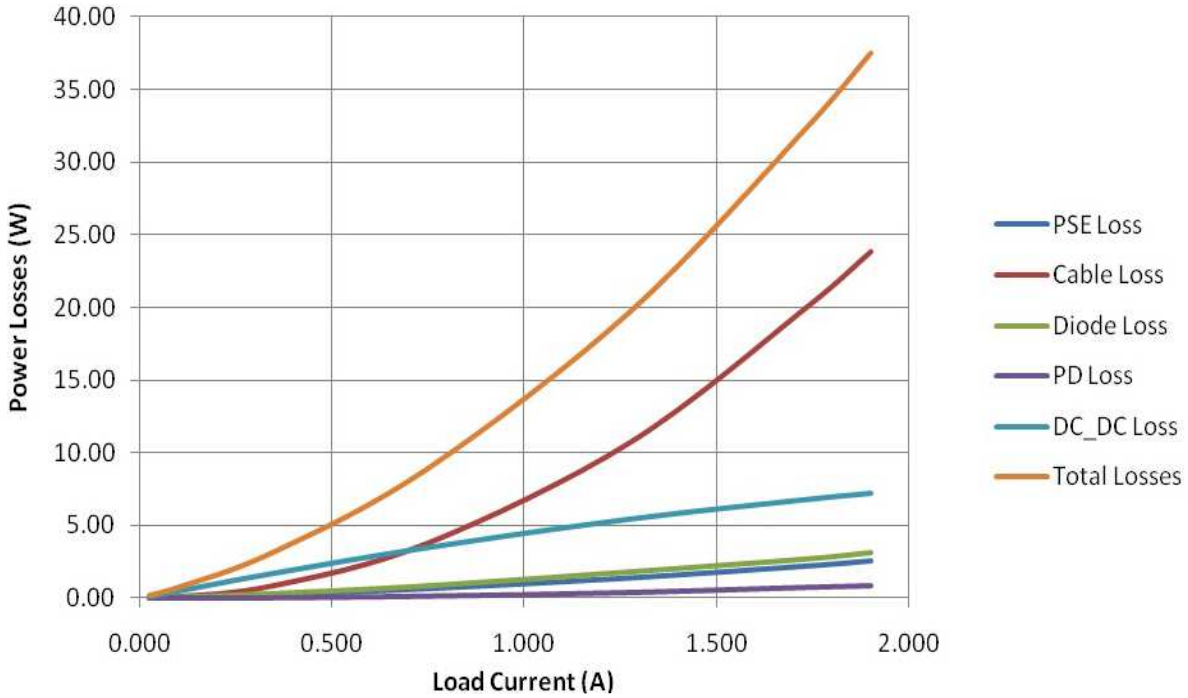

Figure 5. Absolute Power Losses

7.2 PD Overload Response

The 60-W system was tested under several overload conditions to check its robustness.

Figure 6 depicts a condition when the PD load (see Figure 4) was changed to 4 Ω. All of the measurements were taken on the PD side, and the signal names refer to pin voltages on the TPS2379. The PD (current limit not implemented) was connected to a PSE based on the TPS23851, which quickly turns off when a short is encountered. As a result, the PSE current increased to 2 A and quickly came down, preventing stress in the current- carrying components. The gate of the external MOSFET was turned off, when the input voltage fell below 32 V (UVLO). Note that the PSE restarted, and the PD entered inrush limited operation.

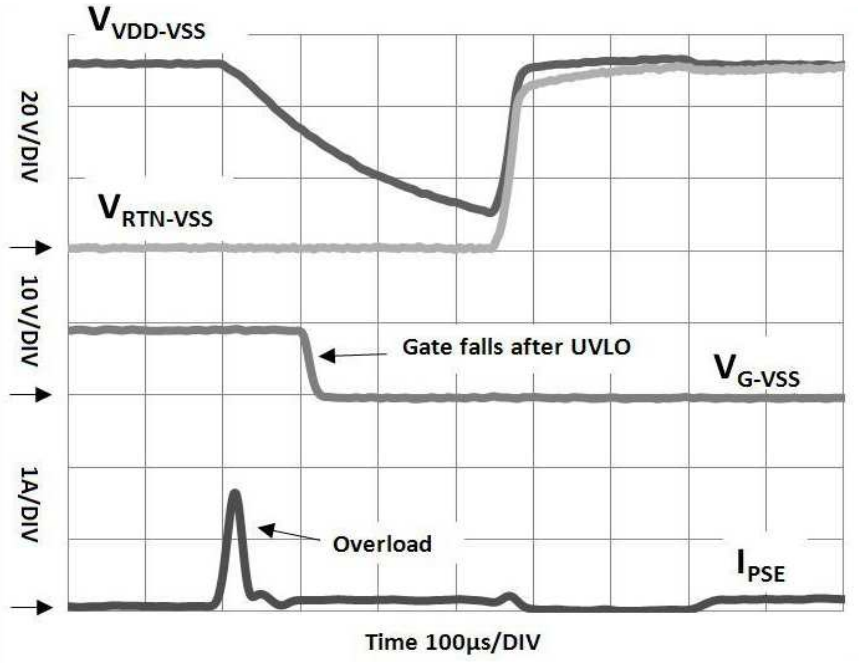

Figure 6. Overload Response With TPS23851 PSE

Figure 7 demonstrates an overload condition (1-Ω short) when the PD operated from the 80-W PSE (POE80U-560G). This test was performed for a PD with current limit and one without under short Ethernet cable conditions. Because this PSE does not have a fast turnoff, a very large current spike (25 A) is observed for the PD that did not implement a current limit. This spike can potentially damage the different current-carrying components; however, all components were still functional after this test, due to the relatively short exposure. The PD with the current limit maintained the current through the external MOSFET below 2.8 A by reducing the gate voltage. Note that a large voltage drop occurred across R_{LIM}, which must be accounted for when Q_1 is selected.

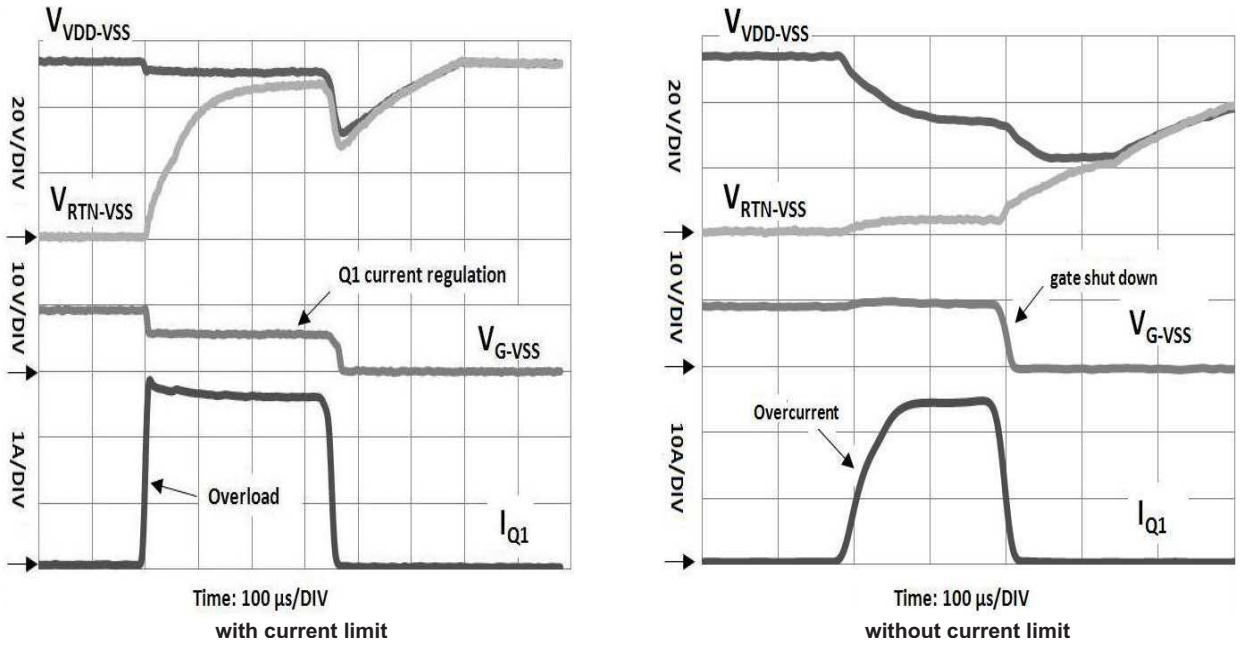

Figure 7. Overload Response With Phihong PSE (POE80U-560G)

7.3 PSE Overcurrent Response

Figure 8 shows a condition that stresses the external MOSFET of the PSE. The signal names in the figure refer to TPS23851 pin voltages. The PSE regulates the current to I_{LIM} when the load current is increased above I_{CUT} by reducing the voltage between PORT+ and PORT–. In this case, V_{DS} of Q_1 is 20 V and I_{DS} is 2 A for duration of 60 ms. Q1 must be able to handle this surge as was discussed in the PSE design section.

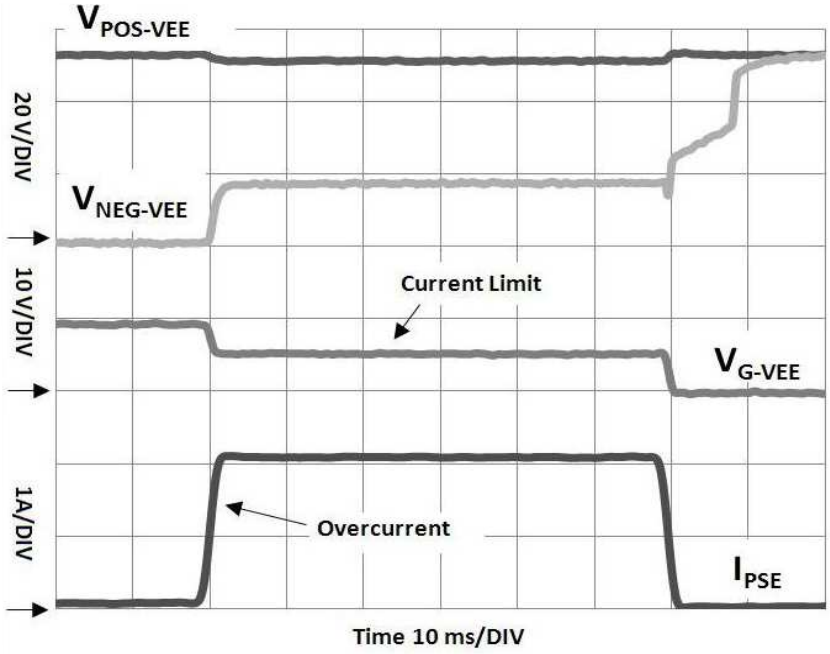

Figure 8. TPS23851 Response to Overcurrent

8 Conclusion

This application report presents a procedure for designing a nonstandard high-power PoE system. A 60-W (output power) example was provided and its performance was analyzed. The power losses become quite significant for applications over 50 W, and using a four-pair architecture is crucial to controlling the I^2 x R losses. For applications below 50 W, the user can have a fast solution by combining the TPS2379EVM and the Phihong PSE. Users can design their own PSE using the TPS23851 for systems that require over 50 W of power.

9 References

1. IEEE Std. 802.3at-2009, IEEE
2. TPS2378/9, IEEE 802.3at PoE High Power PD Controller data sheet
3. *TPS23851, Quad IEEE 802.3at Power-Over-Ethernet PSE Controller* data sheet (SLUSAB3)
4. *Using the TPS23851EVM-001* user's guide (SLUU492)

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