REFERENCES

- 1. P. J. Ashenden, The Designer's Guide to VHDL, 2nd ed., Morgan Kaufmann, 2001.
- 2. J. Axelson, Serial Port Complete, 2nd ed., Lakeview Research, 2007.
- 3. L. Bening and H. D. Foster, Principles of Verifiable RTL Design, 2nd ed., Springer-Verlag, 2001.
- 4. J. Bergeron, Writing Testbenches: Functional Verification of HDL Models, Springer-Verlag, 2003
- 5. K. Chapman, "Creating Embedded Microcontrollers," TechXclusives at www.xilinx.com.
- 6. A. Chapweske, "PS/2 Mouse/Keyboard Protocol," http://www.computer-engineering.org.
- 7. A. Chapweske, "PS/2 Keyboard Interface," http://www.computer-engineering.org.
- 8. A. Chapweske, "PS/2 Mouse Interface," http://www.computer-engineering.org.
- 9. P. P. Chu, RTL Hardware Design Using VHDL: Coding for Efficiency, Portability, and Scalability, Wiley-IEEE Press, 2006.
- 10. M. D. Ciletti, Advanced Digital Design with the Verilog HDL, Prentice Hall, 2003.
- 11. M. D. Ciletti, Starter's Guide to Verilog 2001, Prentice Hall, 2003.
- 12. C. E. Cummings, "Coding and Scripting Techniques for FSM Designs with Synthesis-Optimized, Glitch-Free Outputs," SNUG (Synopsys Users Group Conference), Boston, 2000.
- 13. D. D. Gajski, Principles of Digital Design, Prentice Hall, 1997.
- 14. J. O. Hamblen et al., Rapid Prototyping of Digital Systems: Quartus® II Edition, Springer, 2005.
- 15. IEEE, IEEE Standard for Verilog Hardware Description Language (IEEE Std 1364-2001), Institute of Electrical and Electronics Engineers, 2001.
- 16. IEEE, IEEE Standard VHDL Language Reference Manual (IEEE Std 1076-2001), Institute of Electrical and Electronics Engineers, 2001.

- 17. IEEE, IEEE Standard for VHDL Register Transfer Level (RTL) Synthesis (IEEE Std 1076.6-1999), Institute of Electrical and Electronics Engineers, 2000.
- 18. IEEE, IEEE Standard VHDL Synthesis Packages (IEEE Std 1076.3-1997), Institute of Electrical and Electronics Engineers, 1997.
- 19. IEEE, IEEE Standard Multivalue Logic System for VHDL Model Interoperability (IEEE Std 1164-1993), Institute of Electrical and Electronics Engineers, 1993.
- Integrated Silicon Solution, "Data Sheet of IS61LV25616AL SRAM," Integrated Silicon Solution, Inc.
- 21. R. H. Katz and G. Borriello, Contemporary Logic Design, 2nd ed., Prentice Hall, 2004.
- M. Keating and P. Bricaud, Methodology Manual for System-on-a-Chip Designs, 3rd ed., Springer-Verlag, 2002.
- 23. C. M. Maxfield, The Design Warrior's Guide to FPGAs, Newnes, 2004.
- 24. Mentor Graphics, ModelSim Tutorial, Mentor Graphics Corporation.
- 25. S. Palnitkar, Verilog HDL, 2nd ed., Prentice Hall, 2003.
- D. A. Patterson and J. L. Hennessy, Computer Organization and Design: The Hardware/Software Interface, 3rd ed., Morgan Kaufmann, 2004.
- 27. J. M. Rabaey, Digital Integrated Circuits, 2nd ed., Prentice Hall, 2002.
- 28. J. F. Wakerly, Digital Design: Principles and Practices, Prentice Hall, 2002.
- 29. W. Wolf, FPGA-Based System Design, Prentice Hall, 2004.
- 30. Xilinx, DS099 Spartan-3 FPGA Family: Complete Data Sheet, Xilinx, Inc.
- 31. Xilinx, ISE 8.1i Quick Start Tutorial, Xilinx, Inc.
- 32. Xilinx, ISE In-Depth Tutorial, Xilinx, Inc.
- 33. Xilinx, PicoBlaze 8-bit Embedded Microcontroller User Guide, Xilinx, Inc.
- 34. Xilinx, Spartan-3 Starter Kit Board User Guide, Xilinx, Inc.
- 35. Xilinx, XAPP462 Using Digital Clock Managers (DCMs) in Spartan-3 FPGAs, Xilinx, Inc.
- 36. Xilinx, XAPP463 Using Block RAM in Spartan-3 Generation FPGAs, Xilinx, Inc.
- 37. Xilinx, XAPP464 Using Look-Up Tables as Distributed RAM in Spartan-3 Generation FPGAs, Xilinx, Inc.
- 38. Xilinx, XST User Guide v8.1i, Xilinx, Inc.