Układy Cyfrowe i Systemy Wbudowane 2

Układy FPGA

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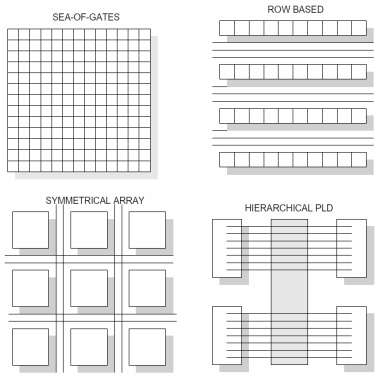
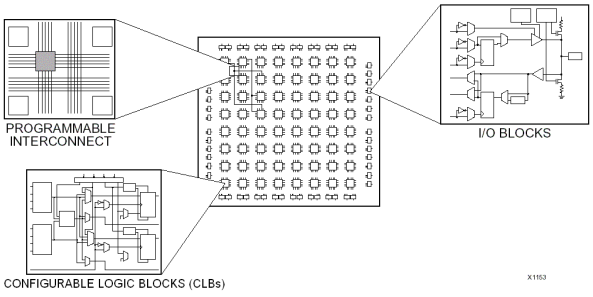
IIAR, pok. 227 C-3

Różne podejścia

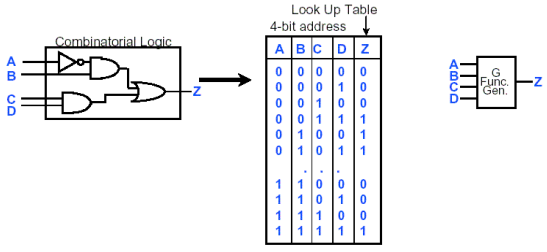
coarse – grain vs. *fine – grain*



Logic Cell Array (LCA) © Xilinx



LUT (Look-Up Table) Function Generator



A	B	C	D	Z
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	1
0	1	0	0	1
0	1	0	1	1
.	.	.	.	.
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	1

Przypomnienie: funkcja konwersji Hex->ASCII

```
(...)
  -- Outputs
  with HalfByte select          -- 0-15 => ASCII '0'-'F'
    DO <= X"30" when "0000",
          X"31" when "0001",
          X"32" when "0010",
          X"33" when "0011",
          X"34" when "0100",
          X"35" when "0101",
          X"36" when "0110",
          X"37" when "0111",
          X"38" when "1000",
          X"39" when "1001",
          X"41" when "1010",
          X"42" when "1011",
          X"43" when "1100",
          X"44" when "1101",
          X"45" when "1110",
          X"46" when others;
(...)
```

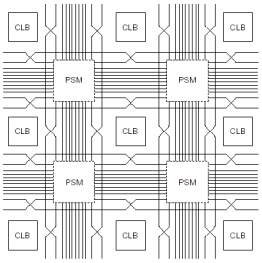

Rodzina układów XC4000

Table 1: XC4000E and XC4000X Series Field Programmable Gate Arrays

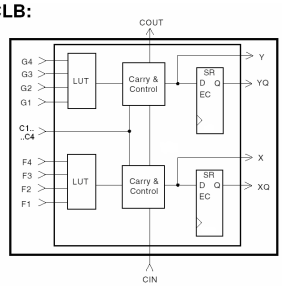
Device	Logic Cells	Max Logic Gates (No RAM)	Max. RAM Bits (No Logic)	Typical Gate Range (Logic and RAM)*	CLB Matrix	Total CLBs	Number of Flip-Flops	Max. User I/O
XC4002XL	152	1,600	2,048	1,000 - 3,000	8 x 8	64	256	64
XC4003E	238	3,000	3,200	2,000 - 5,000	10 x 10	100	360	80
XC4005E/XL	466	5,000	6,272	3,000 - 9,000	14 x 14	196	616	112
XC4006E	608	6,000	8,192	4,000 - 12,000	16 x 16	256	768	128
XC4008E	770	8,000	10,368	6,000 - 15,000	18 x 18	324	936	144
XC4010E/XL	950	10,000	12,800	7,000 - 20,000	20 x 20	400	1,120	160
XC4013E/XL	1368	13,000	18,432	10,000 - 30,000	24 x 24	576	1,536	192
XC4020E/XL	1862	20,000	25,088	13,000 - 40,000	28 x 28	784	2,016	224
XC4025E	2432	25,000	32,768	15,000 - 45,000	32 x 32	1,024	2,560	256
XC4028EX/XL	2432	28,000	32,768	18,000 - 50,000	32 x 32	1,024	2,560	256
XC4036EX/XL	3078	36,000	41,472	22,000 - 65,000	36 x 36	1,296	3,168	288
XC4044XL	3800	44,000	51,200	27,000 - 80,000	40 x 40	1,600	3,840	320
XC4052XL	4598	52,000	61,952	33,000 - 100,000	44 x 44	1,936	4,576	352
XC4062XL	5472	62,000	73,728	40,000 - 130,000	48 x 48	2,304	5,376	384
XC4085XL	7448	85,000	100,352	55,000 - 180,000	56 x 56	3,136	7,168	448

* Max values of Typical Gate Range include 20-30% of CLBs used as RAM.

XC4000



CLB:

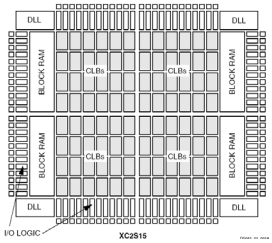


Spartan-II (XC2S)

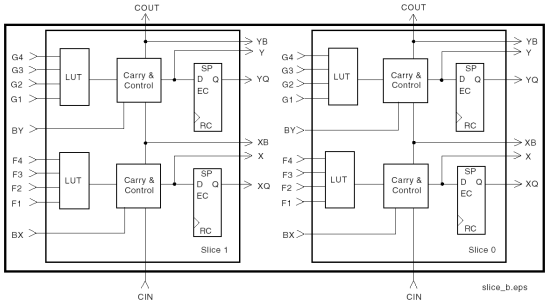
Table 1: **Spartan-II FPGA Family Members**

Device	Logic Cells	System Gates (Logic and RAM)	CLB Array (R x C)	Total CLBs	Maximum Available User I/O(1)	Total Distributed RAM Bits	Total Block RAM Bits
XC2S15	432	15,000	8 x 12	96	86	6,144	16K
XC2S30	972	30,000	12 x 18	216	132	13,824	24K
XC2S50	1,728	50,000	16 x 24	384	176	24,576	32K
XC2S100	2,700	100,000	20 x 30	600	196	38,400	40K
XC2S150	3,888	150,000	24 x 36	864	260	55,296	48K
XC2S200	5,292	200,000	28 x 42	1,176	284	75,264	56K

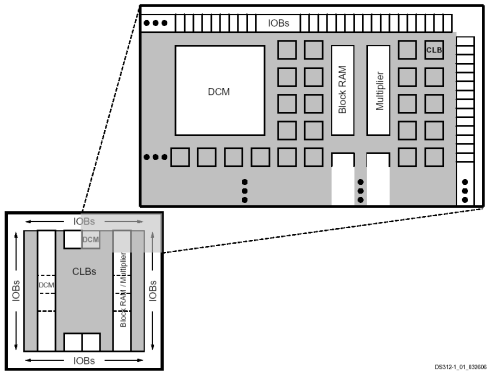
Notes:
1. All user I/O counts do not include the four global clock/user input pins. See details in Table 3, page 3.



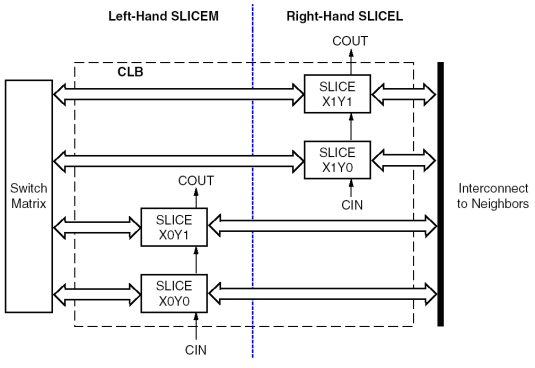
Virtex / Spartan-II



Spartan3 (XC3S)



Virtex-II / Spartan-3



Spartan3 (XC3S)

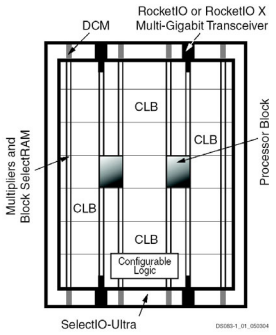
Table 1-6: **Summary of Spartan-3E FPGA Attributes**

Device	System Gates	Equivalent Logic Cells	CLB Array (One CLB = Four Slices)				Distributed RAM Bits	Block RAM Bits	Dedicated Multipliers	DCMs	Maximum User I/O	Maximum Differential I/O Pairs
			Rows	Columns	Total CLBs	Total Slices						
XC3S100E	100K	2,160	22	16	240	960	15K	72K	4	2	108	40
XC3S250E	250K	5,508	34	26	612	2,448	38K	216K	12	4	172	68
XC3S500E	500K	10,476	46	34	1,164	4,656	73K	360K	20	4	232	92
XC3S1200E	1200K	19,512	60	46	2,168	8,672	136K	504K	28	8	304	124
XC3S1600E	1600K	33,192	76	58	3,688	14,752	231K	648K	36	8	376	156

Table 1-5: **Summary of Spartan-3A FPGA Attributes**

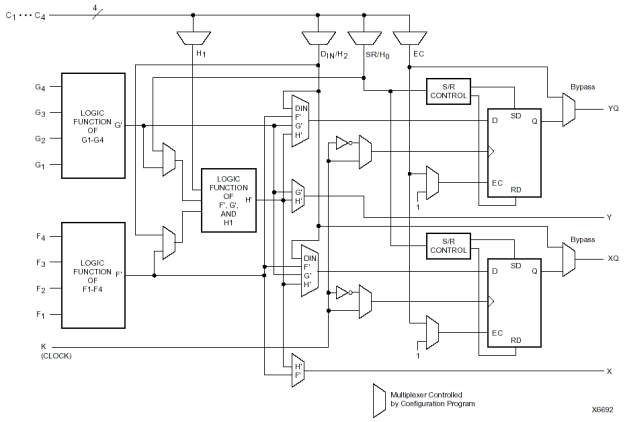
Device	System Gates	Equivalent Logic Cells	CLB Array (One CLB = Four Slices)				Distributed RAM Bits	Block RAM Bits	Dedicated Multipliers	DCMs	Maximum User I/O	Maximum Differential I/O Pairs
			Rows	Columns	Total CLBs	Total Slices						
XC3S50A	50K	1,584	16	12	176	704	11K	54K	3	2	144	64
XC3S200A	200K	4,032	32	16	448	1,792	28K	288K	16	4	248	112
XC3S400A	400K	8,064	40	24	896	3,584	56K	360K	20	4	311	142
XC3S700A	700K	13,248	48	32	1472	5,888	92K	360K	20	8	372	165
XC3S1400A	1400K	25,344	72	40	2816	11,264	176K	576K	32	8	502	227

Virtex-II Pro (and up)

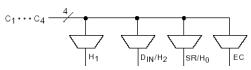


- **Virtex-4 FX**: PowerPC 405 processor cores (x1 / x2)
- **Virtex-5 FXT**: PowerPC 440 processor cores (x1 / x2)

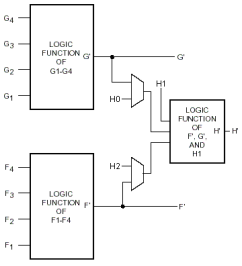
XC4000: Blok CLB



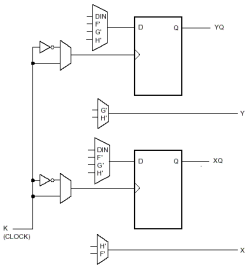
Sygnały sterujące



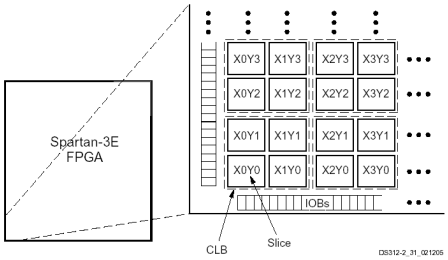
Generacja funkcji



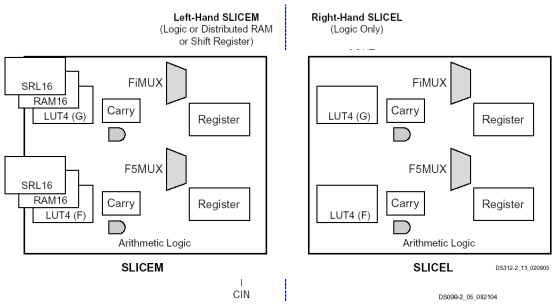
Przerzutniki / WY



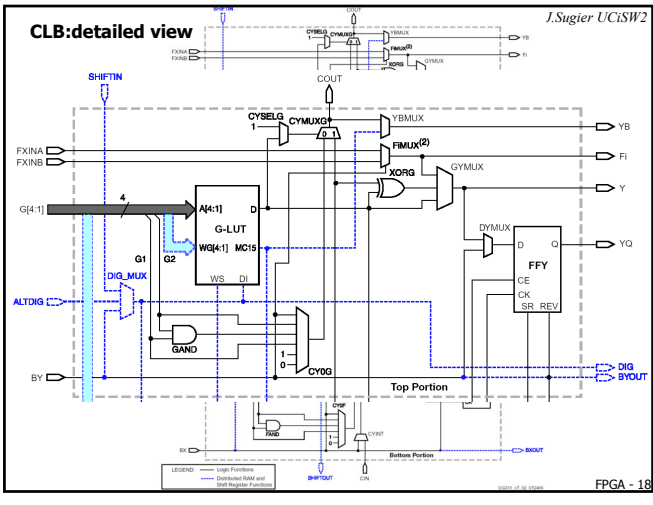
Spartan-3E: Blok CLB



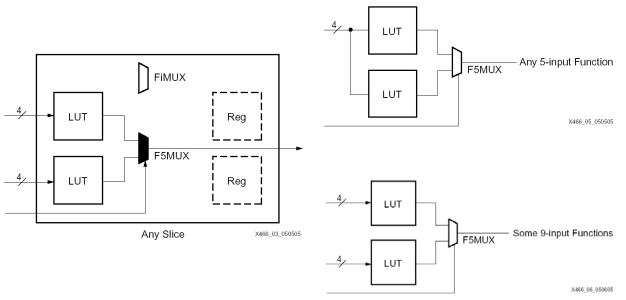
SLICEM vs. SLICEL



CLB:detailed view



Dedykowane multipleksery: F5MUX



Dedykowane multipleksery: FiMUX

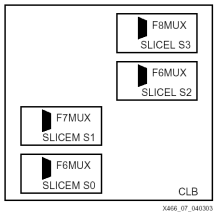
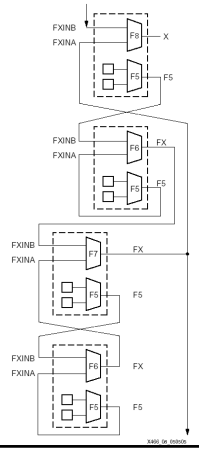


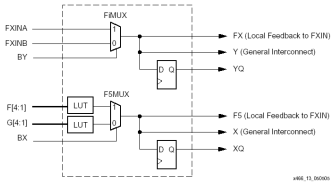
Table 8-1: **Mux Capabilities**

Mux	Usage	Input Source	Total Number of Inputs per Function		
			For Any Function	For Mux	For Limited Functions
F5MUX	F5MUX	LUTs	5	6 (4:1 mux)	9
FiMUX	F6MUX	F5MUX	6	11 (8:1 mux)	19
	F7MUX	F6MUX	7	20 (16:1 mux)	39
	F8MUX	F7MUX	8	37 (32:1 mux)	79

Dedykowane połączenia



Sygnały wyboru



Np.: funkcja do 19 zmiennych w dwóch plastrach (1/2 CLB)

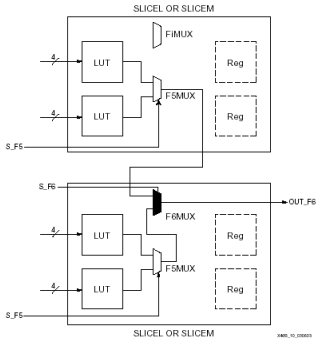
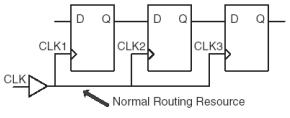
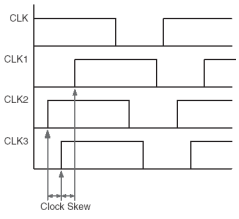


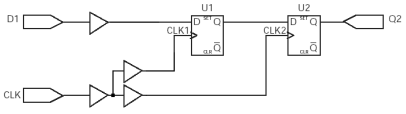
Figure 8-11: **19-input Function Using F6MUX in Two Slices**

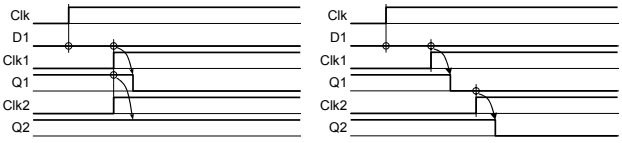
Skos zegara



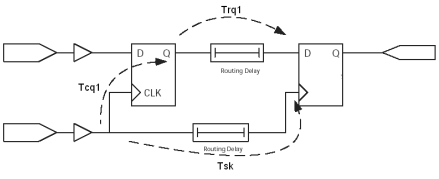


Para rejestrów sekwencyjnie sąsiednich





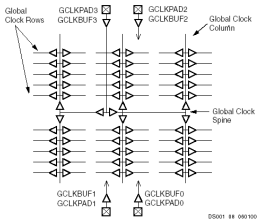
Opóźnienie zegara wzgl. danych

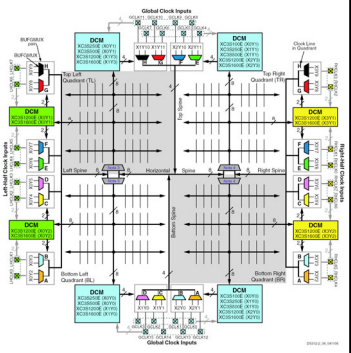


Clock tree

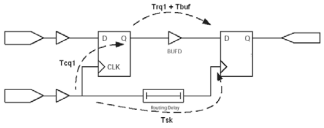
XC3SE

XC2S

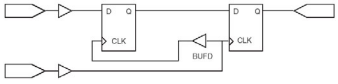




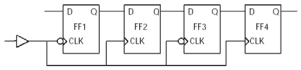
Opóźnianie danych



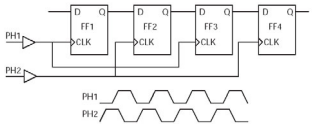
Odwracanie kierunku propagacji Clk



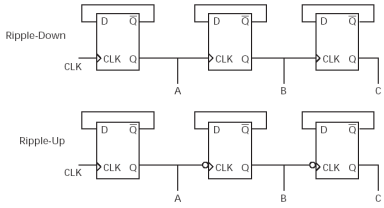
Taktowanie naprzemienne



Taktowanie dwufazowe

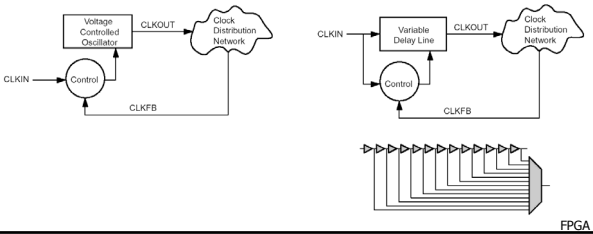


Niekiedy: liczniki asynchroniczne

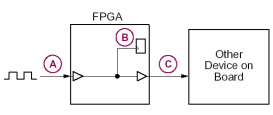


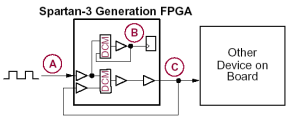
Generacja sygnałów zegarowych

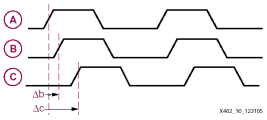
Phase Locked Loop (PLL) vs. Delay Locked Loop (DLL)

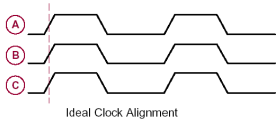


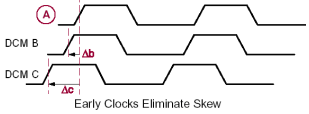
Efekt pracy



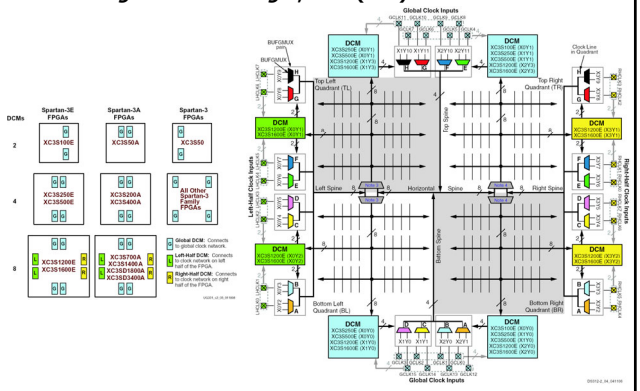








XC3S: *Digital Clock Manager*, DCM (DLL)



Organizacja wewnętrzna

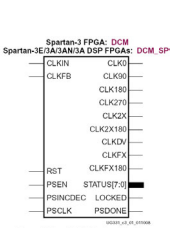
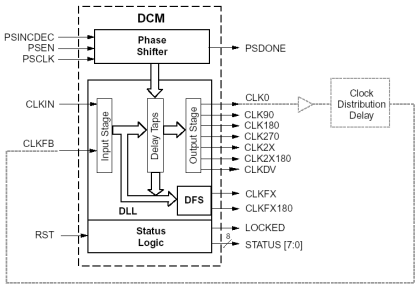


Figure 3-4: **DCM Design Primitive**



Synchronizacja + synteza częstotliwości

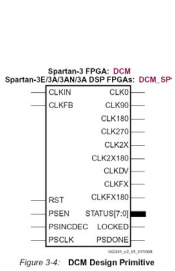
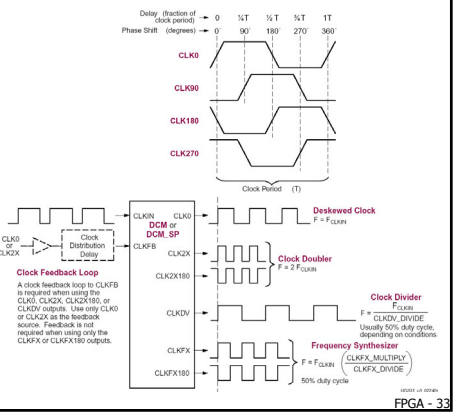


Figure 3-4: **DCM Design Primitive**



Konfiguracje typowe

on-board clock:

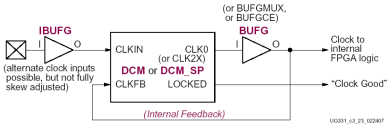


Figure 3-19: **Eliminating Skew on Internal Clock Signals**

off-borad clock:

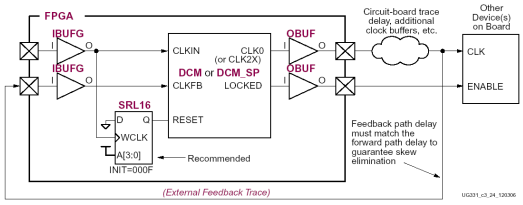
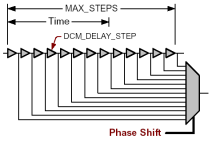


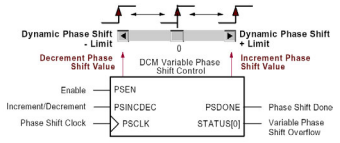
Figure 3-20: **Eliminating Skew on External Clock Signals**

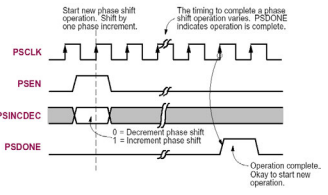
Phase shifter



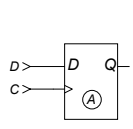
Time > Phase Shift • DCM_DELAY_STEP_MIN
< Phase Shift • DCM_DELAY_STEP_MAX

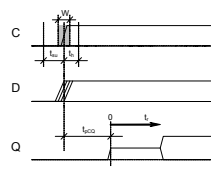
$$\text{Phase} = \frac{\text{Time}}{T_{CLKIN}} \bullet 360°$$

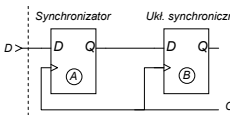


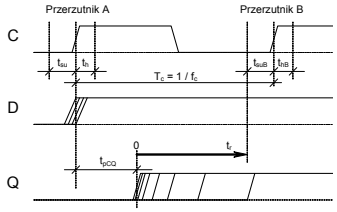


METASTABILNOŚĆ PRZERZUTNIKÓW





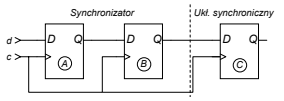




MTBF

	τ [ps]	W [ps]	t_{pCQ} [ns]	t_{su} [ns]	f_c [MHz]	f_d [MHz]	T_r [ns]	MTBF [s]	MTBF [h]	MTBF [d]	MTBF [y]
1)	250	100	3.5	0.5	50	10	16	6.2E+22	1.7E+19	7.2E+17	**2.0E+15**
2)	250	100	3.5	0.5	80	20	8.5	1.8E+09	5.1E+05	2.1E+04	**5.8E+01**
3)	250	100	3.5	0.5	100	30	6	4.4E+04	**1.2E+01**	5.1E-01	1.4E-03
4)	250	100	3.5	0.5	120	40	4.333	**3.5E+01**	9.8E-03	4.1E-04	1.1E-06
5)	250	100	3.5	0.5	150	50	2.667	**2.9E-02**	7.9E-06	3.3E-07	9.1E-10

Synchronizator podwójny



	τ [ps]	W [ps]	t_{pCQ} [ns]	t_{su} [ns]	f_c [MHz]	f_d [MHz]	t_r [ns]	$MTBF_B$ [s]	$MTBF_C$ [s]	$MTBF_C$ [y]
1)	250	100	3.5	0.5	50	10	16	6.2E+22	7.8E+52	**2.5E+45**
2)	250	100	3.5	0.5	80	20	8.5	1.8E+09	1.3E+26	**4.2E+18**
3)	250	100	3.5	0.5	100	30	6	4.4E+04	1.2E+17	**3.7E+09**
4)	250	100	3.5	0.5	120	40	4.333	3.5E+01	9.9E+10	**3.1E+03**
5)	250	100	3.5	0.5	150	50	2.667	2.9E-02	**81802.4722**	0.00259216