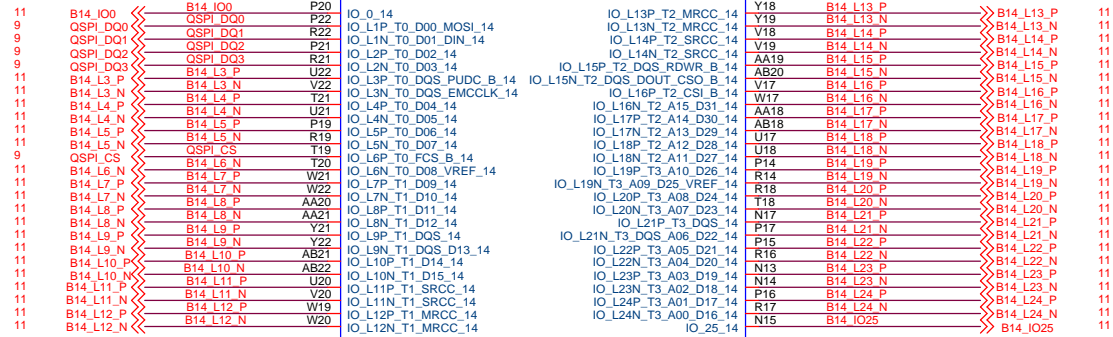
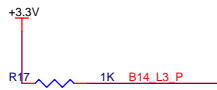
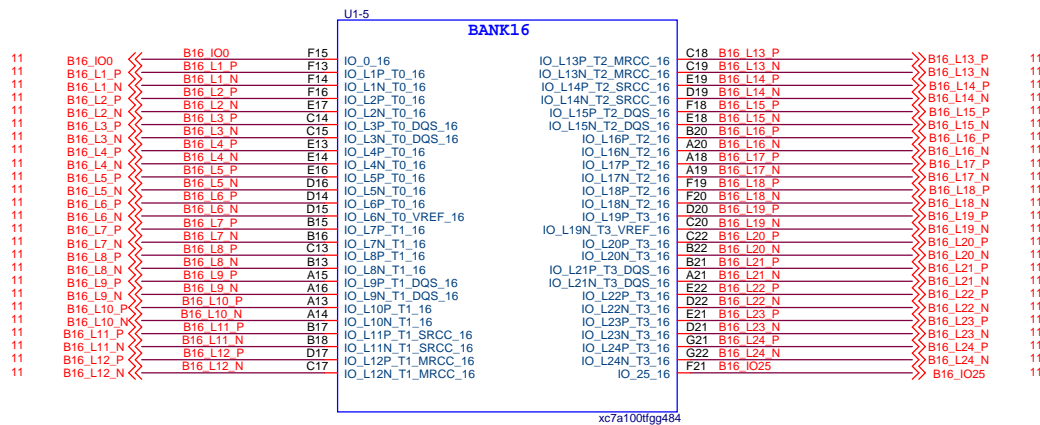
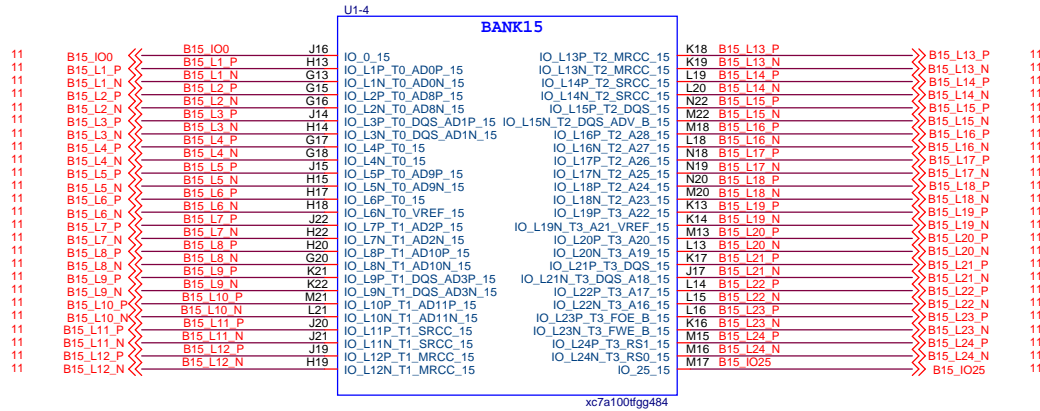
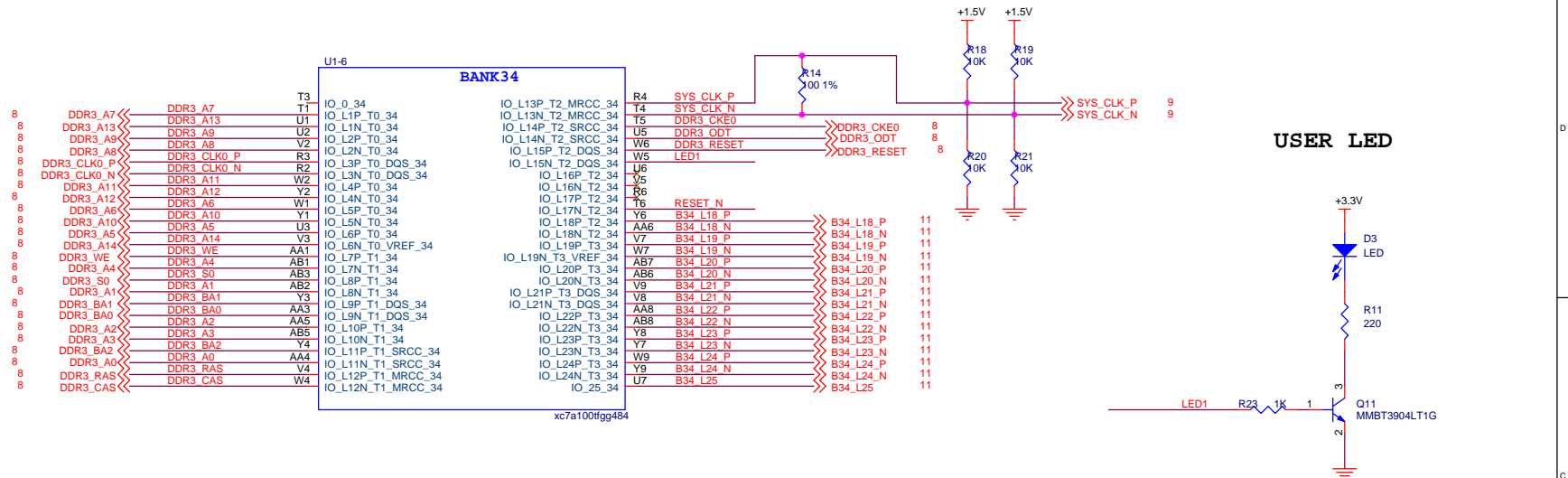


PUDC_B=1: Deactive internal Pull up Resister

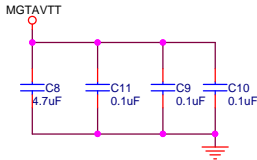


xc7a100tgg484

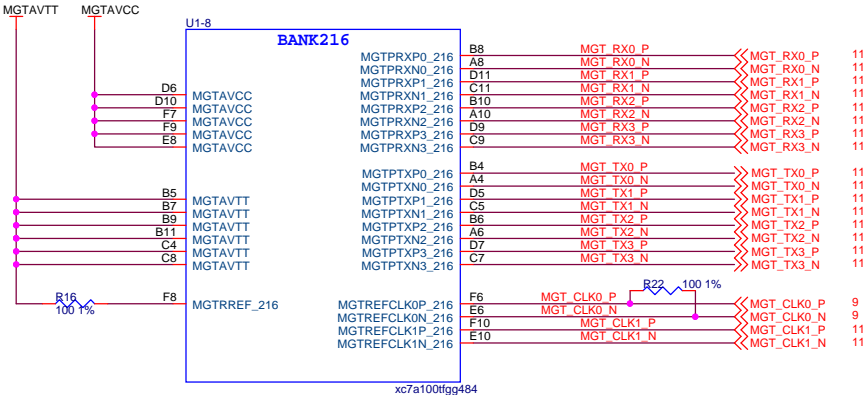
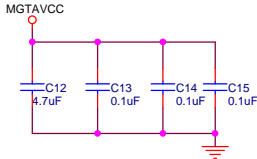


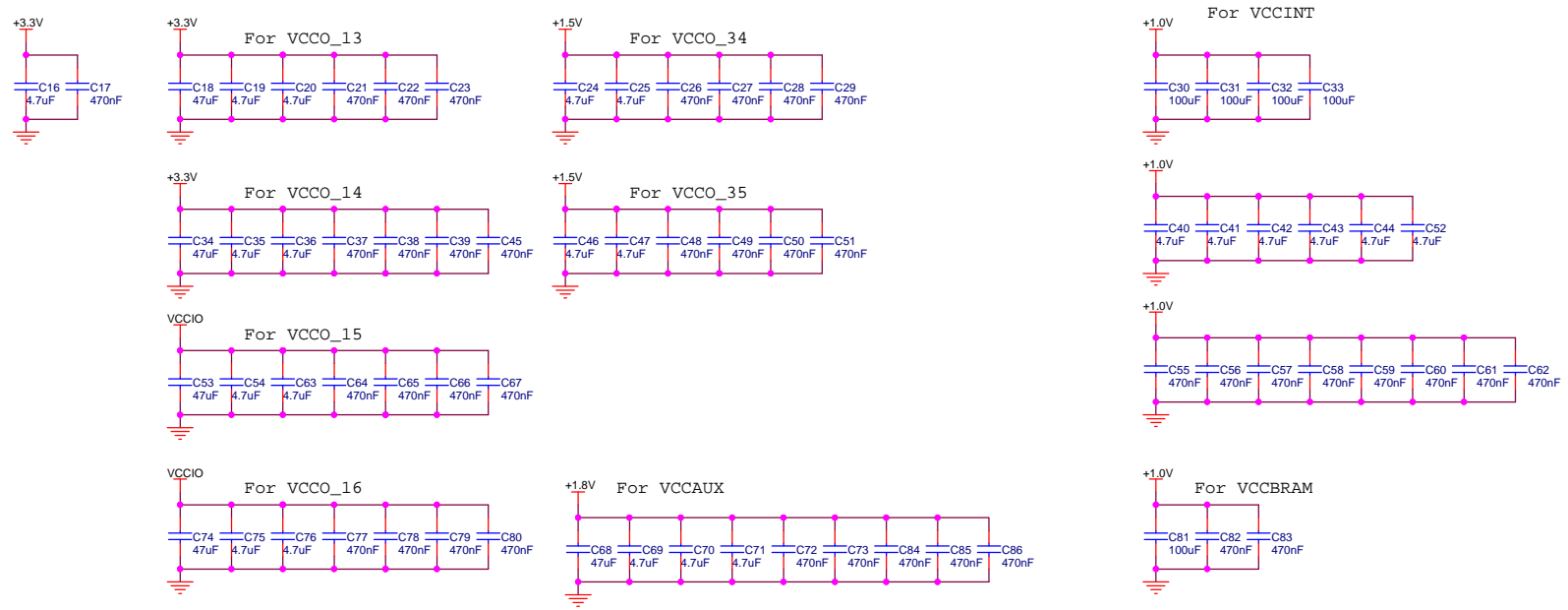
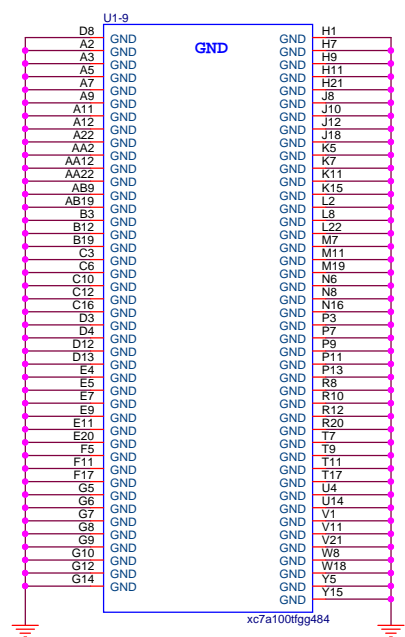
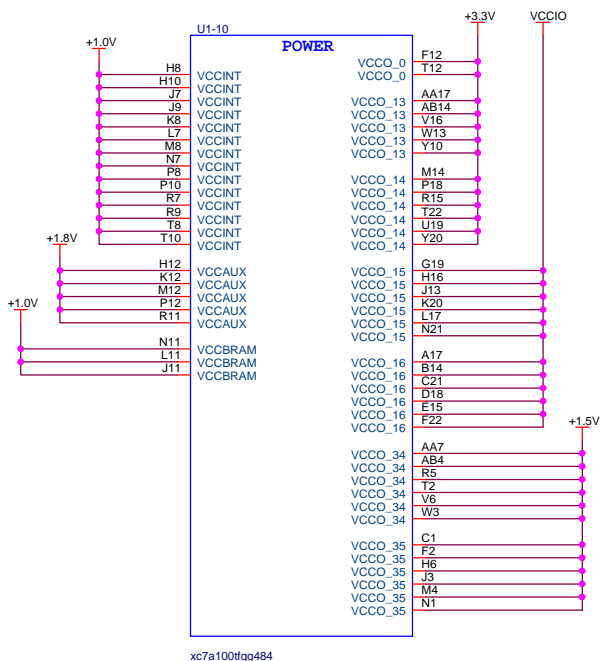


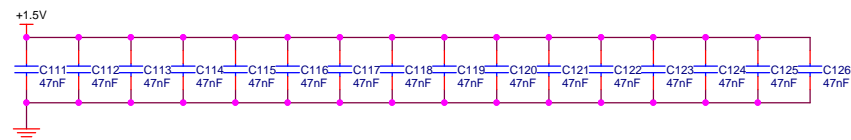
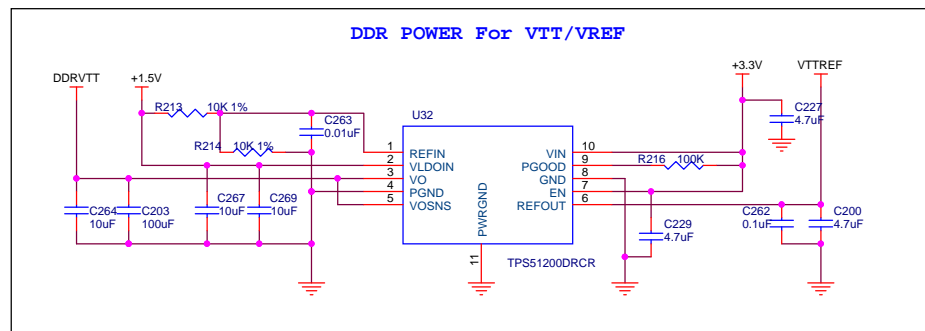
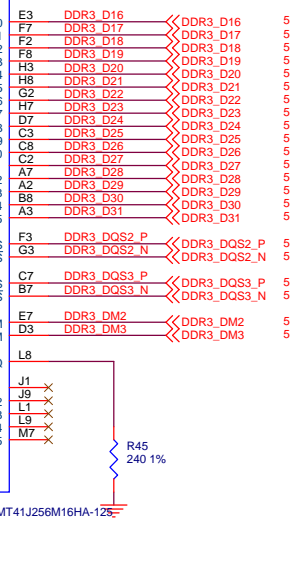
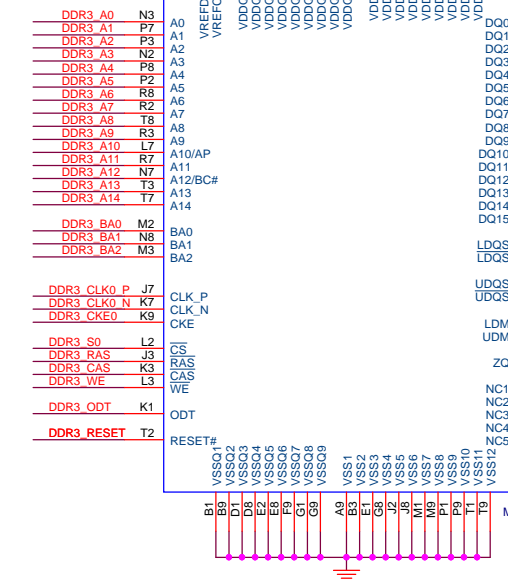
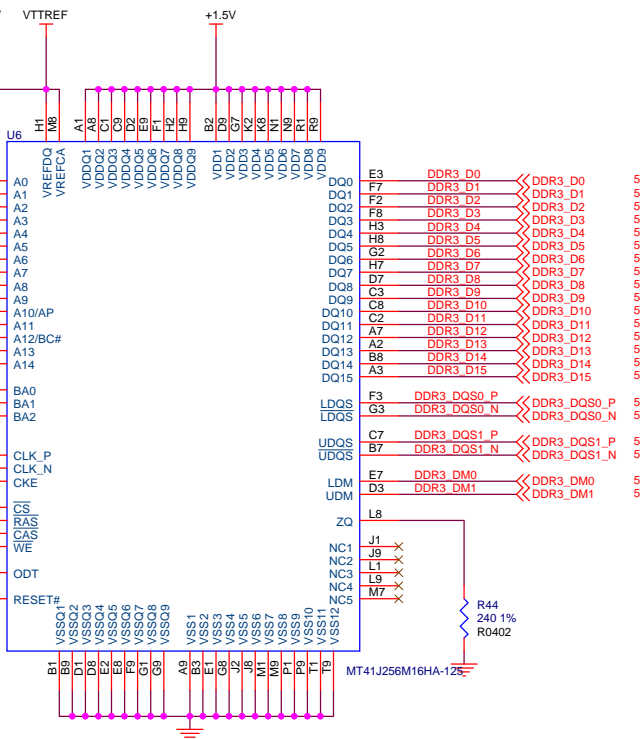
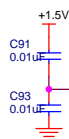
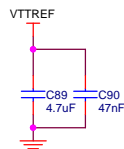
MGTAVTT 4.7uF(1) 0.1uF(2)



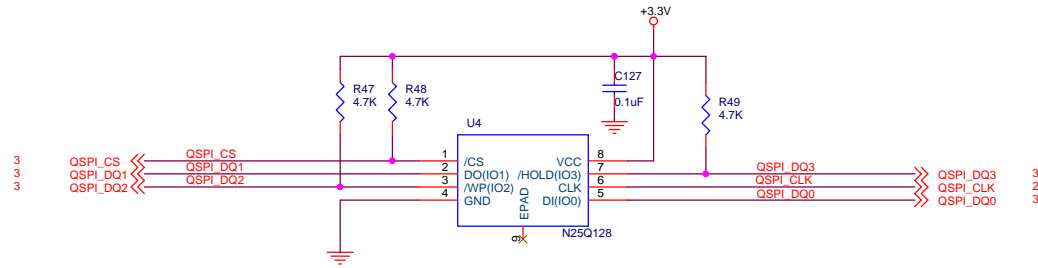
MGTAVCC 4.7uF(1) 0.1uF(2)





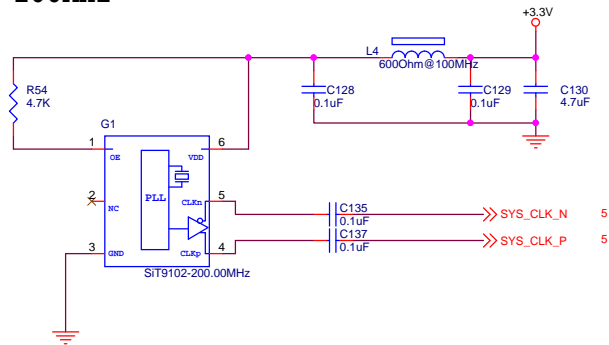


FPGA CONFIG SPI



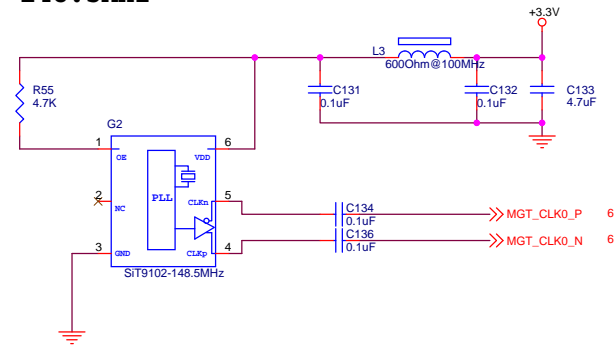
SYSTEM CLOCK

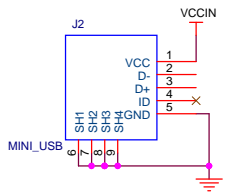
200MHz



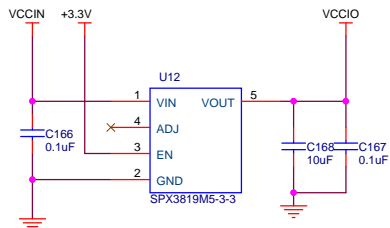
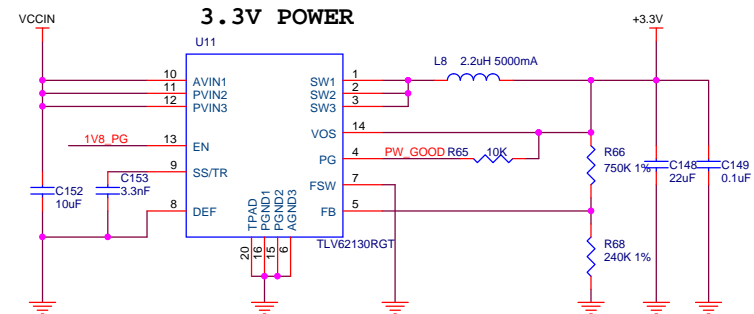
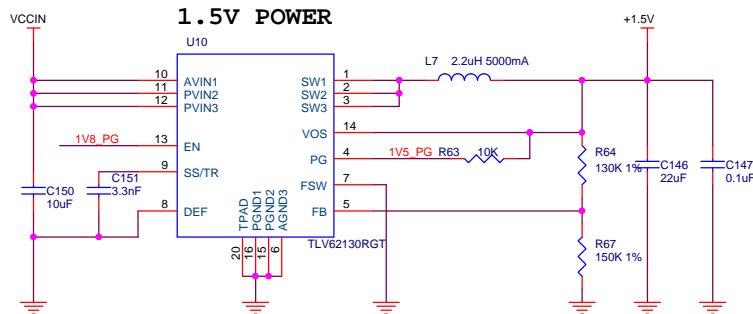
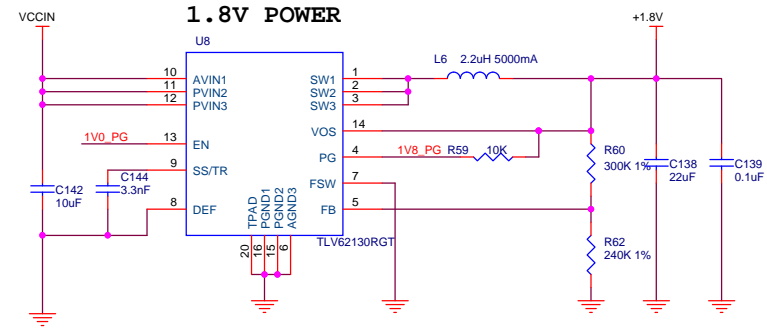
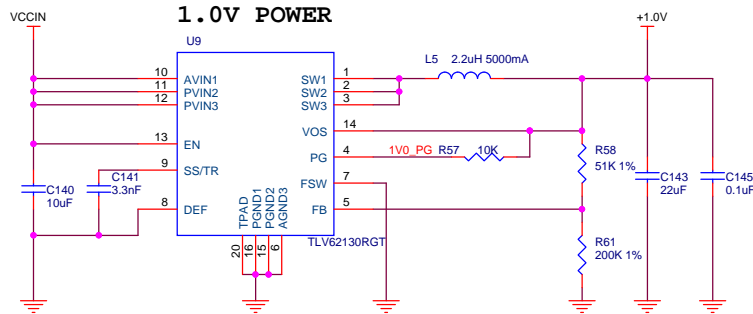
GTP CLOCK

148.5MHz

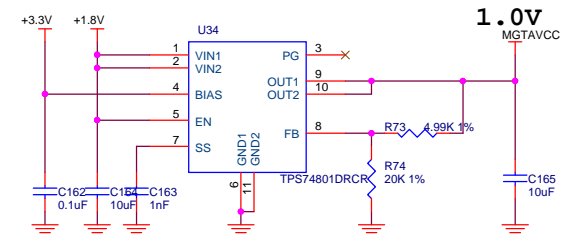
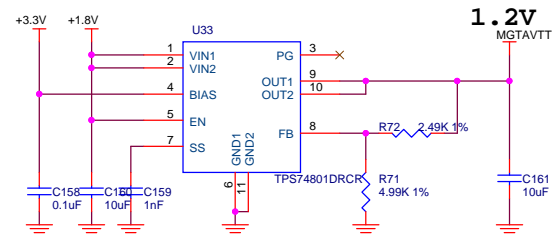




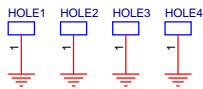
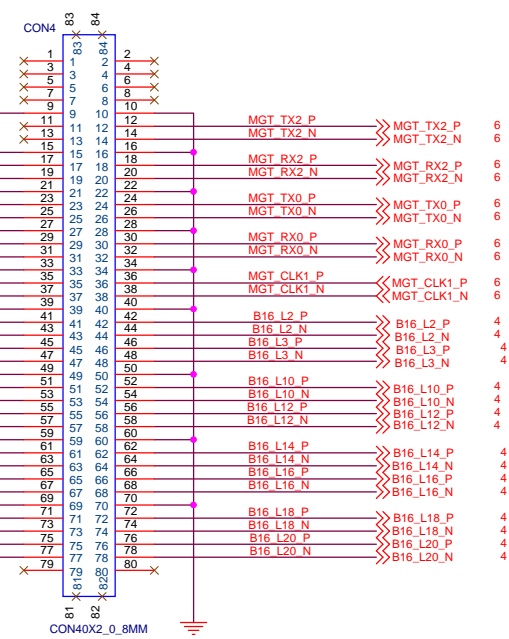
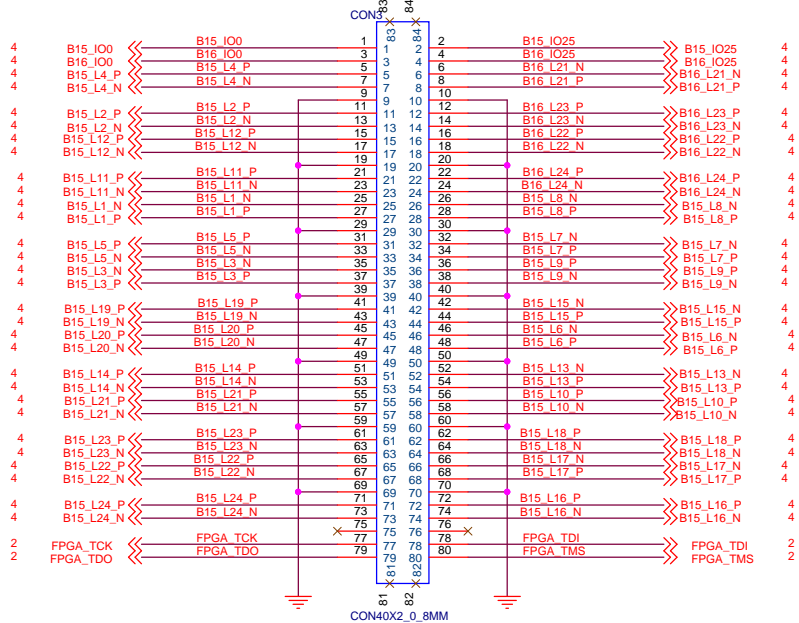
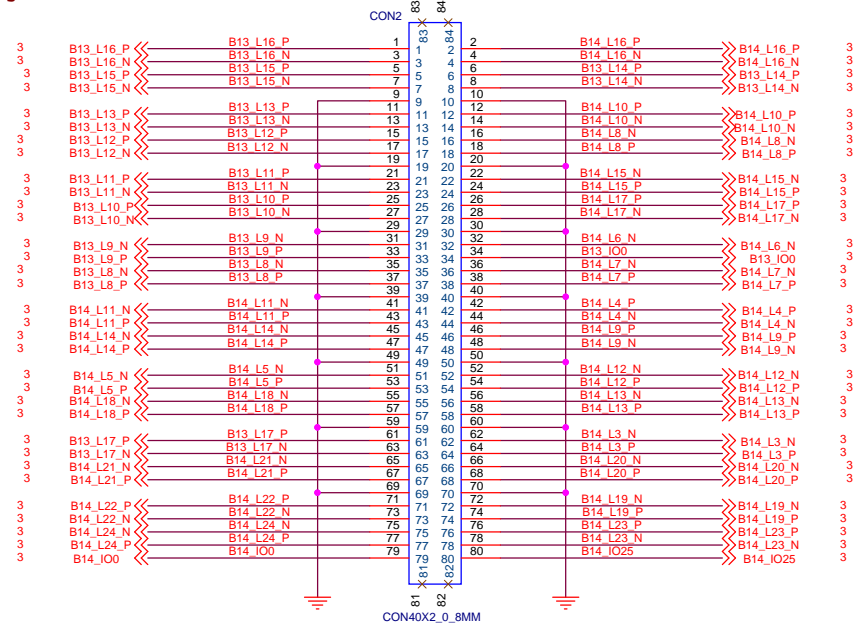
POWER ON: VCCINT(1.0V)->VCCBRAM(1.0V)->VCCAUX-(1.8V)>VCCO(1.5V and 3.3V)



POWER ON: VCCINT(1.0V)->VMGTAVCC(1.0V)->VMGTAVTT(1.2V)



Pinout diagram for the CON40X2_0_8MM connector. The diagram shows a 2x8 pin configuration with VCCIN on pins 1, 2, 81, and 82. It details connections for various signals including B13 L4_P, B13 L4_N, B13 L1_P, B13 L1_N, B13 L2_P, B13 L2_N, B13 L6_P, B13 L6_N, B34 L20_P, B34 L20_N, B34 L21_N, B34 L21_P, B34 L22_P, B34 L22_N, B34 L25, B34 L24_P, and B34 L24_N. Some pins are marked with 'X' indicating no connection.



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