## ISA Design:

- 7-bit instructions with 1 parity bit
- 4 general-purpose registers R0 (00), R1 (01), R2 (10), and R3 (11)
- 1 special register R5 (for saving current PC)
- 16-bit data (Registers and memory)
- RED = RA, BLUE = RB, GREEN = imm

PC	Functionality	Instruction	Coding	Example	
PC ++	RA = RA + RB	add RA, RB	000 <mark>0 A</mark> BB	add R1, R3	000 <mark>01</mark> 11
PC ++	RA: [0,1] RA = RA + imm RA:[2,3] imm:[0,3]	addi RA, imm	0001 A ii	addi R2, 2	0001011
PC ++	RA = RA - RB RA: [0,1]	sub RA, RB	0010 A BB	sub R1, R2	0010110
PC ++	RA = mem[RB] RA: [2,3]	load RA, (RB)	0011 A BB	load R3, (R0)	0011100
PC ++	RA = RA or RB RA: [0,1]	or RA, RB	0100 A BB	or R0, R1	0100001
PC ++	R0 = 1 if RA < RB R0 = 0 if RA > RB RA: [2,3]	slt RA, RB	0101 A BB	slt R3, R2	0101110
PC ++	mem[RB] = RA $RA: [0,1]$	store RA, (RB)	0110 A BB	store R1, R3	0110111
PC ++	RA shift left imm bits RA: [2,3] imm: [0,3]	sll RA, imm	0111 A ii	sll R2, 1	0111001
If RA==0, PC = PC + imm Else, PC++	RA: [0,1] imm: [0,3]	beq RA, imm	1000 A ii	beq R0, 0	1000000
If RA=/=0, PC = PC + imm Else, PC++	RA: [2,3] imm: [0,3]	bne RA, imm	1001 A ii	bne R2, 1	1001001
PC ++	RA = RA and imm RA: [0,1] imm: [0,3]	andi RA, imm	1010 A ii	andi R1, 1	1010101
PC ++	RA shift right imm bits RA: [2,3] imm: [0,3]	srl RA, imm	1011 A ii	srl R2, 1	1011001
PC ++	RA = RA xor RB RA: [0,1]	xor RA, RB	1100 A BB	xor R0, R1	1100001

PC = PC +	imm: [0,7]	j imm	1101 iii	j 6	1101110
imm					
PC = R5	RA = 5	jr R5	1110 <mark>101</mark>	jr R5	1110101
(Replaces PC					
with R5)					
Save PC+1 to	imm: [0,7]	jal imm	1111 iii	jal 7	1111111
R5 and jump					
PC = PC +					
imm					