**Part A) ISA intro**

1. **Introduction: This should include the name of the architecture, overall philosophy, specific goals strived for and achieved.**

Name of architecture: ISA 2.0

This architecture is for an effective and practical ISA Design the goal is to achieve two programs; which were done in Project 1.

1. **Instruction list. Give all the instructions, their formats, opcodes, and an example.**

|  |  |  |  |
| --- | --- | --- | --- |
| Instruction | Format | Example | Opcode |
| init | init Rx, imm | Rx = imm | 1110 xx i |
| add | add Rx,Ry | Rx=Rx+Ry | 001 xx yy |
| load | load Rx, (Ry) | Rx=Mem[Ry] | 011 xx yy |
| store | store Rx, (Ry) | Mem[Ry]=Rx | 010 xx yy |
| jump | jump imm | imm [] | 110 iiii |
| slt | slt Rx, Ry | Rx=1 if Rx<Ry  Else Rx=0 | 101 xx yy |
| sub | sub Rx, Ry | Rx = Rx – Ry | 000 xx yy |
| bezR2 | bezR2 imm | If R2==0, PC+=imm else PC=PC+1 | 100 iiii |
| initR2 | initR2 | Initialize R2 to 5 | 1111000 |
| initR3 | initR3 | Initialize R3 to 5 | 1111001 |
| beqN | beqN | If R1=R0, branch to Next | 1111110 |
| beqInc | beqInc | If R0=R1, branch to Increment | 1111101 |
| stop | stop | Exit the program | 1111111 |

1. **Register design. How many registers are supported? Is there anything special about the registers?**

This architecture supports four registers (R0 to R3)

R2 is used for testing in bezR2 and it is initialized when initR2 is used; R3 is initialized when initR3 is used.

1. **Control flow (branches). What types of branches are supported? How are the target addresses calculated? What is the maximum branch distance supported? Give examples of your assembly branch instructions and their corresponding machine code.**

There are four branches that are supported; which are Jump, bezR2, beqN, beqInc. Jump has 4bits imm which makes it branch to a wide range. While beqN, beqInc are both fixed to branching into the same destination each time they are used. bezR2 branches to PC+imm iff R2=0; otherwise, it goes to PC+1. The maximum branch distance is supported with the Jump instruction which uses 4 imm so it can range from [1-23] in branching forward.

Examples:

|  |  |  |
| --- | --- | --- |
| Branch instruction | Example | Machine code |
| jump | PC = PC + 1 | 1100001 |
| bezR2 | If R2==0, PC+=0 else PC=PC+1 | 1000000 |
| beqN | If R1=R0, branch to Next | 1111110 |
| beqInc | If R0=R1, branch to Increment | 1111101 |

1. **Data memory addressing modes. What addressing modes are supported for data memory? How are the addresses calculated? Give examples of your assembly load / store instructions and their corresponding machine code.**

Addressing Modes supported are M(Ry) with Ry being a register; and the address is calculated such that M(0) is the address 1 of the data memory.

Examples:

|  |  |  |
| --- | --- | --- |
| Instruction | Example | Machine code |
| load | R0=Mem[R0] | 0110000 |
| store | Mem[R0]=R0 | 0100000 |

**Part B) Answers to questions**

1. **Comparing to the sample of “My\_straightforward\_ISA”, what are the unique features of your ISA? Explain why your ISA is better.**

In our ISA design, we are using 1-bit less so we have 7-bits and we have more instructions written within those 7-bits so this can help have less lines of coding.

1. **In what ways did you optimize for the two goals? If you optimized for anything additional, what and how?**

We have got high speed in SW by minimizing the instructions used in each program. And we have low cost HW by simplifying our HW design to make it simpler.

1. **What would you have done differently if you had 1 more bit for instructions? How about 1 fewer bit?**

With 1 more bit, we could have used more registers and therefore make coding part much easier for both programs; however, with 1 less bit, it would be much more difficult to have an efficient design.

1. **How did your team work together to accomplish this project? (Role of each team member, progress milestones, time spent individually and together?)**

Both of us worked together the same amount of time through every procedure.

Time spent is

1. **If you had a chance to restart this project afresh with 3 weeks’ time, how would your team have done differently?**

We would work on the hardware part to make the hardware more efficient.

**Part C) Software package**:

**1. Algorithms (in assembly code) of the two programs. Make sure your assembly format is either obvious or well described, and that the code is well commented. Extra credits: provide a convincing estimation:**

**i. on the dynamic instruction count for P1 (ME) with P = ~1000 and Q = ~500**

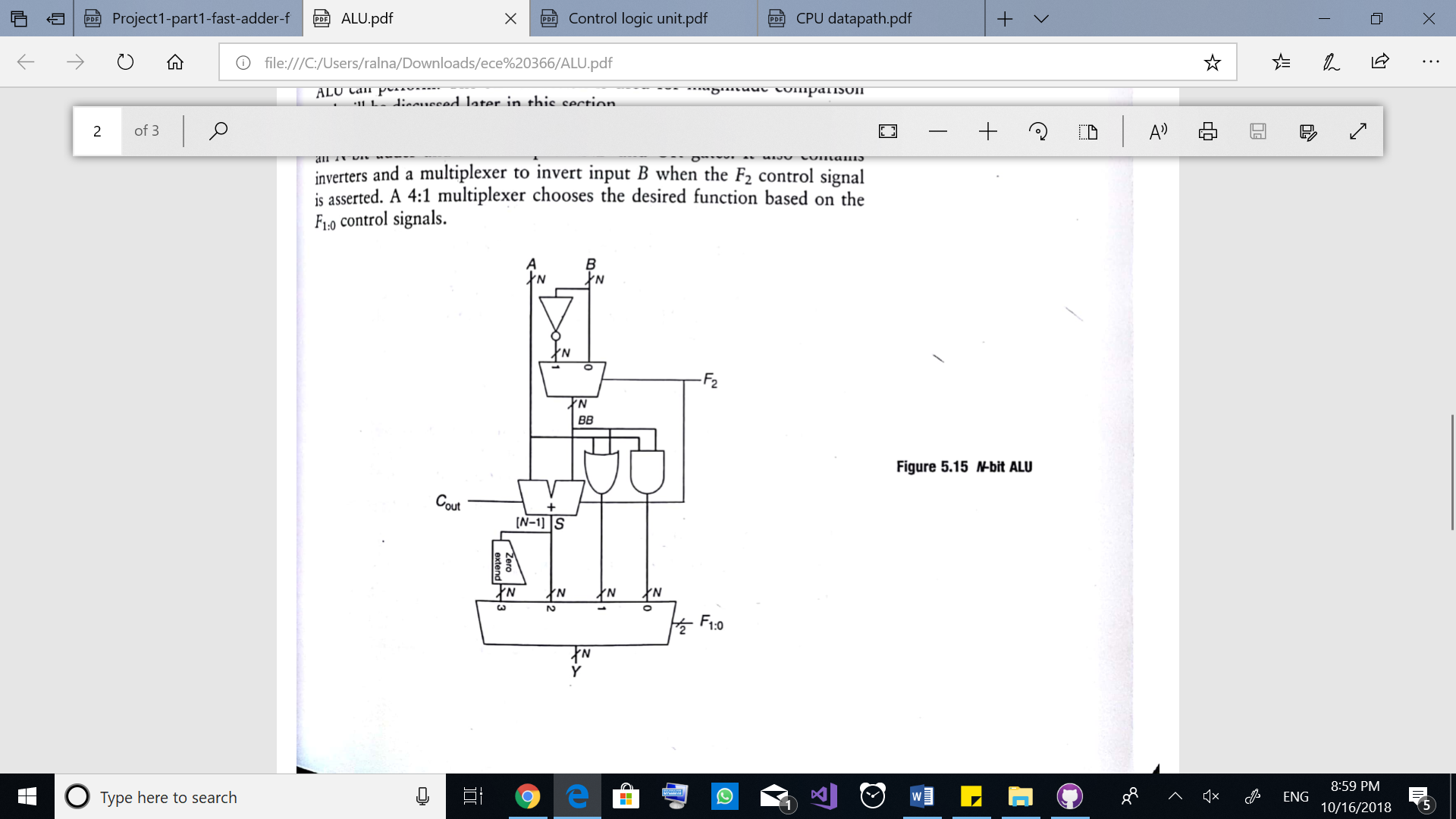
**ii. on the worst-case scenario of dynamic instruction count for P2(BMC).**

**2. Machine code for each of the programs. We will not correct/grade the machine code. You will also not be able to verify whether your code works correctly or not in this project (without a simulator). Therefore, you have to rely on the help of the disassembler, strive to make your algorithm simple and easy to understand, as well as pursue the sw-hw “codesign” – this will avoid putting tremendous complexity at either the software or the hardware end.**

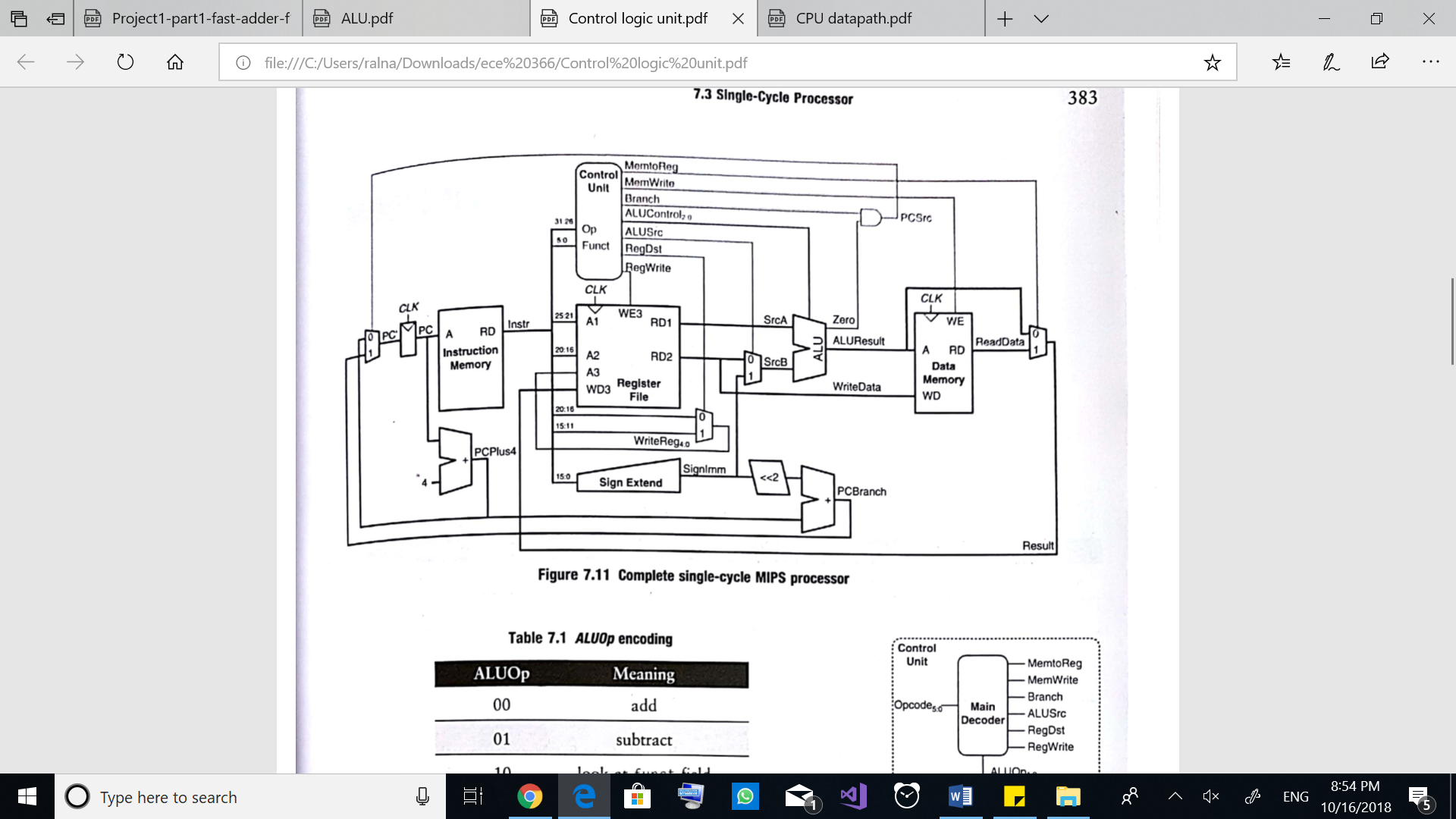
**3. Output of your Python disassembler for each program. This should be a line-by-line explanation of the machine code, what is done by each line of code.**

**4. Python code for your ISA’s disassembler.**

**Part D) Hardware implementation:**

**1. ALU schematic. A hierarchical sketch of your Arithmetic Logic Unit which implements whatever computation that your ISA instructions use (See textbook ch 5.2.4).**

**2. CPU Datapath design. A schematic including your register file, ALU, PC logic, and memory components (see textbook ch 7.3.1).**



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**3. Control logic design. Decoder truth-table indicating how each control signal is generated from an instruction (see textbook ch 7.3.2).**