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Group 6

**ISA Design**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **Instruction** | **opcode** | **Rx** | **Ry** | **imm** | **Range** | **Function** |
| lw | 000 | Rx: **\_ \_** | Ry: **\_ \_** |  | Rx & Ry: [R0, R1, R2, R3] | Load word |
| sw | 001 | Rx: **\_ \_** | Ry: **\_ \_** |  | Rx & Ry: [R0, R1, R2, R3] | Store word |
| add | 100 | Rx: **\_ \_** | Ry: **\_ \_** |  | Rx: [R0, R1]  Ry: [R0, R1, R2, R3] | Add |
| addi | 100 | Rx: **\_ \_** |  | **\_ \_** | Rx: [R2, R3]  imm: [0, 3] | Add w/ imm |
| xor | 110 | Rx: **\_ \_** | Ry: **\_ \_** |  | Rx: [R0, R1]  Ry: [R0, R1, R2, R3] | XOR |
| and | 110 | Rx: **\_ \_** | Ry: **\_ \_** |  | Rx: [R2, R3]  Ry: [R0, R1, R2, R3] | AND |
| Init | 101 | Rx: **\_ \_** |  | **\_ \_** | Rx: [R0, R1]  imm: [-1, 1] | Initialize value |
| sll | 101 | Rx: **\_ \_** |  | **\_ \_** | Rx: [R2, R3]  imm: [0,3] | Bit shift left |
| j | 1110 |  |  | **\_ \_ \_** | imm: [0, 7] | jump by  -5^(imm)-1 |
| sub | 010 | Rx: **\_ \_** | Ry: **\_ \_** |  | Rx: [R0, R1]  Ry: [R0, R1, R2, R3] | Subtract |
| subi | 010 | Rx: **\_ \_** |  | **\_ \_** | Rx: [R2, R3]  imm: [0, 3] | Subtract w/ imm |
| sltR0 | 011 | Rx: **\_ \_** | Ry: **\_ \_** |  | Rx: [R0, R1]  Ry: [R0, R1, R2, R3] | If Rx < Ry,  R0 == 0,  Otherwise,  R0 = 1 |
| seqR0 | 011 | Rx: **\_ \_** | Ry: **\_ \_** |  | Rx: [R2, R3]  Ry: [R0, R1, R2, R3] | If Rx = Ry,  R0 == -1,  Otherwise,  R0 = 1 |
| beqR0 | 1111 |  |  | **\_ \_ \_** | imm: [0,6] | If R0 == 0, PC += 5^(imm)-1  Otherwise,  PC++  Note: imm =/= 111 |
| Halt | 1111111 |  |  |  |  | Stops the processor |