Comparison Of Cache Replacement Policies using Gem-5 Simulator

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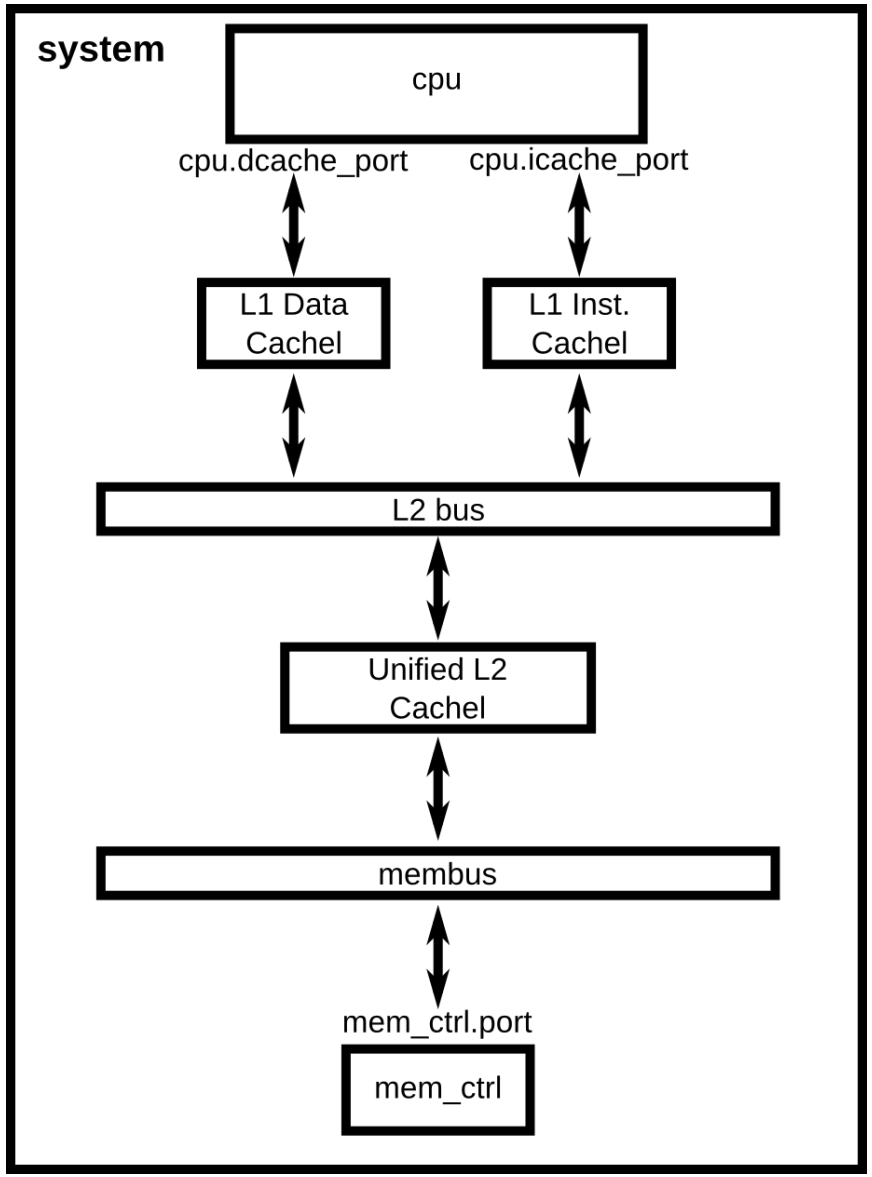
Motivation

- Cache
- Limited Size
- Cache hit rate increase is ideal but what about now?
- Any other alternative?
- Cache Replacement Policy

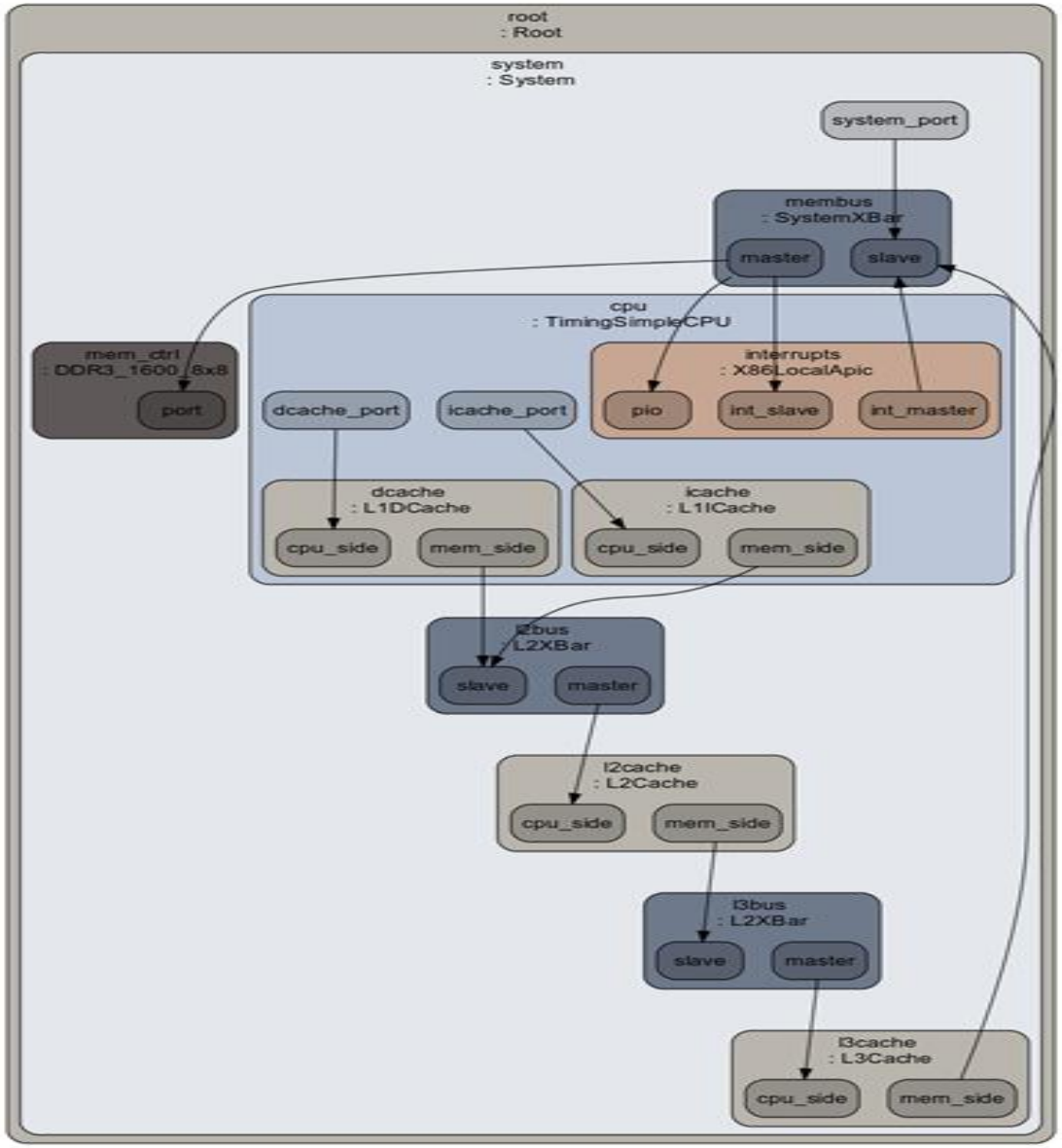
Analysis Overview

- No need of old and less accessed instruction
- Performance analysis through Gem-5
- RR, LRU, FIFO
- Comparative analysis among efficient cache replacement policies

Level 2 Cache Hierarchy



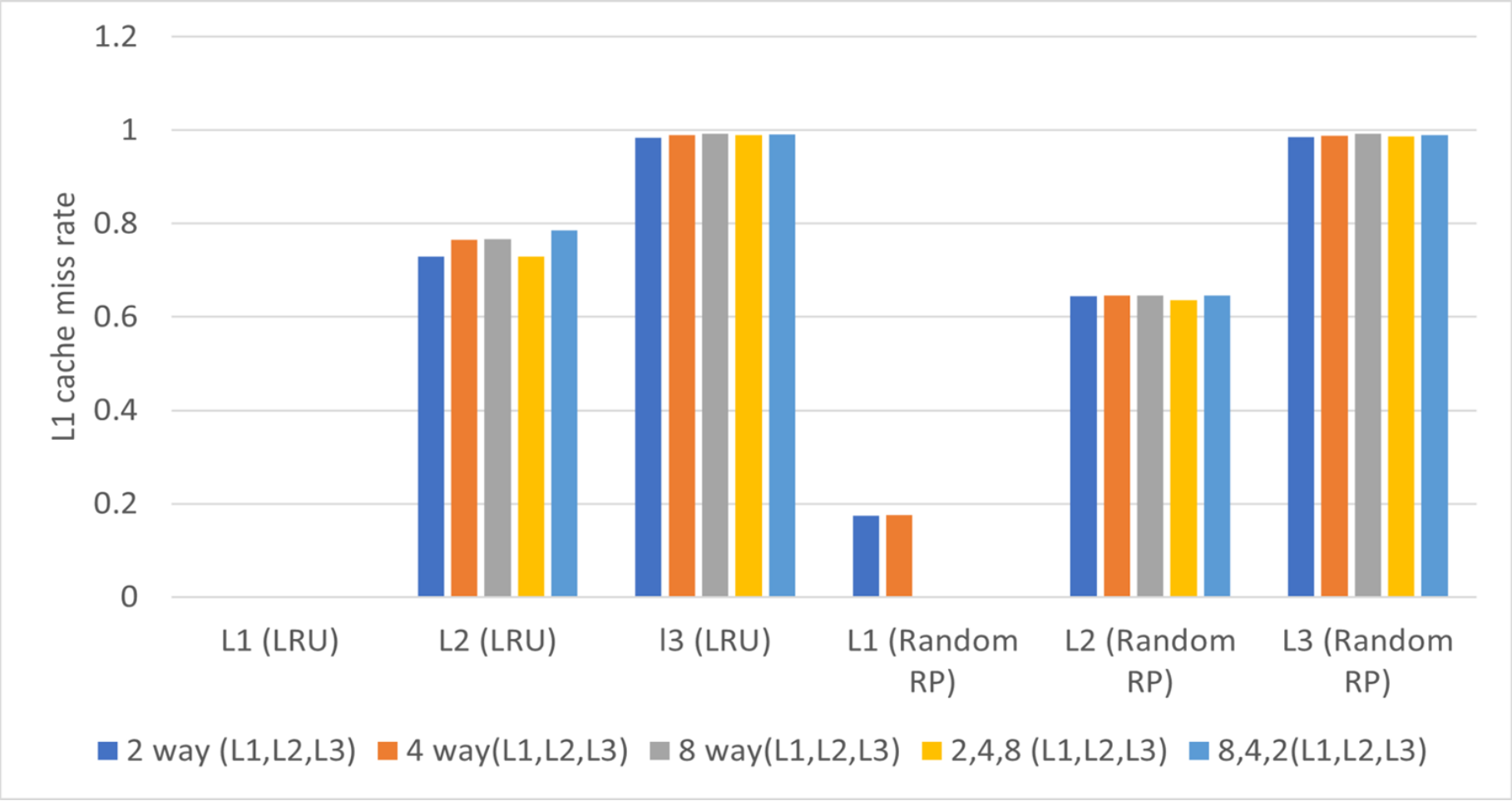
Level 3 Cache Hierarchy



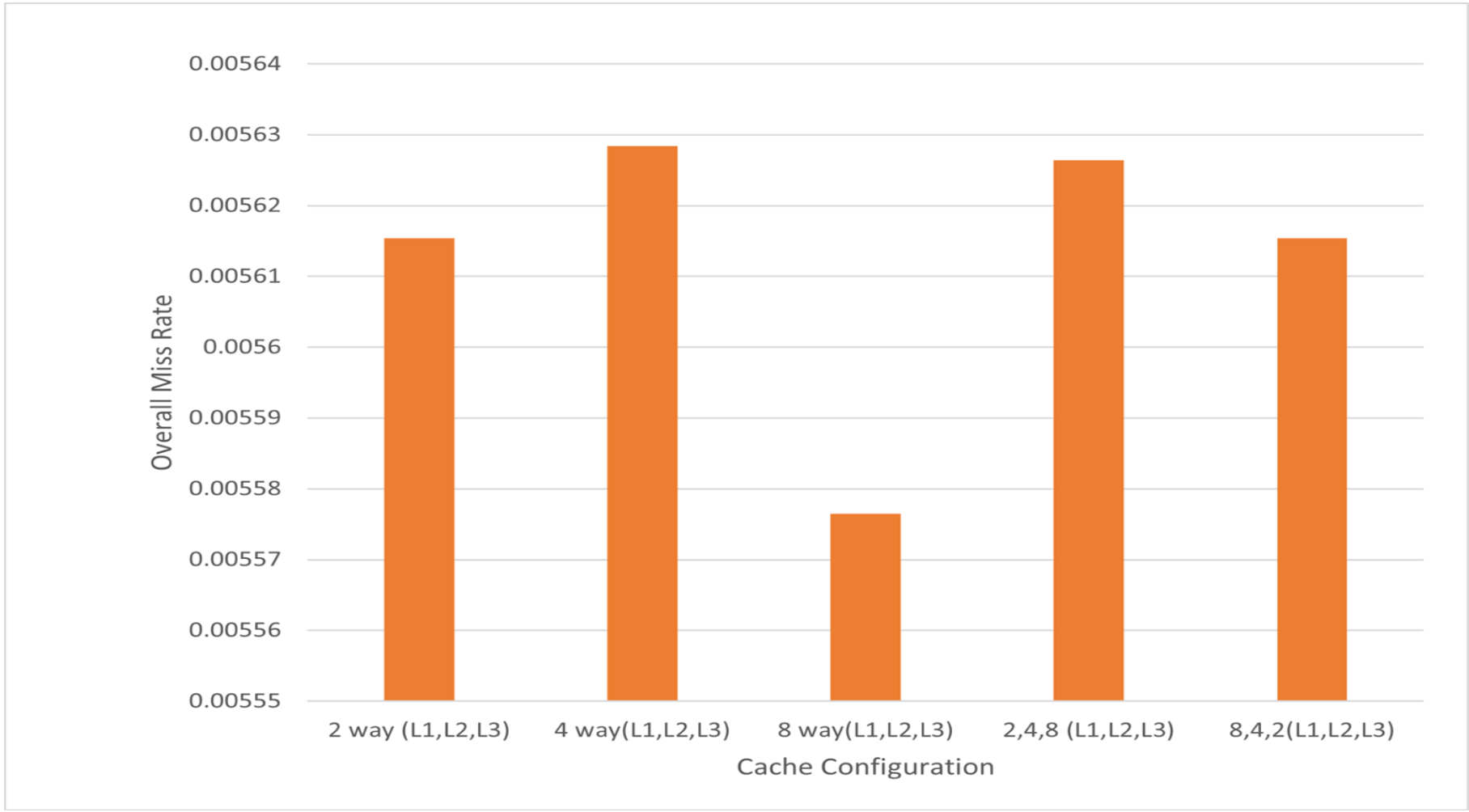
RP: FIFO, LRU, Random, TreePLRU

Configuration # 1	L1 icache (KB)	L1 dcache (KB)	L2 cache (MB)	L1 dcache associativity	L1 icache associativity	L2 cache associativity	Cache line size
1	128	128	4	2	2	1	64
2	256	256	4	2	2	1	64
3	512	512	4	2	2	1	64
4	128	128	8	2	2	1	64
5	128	128	16	2	2	1	64
6	128	128	4	4	4	1	64
7	128	128	4	4	4	4	64
8	128	128	4	8	8	8	64
9	128	128	4	2	2	1	128

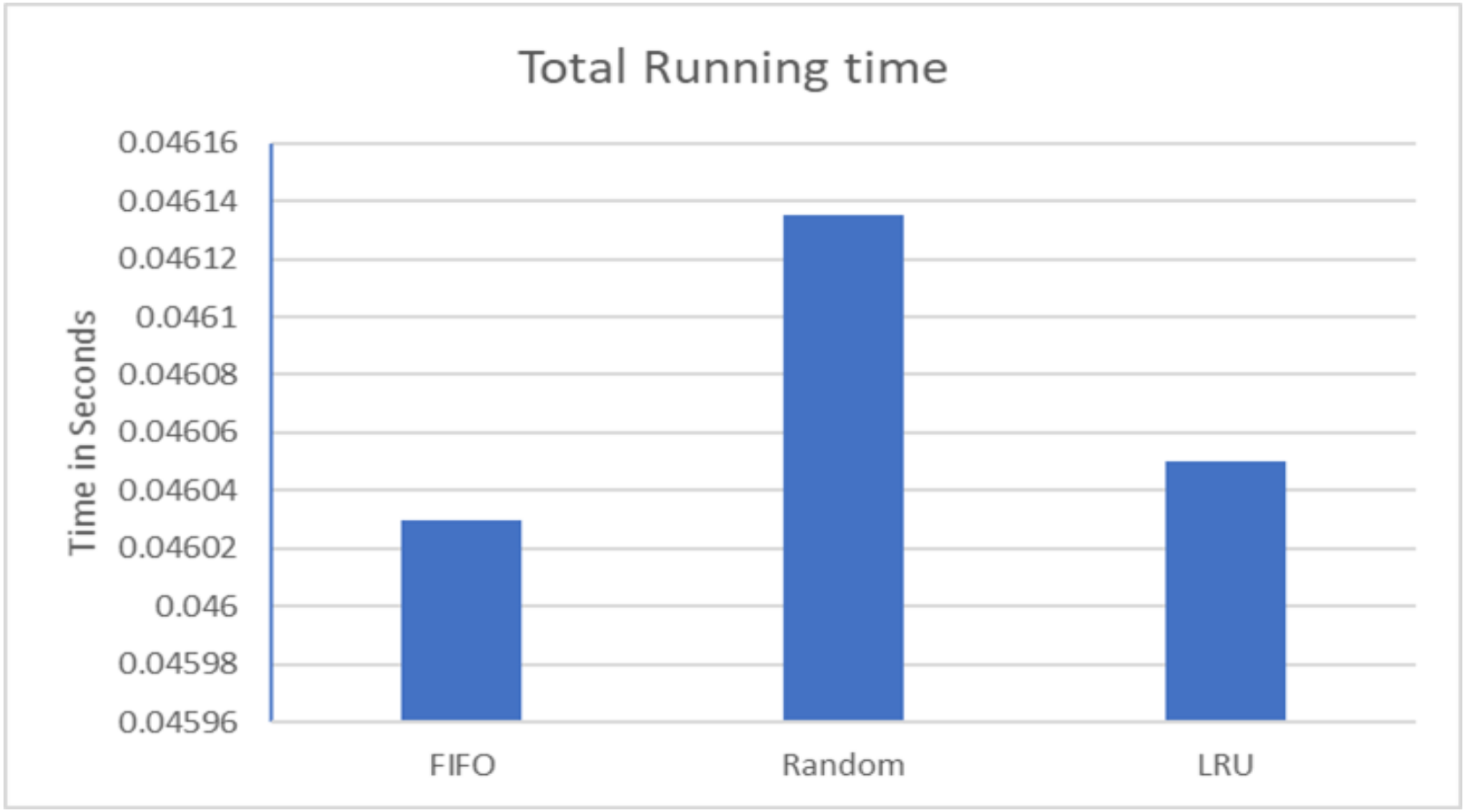
Comparison of L1 cache miss rate with LRU and Random RP



Comparison of overall miss rate with cache configurations having varying associativity



Total running time with different RP while the other parameters remain constant



Time driven Cache side-channel attack

Input Key: 12 34 56 78 9a ab bc d0 30 40 12 45 6f 7e e1 0a

Run time	Expected output 9 a b d 3 4 1 4 6 7 e 0	Successful Nibbles
1	9 d 0 d 2 7 d 4 5 9 8 8	3
2	b 4 b f 3 3 d b 6 7 1 c	4
3	4 9 4 d 0 d b 4 f 7 e d	4
4	d a 3 7 4 4 6 6 6 d e 0	5
5	9 a a d 1 7 1 0 4 7 5 8	5
6	1 a b d 2 0 1 1 0 0 2 3	4
7	9 e 1 7 3 4 c f f 8 3 0	4
8	9 a e 3 3 3 a 4 0 7 e 5	5
9	b 9 a d 9 2 1 2 6 4 e 1	4
10	c 5 b b 3 7 1 b a e e 2	4
	Total = 12 x 10 = 120	= 42

Accuracy = (42/120)x100% = 35%

Future task

1. In the full-system mode, GEM5 runs a real operating system on it and allows users to interact with the OS. Hence, users can run any applications on GEM5 as running on real-world hardware.
2. The downside of GEM5 is that its execution is 1000X slower than real hardware.
3. Run GEM5 in FS mode and run the AES attack to observe the effects.
4. Implementation on multi-core system.