VHDL Assignment 1

1)

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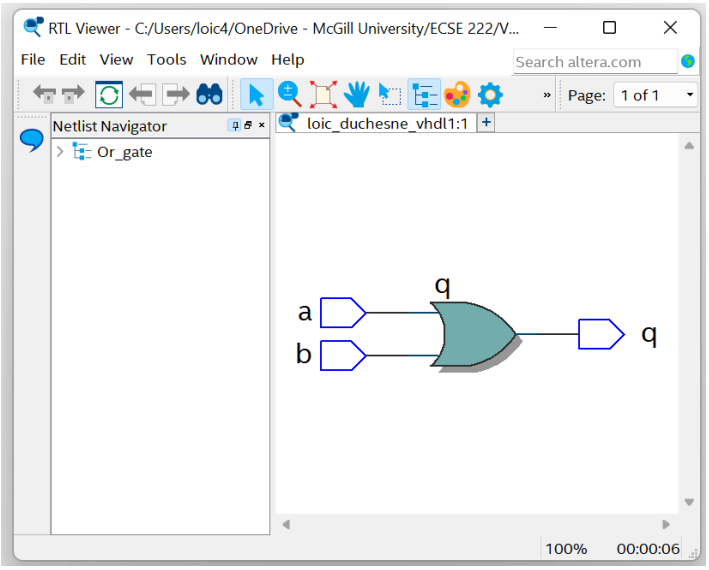
2) Executive Summary

For this lab, we wanted to program and simulate an OR gate using different kinds of parameters. We started by writing the OR gate itself by creating a new VHDL file in the project. Afterwards, we defined the test scenarios (e.g.: defining the inputs) writing a testbench VHDL file. We then compiled all the code so that it could be ran. After that, we ran an RTL simulation using the ModelSim Altera plugin. Finally, after running the simulation, we visualized the inputs and outputs and adjusted the timescale so the graphs would be properly shown.

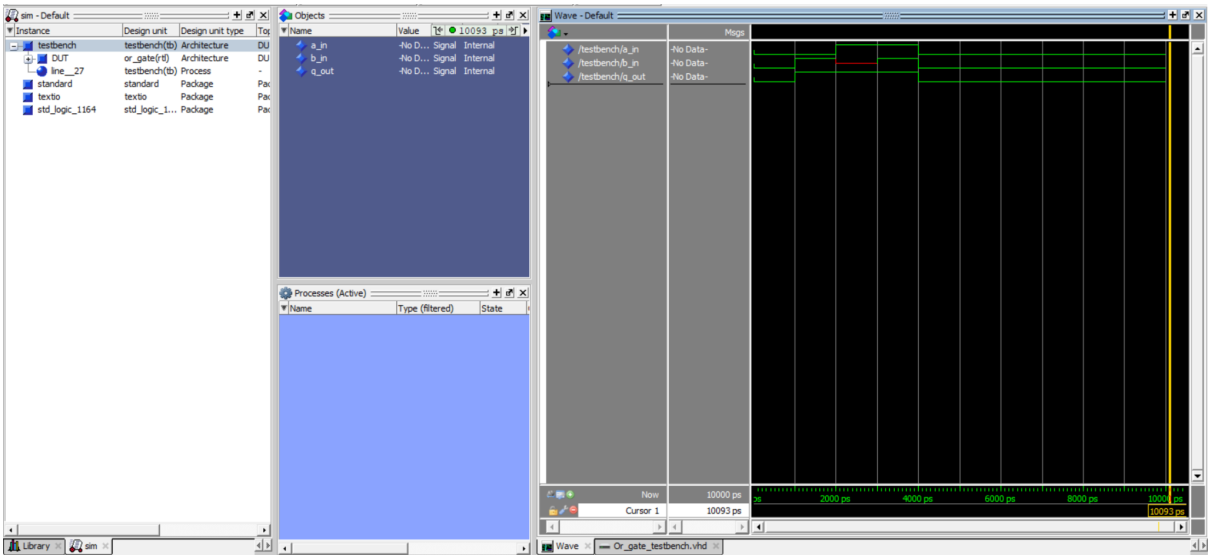
3) *There is no further questions in this assignment.*

4, 5)

The following pictures consist of all of our simulation results. The first picture was simply the schematic, while the second one consists of the results themselves.



In this picture, we visualized the architecture of our system (in that case just an OR gate) using the RTL Viewer associated with the Altera plugin.



For this picture: After we ran the simulation we got a function that actually describes an OR gate.

- *when a is 0 and b is 0 the output is 0*
- *when a is 0 and b is 1 the output is 1*
- *when a is 1 and b is X (unknown) the output is 1 because we have one input that is 1*
- *when a is 1 and b is 1 the output would definitely be 1*

6-

In this lab, we developed a basic understanding VHDL, and also visualizing basic gates using the Quartus Prime II as well as the modelsim altera plugin(for visualizing). During our simulation we encountered some problems, one of them was having to run the simulation twice for it to work and as well as some directory issues. But at the end the simulation worked just fine and we got the result that we should actually get. This also allowed us to familiarize with the small workarounds that we have to do to get proper results using this software, which will be useful for future VHDL assignments.