Zre

Cre

A*B+C   P

<<1

Zim

Zre_N+1

C - A*B   P

A

B

C

A*B+C   P

Cim

Zim_N+1

A*B   P

A*B+C   P

one clock per DSP block
A = 18 bits, B = 18 bits, C = 36 bits, P = 37 bits
MSB truncated