NGUYEN PHUOC LOI

FOUNDATION IP FRONT-END ENGINEER FRESH GRADUATES

CONTACT

0359561607
Loinp.dn@gmail.com
www.linkedin.com/in/phước-lợi-nguyễn-691024382

COMMUNICATION

Friendly and dedicated, enjoy sports and exploring new things. Have experience in teamwork and volunteer activities.

REFERENCES

Thesis: Digital System Design and Verification using SystemC

Certificate: Internship Faraday, Toeic 515 (Aug 2024), GPA 3.0/4.0.

EDUCATION

Can Tho University

Major: Computer Engineering

Graduated: October 2025

SKIILS

Langues: SystemC, Verilog, SystemVerilog, Tcl.

Tools: Quartus, Questasim, Innovus, Calibre, Thunder.

Basic Knowledge: CMOS, MMMC, Lib/LEF, Avalon-MM.

English: Toeic 515 (Aug 2024).

EXPERIENCE

Graduation Thesis – Digital System Design and Verification using SystemC

- Designed and simulated basic digital circuits, FSMs, and a 32-bit MIPS processor at the RTL level using SystemC.
- Developed an IP core for integration with the Nios II CPU and performed HW/SW co-design using SystemC.
- Synthesized SystemC models into SystemVerilog RTL, implemented and verified the design on FPGA.

Physical Design Internship – Faraday Vietnam

- Received basic training in CMOS, Tcl, MMMC, Lib, LEF, Floorplan, Power Grid, CTS, PnR, PV, and STA.

EXPECTATION

Learn and gain experience from seniors in a friendly and professional environment at Connexus. Desire to stay long-term and contribute to the company.