Lois Orosa

Department of Information Technology and Electrical Engineering (D-ITET), H 62.1
ETH Zürich • Switzerland
https://loisorosa.github.io lois.orosa@safari.ethz.ch

Research Interests

Computer Architecture, Memory Systems, Hardware Security, New Memory Technologies, Machine Learning, Processing in Memory, Storage Systems, Photonics, Hardware/Software Reliability, Parallel Systems.

Education

- **Senior Researcher** — **ETH Zürich, Switzerland**
  Department of Information Technology and Electrical Engineering (D-ITET) — *January 2019 -*
  - Supervisor: Onur Mutlu.
- **PostDoctoral Fellow** — **University of Campinas (UNICAMP), Brazil**
  Computer Systems Laboratory (LSC) — *June 2014 – July 2018*
  - Architectural Support for Speculative Program Execution.
  - Supported by FAPESP grant 2014/03840-2.
  - Supervisor: Rodolfo Azevedo.
- **Academic Guest** — **ETH Zürich, Switzerland**
  Department of Computer Science, Systems Group — *January 2017 - January 2018*
  - Enabling security features in commodity DRAM chips.
  - Supported by FAPESP grant 2016/18929-4.
  - Supervisor: Onur Mutlu.
- **PostDoctoral Researcher** — **University of Santiago de Compostela, Spain**
  CiTIUS — *January 2014 – May 2014*
  - Supervisors: Elisardo Antelo and Javier Bruguera.
- **PostDoctoral Researcher** — **Universidade Nova de Lisboa, Portugal**
  Computer Science Department — *September 2013 – December 2013*
  - Hardware support for detecting atomicity violations.
  - Supported by European Cooperation in Science and Technology (COST) with a Short-term Scientific Mission (STSM).
  - Supervisor: João Lourenço.
- **Phd Student** — **University of Santiago de Compostela, Spain**
  Department of Electronics and Computer Science - Computer Architecture group — *2008 – September 2013*
  - Thesis title: "New Hardware Support for Transactional Memory and Parallel Debugging in Multicore Processors"
  - Supported by the project “Hardware and software support for high performance computing" (TIN2010-17541).
  - Advisors: Elisardo Antelo Suárez and Javier Díaz Bruguera.
- **Phd Courses** — **University of Santiago de Compostela, Spain**
  Department of Electronics and Computer Science — *September 2008 – June 2010*
  - Interuniversity PhD in Information Technology (University of Santiago de Compostela and University of Coruña)
- **Scholarship** — **University of Illinois at Urbana-Champaign, U.S.A.**
  Department of Computer Science - IACOMA group — *September 2009 – December 2009*

- Research topic: Tolerating concurrency bugs in multicore processors.
- Advisor: Josep Torrellas

- **M.Eng** **University of Vigo, Spain**
  Telecommunications Engineering *2000 – 2005*

Industry Experience

- **Xilinx Research** **Dublin, Ireland**
  Internship *July 2018 – December 2018*
  - Research on Training Convolutional Neural Networks (CNNs)
  - Mentor: Michaela Blott
- **Recore Systems** **Enschede, Netherlands**
  Internship *August 2012 – December 2012*
  - Development of a shared memory multicore simulator.
  - Mentor: Gerard Rauwerda
- **IBM R&D Labs** **Haifa, Israel**
  Summer internship *July 2010 – October 2010*
  - Development of compiler-based deterministic replay for X10 Language.
  - Mentors: Olga Golovanevsky, Marina Biberstein, Bilha Mendelson.
- **ARANTIA 2010 (Televes group)** **Santiago de Compostela, Spain**
  R&D engineer *November 2006 – January 2008*
  - Development of network multimedia applications (TV streaming, multimedia contents).
- **Communitel Global S.A. (Vodafone)** **Vigo, Spain**
  Engineer *April 2006 – November 2006*
  - Resolve second level maintenance issues, and automatize large-scale production tasks with perl and C.
- **Communitel Global S.A. (Vodafone)** **Vigo, Spain**
  Engineer *July 2005 – October 2005*
  - Development of WebServices.

Published Papers

Conference Papers

- **Lois Orosa**, Yaohua Wang, Mohammad Sadrosadati, Jeremie S. Kim, Minesh Patel, Ivan Puddu, Haocong Luo, Kaveh Razavi, Juan Gómez-Luna, Hasan Hassan, Nika Mansouri-Ghiasi, Saugata Ghose, Onur Mutlu, "CODIC: A Low-Cost Substrate for Enabling Custom In-DRAM Functionalities and Optimizations", 48th IEEE International Symposium on Computer Architecture (ISCA'21)
- Jawad Haj-Yahya, Jeremie Kim, Ivan Puddu, Abdullah Giray Yaglikci, Mohammed Alser, **Lois Orosa**, Juan Gómez-Luna, Onur Mutlu, "IChannels: Exploiting Current Management Mechanisms to Create Covert Channels in Modern Processors", 48th IEEE International Symposium on Computer Architecture (ISCA'21)
- Jisung Park, Myungsuk Kim, Myoungjun Chun, **Lois Orosa**, Jihong Kim, Onur Mutlu, "Reducing Solid-state Drive Read Latency by Optimizing Read-retry", 26th International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS'21)
- Christina Giannoula, Nandita Vijaykumar, Nikela Papadopoulou, Ivan Fernandez, Vasileios Karakostas, **Lois Orosa**, Juan Gómez Luna, Georgios Goumas, Nectarios Koziris, Onur Mutlu, "SynCron: Enabling Efficient Synchronization Support for Near-Data-Processing Architectures", 27th IEEE International Symposium on High-Performance Computer Architecture (HPCA'21)
- Abdullah Giray Yaglikci, Minesh Patel, Jeremie Kim, Roknoddin AziziBarzoki, Jisung Park, Hasan Hassan, Ataberk Olgun, **Lois Orosa**, Konstantinos Kanellopoulos, Taha Shahroodi, Saugata Ghose, Onur Mutlu, "BlockHammer: Preventing RowHammer at Low Cost by Blacklisting Rapidly-Accessed DRAM Rows", 27th IEEE International Symposium on High-Performance Computer Architecture (HPCA'21)

- Jawad Haj-Yihia, Mohammed Alser, **Lois Orosa**, Jeremie Kim, Efraim Rotem, Avi Mendelson, Anupam Chattopadhyay, Onur Mutlu, "A Power- and Workload-Aware Hybrid Power Delivery Network for Energy-Efficient High-end Client Processors", 53rd IEEE/ACM International Symposium on Microarchitecture (MICRO'20)

- Yaohua Wang, **Lois Orosa**, Xiangjun Peng, Yang Guo, Saugata Ghose, Minesh Patel, Jeremie Kim, Juan Gómez Luna, Mohammad Sadrosadati, Nika Mansouri Ghiasi, Onur Mutlu, "Reducing DRAM Latency via Fine-grained In-DRAM Cache", 53rd IEEE/ACM International Symposium on Microarchitecture (MICRO'20)

- Leonid Yavits, **Lois Orosa**, Suyash Mahar, João Dinis Ferreira, Ran Ginosar, Onur Mutlu, Mattan Erez, "WoL-FRaM: Enhancing Wear-Leveling and Fault Tolerance in Resistive Memories Using Programmable Address Decoders", 38th IEEE International Conference on Computer Design (ICCD'20)

- Jorge Gonzalez, Alexander Gazman, Maarten Hattink, Mauricio G. Palma, Meisam Bahadori, Ruth Rubio-Noriega, **Lois Orosa**, Madeleine Glick, Onur Mutlu, Keren Bergman, and Rodolfo Azevedo, "Optically Connected Memoryfor Disaggregated Data Centers", 32nd International Symposium on Computer Architecture and High Performance Computing (SBAC-PAD'20)

- Jeremie Kim, Minesh Patel, Abdullah Giray Yaglikci, Hasan Hassan, Roknoddin Azizi, **Lois Orosa**, and Onur Mutlu, "Revisiting RowHammer: An Experimental Analysis of Modern DRAM Devices and Mitigation Techniques", 47th Annual International Symposium on Computer Architecture (ISCA'20)

- Haocong Luo, Taha Shahroodi, Hasan Hassan, Minesh Patel, Abdullah Giray Yaglikci, **Lois Orosa**, Jisung Park, and Onur Mutlu, "CLR-DRAM: A Low-Cost DRAM Architecture Enabling Dynamic Capacity-Latency Trade-Off", 47th Annual International Symposium on Computer Architecture (ISCA'20)

- Myungsuk Kim, Jisung Park, Genhee Cho, Yoona Kim, **Lois Orosa**, Onur Mutlu, and Jihong Kim, "Evanesco: Architectural Support for Efficient Data Sanitization in Modern Flash-Based Storage Systems", 25th International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS'20)

- Skanda Koppula, **Lois Orosa**, Giray Yaglikci, Roknoddin Azizi, Taha Shahroodi, Konstantinos Kanellopoulos, and Onur Mutlu, "EDEN: Enabling Energy-Efficient, High-Performance Deep Neural Network Inference Using Approximate DRAM", 52nd Annual IEEE/ACM International Symposium on Microarchitecture (MICRO'19)

- Jeremie S. Kim, Minesh Patel, Hasan Hassan, **Lois Orosa** and Onur Mutlu, "D-RaNGe: Using Commodity DRAM Devices to Generate True Random Numbers with Low Latency and High Throughput", 25th IEEE International Symposium on High-Performance Computer Architecture (HPCA'19)

- Yaohua Wang, Arash Tavakkol, **Lois Orosa**, Saugata Ghose, Nika Mansouri Ghiasi, Minesh Patel, Jeremie Kim, Hasan Hassan and Onur Mutlu, "Reducing DRAM Latency via Charge-Level-Aware Look-Ahead Partial Restoration ", 51st Annual IEEE/ACM International Symposium on Microarchitecture (MICRO'18).

- Arash Tavakkol, Mohammad Sadrosadati, Saugata Ghose, Jeremie Kim, Yixin Luo, Yaohua Wang, Nika Mansouri Ghiasi, **Lois Orosa**, Juan Gomez-Luna and Onur Mutlu, "FLIN: Enabling Fairness and Enhancing Performance in Modern NVMe Solid State Drives", 45th International Symposium on Computer Architecture (ISCA'18), Los Angeles, 2018, pp. 397-410.

- Jorge Gonzalez, **Lois Orosa** and Rodolfo Azevedo, "Architecting a computer with a full optical RAM," 23rd IEEE International Conference on Electronics, Circuits and Systems (ICECS'16), Monte Carlo, 2016, pp. 716-719.

- **Lois Orosa** and Rodolfo Azevedo, "Temporal frequent value locality," 27th IEEE International Conference on Application-specific Systems, Architectures and Processors (ASAP'16), London, 2016, pp. 147-152.

- **Lois Orosa** and João Lourenço, "A Hardware Approach for Detecting, Exposing and Tolerating High Level Atomicity Violations", 24th Euromicro International Conference on Parallel, Distributed, and Network-Based Processing (PDP'16), Heraklion, 2016, pp. 159-167.

- Shanxiang Qi, Norimasa Otsuki, **Lois Orosa**, Abdullah Muzahid, and Josep Torrellas, "Pacman: Tolerating Asymmetric Data Races with Unintrusive Hardware", 18th International Symposium on High Performance Computer Architecture (HPCA'12), New Orleans, Lousiana, 2012, pp. 1-12.

- **Lois Orosa**, J.D. Bruguera and E. Antelo, "A Cache Filtering Mechanism for Hardware Transactional Memory Systems Decoupled from Caches", XX Jornadas de Paralelismo, A Coruña (Spain), 2009.

Journals

- Muhammad Shafique, Mahum Naseer, Theocharis Theocharides, Christos Kyrkou, Onur Mutlu, **Lois Orosa**, Jungwook Choi, "Robust Machine Learning Systems: Challenges, Current Trends, Perspectives, and the Road Ahead", IEEE Design & Test 2020
- **Lois Orosa**, Rodolfo Azevedo and Onur Mutlu, "AVPP: Address-first Value-next Predictor with Value Prefetching for Improving the Efficiency of Load Value Prediction", ACM Transactions on Architecture and Code Optimization (TACO), 2018.
- Mohammad Sadrosadati, Borna Ehsani, Hajar Falahati, Rachata Ausavarungnirun, Arash Tavakkol, Mojtaba Abaei, **Lois Orosa**, Yaohua Wang, Hamid Sarbazi-Azad and Onur Mutlu, "ITAP: Idle-Time-Aware Power Management Technique for GPU Execution Units", ACM Transactions on Architecture and Code Optimization (TACO), 2018.
- **Lois Orosa**, J.D. Bruguera and E. Antelo, "Asymmetric Allocation in a Flexible Signature Module for Multicore Processors", The Computer Journal, Oct. 2016, vol. 59, no. 10, pp. 1453-1469.
- **Lois Orosa**, E. Antelo and J.D. Bruguera, "FlexSig: Implementing Flexible Hardware Signatures", ACM Transactions on Architecture and Code Optimization (TACO), January 2012, Volume 8 Issue 4.

Workshops (refereed)

- **Lois Orosa** and Rodolfo Azevedo, "LogSI-HTM: Log Based Snapshot Isolation in Hardware Transactional Memory", 7th Workshop on the Theory of Transactional Memory (WTTM 2015), July 20th, 2015, Donostia-San Sebastián, Spain - in conjunction with PODC 2015.
- **Lois Orosa** and João Lourenço, "A Hardware Approach for Detecting, Exposing and Tolerating High Level Atomicity Violations", Workshop on Dependable Multicore and Transactional Memory Systems (DMTM), January 22nd, 2014, Vienna, Austria

---

Posters

- **Lois Orosa**, Yaohua Wang, Ivan Puddu, Mohammad Sadrosadati, Hasan Hassan, Arash Tavakkol, Nika Mansouri Ghiasi, Minesh Patel, Jeremie Kim, Juan Gomez-Luna, Vivek Seshadri, Rodolfo Azevedo and Onur Mutlu, "Dataplant: A Low-Cost In-DRAM Value Generation Primitive for Enabling System Security Features", ETH Systems Group Industry Retreat, January 22-24, 2018, Engelberg, Switzerland.
- Mohammad Sadrosadati, Amirhossein Mirhosseini, Borna Ehsani, Rachata Ausavarungnirun, Arash Tavakkol, Hajar Falahati, **Lois Orosa**, Yaohua Wang, Hamid Sarbazi-Azad, Babak Falsafi and Onur Mutlu, "Improving GPU Power and Energy Efficiency", ETH Systems Group Industry Retreat, January 22-24, 2018, Engelberg, Switzerland.
- Juan Gómez-Luna, Arash Tavakkol, Amirali Boroumand, Geraldo Francisco de Oliveira Junior, Mert Atamaner, Mohammad Sadrosadati, Nika Mansouri Ghiasi, **Lois Orosa** and Onur Mutlu, "Processing-In-Memory Benchmark Suite and Analysis", ETH Systems Group Industry Retreat, January 22-24, 2018, Engelberg, Switzerland.
- **Lois Orosa**, Yaohua Wang, Ivan Puddu, Mohammad Sadrosadati, Hasan Hassan, Arash Tavakkol, Minesh Patel, Vivek Seshadri, Rodolfo Azevedo and Onur Mutlu, "A Case for an Amnesic DRAM Chip", ETH Industry day, Zurich, Switzerland, 29 August 2017.
- **Lois Orosa**, Rodolfo Azevedo and Onur Mutlu, "AVPP: Address-first Value-next Predictor with Value Prefetching", ETH Systems Group Industry Retreat, January 30 - February 1, 2017, Engelberg, Switzerland.
- **Lois Orosa**, E. Antelo and J.D. Bruguera, "FlexSig: Implementing Flexible Hardware Signatures", 7th HiPEAC Conference on High-Performance and Embedded Architectures and Compilers (HiPEAC'12), January 23-25, 2012, Paris, France

---

Master Thesis

- Title: "Hardware to Improve the Parallel Programming Support on CMPs"
- Department of Electronics and Computer Science, University of Santiago de Compostela, July 2010
- Advisors: Javier D. Bruguera and Elisardo Antelo

Undergraduate Thesis

- Title: "Design and Development of an Interface to Access and Remotely Control a QoS Parameter Measurement Device in VoIP networks"
- Telecommunications Engineering School, University of Vigo, April 2006
- Advisor: J. Carlos López Ardao. In collaboration with Comunitel Global S.A. (Vodafone)

(Invited) Talks

- "CODIC: A Low-Cost Substrate for Enabling Custom In-DRAM Functionalities and Optimizations"", 48th IEEE International Symposium on Computer Architecture, June 15th, 2021, Global Online event
- "FIGARO: Improving System Performance via Fine-grained in-DRAM Data Relocation and Caching", 53th IEEE/ACM International Symposium on Microarchitecture, October 19th, 2020, Global Online event
- "More Capable and Efficient DRAM Main Memory Designs", Swiss Joint Research Center Workshop, École Polytechnique Fédérale de Lausanne (EPFL), January 30, 2020
- "EDEN: Enabling Energy-Efficient, High-Performance Deep Neural Network Inference Using Approximate DRAM", Computer Architecture Course (263-2210-00L), ETH Zurich, October 24th, 2019
- "AVPP: Address-first Value-next Predictor with Value Prefetching for Improving the Efficiency of Load Value Prediction", 14th HiPEAC Conference on High-Performance and Embedded Architectures and Compilers (HiPEAC'19), January 22th, 2019, Valencia, Spain. .
- "ITAP: Idle-Time-Aware Power Management for GPU Execution Units", 14th HiPEAC Conference on High-Performance and Embedded Architectures and Compilers (HiPEAC'19), January 23th, 2019, Valencia, Spain..
- "Temporal Frequent Value Locality", 27th Annual IEEE International Conference on Application-specific Systems, Architectures and Processors (ASAP'16), July 6th, 2016, London, England.
- "Detecting, Exposing and Tolerating High Level Data Races", 2nd Manycore Workshop on Micro architectural Challenges in Performance, Energy Efficiency and Resilience, March 15th, 2016, Campinas, Brazil.
- "A Hardware Approach for Detecting, Exposing and Tolerating High Level Atomicity Violations", 24th Euromicro International Conference on Parallel, Distributed, and Network-Based Processing (PDP'16), February 19th, 2016, Heraklion, Greece.
- "Revisiting Load Value Speculation", Seminar series, April 17th, 2015, University of Campinas, Brazil.
- "Revisiting Load Value Speculation", Research Meeting: Performance, Energy and Reliability Challenges in Multi- and Many-core Platforms, March 19th, 2015, Porto Alegre, Brazil.
- "A Hardware Approach for Detecting, Exposing and Tolerating High Level Atomicity Violations", Workshop on Dependable Multicore and Transactional Memory Systems (DMTM), January 22nd, 2014, Vienna, Austria.
- "FlexSig: Implementing Flexible Hardware Signatures", 7th HiPEAC Conference on High-Performance and Embedded Architectures and Compilers (HiPEAC'12), January 23th, 2012, Paris, France.
- "A Cache Filtering Mechanism for Hardware Transactional Memory Systems Decoupled from Caches", XX Jornadas de Paralelismo, A Coruña (Spain), 2009.
- "Introduction to microprocessors and microcontrollers", XCARFOS Summer course (Days of automatic control and robotics with open source tools), July 2009

Projects and Grants

- Researcher in the project "Memory System Design for AI/ML Accelerators & ML/AI Techniques for Memory System Design", Semiconductor Research Corporation (SRC), Task 2946.001, 1 year, **100.000 CHF**
- FAPESP 2016/18929-4, Speculative Techniques for Reducing the Memory Bottleneck Problem, ETH Zurich (Switzerland), 1 year, **68.735 CHF**.
- FAPESP 2014/03840-2, Architecture Support for Speculative Program Execution, University of Campinas (Brazil), 3 years, **239.990 BRL**.
- Euro-TM Short Term Scientific Mission, Universidade Nova de Lisboa, Lisbon (Portugal), 3 months, **3.500 EUR**.
- HiPEAC Industrial PhD Internship, Recore Systems, Enschede (Netherlands), 4 months, **5.000 EUR**.
- HiPEAC Industrial PhD Internship, IBM Haifa (Israel), 3 months, **5.000 EUR**.
- Researcher in the project "Hardware and software support for high performance computing" (TIN2010-17541), **185.400 EUR**.

Services

Program committee member for:

- Fifth Workshop on Attacks and Solutions in hardware security (ASHES 2021), co-located with ACM CCS 2021

Reviewer for:

- ACM Computing Surveys (CSUR) 2020
- Transactions on Architecture and Code Optimization (TACO) 2020
- IEEE MICRO [2019, 2020]
- Computers and Security 2019
- Design, Automation and Test in Europe Conference (DATE) 2019
- IEEE Transactions on Computers [2015, 2016, 2017, 2019]
- ERAD-SP 2018
- Journal of Universal Computer Science 2018

Teaching Experience

Teaching Assistant, ETH Zurich (Switzerland)

- 263-2210-00L - Computer Architecture [Falls'17, Fall'19, Fall'20]
- 263-2211-00L - Seminar in Computer Architecture [Spring'19, Fall'19, Spring'20, Fall'20, Spring'21]
- 252-0028-00L - Digital Design and Computer Architecture [Spring'19. Spring'20, Spring'21]

Lecturer, Institute of Computing, University of Campinas (Brazil)

- MC102 - Algorithms and Computer Programming (90h), Spring'16

PhD Students

- **Jorge Luis Gonzalez Reaño** — **University of Campinas, Brazil**
  Thesis Title: "An All-Optical Computer System" — *2014 - 2021*
  - Co-advising with Rodolfo Azevedo.

Technical Skills

Programming Languages: C, C++, assembly, LaTeX, Perl, Python, bash
Instrumentation Tools: Intel Pin
Simulators: Simics, GEMS, QEMU, Bochs, ZSIM, Ramulator, McPAT, DRAMPower

---

Languages

Galician: Native | **Spanish:** Native | **English:** C1 | **Portuguese:** Professional working proficiency