The *2023 IRDS Beyond CMOS* chapter explores how modern semiconductor technology is preparing for the post-CMOS era, addressing the limitations of continued scaling and the emergence of new computational paradigms. The report defines two strategic focus areas: “More Moore,” which enhances existing CMOS capabilities through heterogeneous integration, and “Beyond CMOS,” which involves exploring fundamentally different devices, materials, and computing models. The overarching goal of this roadmap chapter is to systematically assess the maturity, challenges, and opportunities of novel devices and architectures that could redefine future information processing technologies.

The report begins by identifying five broad categories of technical challenges: (1) scalable memory technologies that outperform SRAM and FLASH, (2) extending CMOS scaling with new materials and device structures, (3) developing entirely new logic and memory technologies to replace CMOS, (4) expanding CMOS functionality into new domains (More-than-Moore), and (5) enabling unconventional computing paradigms that bridge devices and architectures. Each of these challenges corresponds to a major thematic section in the document, reflecting the growing difficulty of sustaining Moore’s Law and the need for radical innovation.

One of the first technical focus areas addressed is *emerging memory technologies*. The report categorizes these into volatile, non-volatile, and analog memory types, including STT-MRAM, RRAM (OxRAM), FeFETs, and Phase-Change Memory (PCM). For analog in-memory computing, the chapter highlights resistive and ferroelectric devices capable of vector-matrix multiplication, particularly useful in neural networks and AI workloads. A significant concern for these devices is variability, endurance, and integration compatibility with CMOS fabrication. Memory selector devices are also discussed as a necessary component for enabling dense crossbar arrays without sneak paths, improving read/write reliability.

Following memory, the document examines *emerging logic devices*, which are categorized into CMOS extension devices and Beyond-CMOS devices. CMOS extensions include FinFET successors like Gate-All-Around FETs, Negative Capacitance FETs (NCFETs), Tunnel FETs (TFETs), and devices with 2D channel materials such as MoS₂. Beyond-CMOS devices include spintronic (STT-MRAM logic), excitonic, superconducting, and quantum devices. While these novel devices promise gains in energy efficiency and new forms of data representation, they often suffer from manufacturing challenges, low temperature operation requirements, or immature modeling frameworks. The chapter stresses the importance of benchmarking these devices using metrics like energy-delay product (EDP), switching time, scalability, and compatibility with Boolean logic.

The roadmap continues by exploring the *interplay between device technologies and system architectures*. It emphasizes a co-design philosophy, where devices and architectures are developed in tandem to optimize for energy efficiency and application-specific performance. Computational kernels such as matrix multiplication, convolution, and search/match operations are used to evaluate how well new devices support key workloads. Architectures discussed include neuromorphic systems, in-memory computing, probabilistic computing, and reversible logic. Device-level features such as non-volatility, stochasticity, and analog behavior are leveraged to design new computing paradigms that deviate from von Neumann architecture, thus reducing the data movement bottleneck.

In the section on *More-than-Moore applications*, the report highlights how Beyond-CMOS devices can address emerging needs in hardware security, sensing, and edge computing. Security primitives such as Physically Unclonable Functions (PUFs), True Random Number Generators (TRNGs), and cryptographic accelerators are presented. These make use of device-level randomness, process variability, and noise to ensure secure key storage and authentication. For example, memristive and spintronic PUFs exploit fabrication-induced randomness for secure identification. Additionally, emerging devices are shown to be promising for low-power and always-on sensing applications in IoT devices.

The section on *emerging materials integration (EMI)* addresses the growing need for new materials with specific electrical, magnetic, and structural properties to support Beyond-CMOS devices. This includes 2D materials like graphene and TMDs, topological insulators, multiferroics, and complex oxides. Materials for low-leakage, high-k dielectrics, and resistive switching are also discussed. A critical theme is the control of interfaces, defects, and doping at atomic scales. The report stresses the importance of combining traditional semiconductor processing techniques with directed self-assembly and machine learning-guided materials discovery. Challenges remain in integrating these materials into CMOS-compatible processes, especially when high-temperature steps or non-planar structures are required.

In the *assessment section*, the report revisits earlier benchmarking efforts like the Nanoelectronics Research Initiative (NRI) and survey-based assessments from ITRS. Devices were benchmarked using conventional logic circuits (inverters, NAND gates, shift registers) and compared against 5 nm CMOS in terms of area, energy, speed, and functionality. The findings indicate that while no Beyond-CMOS device has universally outperformed CMOS, several show potential in niche applications. Charge-based devices like TFETs and 2D-FETs scored better in compatibility and scalability than non-charge-based devices like spintronics and excitonics, which often face integration or operating temperature challenges. However, the report suggests that the success of Beyond-CMOS technologies may lie not in replacing CMOS but in augmenting it in hybrid systems optimized for specific tasks.

The concluding summary synthesizes the key principles to guide research in Beyond-CMOS technologies: embracing new computational state variables beyond electron charge (e.g., spin, phase, flux), leveraging non-equilibrium systems, exploring new energy transfer mechanisms (e.g., dipole interactions, tunneling), managing nanoscale thermal effects, enabling sub-lithographic manufacturing, and co-developing new system architectures. The chapter recognizes that while CMOS will remain dominant in the near term, future breakthroughs will likely emerge from cross-disciplinary innovation involving materials science, quantum physics, and computer architecture.