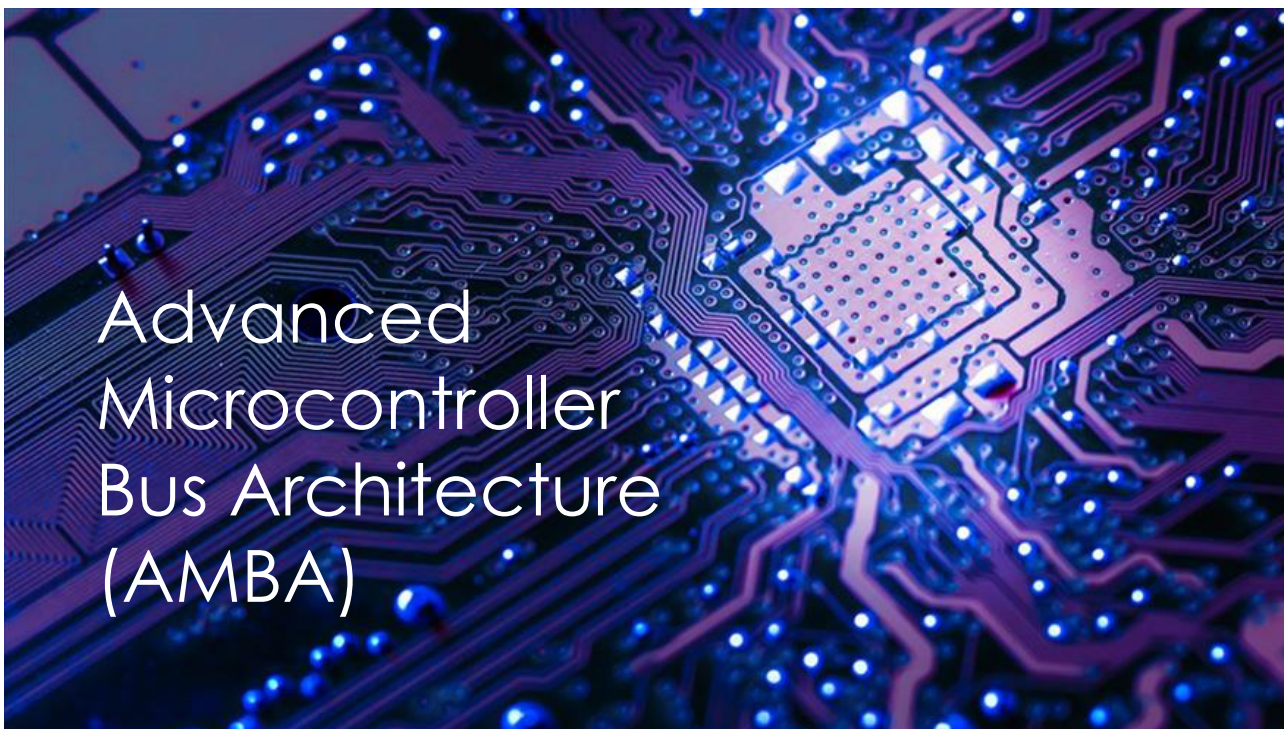
在调试器下理解ARMv8

——设备管理和外存

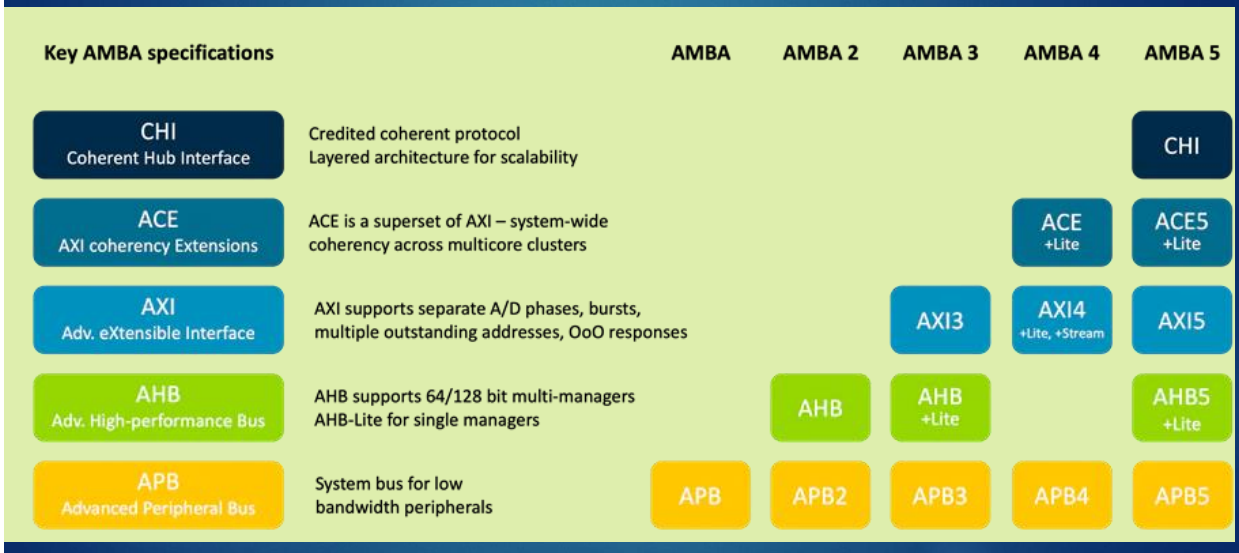
张银奎 2022-1-23



芯片内通信的开放标准

AMBA (Advanced Microcontroller Bus Architecture) is a freely-available, open standard for the connection and management of functional blocks in a system-on-chip (SoC). It facilitates right-first-time development of multi-processor designs, with large numbers of controllers and peripherals.

https://developer.arm.com/architectures/system-architectures/amba

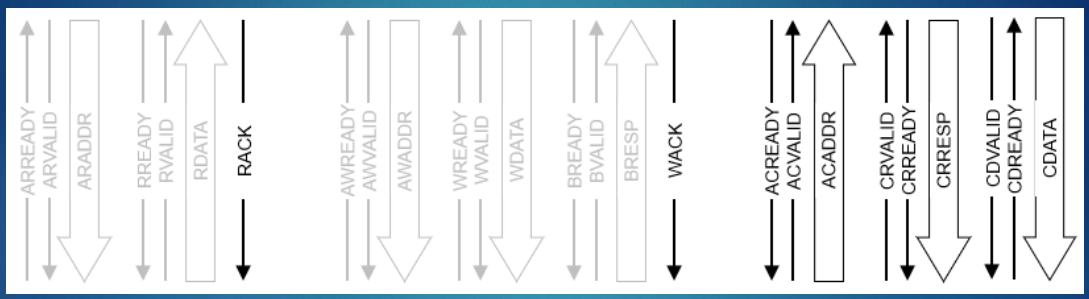


Interface/Link 专车

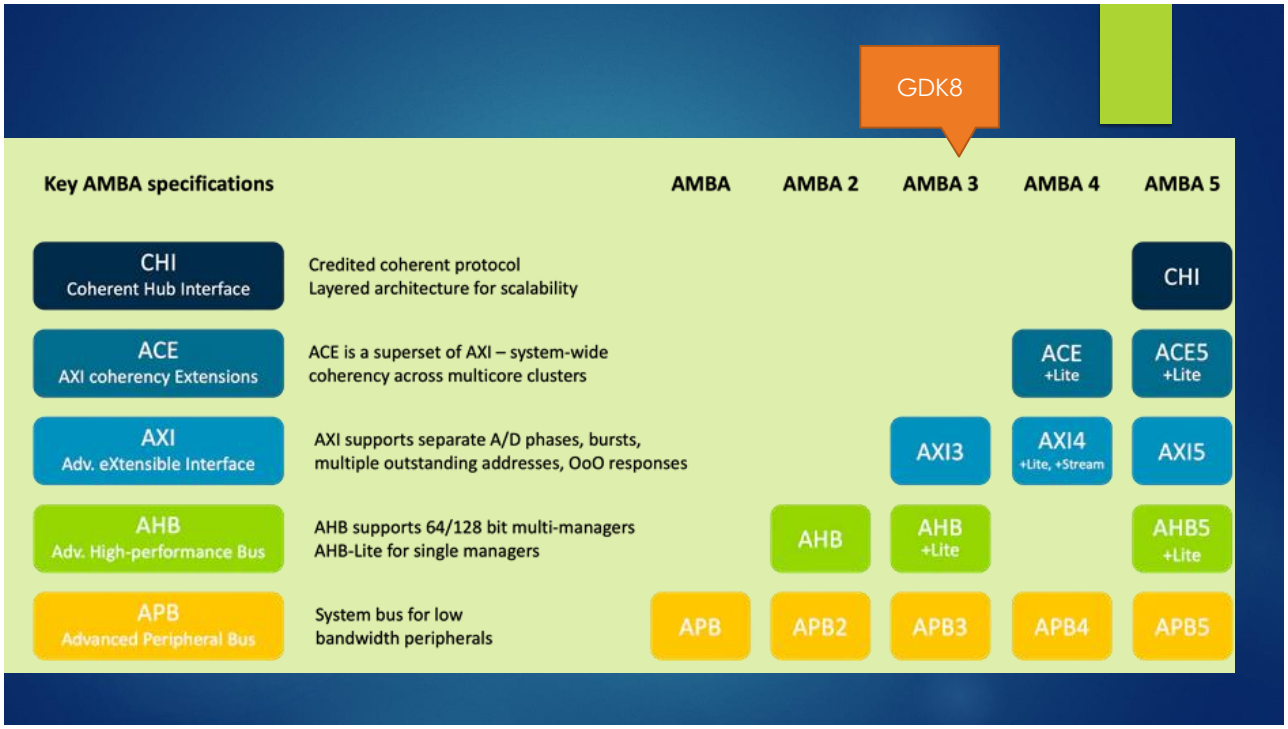
Bus 公交

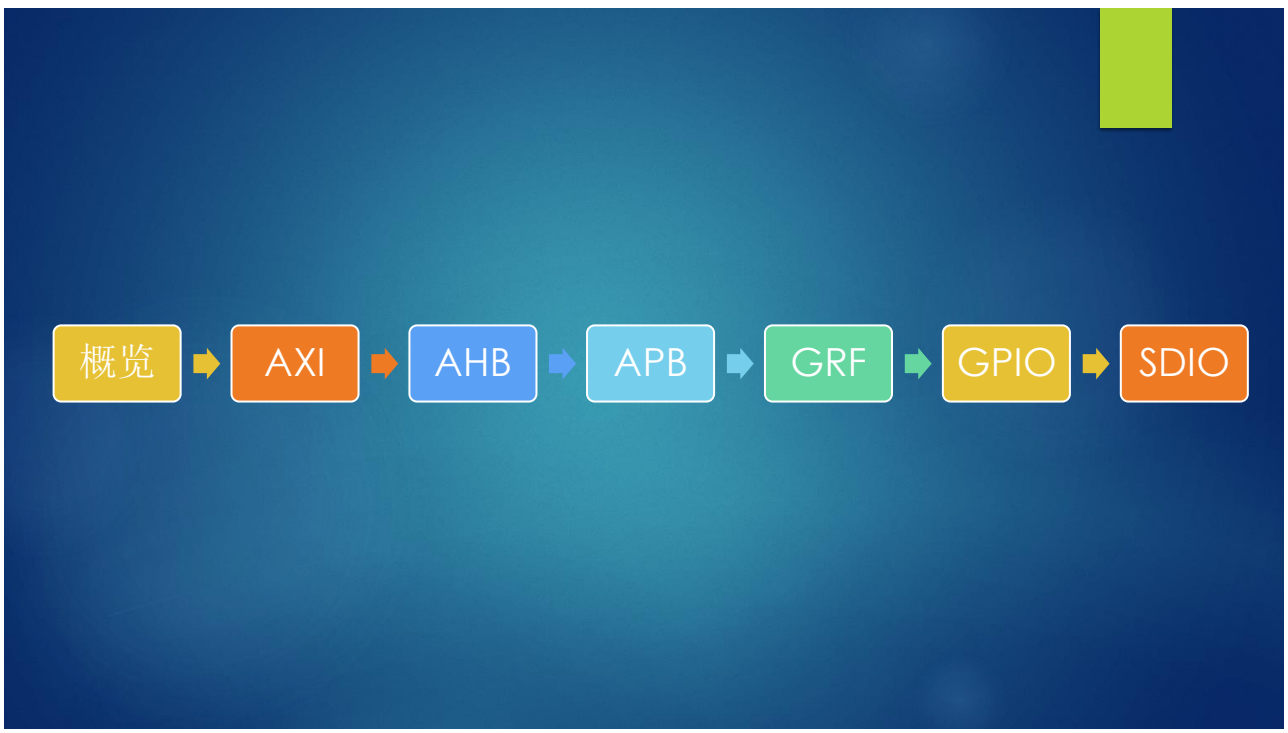
偶尔，也用BUS泛指总线和和互联接口，但这是不精确的

AXI + **ACE信号**



图中灰色为AXI信号，黑色为ACE信号





ARM Extends AMBA Specification With AXI Protocol For High-Performance System-on-chip Design

AXI delivers ground-breaking performance while building on key AMBA strengths

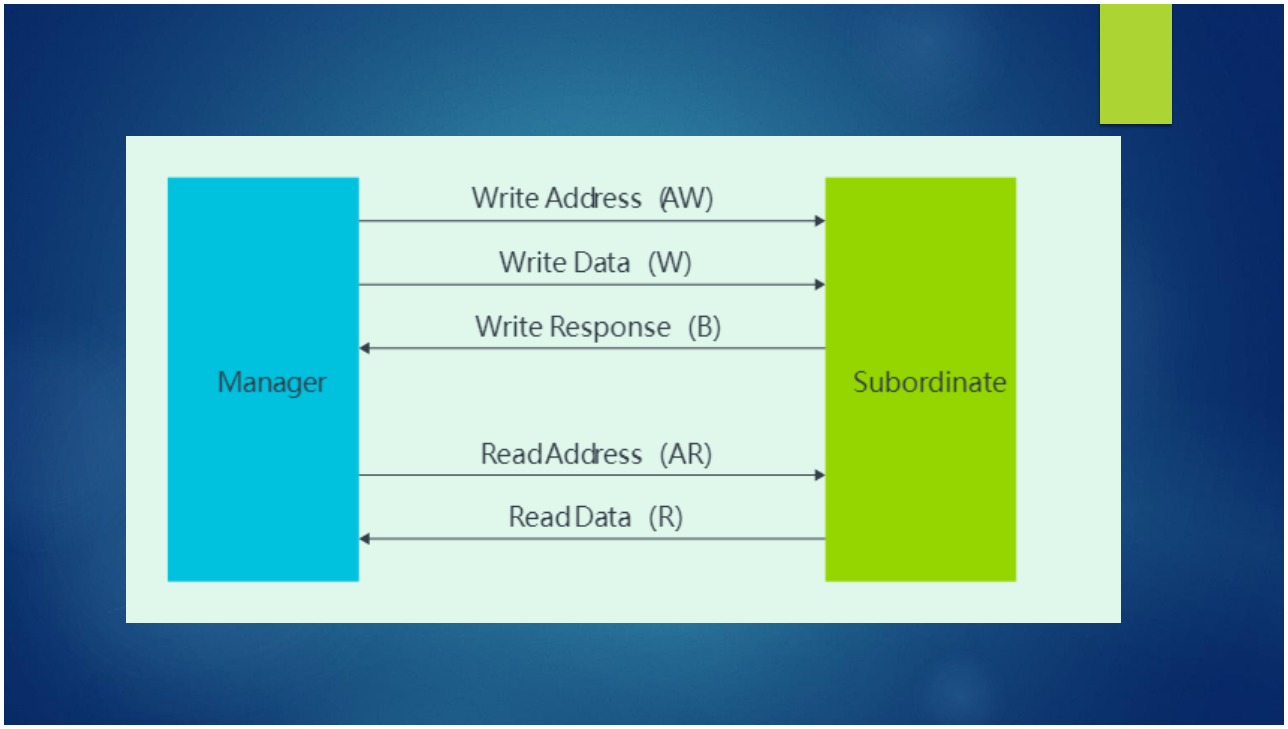
CAMBRIDGE, UK -- June 16, 2003 – ARM [(LSE: ARM); (Nasdaq: ARMHY)], the industry's leading provider of 16/32-bit embedded RISC microprocessor solutions, today announced at Embedded Processor Forum, San Jose, Calif., the release of the AXI definition, a new high-performance protocol within the AMBA™ methodology portfolio of specifications. AXI technology enhances the existing AMBA specification providing a protocol that has been designed to meet the needs of ultra high performance and complex system-on-chip (SoC) designs.

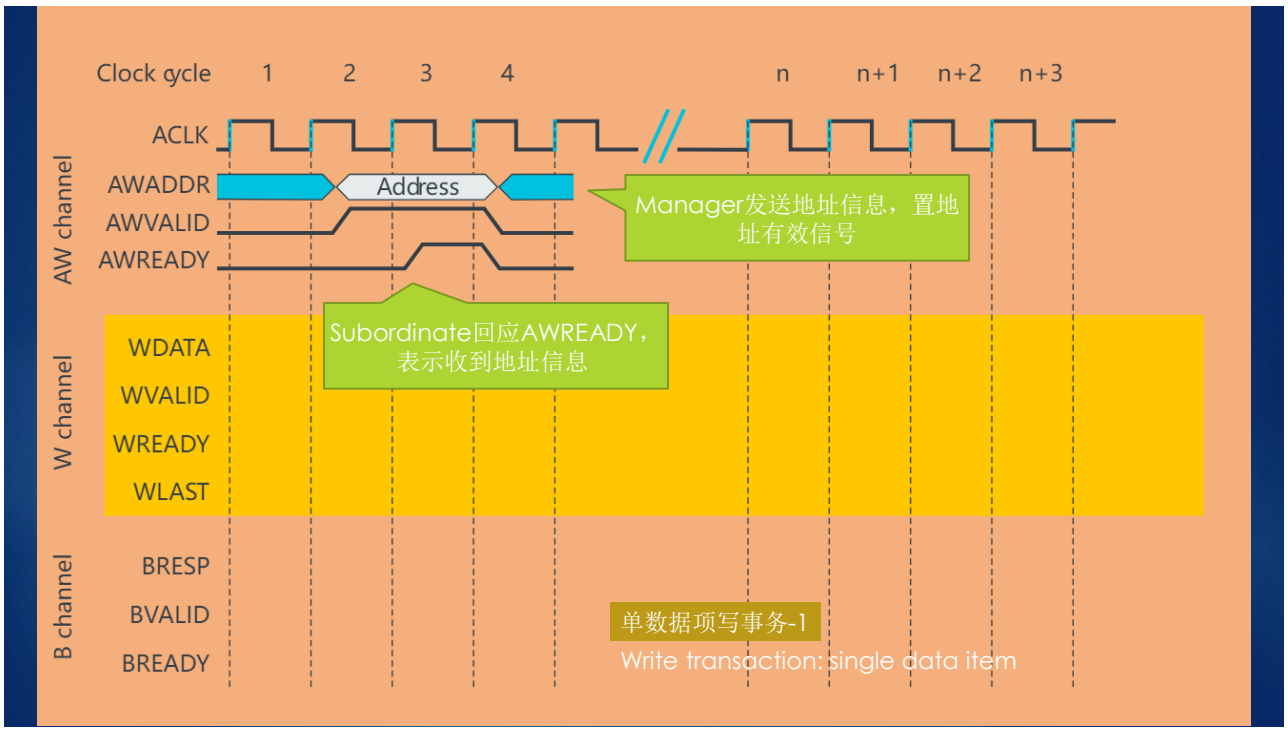
Change history

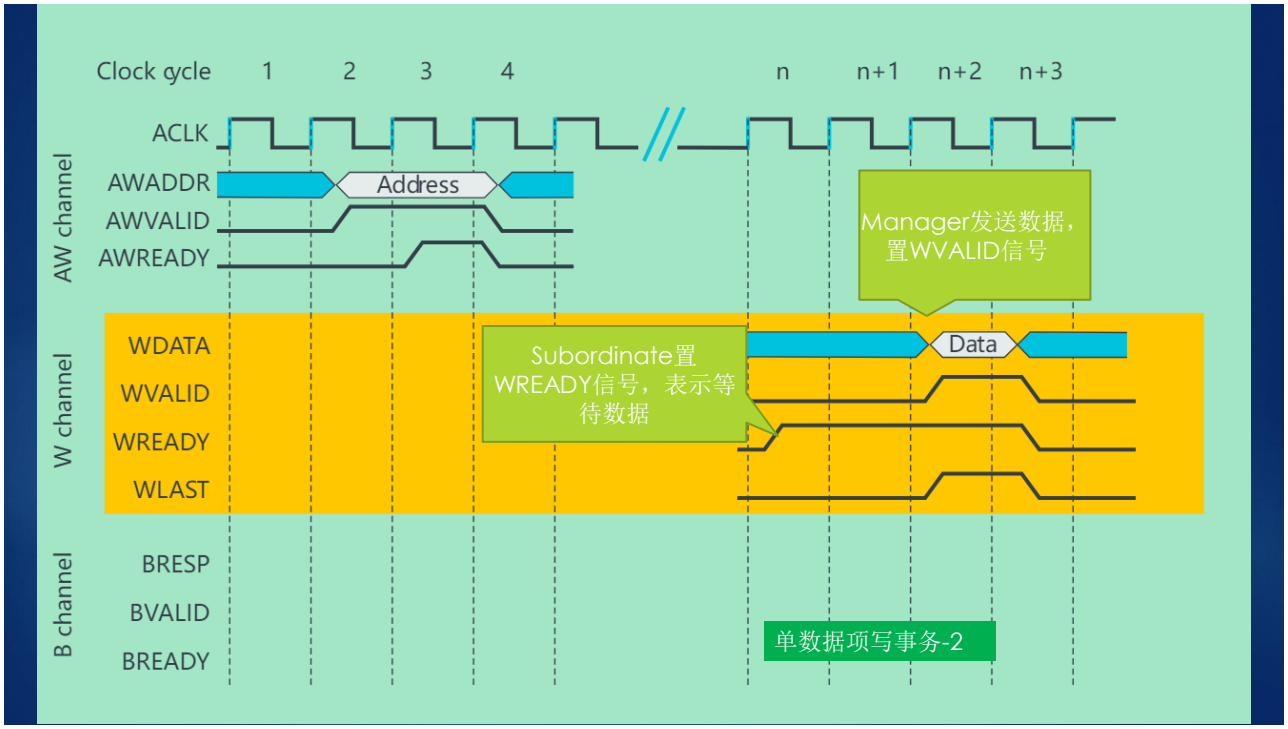
Date	Issue	Confidentiality	Change
16 June 2003	A	Non-Confidential	First release
19 March 2004	B	Non-Confidential	First release of AXI specification v1.0
03 March 2010	C	Non-Confidential	First release of AXI specification v2.0
03 June 2011	D-2c	Non-Confidential	Public beta draft of AMBA AXI and ACE Protocol Specification
28 October 2011	D	Non-Confidential	First release of AMBA AXI and ACE Protocol Specification
22 February 2013	E	Non-Confidential	Second release of AMBA AXI and ACE Protocol Specification
18 December 2017	F	Non-Confidential	EAC-0 release of version F. New interfaces defined for AMBA protocol: AXI5, AXI5-Lite, ACE5, ACE5-Lite, ACE5-LiteDVM, ACE5-LiteACP.
21 December 2017	F.b	Non-Confidential	EAC-1 release to address issues found with the EAC-0 release of release F. No change in content compared to the EAC-0 version.
30 July 2019	G	Non-Confidential	EAC-0 release of version G. New optional features defined for AMBA 5 interface variants.
31 March 2020	H	Non-Confidential	EAC-0 release of version H. New optional features defined for AMBA 5 interface variants.
11 January 2021	H.b	Non-Confidential	Regularized terminology to use *Manager* to indicate the agent that initiates transactions and *Subordinate* to indicate the agent that receives and responds to requests.
26 January 2021	H.c	Non-Confidential	Corrected error in table D13-22 for AxADDR[15]

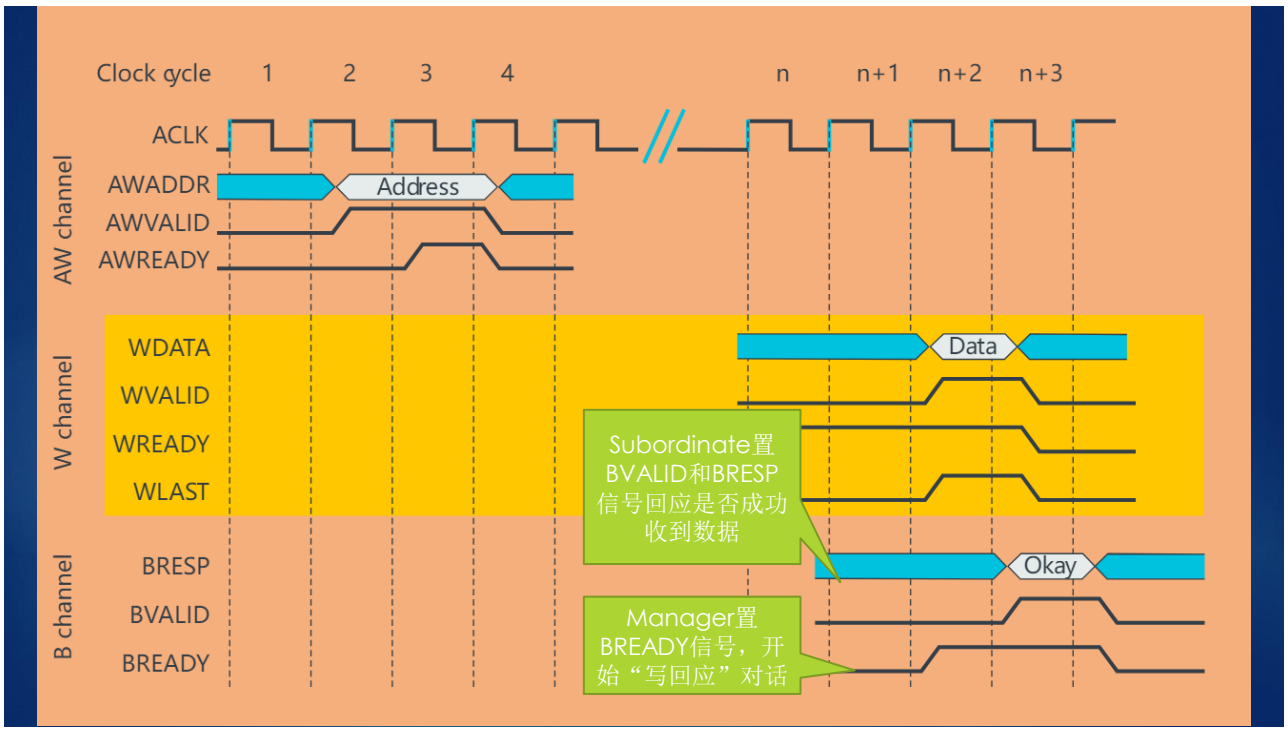
AMBA® AXI and ACE

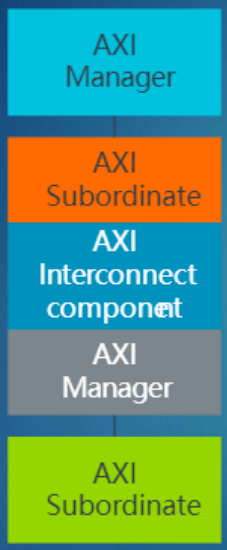
Protocol Specification


Write Address (AW)
Write Data (W)
Write Response (B)
Manager
Subordinate
ReadAddress (AR)
ReadData (R)


Clock cycle
1
2
3
4
n
n+1
n+2
n+3
ACLK
AW channel
AWADDR
Address
AWVALID
AWREADY
Manager发送地址信息，置地址有效信号
Subordinate回应AWREADY，表示收到地址信息
W channel
WDATA
WVALID
WREADY
WLAST
B channel
BRESP
BVALID
BREADY
单数据项写事务-1
Write transaction: single data item







AXI的通信是点对点的，数据传输总是发生在Manager和Subordinate之间，因此连接也只发生在Manager和Subordinate之间

AXI Interconnect v2.1

LogiCORE IP Product Guide

Vivado Design Suite

PG059 December 20, 2017

XILINX

赛灵思(XILINX)的AXI互联设计方案(IP)

https://www.xilinx.com/content/dam/xilinx/support/documentation/ip_documentation/axi_interconnect/v2_1/pg059-axi-interconnect.pdf

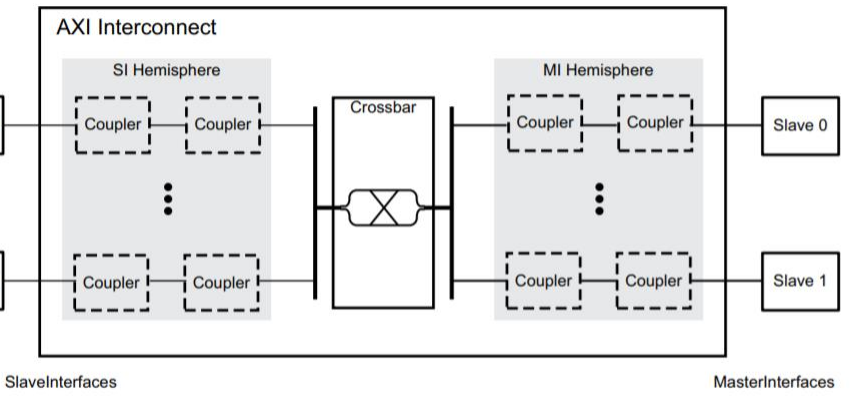


Figure 2-1: **AXI Interconnect Core Diagram**

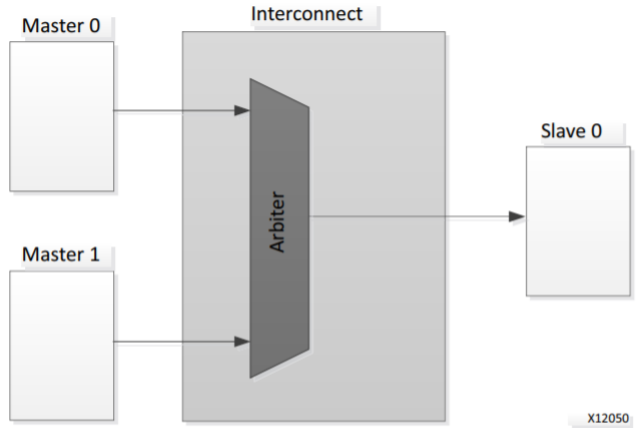


Figure 2-2: **N-to-1 AXI Interconnect**

N-to-1互联
RK3328中四个
A53与内存管理器
之间当属此模式

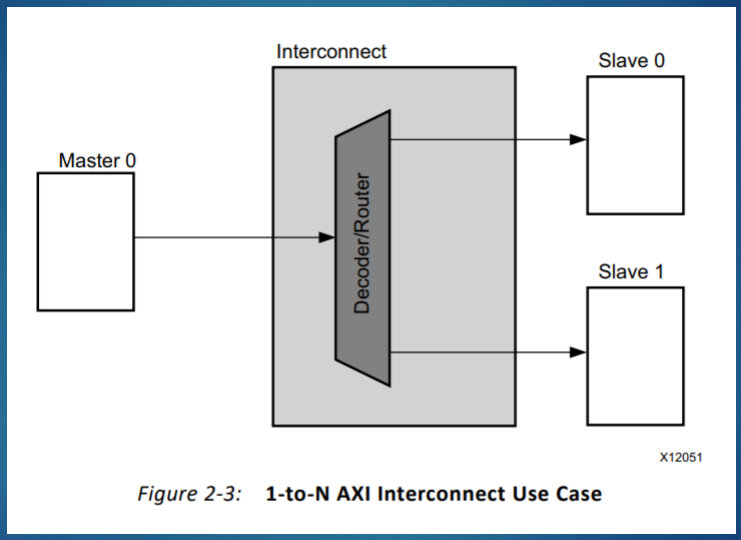


Figure 2-3: **1-to-N AXI Interconnect Use Case**

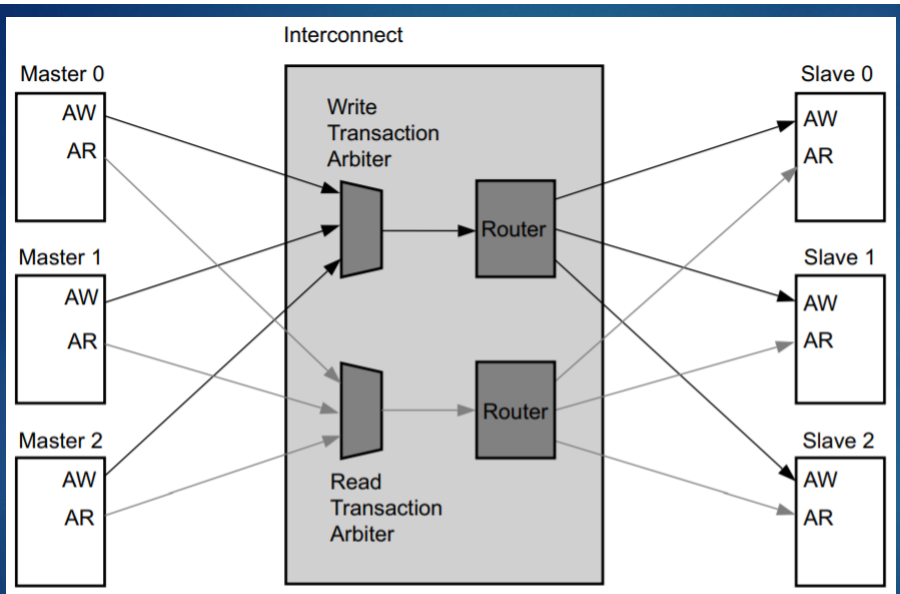


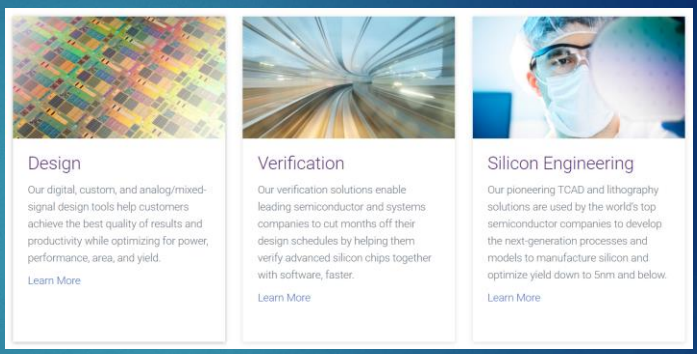
Figure 2-4: **Shared Write and Read Address Arbitration**

N-to-M模型
交叉互联(Crossbar)

SYNOPSYS®

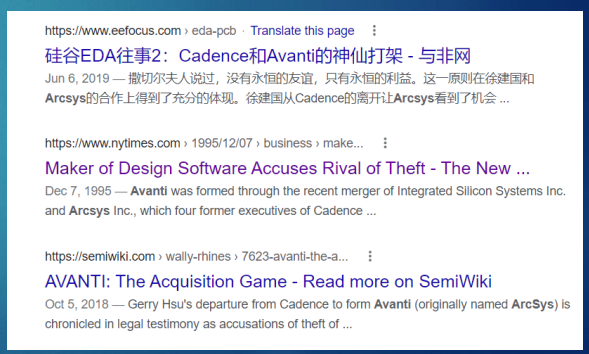
1986年成立
EDA(Electronic design automation)是主业

2021年总收入：US$4.2 billion (2021)



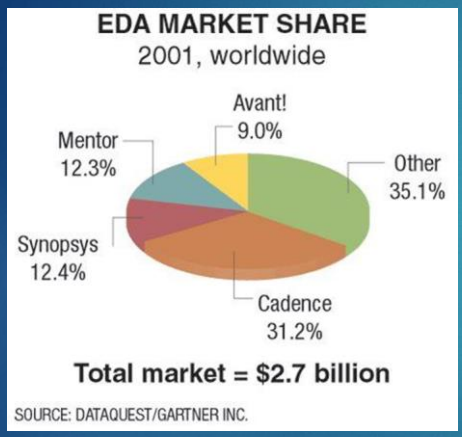
cadence®

ArcSys/Avanti



SYNOPSYS®

1995-2001年，Cadence与Avanti互相诉讼，鹤蚌相争渔翁得利，Synopsys快速发展，市场份额逐步扩大，最后收购Avanti，成为EDA领域的老大



2011/12

$5.77 billion[6] – Synopsys
$4.46 billion[7] – Cadence
$2.33 billion – Mentor Graphics
$507 million – Magma Design Automation; Synopsys acquired Magma in February 2012[8][9]
NT$6.44 billion – SpringSoft; Synopsys acquired SpringSoft in August 2012
¥11.95 billion – Zuken Inc.

Everything You Need to Enable Innovation from Chips to Software

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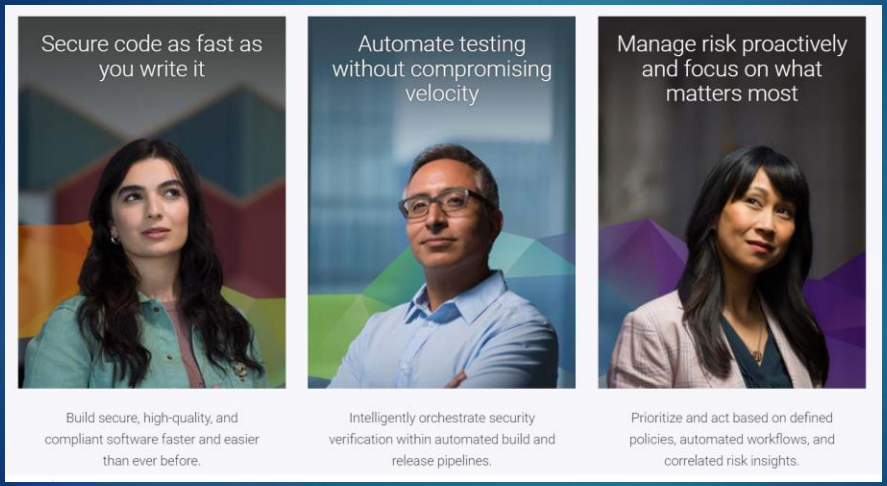
#1 in Electronic Design Automation Solutions & Services

Silicon IP
#1 in Interface, Foundation, & Physical IP

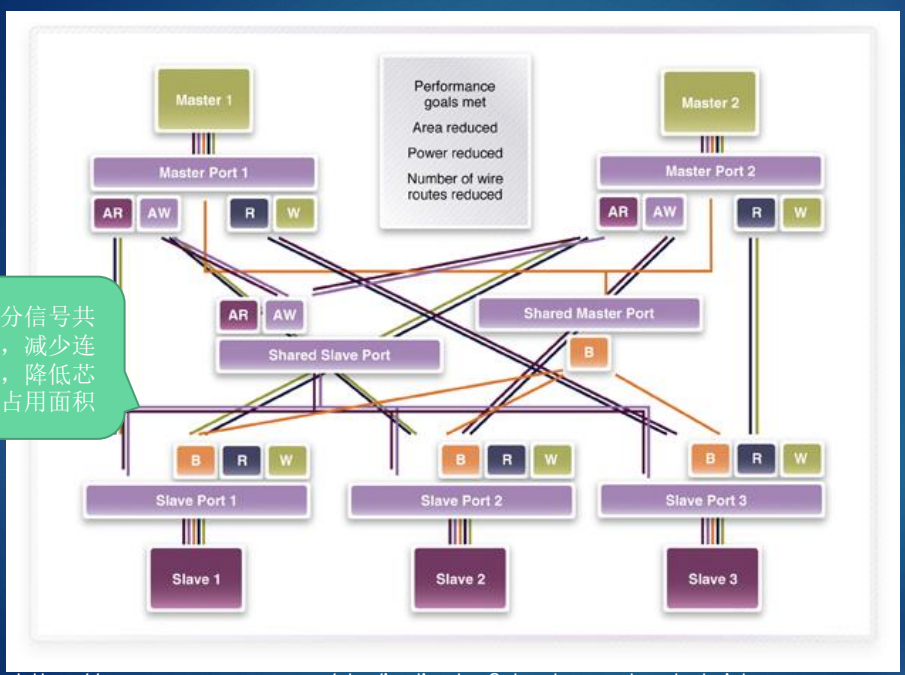
Software Security & Quality
Global Leader in Application Security & Managing Software Risk



coverity®

NOVAS

https://www.synopsys.com/software-integrity.html

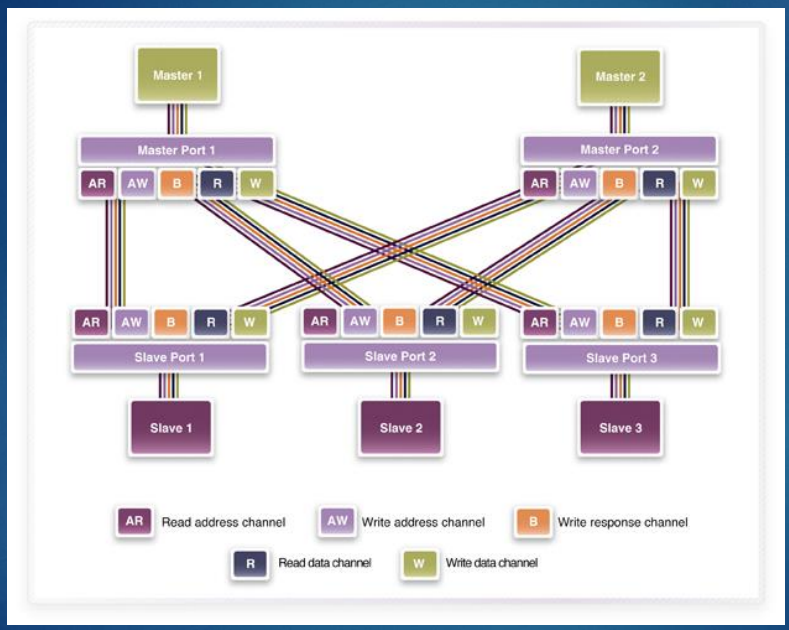


部分信号共享，减少连线，降低芯片占用面积

Advanced hybrid architecture for the AMBA 3 AXI interconnect

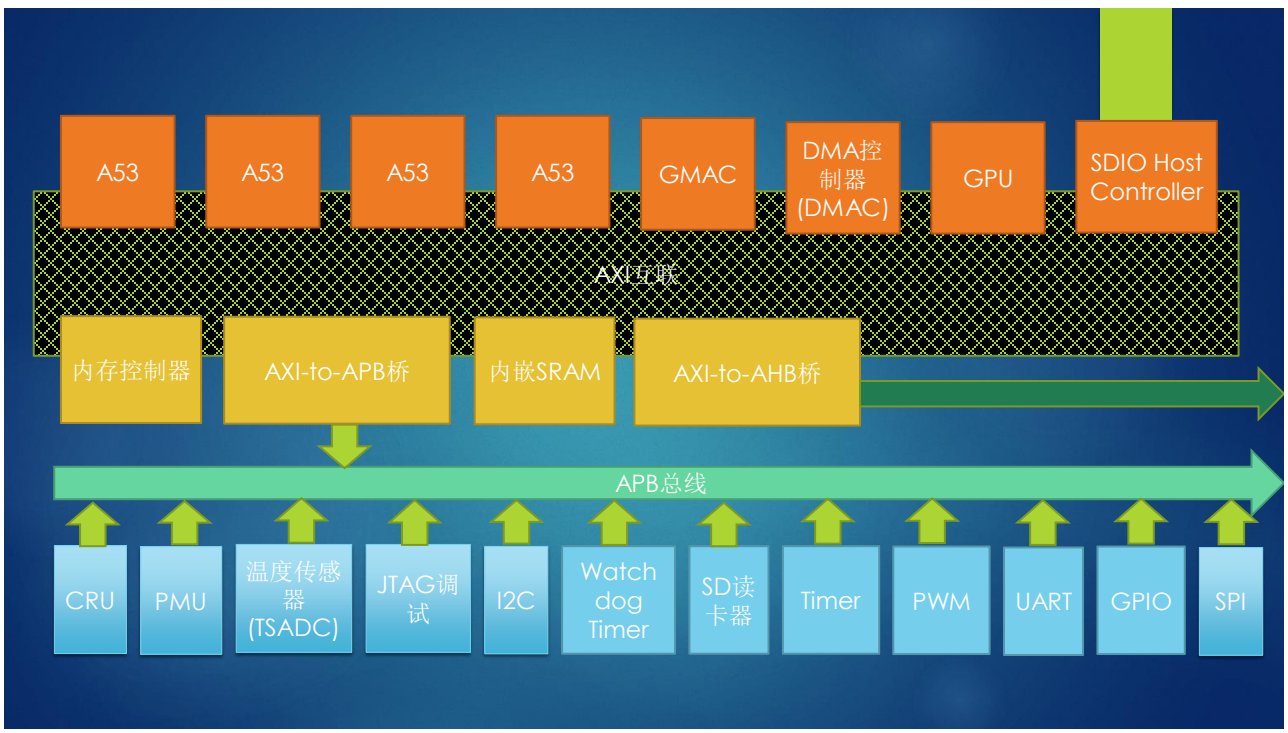
Synopsys的AXI互联混合设计方案

https://www.synopsys.com/dw/ipdir.php?ds=dw_amba_hybrid



对比用的传统设计

主从两两之间都有五类信号



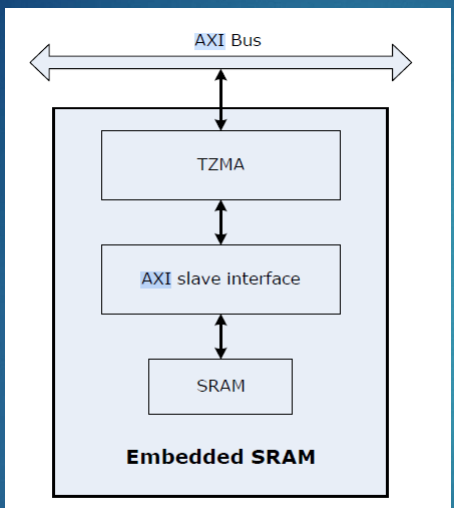


Fig. 5-1 Embedded SRAM block diagram

芯片内部的36K SRAM

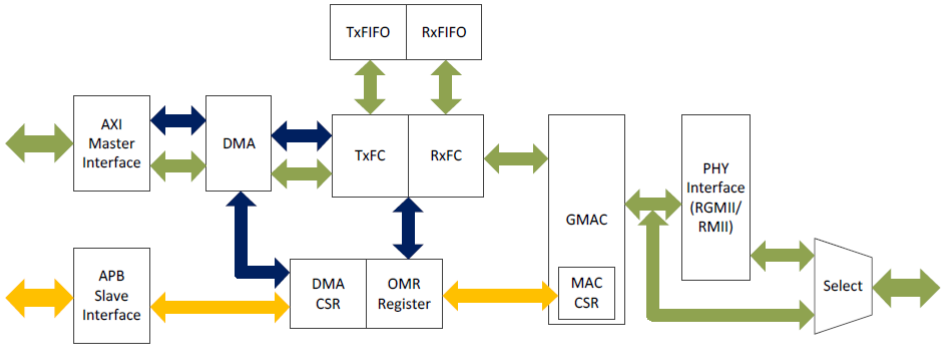


Table 22-1 GMACArchitecture

千兆网卡的结构框图，摘自RK3328 TRM

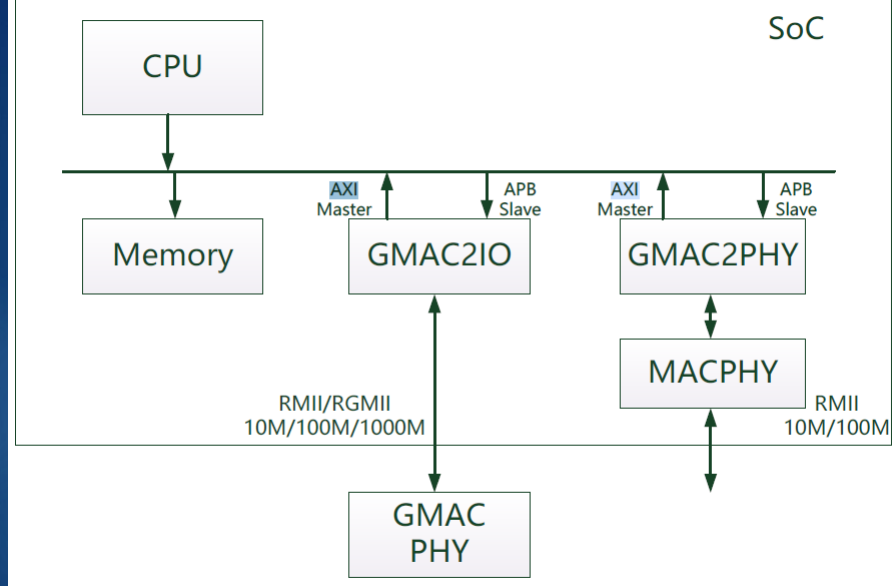
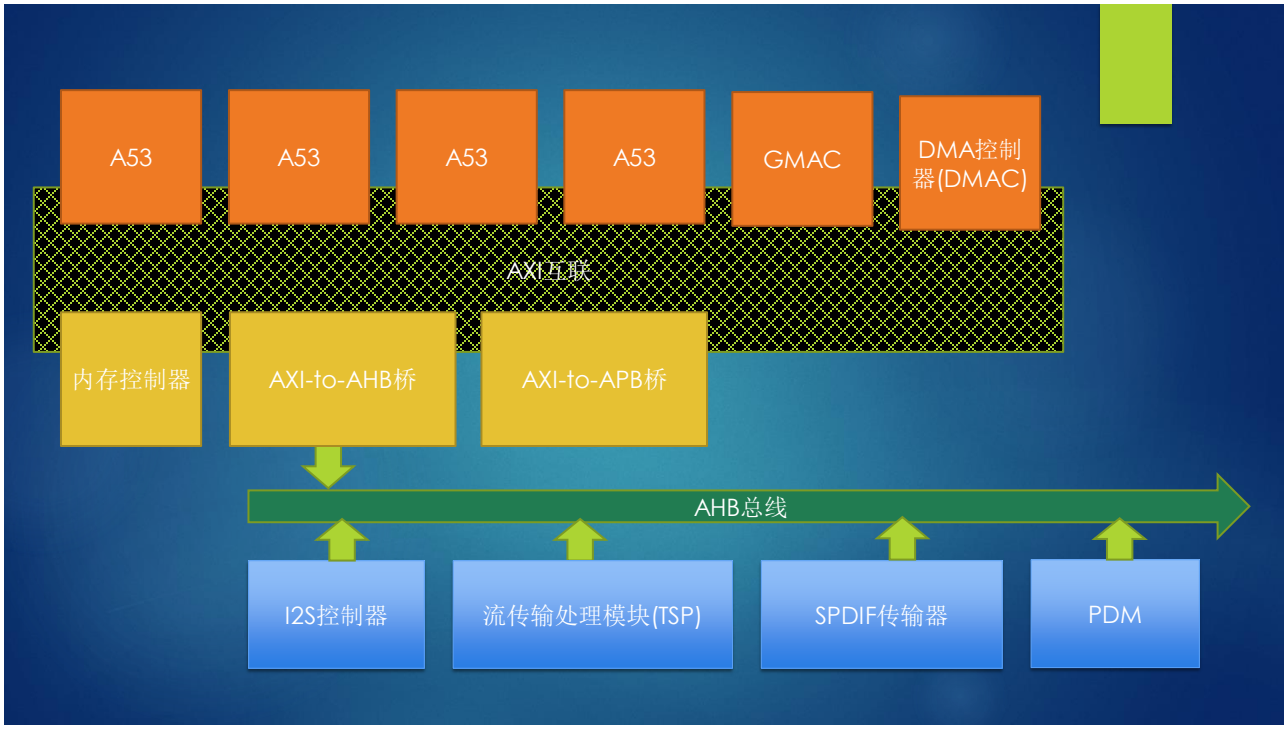
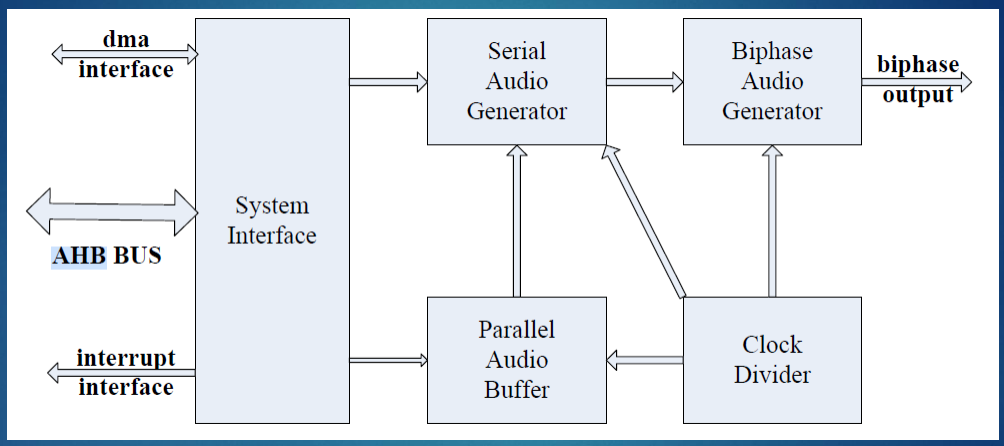


Fig.22-1 GMAC Architecture

概览 AXI AHB APB GRF GPIO SDIO

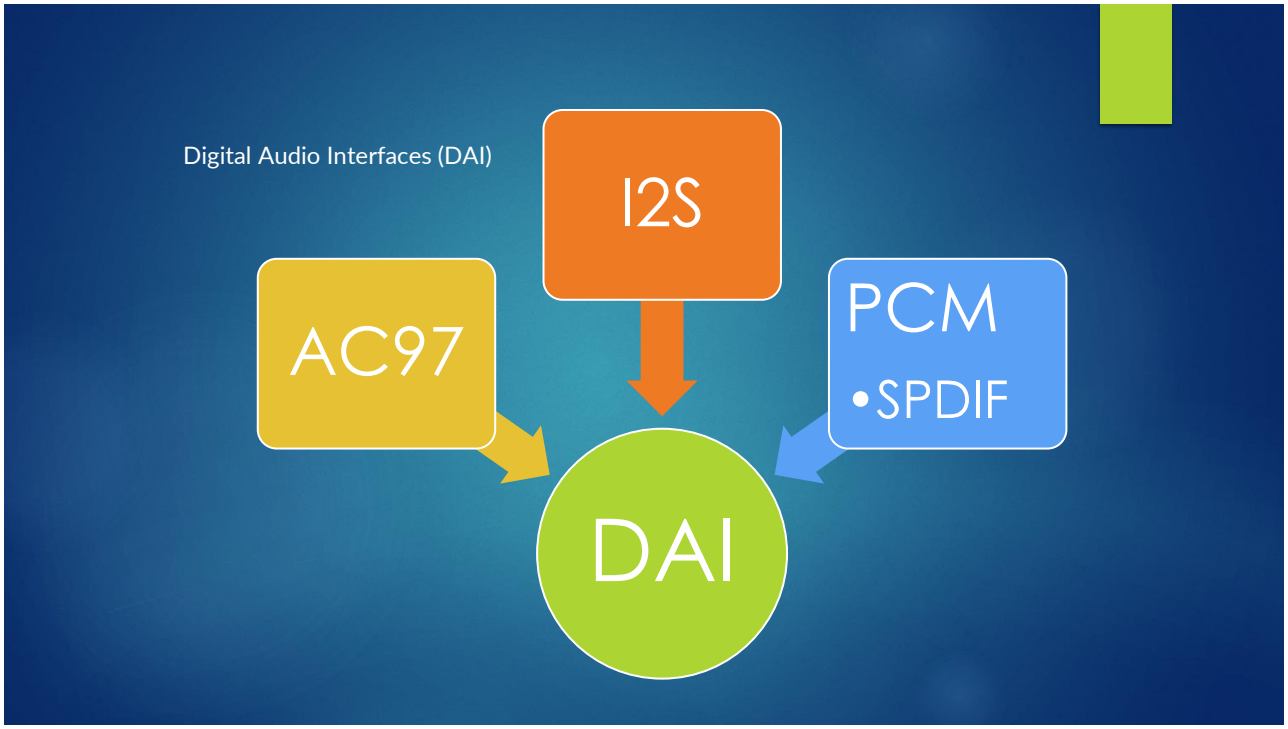




SPDIF Transmitter 声音回放

ALSA (Advanced Linux Sound Architecture)

Device Drivers
[*] Sound card support
[*] Advanced Linux Sound Architecture
[*] ALSA for SoC audio support
[*] ASoC support for Rockchip
    [*] Rockchip I2S Device Driver CODEC drivers
        [*] Realtek ALC5640 CODEC
[*] ASoC Simple sound card support

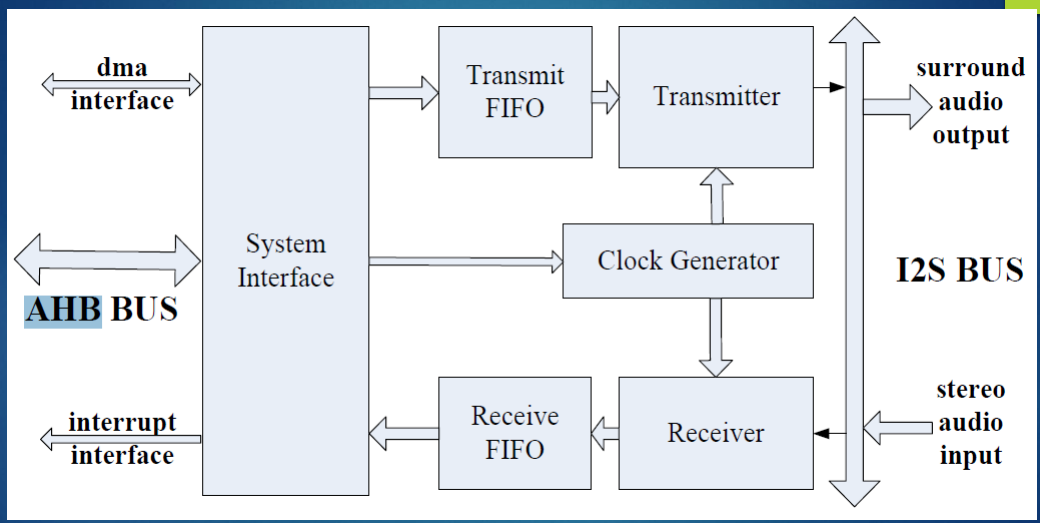



```
sound {
        compatible = "simple-audio-card";
        simple-audio-card,format = "i2s";
        simple-audio-card,mclk-fs = <256>;
        simple-audio-card,name = "rockchip-rk3328";
        simple-audio-card,cpu {
                sound-dai = <&i2s1>;
        };
        simple-audio-card,codec {
                sound-dai = <&codec>;
        };
};

hdmi-sound {
        compatible = "simple-audio-card";
        simple-audio-card,format = "i2s";
        simple-audio-card,mclk-fs = <128>;
        simple-audio-card,name = "rockchip-hdmi";
        simple-audio-card,cpu {
                sound-dai = <&i2s0>;
        };
        simple-audio-card,codec {
                sound-dai = <&hdmi>;
        };
};
```

rk3328-box-liantong.dtsi

```
i2s@ff000000 {
        reg = <0x0 0xff000000 0x0 0x1000>;
        dmas = <0xc 0xb 0xc 0xc>;
        interrupts = <0x0 0x1a 0x4>;
        rockchip,bclk-fs = <0x80>;
        compatible = "rockchip,rk3328-i2s", "rockchip,rk3066-i2s";
        clock-names = "i2s_clk", "i2s_hclk";
        reset-names = "reset-m", "reset-h";
        clocks = <0x2 0x29 0x2 0x137>;
        resets = <0x2 0x20 0x2 0x23>;
        status = "okay";
        #sound-dai-cells = <0x0>;
        phandle = <0x8f>;
        dma-names = "tx", "rx";
};
```



Lister - [H:\kernel\drivers\pwm\pwm-rockchip-i2s.c]

File Edit Options Help 85 %

```
        .mask_clkdiv = GENMASK(23, 16),
};

static const struct rockchip_i2s_pwm_data i2s_pwm_data_v2 = {
        .reg_clkdiv = 0x38,
        .bit_clkdiv = 0,
        .mask_clkdiv = GENMASK(7, 0),
};

static const struct of_device_id rockchip_i2s_pwm_match[] = {
        { .compatible = "rockchip,i2s-pwm", .data = &i2s_pwm_data_v1 },
        { .compatible = "rockchip,rk3308-i2s-pwm", .data = &i2s_pwm_data_v2 },
        { /* sentinel */ },
};

static int rockchip_i2s_pwm_probe(struct platform_device *pdev)
{
        struct rockchip_i2s_pwm_chip *pc;
        const struct of_device_id *id;
        struct resource *res;
        int ret;

        id = of_match_device(rockchip_i2s_pwm_match, &pdev->dev);
        if (!id)
                return -EINVAL;

        pc = devm_kzalloc(&pdev->dev, sizeof(*pc), GFP_KERNEL);
        if (!pc)
                return -ENOMEM;

        res = platform_get_resource(pdev, IORESOURCE_MEM, 0);
        pc->base = devm_ioremap_resource(&pdev->dev, res);
```

Lister - [H:\kernel\drivers\gpu\drm\bridge\synopsys\dw-hdmi-i2s-audio.c]

File Edit Options Help 96 %

```
        pdata.i2s               = 1;
        pdata.max_i2s_channels  = 8;
        pdata.data              = audio;

        memset(&pdevinfo, 0, sizeof(pdevinfo));
        pdevinfo.parent         = pdev->dev.parent;
        pdevinfo.id             = PLATFORM_DEVID_AUTO;
        pdevinfo.name           = HDMI_CODEC_DRV_NAME;
        pdevinfo.data           = &pdata;
        pdevinfo.size_data      = sizeof(pdata);
        pdevinfo.dma_mask       = DMA_BIT_MASK(32);

        audio->pdev = platform_device_register_full(&pdevinfo);
        return IS_ERR_OR_NULL(audio->pdev);
}

static int snd_dw_hdmi_remove(struct platform_device *pdev)
{
        struct dw_hdmi_i2s_audio_data *audio = pdev->dev.platform_data;

        if (!IS_ERR_OR_NULL(audio->pdev))
                platform_device_unregister(audio->pdev);

        return 0;
}

static struct platform_driver snd_dw_hdmi_driver = {
        .probe  = snd_dw_hdmi_probe,
        .remove = snd_dw_hdmi_remove,
        .driver = {
                .name = DRIVER_NAME,
                .owner = THIS_MODULE,
```

Synopsis Designware HDMI I2S ALSA SoC interface

```
sound {
        simple-audio-card,format = "i2s";
        compatible = "simple-audio-card";
        simple-audio-card,mclk-fs = <0x100>;
        simple-audio-card,name = "rockchip-rk3328";

        simple-audio-card,codec {
                sound-dai = <0x8d>;
        };

        simple-audio-card,cpu {
                sound-dai = <0x8c>;
        };
};
```

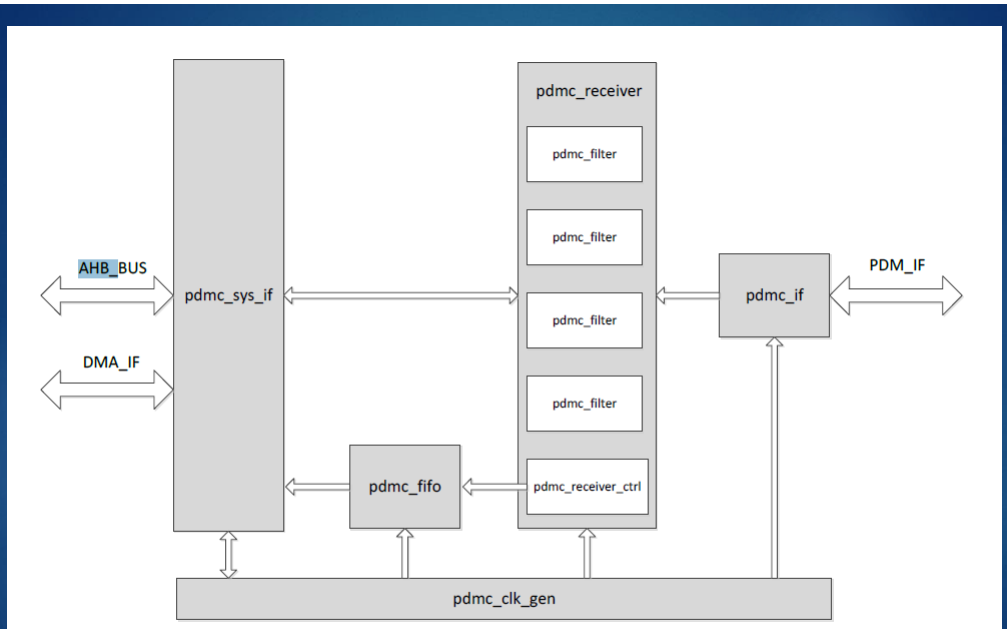


Fig.23-1 PDMC Block Diagram

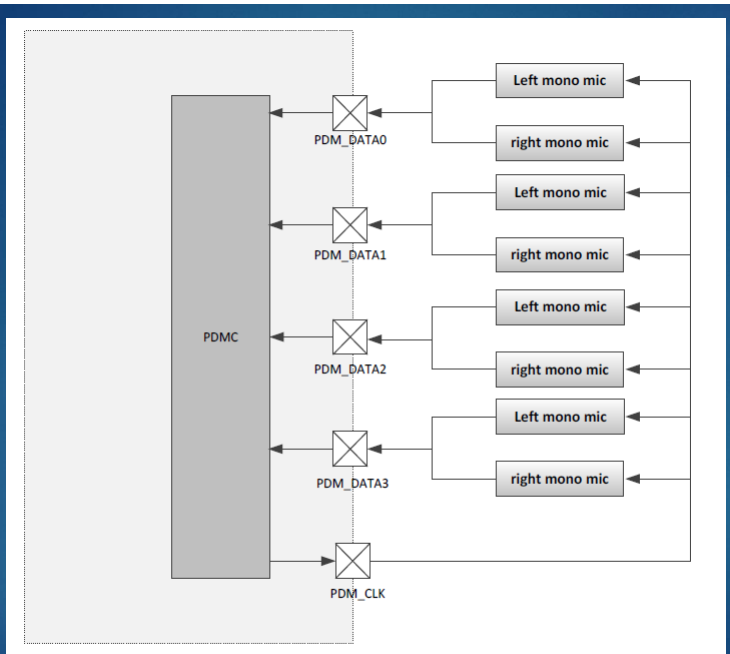
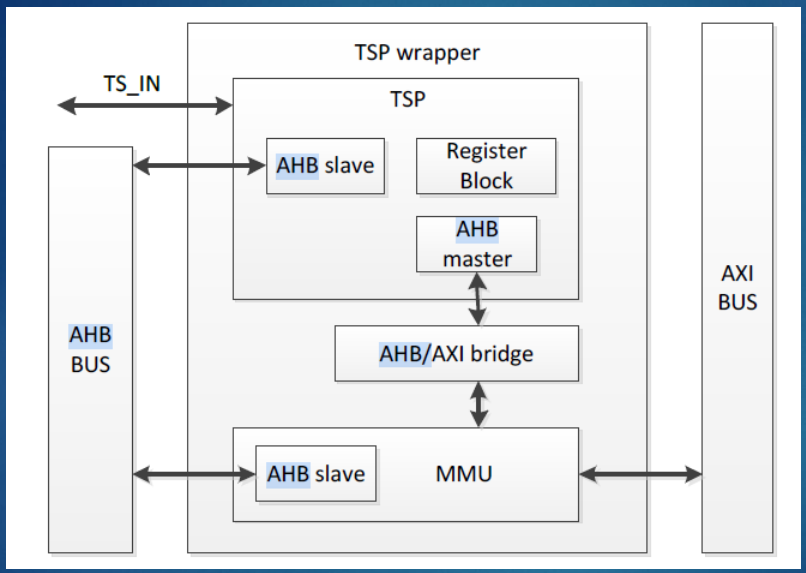


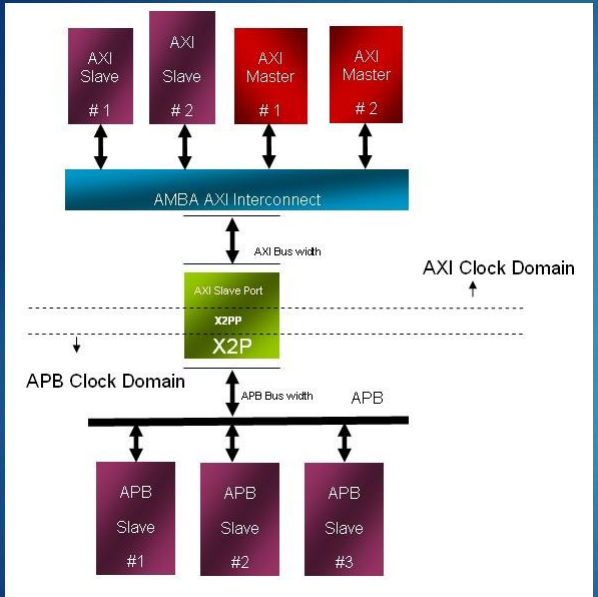
Fig.23-2 PDMC with Eight Mono MIC



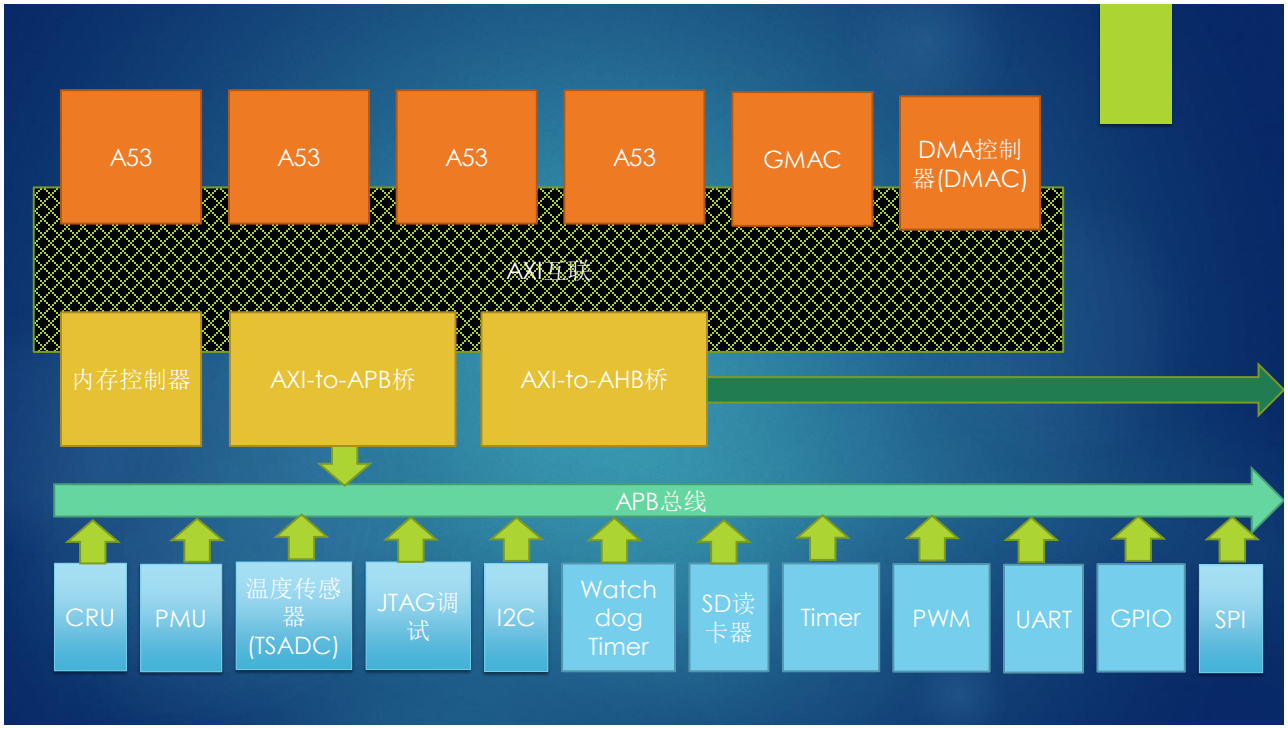
Transport Stream Processing Module(TSP)的结构框图，摘自RK3328 TRM

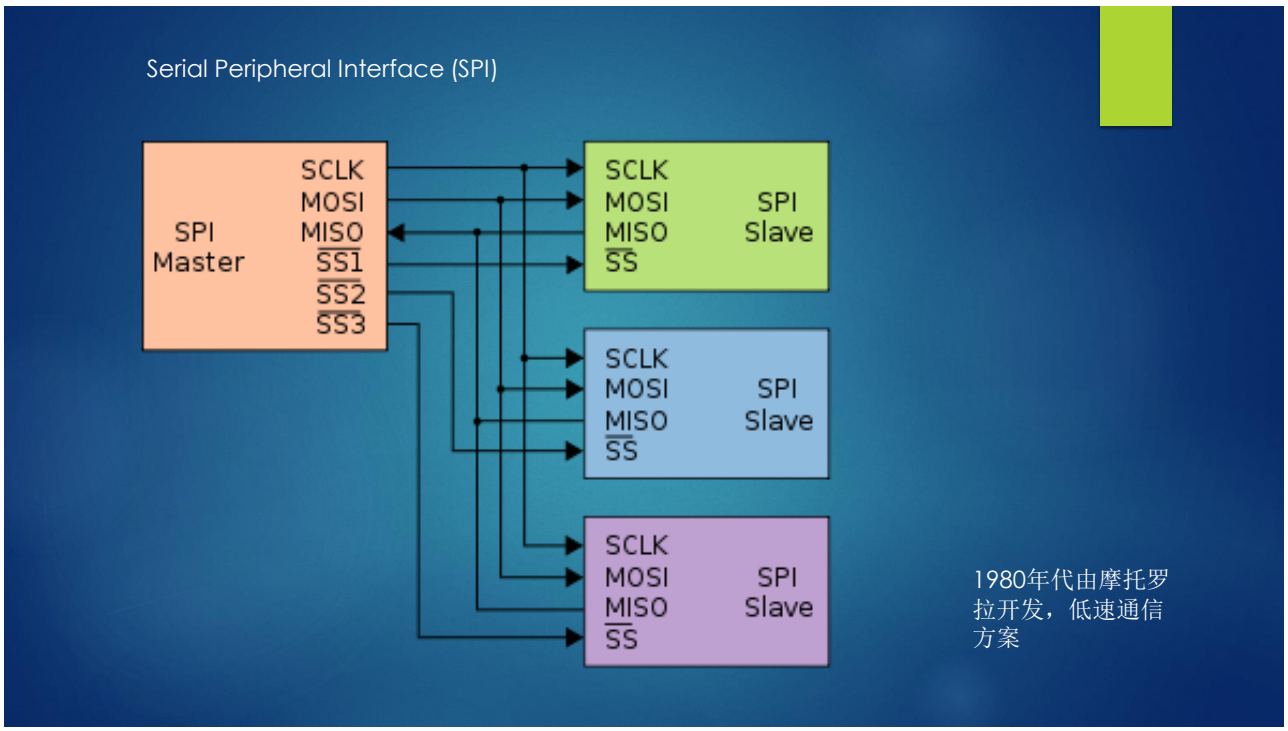
Transport Stream Processing Module(TSP)

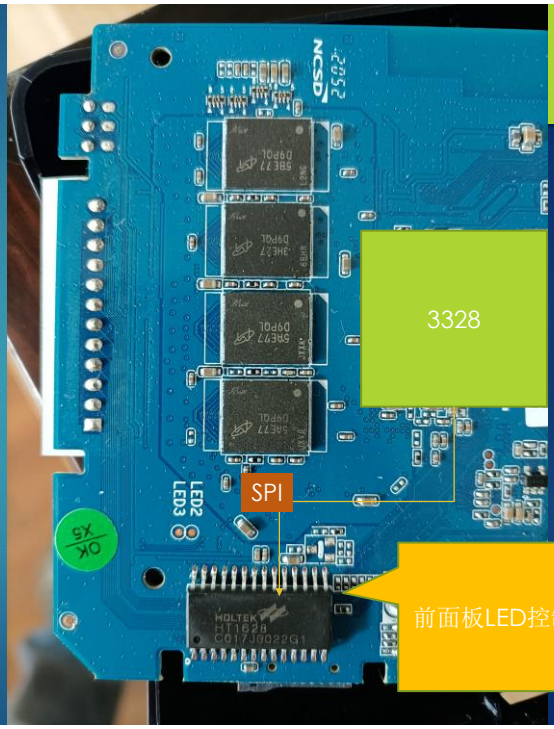
概览 → AXI → AHB → APB → GRF → GPIO → SDIO



Synopsys的AXI到APB桥

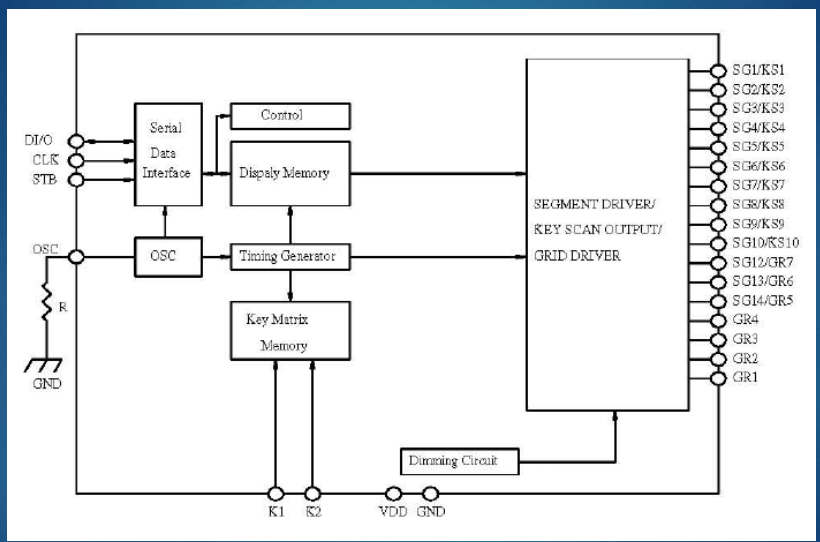




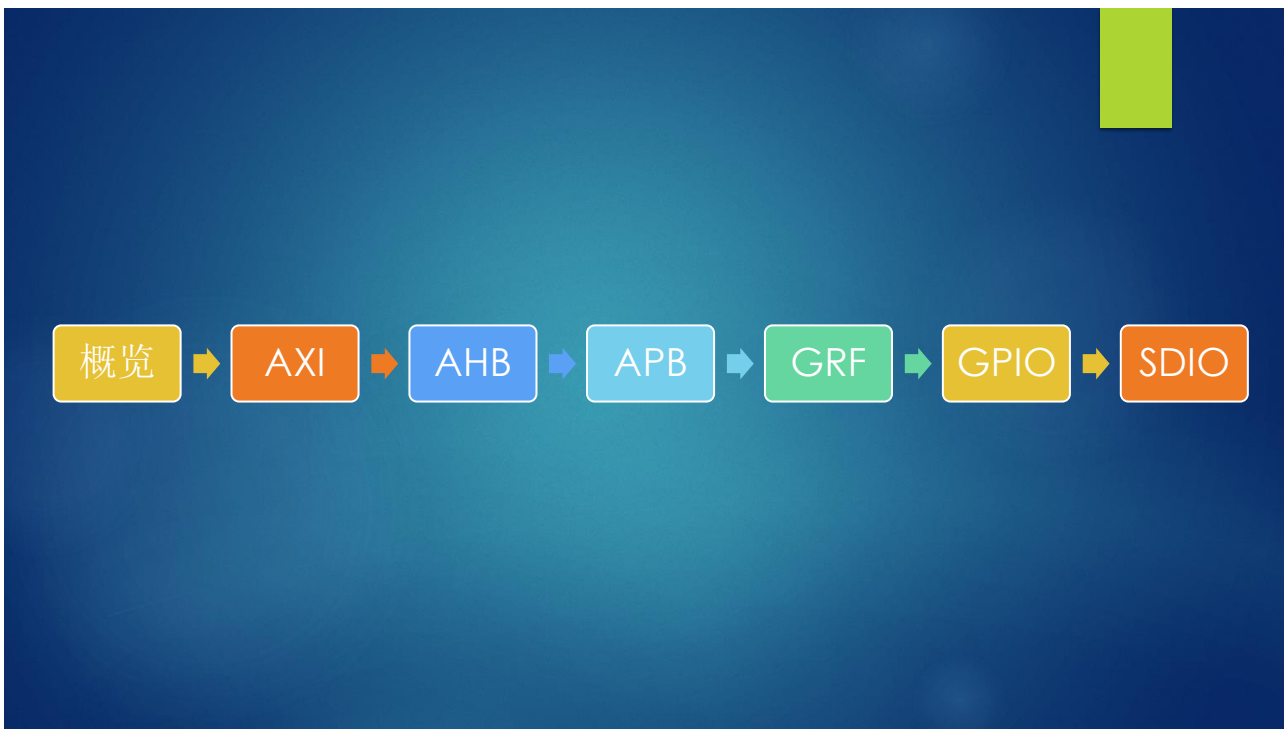



```
skykirin_led {
    compatible = "skykirin-ht1628";
    spi_data = <0x8e 0x16 0x0>;
    spi_clk = <0x8e 0x13 0x0>;
    spi_cs = <0x8e 0x12 0x0>;
    status = "okay";
};
```

```
[    0.508531] led_HT1628_init
          ================================================
[    0.509609] register device lcd_HT1628 success.
[    0.510485] of_get_named_gpiod_flags: parsed 'spi_cs' property of node '/skykirin_led[0]' - status (0)
[    0.510563] HT1628_probe: get property: gpio,spi_cs = 82
[    0.511126] of_get_named_gpiod_flags: parsed 'spi_clk' property of node '/skykirin_led[0]' - status (0)
[    0.511168] HT1628_probe: get property: gpio,spi_clk = 83
[    0.511684] of_get_named_gpiod_flags: parsed 'spi_data' property of node '/skykirin_led[0]' - status (0
[    0.511747] HT1628_probe: get property: gpio,spi_data = 86
[    0.512242] ==========LED_HT1628 probe ok========
[    0.521055] HT1628_init success
```



The GPU contains a 32-bit APB bus and 2 128-bit AXI bus. CPU configures GPU through
APB bus, GPU read and write data through AXI bus.



General Register Files (GRF)

RK3328 TRM-Part1

Chapter 3 General Register Files (GRF)

3.1 Overview

The general register file will be used to do static set by software, which is composed of many registers for system control. The GRF is divided into four sections,

- GRF, used for general non-secure system,
- DDR_GRF, used for always on system
- USB2PHY_GRF, used for USB2 PHY control and query
- USB3PHY_GRF, used for USB3 PHY control and query

3.2 Function Description

The function of general register file is:

- IOMUX control
- Control the state of GPIO in power-down mode
- GPIO PAD pull down and pull up control
- Used for common system control
- Used to record the system state

```
syscon@ff100000 {
        reg = <0x0 0xff100000 0x0 0x1000>;
        compatible = "rockchip,rk3328-grf", "syscon", "simple-mfd";
        #address-cells = <0x1>;
        phandle = <0x1c>;
        #size-cells = <0x1>;

        power-controller {
                compatible = "rockchip,rk3328-power-controller";
                status = "okay";
                #address-cells = <0x1>;
                #power-domain-cells = <0x1>;
                phandle = <0x4b>;
                #size-cells = <0x0>;

                pd_vpu@8 {
                        reg = <0x8>;
                        clocks = <0x2 0x8f 0x2 0x146>;
                        pm_qos = <0x2d>;
                };

                pd_video@5 {
                        reg = <0x5>;
                        clocks = <0x2 0x8b 0x2 0x142 0x2 0x41 0x2 0x42>;
                        pm_qos = <0x2b 0x2c>;
                };

                pd_hevc@6 {
                        reg = <0x6>;
                };
        };
```

TS-ADC Controller

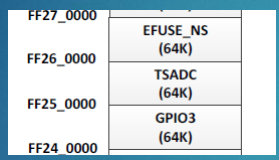
- 两路温度传感器
  - 0 - CPU
  - 1 - GPU
- 支持用户模式和自动模式
- 自动触发报警或关机

Address: Operational Base + offset (0x0020)
This register contains the data after A/D Conversion.

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:0	RO	0x000	adc_data A/D value of the channel 0 last conversion (DOUT[11:0]).

TSADC_DATA1
Address: Operational Base + offset (0x0024)
This register contains the data after A/D Conversion.

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:0	RO	0x000	adc_data A/D value of the channel 0 last conversion (DOUT[11:0]).



```
int ge_arm_read_tsadc(int channel)
{
    int val = 0, reads, ret;
    void* base;

    if ((channel != 0) && (channel != 1))
    {
        printk("bad channel no.\n");
        return -1;
    }
    base = ioremap_nocache(GDK8_TSADC_BASE, GDK8_TSADC_GRF_SIZE);
    if (base == NULL) {
        printk(KERN_ERR "failed to map TSADC GRF at %x\n", GDK8_TSADC_BASE);
        return -1;
    }
    reads = readl(base + TSADCV2_DATA(channel));
    ret = rk_tsadcv2_code_to_temp(&rk3328_therm_table, reads, &val);
    if (ret != 0) {
        printk("bad reading %d\n", ret);
        return ret;
    }

    //d = (int)(0.5823 * (float)reads-273.62); //y = 0.5823x - 273.62

    printk("tsadc_temp[%d] = %d 0x%x\n", channel, val, reads);

    return val;
}
```

```
[ 5733.568068] proc_lll_write called legnth 0x4, 0000007fef5e1c58
[ 5733.568145] tsadc_temp[0] = 50416 0x1da
[ 5733.568154] bad reading -11
[ 5746.356145] proc_lll_write called legnth 0x4, 0000007feace9ce8
[ 5746.356173] tsadc_temp[0] = 49545 0x1d8
[ 5746.356180] bad reading -11
[ 5748.404158] proc_lll_write called legnth 0x4, 0000007ff81f9498
[ 5748.404186] tsadc_temp[0] = 49090 0x1d7
[ 5748.404195] bad reading -11
[ 5749.223218] proc_lll_write called legnth 0x4, 0000007fd2637828
[ 5749.223246] tsadc_temp[0] = 49545 0x1d8
[ 5749.223254] bad reading -11
[ 5749.940915] proc_lll_write called legnth 0x4, 0000007ff1689588
[ 5749.940943] tsadc_temp[0] = 49545 0x1d8
[ 5749.940951] bad reading -11
[ 5750.657088] proc_lll_write called legnth 0x4, 0000007fe81ca918
[ 5750.657114] tsadc_temp[0] = 50000 0x1d9
[ 5750.657122] bad reading -11
```

/* millicelsius */ 除以1000，为摄氏度

```
tsadc@ff250000 {
	reg = <0x0 0xff250000 0x0 0x100>;
	interrupts = <0x0 0x3a 0x4>;
	rockchip,hw-tshut-temp = <0x1d4c0>;
	#thermal-sensor-cells = <0x1>;
	pinctrl-0 = <0x33>;
	pinctrl-1 = <0x34>;
	compatible = "rockchip,rk3328-tsadc";
	clock-names = "tsadc", "apb_pclk";
	reset-names = "tsadc-apb";
	clocks = <0x2 0x24 0x2 0xd5>;
	assigned-clock-rates = <0xc350>;
	resets = <0x2 0x42>;
	assigned-clocks = <0x2 0x24>;
	status = "okay";
	phandle = <0x2e>;
	rockchip,grf = <0x1c>;
	pinctrl-names = "gpio", "otpout";
};
```

```
[    1.297433] rockchip-thermal ff250000.tsadc: Missing tshut mode property, using default (cru)
[    1.298247] rockchip-thermal ff250000.tsadc: Missing tshut-polarity property, using default (low)
[    1.299451] rockchip-thermal ff250000.tsadc: tsadc is probed successfully!
```

SGRF = Secure GRF

RK3328 TRM-Part1

Chapter 1 System Overview

1.1 Address Mapping

RK3328 supports to boot from internal bootrom, which supports remap function by software programming. Remap is controlled by SGRF_SOC_CON2[10]. When remap is set to 1, the bootrom is mapped to address 0Xff080000 and internal memory is mapped to address 0Xffff0000.

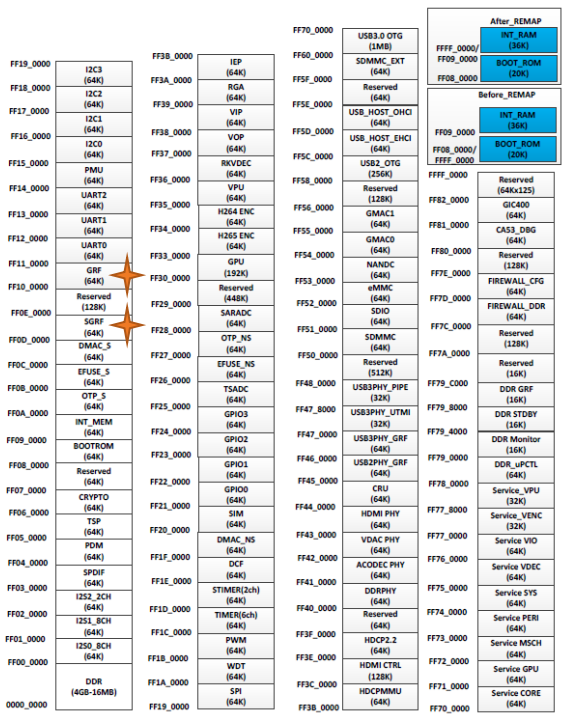


Fig. 1-1 RK3328 Address Mapping

概览 AXI AHB APB GRF GPIO SDIO

RK3328 TRM-Part1

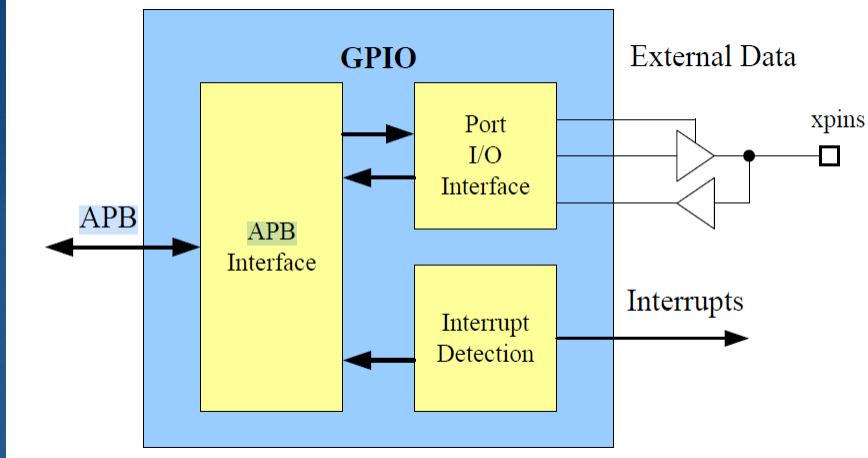
Chapter 18 GPIO

18.1 Overview

GPIO is a programmable General Purpose Programming I/O peripheral. This component is an APB slave device. GPIO controls the output data and direction of external I/O pads. It also can read back the data on external pads using memory-mapped registers.

GPIO supports the following features:

- 32 bits APB bus width
- 32 independently configurable signals
- Separate data registers and data direction registers for each signal
- Software control for each signal, or for each bit of each signal
- Configurable interrupt mode



概览 → AXI → AHB → APB → GRF → GPIO → SDIO

SDA

SD Association

- At the 2000 Consumer Electronics Show (CES), SanDisk, Matsushita, and Toshiba announced the creation of the SD Association (SDA) to promote SD cards.
- https://www.sdcard.org

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All Members | Board Members | Executive Members | General Members

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- Canon Inc.
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- Micron Consumer Products Group, Inc.
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- Samsung Electronics Co., Ltd
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- Sony Corporation
- Tokyo Electron Device Ltd
- Toshiba
- Trek Technology

发展

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Secure Digital (SD) Memory Card

SD Association (SDA)

Secure Digital Input Output (SDIO)

1999 2000 2006

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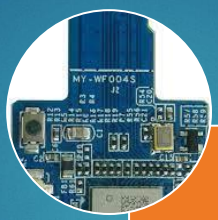
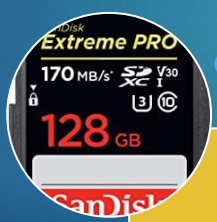
SDIO



外部设备总线

SD



移动外存

Specs

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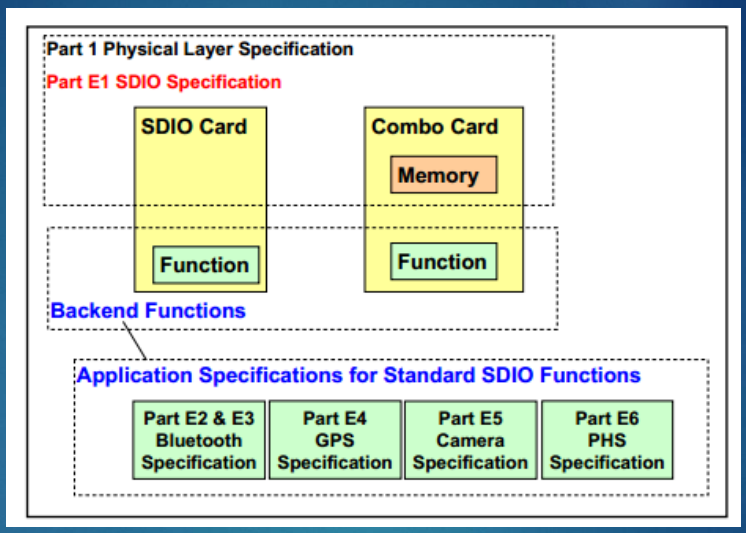

- https://www.sdcard.org/downloads/pls/simplified_specs/index.html

Hardware View

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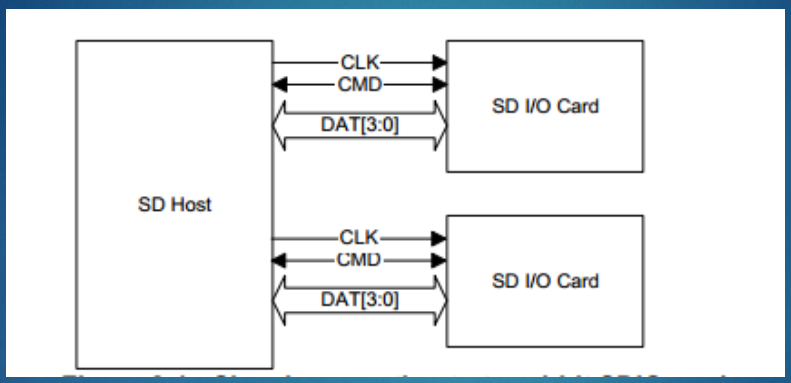

- Signal connection to two 4-bit SDIO cards

Atom Z3600/Z3700

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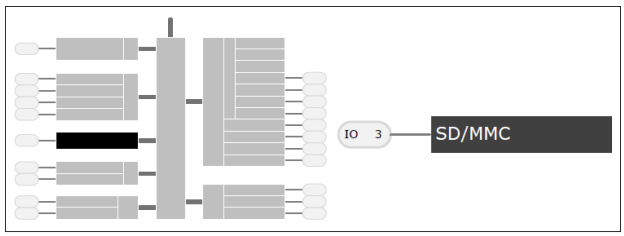
The Storage Control Cluster (SCC) consists of SDIO, SD Card and eMMC controllers to support mass storage and IO devices.

- One eMMC 4.5 interface
- One SD Card 3.0 interface
- One SDIO 3.0 interface for SDIO-based Wi-Fi

All units in the SCC support both PCI mode and ACPI mode of operation. A level shifter may be needed on the platform for SDIO 3.0 compliance.



- http://www.intel.com/content/dam/www/public/us/en/documents/datasheets/atom-z36xxx-z37xxx-datasheet-vol-1.pdf

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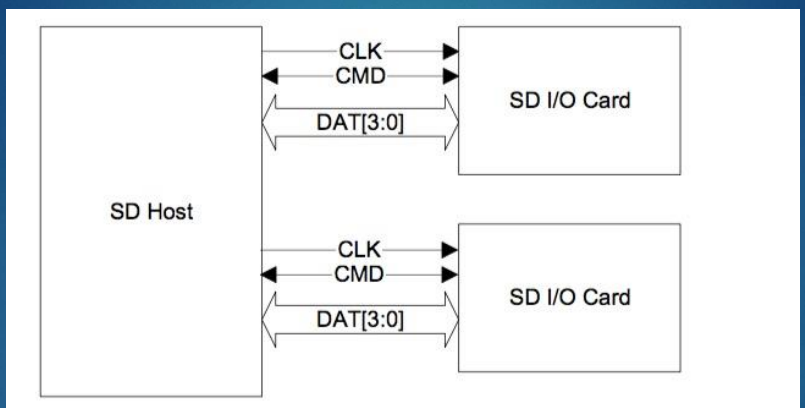


Figure 2-1 Signal connection to two 4-bit SDIO cards

```
sdmmc: dwmmc@ff500000 {
        compatible = "rockchip,rk3328-dw-mshc", "rockchip,rk3288-dw-mshc";
        reg = <0x0 0xff500000 0x0 0x4000>;
        max-frequency = <150000000>;
        clocks = <&cru HCLK_SDMMC>, <&cru SCLK_SDMMC>,
                 <&cru SCLK_SDMMC_DRV>, <&cru SCLK_SDMMC_SAMPLE>;
        clock-names = "biu", "ciu", "ciu-drive", "ciu-sample";
        fifo-depth = <0x100>;
        interrupts = <GIC_SPI 12 IRQ_TYPE_LEVEL_HIGH>;
        status = "disabled";
};

sdio: dwmmc@ff510000 {
        compatible = "rockchip,rk3328-dw-mshc", "rockchip,rk3288-dw-mshc";
        reg = <0x0 0xff510000 0x0 0x4000>;
        max-frequency = <150000000>;
        clocks = <&cru HCLK_SDIO>, <&cru SCLK_SDIO>,
                 <&cru SCLK_SDIO_DRV>, <&cru SCLK_SDIO_SAMPLE>;
        clock-names = "biu", "ciu", "ciu-drive", "ciu-sample";
        fifo-depth = <0x100>;
        interrupts = <GIC_SPI 13 IRQ_TYPE_LEVEL_HIGH>;
        status = "disabled";
};

emmc: dwmmc@ff520000 {
        compatible = "rockchip,rk3328-dw-mshc", "rockchip,rk3288-dw-mshc";
        reg = <0x0 0xff520000 0x0 0x4000>;
        max-frequency = <150000000>;
        clocks = <&cru HCLK_EMMC>, <&cru SCLK_EMMC>,
                 <&cru SCLK_EMMC_DRV>, <&cru SCLK_EMMC_SAMPLE>;
        clock-names = "biu", "ciu", "ciu-drive", "ciu-sample";
        fifo-depth = <0x100>;
        interrupts = <GIC_SPI 14 IRQ_TYPE_LEVEL_HIGH>;
        status = "disabled";
};
```

```
[    1.312276] sdhci: Secure Digital Host Controller Interface driver
[    1.312857] sdhci: Copyright(c) Pierre Ossman
[    1.313263] Synopsys Designware Multimedia Card Interface Driver
[    1.315532] dwmmc_rockchip ff500000.dwmmc: IDMAC supports 32-bit address mode.
[    1.316253] dwmmc_rockchip ff500000.dwmmc: Using internal DMA controller.
[    1.316888] dwmmc_rockchip ff500000.dwmmc: Version ID is 270a
[    1.317480] dwmmc_rockchip ff500000.dwmmc: DW MMC controller at irq 18,32 bit host data width,25
[    1.318410] dwmmc_rockchip ff500000.dwmmc: Looking up vmmc-supply from device tree
[    1.318552] dwmmc_rockchip ff500000.dwmmc: Looking up vqmmc-supply from device tree
[    1.318575] dwmmc_rockchip ff500000.dwmmc: Looking up vqmmc-supply property in node /dwmmc
[    1.318607] dwmmc_rockchip ff500000.dwmmc: No vqmmc regulator found
[    1.319213] dwmmc_rockchip ff500000.dwmmc: GPIO lookup for consumer cd
[    1.319229] dwmmc_rockchip ff500000.dwmmc: using device tree for GPIO lookup
```

```
[    1.617228] sdhci: Secure Digital Host Controller Interface driver
[    1.617808] sdhci: Copyright(c) Pierre Ossman
[    1.618211] Synopsys Designware Multimedia Card Interface Driver
[    1.620497] dwmmc_rockchip ff500000.dwmmc: IDMAC supports 32-bit address mode.
[    1.621191] dwmmc_rockchip ff500000.dwmmc: Using internal DMA controller.
[    1.621834] dwmmc_rockchip ff500000.dwmmc: Version ID is 270a
[    1.622430] dwmmc_rockchip ff500000.dwmmc: DW MMC controller at irq 18,32 bit host data width,256 deep fifo
[    1.623357] dwmmc_rockchip ff500000.dwmmc: Looking up vmmc-supply from device tree
[    1.623549] dwmmc_rockchip ff500000.dwmmc: Looking up vqmmc-supply from device tree
[    1.623569] dwmmc_rockchip ff500000.dwmmc: Looking up vqmmc-supply property in node /dwmmc@ff500000 failed
[    1.623605] dwmmc_rockchip ff500000.dwmmc: No vqmmc regulator found
[    1.624194] dwmmc_rockchip ff500000.dwmmc: GPIO lookup for consumer cd
[    1.624212] dwmmc_rockchip ff500000.dwmmc: using device tree for GPIO lookup
[    1.624234] of_get_named_gpiod_flags: can't parse 'cd-gpios' property of node '/dwmmc@ff500000[0]'
[    1.624251] of_get_named_gpiod_flags: can't parse 'cd-gpio' property of node '/dwmmc@ff500000[0]'
[    1.624269] dwmmc_rockchip ff500000.dwmmc: using lookup tables for GPIO lookup
[    1.624290] dwmmc_rockchip ff500000.dwmmc: lookup for GPIO cd failed
[    1.624311] dwmmc_rockchip ff500000.dwmmc: GPIO lookup for consumer wp
[    1.624324] dwmmc_rockchip ff500000.dwmmc: using device tree for GPIO lookup
[    1.624341] of_get_named_gpiod_flags: can't parse 'wp-gpios' property of node '/dwmmc@ff500000[0]'
[    1.624359] of_get_named_gpiod_flags: can't parse 'wp-gpio' property of node '/dwmmc@ff500000[0]'
[    1.624373] dwmmc_rockchip ff500000.dwmmc: using lookup tables for GPIO lookup
[    1.624387] dwmmc_rockchip ff500000.dwmmc: lookup for GPIO wp failed
[    1.635554] mmc_host mmc0: Bus speed (slot 0) = 400000Hz (slot req 400000Hz, actual 400000HZ div = 0)
[    1.646627] dwmmc_rockchip ff500000.dwmmc: 1 slots initialized
[    1.648047] dwmmc_rockchip ff520000.dwmmc: IDMAC supports 32-bit address mode.
[    1.648814] dwmmc_rockchip ff520000.dwmmc: Using internal DMA controller.
[    1.649437] dwmmc_rockchip ff520000.dwmmc: Version ID is 270a
[    1.650049] dwmmc_rockchip ff520000.dwmmc: DW MMC controller at irq 19,32 bit host data width,256 deep fifo
[    1.650979] dwmmc_rockchip ff520000.dwmmc: Looking up vmmc-supply from device tree
[    1.651002] dwmmc_rockchip ff520000.dwmmc: Looking up vmmc-supply property in node /dwmmc@ff520000 failed
[    1.651039] dwmmc_rockchip ff520000.dwmmc: Looking up vqmmc-supply from device tree
[    1.651059] dwmmc_rockchip ff520000.dwmmc: Looking up vqmmc-supply property in node /dwmmc@ff520000 failed
[    1.651083] dwmmc_rockchip ff520000.dwmmc: No vmmc regulator found
[    1.651656] dwmmc_rockchip ff520000.dwmmc: No vqmmc regulator found
[    1.652238] dwmmc_rockchip ff520000.dwmmc: GPIO lookup for consumer wp
[    1.652254] dwmmc_rockchip ff520000.dwmmc: using device tree for GPIO lookup
```

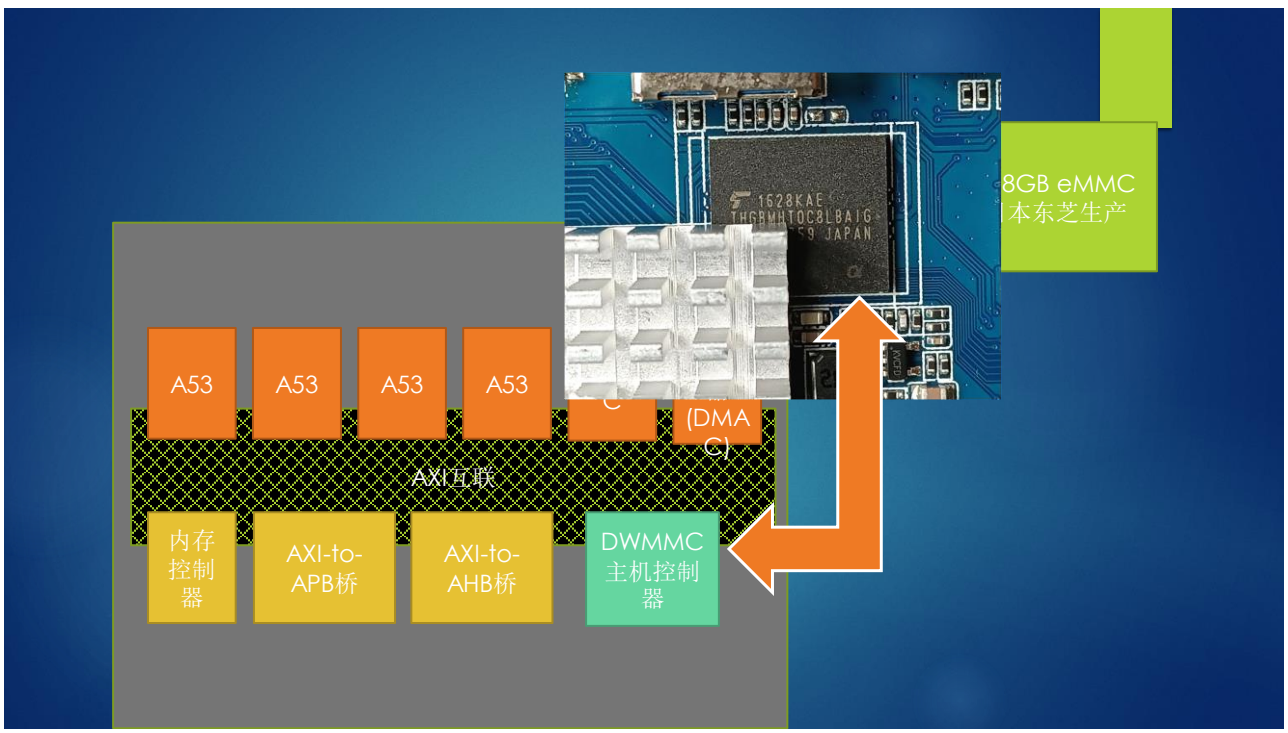
[1.650049] dwmmc_rockchip ff520000.dwmmc: DW MMC controller at irq 19,32 bit host data width,256 deep fifo

DesignWare SD/eMMC Host Controller IP

The DesignWare® SD/eMMC Host Controller IP addresses the growing storage needs of mobile, consumer, IoT and automotive applications. The IP provides advanced features such as ADMA3 supporting the SD 6.0 and SDIO 4.10 specifications as well as Command Queuing Engine (CQE) supporting the SD 6.0 and eMMC 5.1 specifications. The IP also provides advanced high-performance 32- and 64-bit AXI interface to the SoC.

The IP architecture leverages power management techniques, making it ideal for low-power applications. The highly configurable and scalable IP is packaged with Synopsys coreConsultant tool and is optimized to reduce gate count and power consumption while ensuring compatibility with previous and future generation SD and eMMC standards.

A rigorous UVM-based verification methodology is applied to the DesignWare SD/eMMC Host Controller IP, consisting of directed tests and constrained random verification. The simulation-based verification is further augmented with FPGA hardware verification based on Synopsys' HAPS®-DX FPGA-based prototyping system. The FPGA development board is tested with all major SD cards, SDIO commands, and eMMC devices. The IP is in volume production and has been successfully implemented in a wide range of applications.



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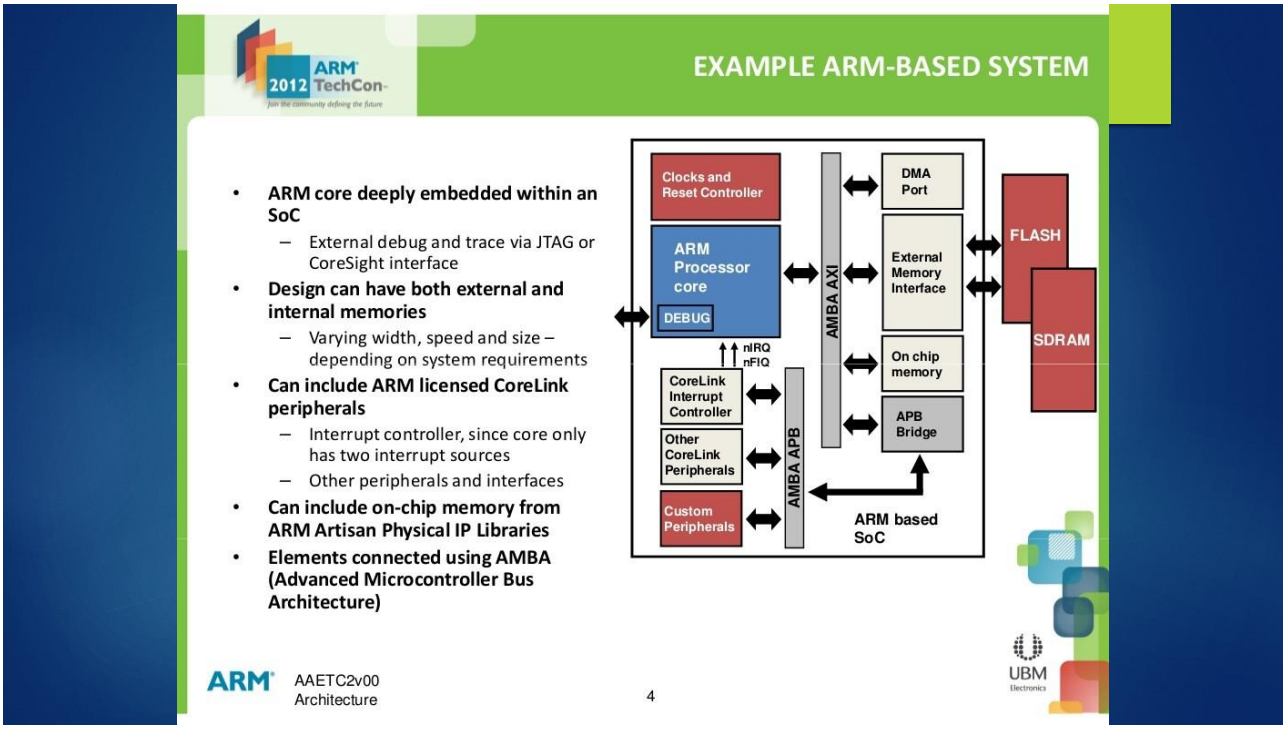
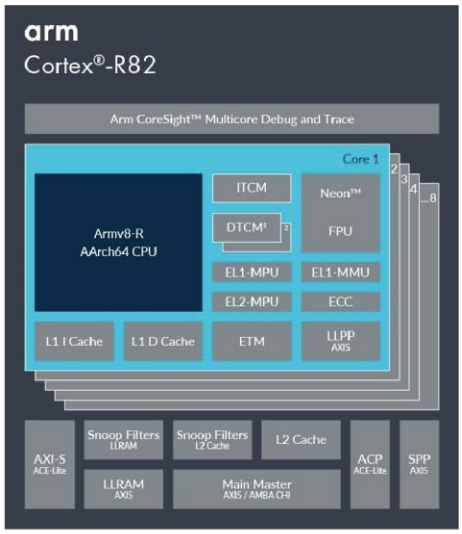


Cortex-R82: Enabling Next Generation Storage Solutions



- Highest performance real-time processor
  - Up to 2x improvement compared to Cortex-R8
  - Specialized hard real time features: lowest latencies and consistent performance
- Wider physical address space enables up to 1TB of DRAM
  - Enables larger memories
  - Shared coherent view of memory across the system
- Advanced Machine Learning support
  - Optional Arm Neon for SIMD and floating point
  - 14x faster for Neural Network workloads per cycle*
  - Dot product instructions
  - Arm Compute Library support

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* Compared to Cortex-R8

arm

Under Embargo until Thursday, Sept 3rd at 6am Pacific Standard Time. Corresponding UK time is: 2pm BST