EECE 4712/6712 Embedded Systems

Weekly Assignment 7: Introduction to Embedded Systems

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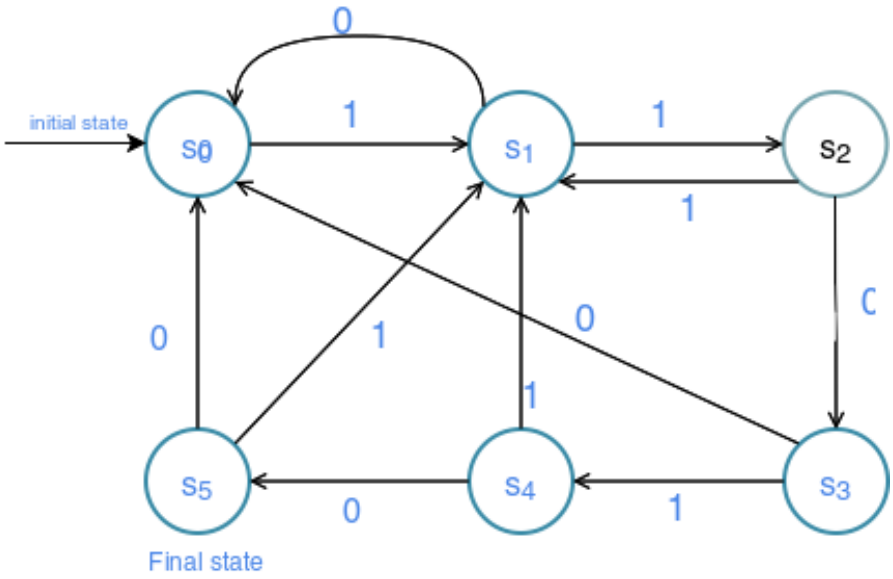
Problem:

a) The state flow diagram for detecting the binary sequence “11010”



b) Code design using VHDL for detecting binary sequence
binarySequence.vhd

binarySequence.vhd | binarySequenceTB.vhd

```vhdl
-- A VHDL program for detecting binary sequence "11010"
library ieee;
use ieee.std_logic_1164.all;

entity binarySequence is
    port(clk, reset, sequenc_in : in std_logic;
         F              : out std_logic
         );
end entity;

architecture seq_arch of binarySequence is
    type states is (s0, s1, s2, s3, s4, s5);
    signal state : states;

    begin
    process(clk, reset)
        begin
        if reset = '1' then
            state <= s0;
        elsif rising_edge(clk) then
            case state is
                when s0 =>
                    if sequenc_in = '1' then
                        state <= s1;
                    else
                        state <= s0;
                    end if;
                when s1 =>
                    if sequenc_in = '1' then
                        state <= s2;
                    else
                        state <= s0;
                    end if;
                when s2 =>
                    if sequenc_in = '0' then
                        state <= s3;
                    else
                        state <= s1;
                    end if;
                when s3 =>
                    if sequenc_in = '1' then
                        state <= s4;
                    else
                        state <= s0;
                    end if;
                when s4 =>
                    if sequenc_in = '0' then
                        state <= s5;
                    else
                        state <= s1;
                    end if;
                when s5 =>
                    if sequenc_in = '1' then
                        state <= s1;
                    else
                        state <= s0;
                    end if;
            end case;
        end if;
    end process;
    -- output process
    process(state)
    begin
        case state is
            when s0 =>
                F <= '0';
            when s1 =>
                F <= '0';
            when s2 =>
                F <= '0';
            when s3 =>
                F <= '0';
            when s4 =>
                F <= '0';
            when s5 =>
                F <= '1';
        end case;
    end process;
end architecture;
```

binarySequenceTB.vhdl

binarySequence.vhd | binarySequenceTB.vhd

```
-- A VHDL program to detect binary sequence "11010"
-- Developed By: Lokesh
-- Date : 04/10/2021
-- TestBench File

-- all necessary libraries
library ieee;
use ieee.std_logic_1164.all;

-- declare entity for testbench

entity binarySequenceTB is
end entity;

-- architecture of binary sequence
architecture sqTB_arch of binarySequenceTB is
    -- component declaration for finite state
    component binarySequence
        port(clk, reset, sequenc_in : in std_logic;
         F              : out std_logic
         );
    end component;

    -- inputs
    signal clk : std_logic :='0';
    signal reset : std_logic :='0';
    signal sequenc_in : std_logic :='0';

    -- outputs

    signal F : std_logic;

    -- clock period definitions
    constant clock_period : time := 10 ns;

    begin
    uut: binarySequence port map(
        clk => clk,
        reset => reset,
        sequenc_in => sequenc_in,
        F => F
    );

    clock_process :process
    begin
        clk <= '0';
        wait for clock_period/2;
        clk <='1';
        wait for clock_period/2;
    end process;

    -- stimulus process
    stim_proc: process
        begin
         sequenc_in <= '1';
         reset <='1';
        wait for 10 ns;
            reset <= '0';
        wait for 10 ns;
            sequenc_in <= '1';
        wait for 10 ns;
            sequenc_in <= '0';
        wait for 10 ns;
            sequenc_in <= '1';
        wait for 10 ns;
            sequenc_in <= '0';
        wait for 10 ns;
    end process;
end architecture;
```

c) Snapshot of successful code compilation and simulation